MPQ2179

5.5V, Peak 3A, 2.4MHz, Synchronous Step-Down Converter with PG and SS, AEC-Q100 Qualified

DESCRIPTION

The MPQ2179 is a monolithic, step-down switch-mode converter with built-in internal power MOSFETs. The device achieves 3A of peak output current from a 2.5V to 5.5V input voltage range, with excellent load and line regulation. The output voltage can be regulated to as low as 0.6V.

Constant-on-time (COT) control provides fast transient response and eases loop stabilization. Fault protections include cycle-by-cycle current limiting and thermal shutdown.

The MPQ2179 is ideal for a wide range of applications, including automotive infotainment systems, clusters, and telematics.

The MPQ2179 requires a minimal number of readily available, standard external components, and is available in an ultra-small QFN-8 (1.5mmx2mm) package.

FEATURES

- Wide 2.5V to 5.5V Operating Input Voltage Range
- Up to 3A Peak Output Current
- 2.4MHz Switching Frequency
- EN for Power Sequencing
- 1% FB Accuracy
- Output Adjustable from 0.6V
- 65mΩ and 35mΩ Internal Power MOSFET Switches
- 100% Duty On
- Output Discharge
- Power Good (PG)
- External Soft Start (SS) Control
- Output Over-Voltage Protection (OVP)
- Short-Circuit Protection (SCP) with Hiccup Mode
- Forced Continuous Conduction Mode (FCCM)
- Available in a QFN-8 (1.5mmx2mm) Package
- Available in a Wettable Flank Package
- AEC-Q100 Grade 1

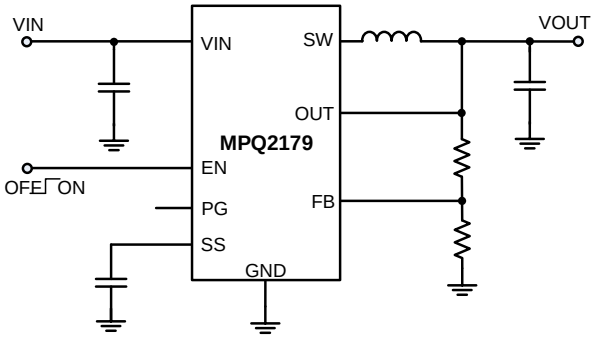
APPLICATIONS

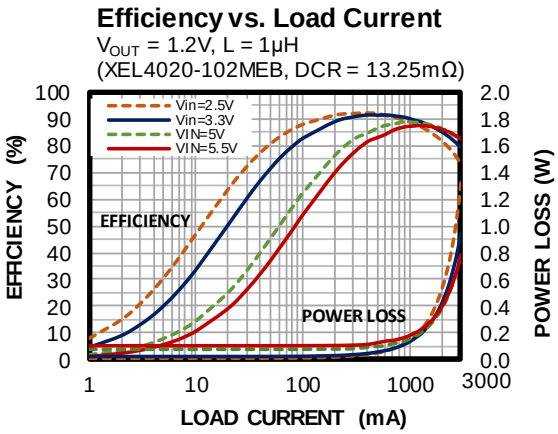
- Automotive Infotainment
- Camera Modules
- Key Fobs
- Automotive Clusters
- Automotive Telematics
- Industrial Supplies
- Battery-Powered Devices

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. “MPS”, the MPS logo, and “Simple, Easy Solutions” are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

TYPICAL APPLICATION





MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ2179GQHE***	QFN-8 (1.5mmx2mm)	*See Below*	1
MPQ2179GQHE-AEC1***			

* For Tape & Reel, add suffix –Z (e.g. MPQ2179GQHE–Z).

** Moisture Sensitivity Level Rating

*** Wettable flank

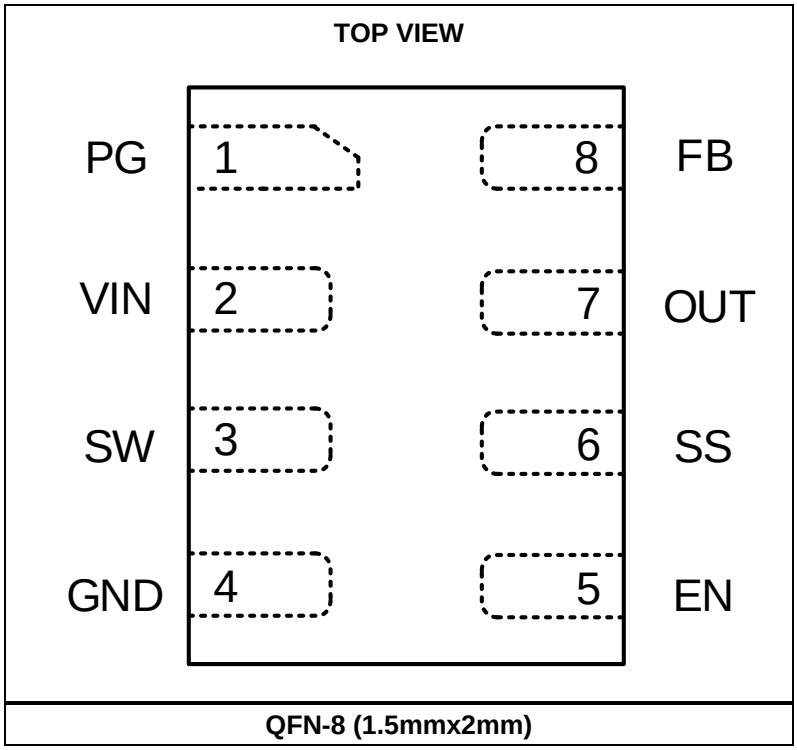
TOP MARKING

$\overline{\text{KJ}}$

LL

KJ: Product code of MPQ2179GQHE-AEC1 & MPQ2179GQHE
LL: Lot number

PACKAGE REFERENCE



QFN-8 (1.5mmx2mm)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Description
1	PG	**Power good indicator.** The output of this pin is an open drain. Connect PG to a voltage source using an external resistor. PG is pulled high when V_{FB} exceeds 90% of V_{REF}; PG is pulled low to GND if V_{FB} drops below 85% of V_{REF}. Float the pin if it is not used.
2	VIN	**Supply voltage.** The MPQ2179 operates from a 2.5V to 5.5V input. Use a decoupling capacitor to prevent large voltage spikes from appearing at the input.
3	SW	**Output switching node.** SW is the drain of the internal P-channel MOSFET, which is also called the high-side MOSFET (HS-FET). Connect an inductor to SW to complete the converter.
4	GND	**Ground.**
5	EN	**On/off control.** Pull EN below the falling threshold (0.4V) to shut down the chip. Pull EN above the rising threshold (1.2V) to enable the chip. There is an internal 2MΩ resistor connected from the EN pin to ground.
6	SS	**Soft start.** Connect a capacitor from SS to GND to set the soft-stat time and avoid start-up inrush current. The SS capacitor is recommended to be at least 1nF.
7	OUT	**Output voltage.** Power rail and input sense pin for the output voltage. Connect the load to this pin. Use an output capacitor to reduce the output voltage ripple.
8	FB	**Feedback pin.** An external resistor divider should be connected from the output to GND, and tapped to the FB pin. The voltage on FB is compared to the internal 0.6V reference to set the regulation voltage.

ABSOLUTE MAXIMUM RATINGS (1)

All pins .....-0.3V to +6.5V
Junction temperature .....150°C
Lead temperature .....260°C
Continuous power dissipation (T_A = 25°C) (2) (4)
……. 2.2W
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±2000V
Charged device model (CDM) ..... ±750V

Recommended Operating Conditions

Supply voltage (V_{IN}) .....2.5V to 5.5V
Output voltage (V_{OUT}) ..... 0.6V to V_{IN} - 0.5V
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-8 (1.5mmx2mm)
JESD51-7 (3)…....130.....25.... °C/W
EVQ2179-LE-00A (4).....59.....14.... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.
4) Measured on EVQ2179-LE-00A, 4-layer PCB, 2oz each layer, 6.3cmx6.3cm.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6V, T_J = -40°C to +150°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{IN} range			2.5		5.5	V
Under-voltage lockout rising threshold				2.3	2.45	V
Under-voltage lockout threshold hysteresis				200		mV
Shutdown supply current		V_{EN} = 0V, T_J = 25°C		0.01	1	µA
		V_{EN} = 0V, T_J = -40°C to +125°C (6)			3	µA
		V_{EN} = 0V, T_J = -40°C to +150°C			20	µA
Quiescent supply current		V_{EN} = 2V, V_{FB} = 0.63V, V_{IN} = 3.6V		460	650	µA
Feedback voltage	V_{FB}	T_J = 25°C	594	600	606	mV
		T_J = -40°C to +150°C	591	600	609	
Feedback current	I_{FB}	V_{FB} = 0.63V		50	100	nA
P-channel MOSFET switch on resistance	$R_{DS(ON)_P}$	V_{IN} = 5V		65	85	mΩ
N-channel MOSFET switch on resistance	$R_{DS(ON)_N}$	V_{IN} = 5V		35	55	mΩ
Switch leakage		V_{EN} = 0V, V_{IN} = 6V V_{SW} = 0V or 6V, T_J = 25°C		0	1	µA
		V_{EN} = 0V, V_{IN} = 6V V_{SW} = 0V or 6V, T_J = -40°C to +125°C (6)			30	µA
Switching frequency	f_{SW}	V_{IN} = 5V, V_{OUT} = 1.2V, operating under CCM.	2000	2400	2640	kHz
Minimum on time (6)	t_{MIN-ON}	V_{IN} = 5V		50		ns
Minimum off time (6)	$t_{MIN-OFF}$	V_{IN} = 5V		80		ns
P-channel MOSFET peak current limit			4	5	6	A
N-channel MOSFET valley current limit			1.5	3	4.5	A
Soft-start current	I_{SS_ON}		1.5	3	4.5	µA
Maximum duty cycle				100		%
Power good UV rising threshold		FB rising edge	87	90	93	%
Power good UV falling threshold		FB falling edge	82	85	88	%
Power good delay	t_{PGD}	PG rising/falling edge		80		µs
Power good sink current capability	V_{PG-L}	Sink 1mA			0.4	V
Power good logic high voltage	V_{PG-H}	V_{IN} = 5V, V_{FB} = 0.6V	4.9			V
Self-bias PG (5)					0.7	V

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_J = -40°C to +150°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power good leakage current/logic high		5V logic high			100	nA
EN turn-on delay		EN on to SW active		100		us
EN turn-off delay		EN off to stop switching		30		us
EN input logic low voltage					0.4	V
EN input logic high voltage			1.2			V
EN pull-down resistor				2		MΩ
Output discharge resistor	R_{DIS}	V_{EN} = 0V, V_{OUT} = 1.2V		150		Ω
EN input current		V_{EN} = 2V		1.2		μA
		V_{EN} = 0V		0		μA
Output over-voltage rising threshold	V_{OVP}		110%	115%	120%	V_{FB}
Output over-voltage hysteresis	V_{OVP_HYS}			10%		V_{FB}
Output over-voltage delay				2		us
Low-side current limit		Current flow from SW to GND		1.2		A
Absolute VIN OVP		After V_{OUT} OVP enable		6.1		V
Absolute VIN OVP hysteresis				160		mV
Thermal shutdown (6)				170		°C
Thermal shutdown hysteresis (6)				20		°C

Notes:

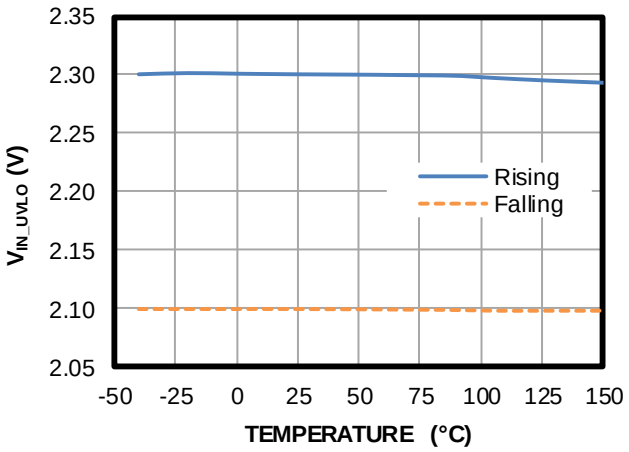
5) If VIN = 0V and EN=0V, PG should be pulled up between 3.0V and 5.5V with a 100kΩ resistor.
6) Guaranteed by design and bench characterization, not tested in production.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

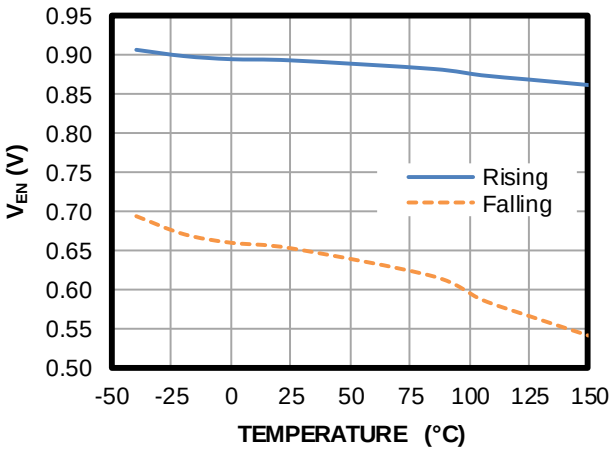
TYPICAL CHARACTERISTICS

V_{IN} = 3.6V, T_J = -40°C to +150°C, unless otherwise noted.

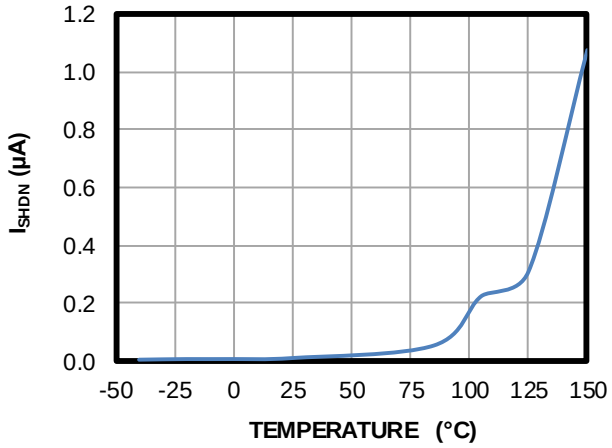
V_{IN} UVLO Threshold vs. Temperature



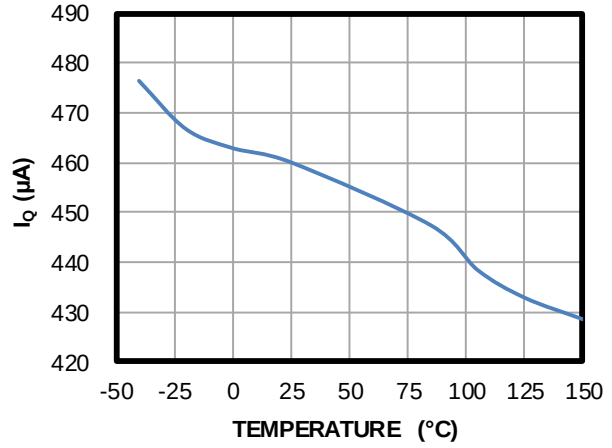
EN Rising and Falling Threshold vs. Temperature



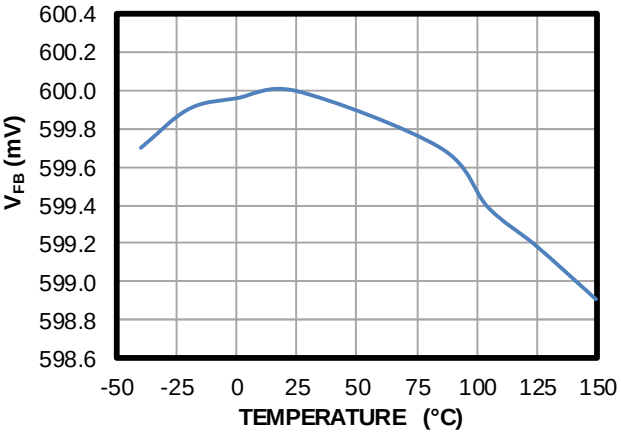
Shutdown Current vs. Temperature



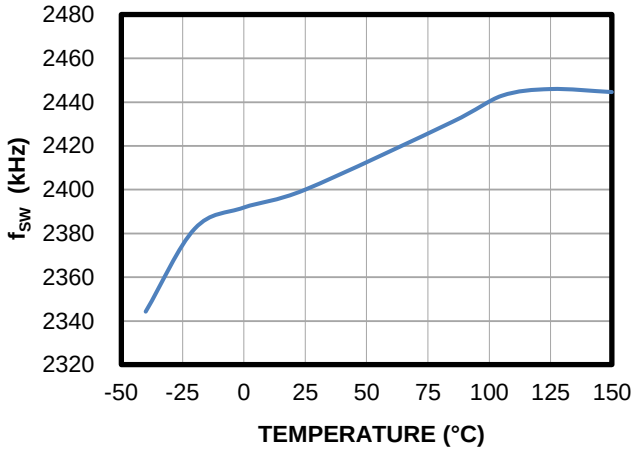
Quiescent Current vs. Temperature



V_{FB} vs. Temperature



f_{SW} vs. Temperature

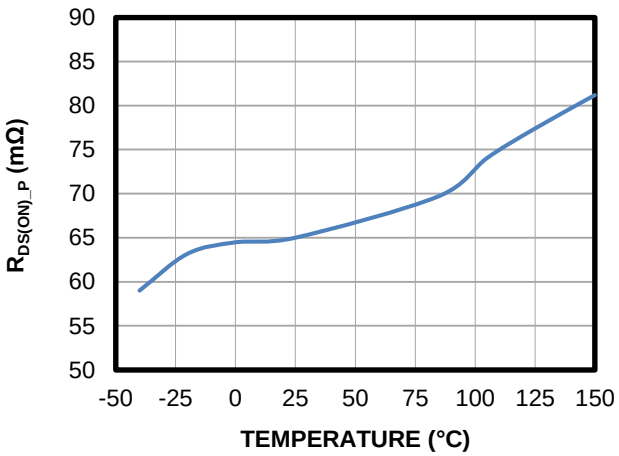


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

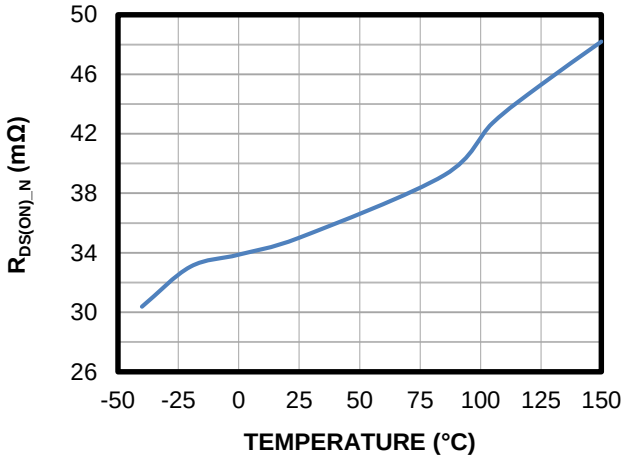
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_J = -40°C to +150°C, unless otherwise noted.

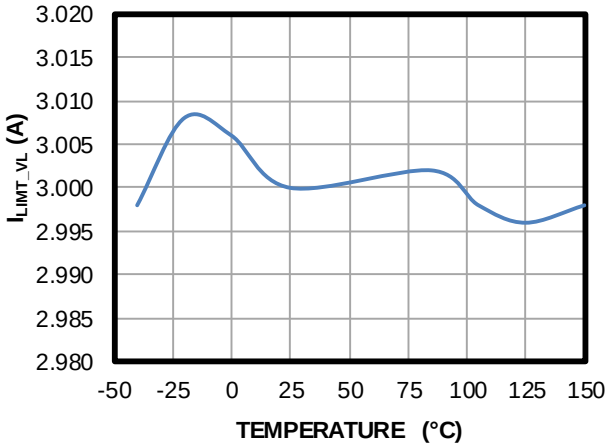
$R_{DS(ON)_P}$ vs. Temperature



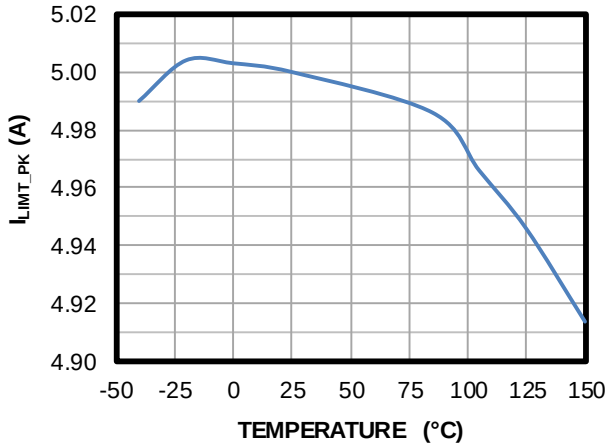
$R_{DS(ON)_N}$ vs. Temperature



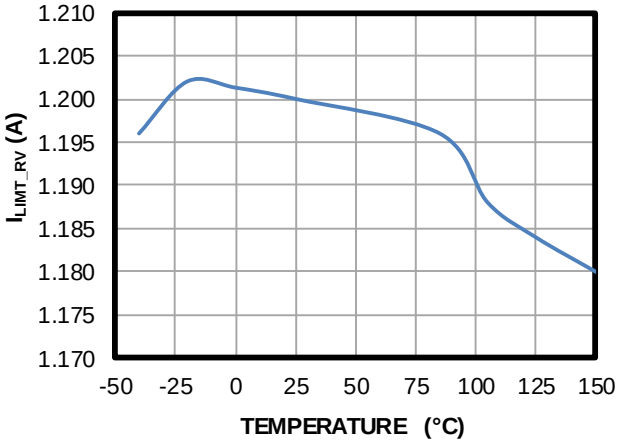
LS-FET Valley Current Limit vs. Temperature



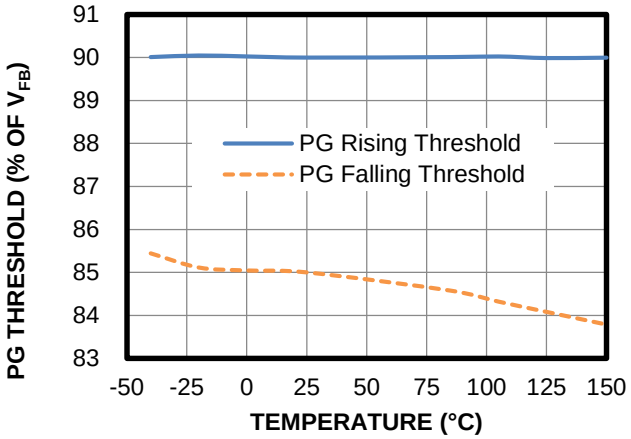
HS-FET Peak Current Limit vs. Temperature



Low-Side Reverse Current Limit vs. Temperature



PG Rising/Falling Threshold vs. Temperature

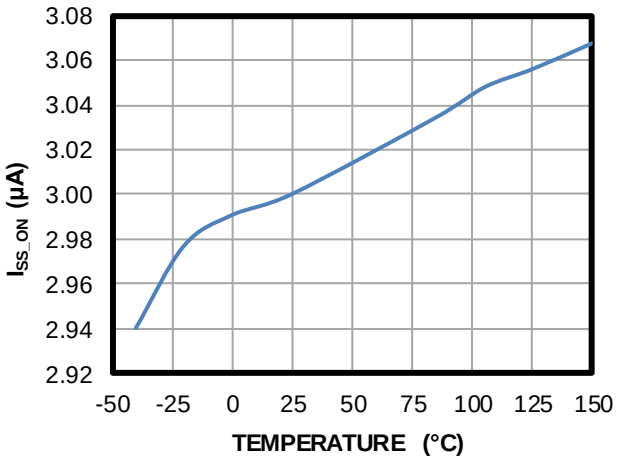


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_J = -40°C to +150°C, unless otherwise noted.

Soft-Start Current vs. Temperature



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

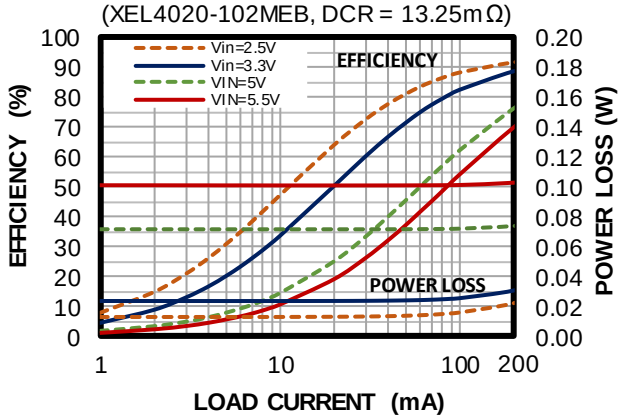
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3V, V_{OUT} = 1.2V, L = 1µH, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

Efficiency vs. Load Current (Light Load)

V_{OUT} = 1.2V, L = 1µH

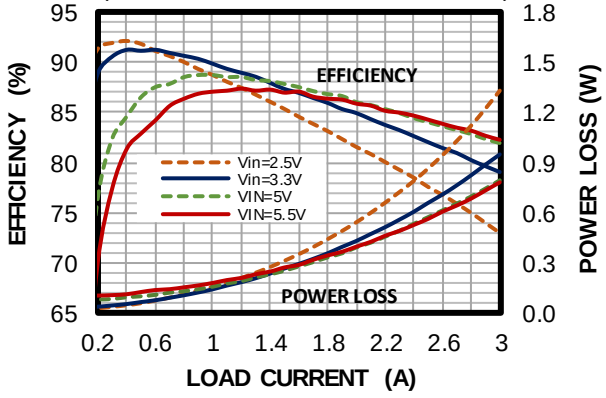
(XEL4020-102MEB, DCR = 13.25mΩ)



Efficiency vs. Load Current

V_{OUT} = 1.2V, L = 1µH

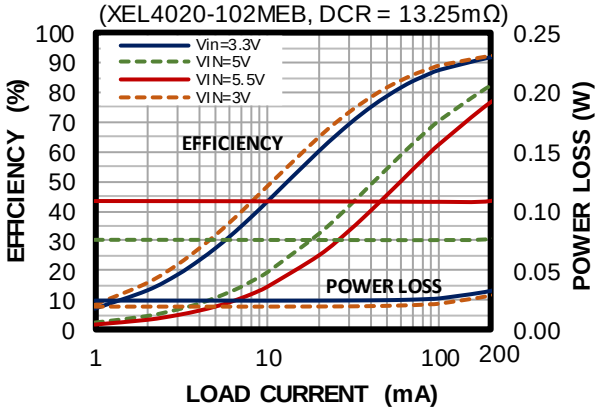
(XEL4020-102MEB, DCR = 13.25mΩ)



Efficiency vs. Load Current (Light Load)

V_{OUT} = 1.8V, L = 1µH

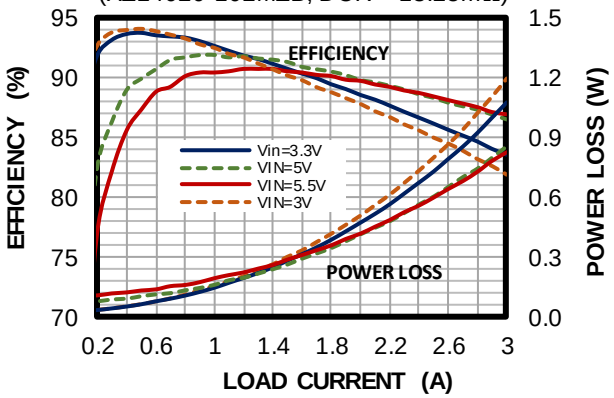
(XEL4020-102MEB, DCR = 13.25mΩ)



Efficiency vs. Load Current

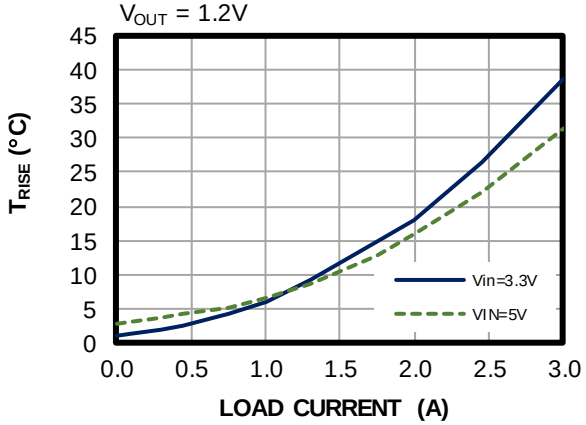
V_{OUT} = 1.8V, L = 1µH

(XEL4020-102MEB, DCR = 13.25mΩ)



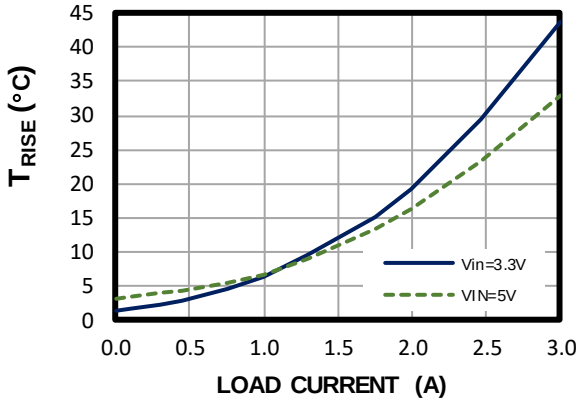
Case Thermal Rise

V_{OUT} = 1.2V



Case Thermal Rise

V_{OUT} = 1.8V



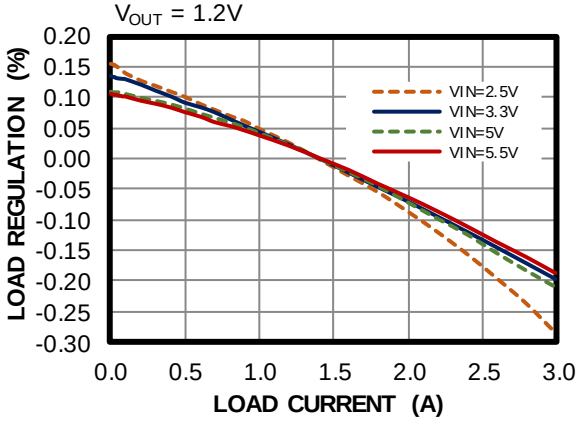
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 1.2V, L = 1µH, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

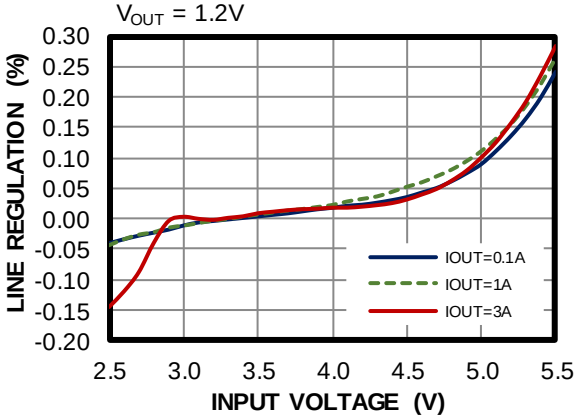
Load Regulation

V_{OUT} = 1.2V



Line Regulation

V_{OUT} = 1.2V



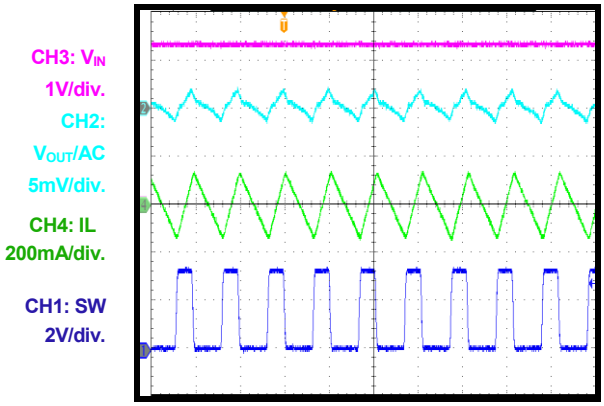
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 1.2V, L = 1µH, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

Steady State

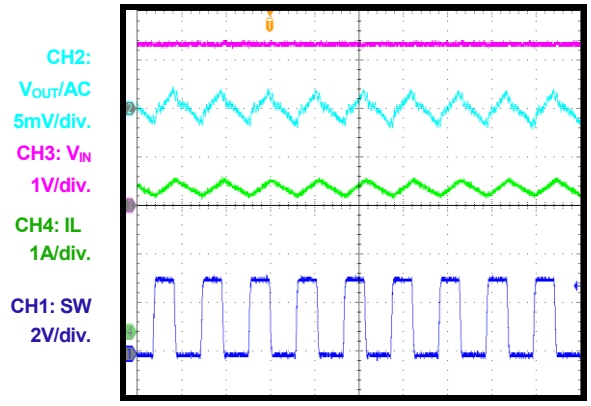
I_{OUT} = 0A



400ns/div.

Steady State

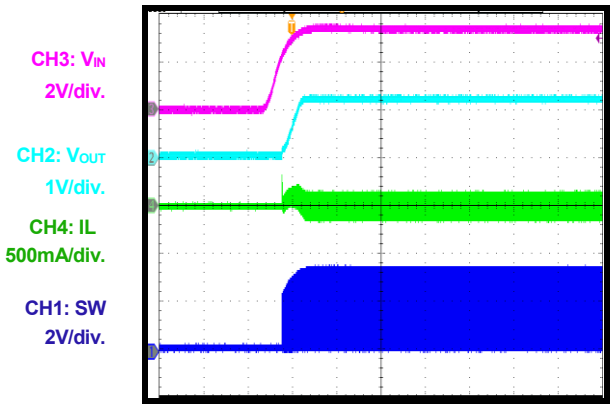
I_{OUT} = 3A



400ns/div.

Start-Up through VIN

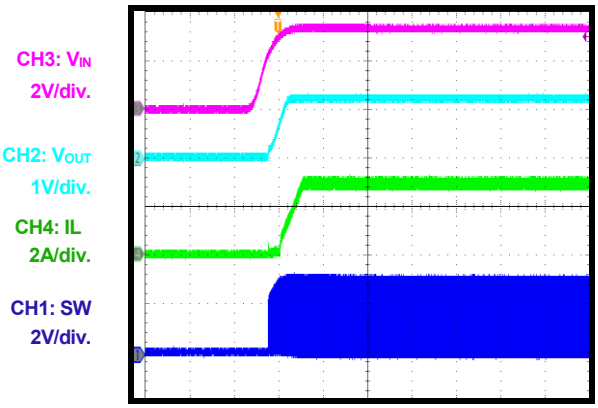
I_{OUT} = 0A



1ms/div.

Start-Up through VIN

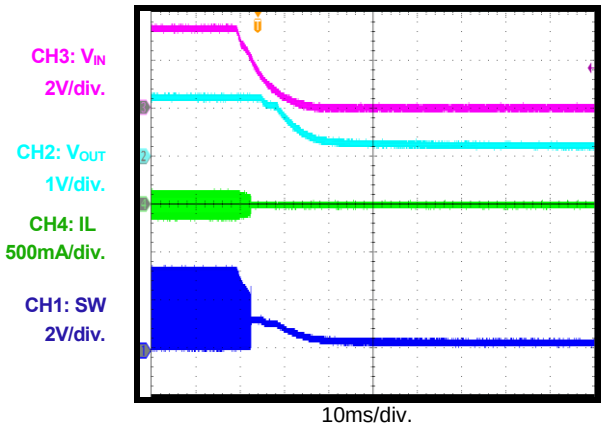
I_{OUT} = 3A



1ms/div.

Shutdown through VIN

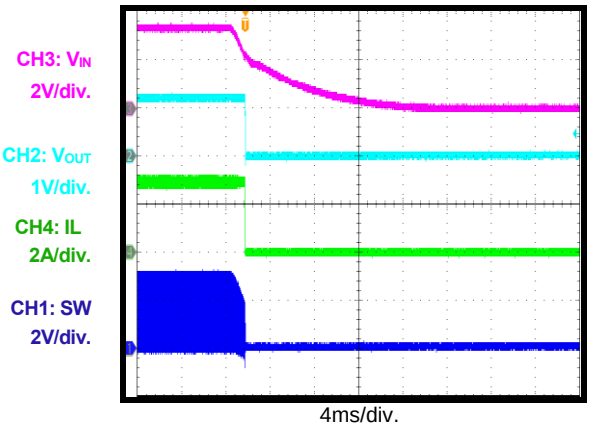
I_{OUT} = 0A



10ms/div.

Shutdown through VIN

I_{OUT} = 3A



4ms/div.

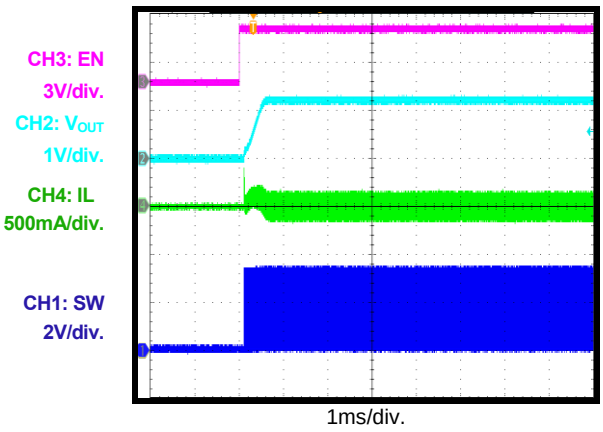
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 1.2V, L = 1µH, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

Start-Up through EN

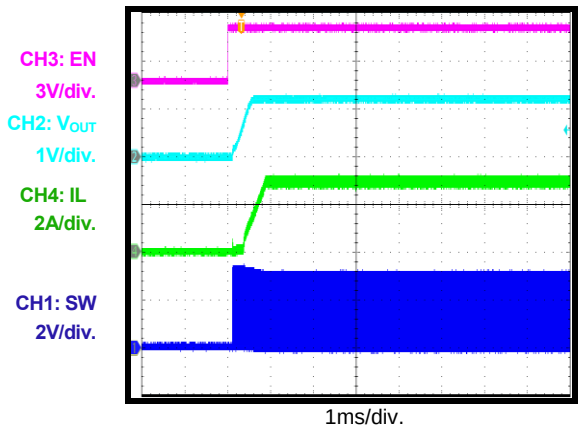
I_{OUT} = 0A



1ms/div.

Start-Up through EN

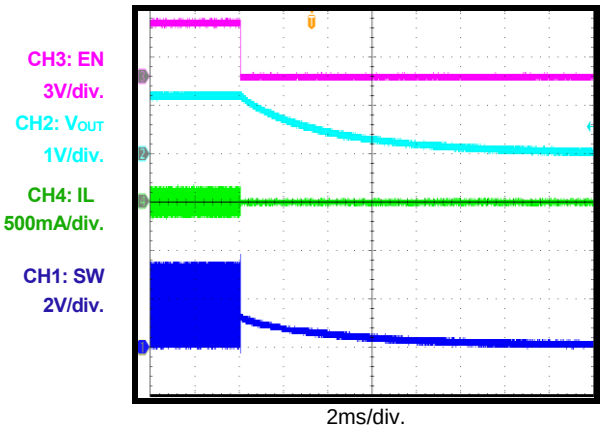
I_{OUT} = 3A



1ms/div.

Shutdown through EN

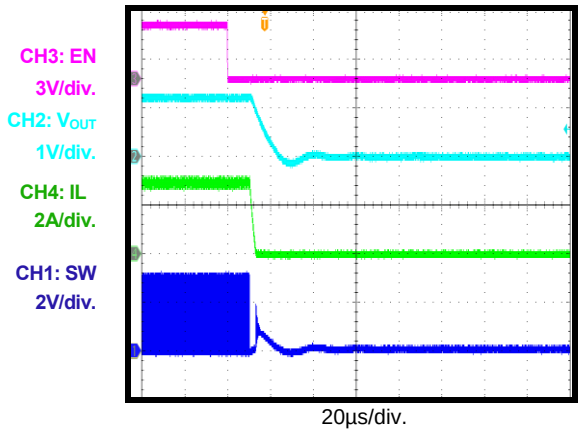
I_{OUT} = 0A



2ms/div.

Shutdown through EN

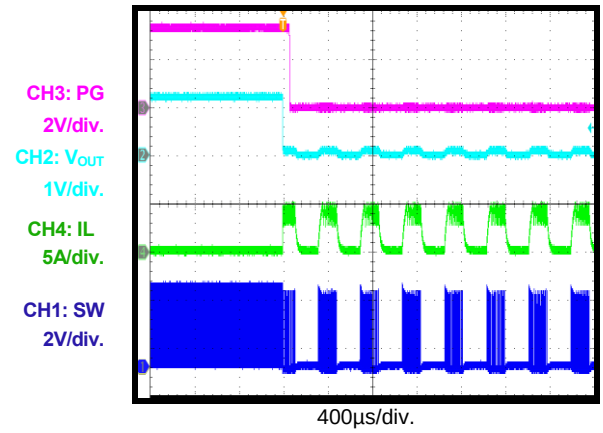
I_{OUT} = 3A



20µs/div.

SCP Entry

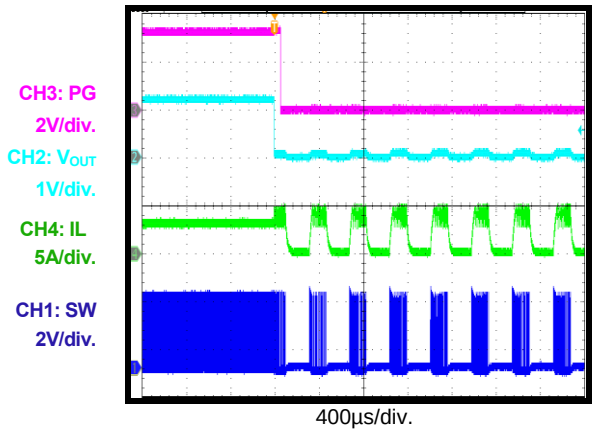
I_{OUT} = 0A



400µs/div.

SCP Entry

I_{OUT} = 3A



400µs/div.

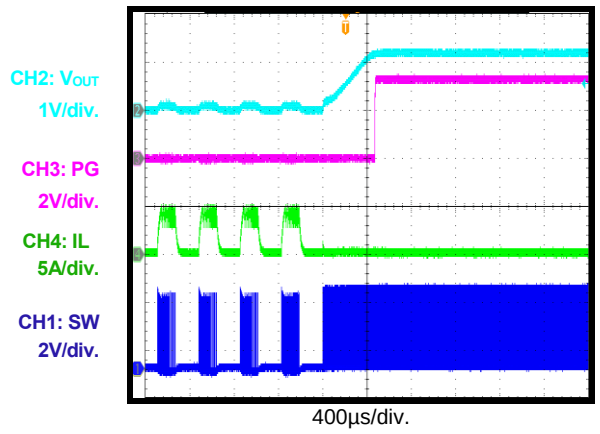
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 1.2V, L = 1µH, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

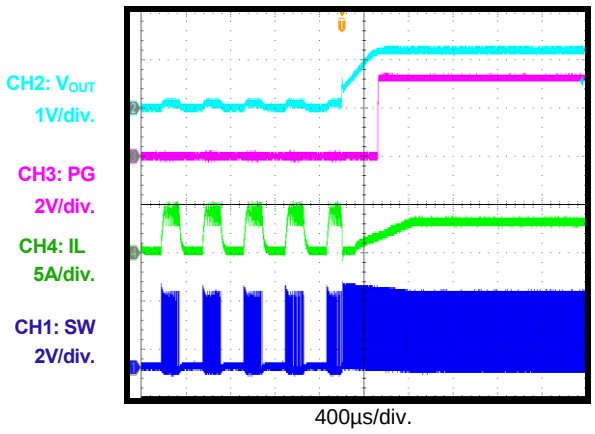
SCP Recovery

I_{OUT} = 0A

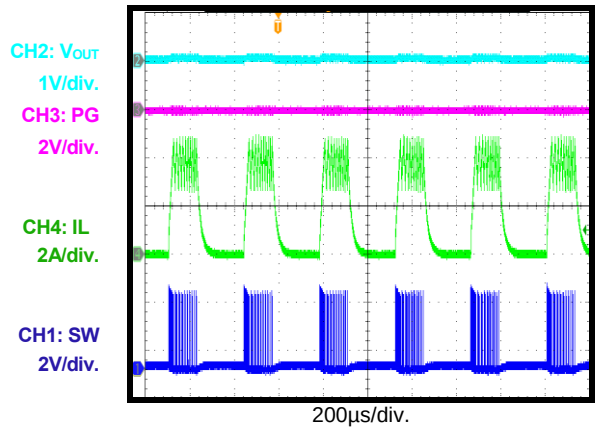


SCP Recovery

I_{OUT} = 3A

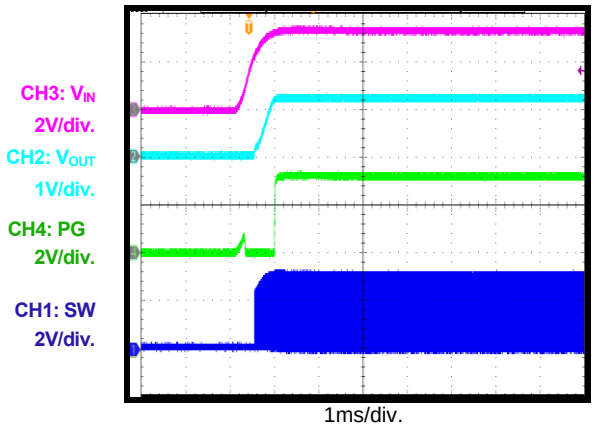


Short Circuit



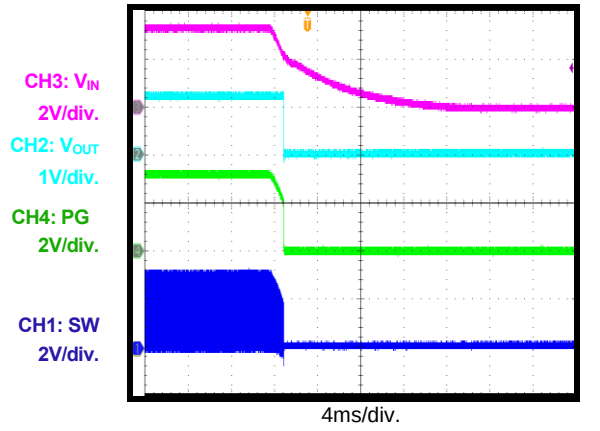
PG Start-Up through VIN

I_{OUT} = 3A



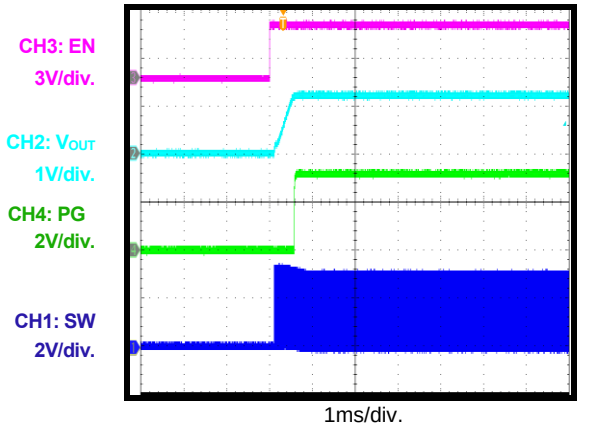
PG Shutdown through VIN

I_{OUT} = 3A



PG Start-Up through EN

I_{OUT} = 3A



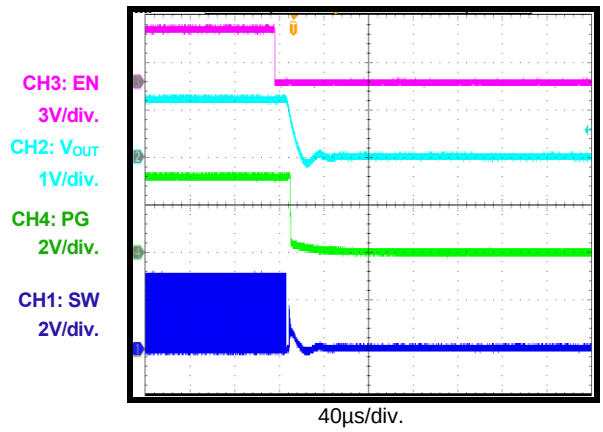
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 1.2V, L = 1µH, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

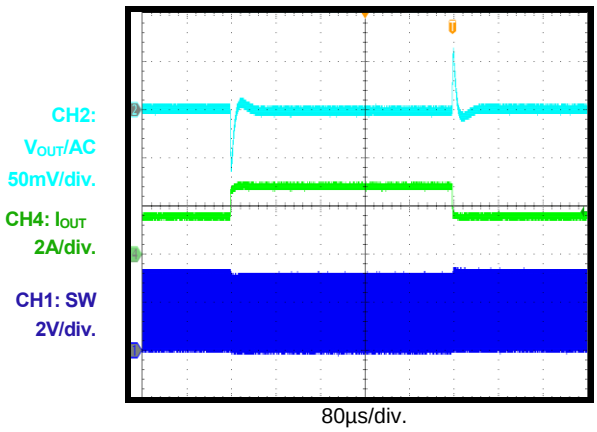
PG Shutdown through EN

I_{OUT} = 3A



Load Transient

I_{OUT} = 1.5 to 3A, 1A/µs



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

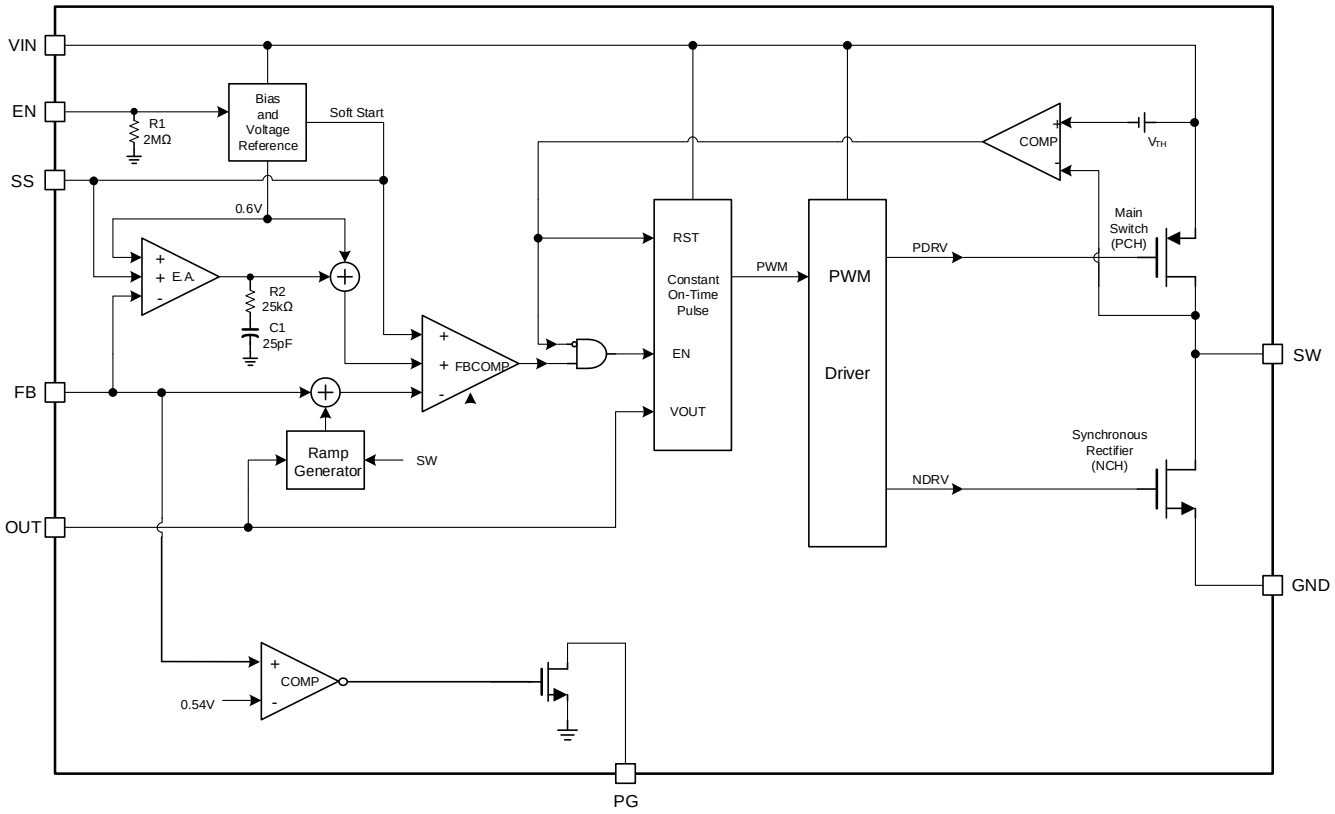


Figure 1: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

OPERATION

The MPQ2179 uses constant-on-time (COT) control with input voltage feed-forward to stabilize the switching frequency across the full input voltage range. The device achieves 3A of peak output current from a 2.5V to 5.5V input voltage range, with excellent load and line regulation. The output voltage can be regulated to as low as 0.6V. A 100% maximum duty cycle can be reached in dropout.

Constant-On-Time (COT) Control

Compared to fixed frequency PWM control, constant on-time (COT) control offers a simpler control loop and faster transient response. To prevent inductor current runaway during load transient, the MPQ2179 switching cycles have a fixed minimum off time. When the low-side MOSFET (LS-FET) turns on, it remains on for at least as long as $t_{MIN-OFF}$. Then the high-side MOSFET (HS-FET) turns on when the feedback voltage (V_{FB}) drops below the reference voltage (V_{REF}). This indicates an insufficient output voltage. By using input voltage feed-forward, the MPQ2179 maintains a nearly constant switching frequency across the input and load ranges. The switching pulse on time can be calculated with Equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 400ns \quad (1)$$

To improve frequency stability and reduce the output voltage ripple, the part operates in forced continuous conduction mode (FCCM).

Enable (EN)

EN is a digital control pin that can turn the regulator on and off. When EN is pulled below the falling threshold voltage (0.4V), the chip shuts down. Force EN above its rising threshold voltage (1.2V) to turn the part on. Leave EN floating or pull it down to ground to disable the MPQ2179. There is an internal 2MΩ resistor connected from the EN pin to ground.

When the device is disabled, the part automatically goes into output discharge mode, and its internal discharge MOSFET provides a resistive discharge path for the output capacitor.

Soft Start (SS)

The MPQ2179 has an external soft start (SS) pin that ramps up the output voltage at a controlled slew rate to avoid overshoot at start-up. The SS pin's charge current is typically 3µA.

The soft-start time (t_{SS}) is determined by the SS capacitor. t_{SS} can be calculated with Equation (2):

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times 0.6V}{I_{SS}(\mu A)} \quad (2)$$

Where C_{SS} is the external SS capacitor, and I_{SS} is the internal 3µA SS charge current. The minimum SS capacitor is recommended to be 1nF.

Peak and Valley Current Limit

Both the P-channel MOSFET (also called the HS-FET) and N-channel MOSFET (also called the LS-FET) have current limit protection. When the inductor current (I_L) reaches the HS-FET peak current limit (typically 5A) during the HS-FET on period, the HS-FET is forced off immediately to prevent the current from rising further. Then the LS-FET turns on, and stays on until I_L drops below the LS-FET valley current limit (typically 3.5A). The HS-FET turns on once I_L has dropped to a sufficiently low threshold. The MPQ2179 remains in hiccup mode until the current drops. This current limit scheme prevents current runaway in overload and short-circuit events.

Short-Circuit Protection (SCP) and Recovery

If the output is shorted to ground, the MPQ2179 initiates short-circuit protection (SCP) when the inductor current reaches the current limit. The device tries to recover with hiccup mode. The IC disables the output power stage and begins discharging the SS voltage. The device restarts with a full soft-start once the SS voltage is fully discharged. This hiccup process is repeated until the fault is removed.

Output Over-Voltage Protection (V_{OUT} OVP)

The MPQ2179 monitors a resistor-divided feedback voltage to detect over-voltage (OV) conditions. If the feedback voltage (V_{FB}) rises above 115% of the reference voltage (V_{REF}), the controller enters a dynamic regulation period.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

During this period, the LS-FET stays until the LS-FET current drops to -1.2A. This discharges the output and tries to keep the output voltage within the normal range.

If the OV condition still exists after this process, the LS-FET turns on after an 1.5μs time delay. The device exits this regulation period when feedback voltage drops below 105% of the reference voltage. If dynamic regulation cannot limit V_{OUT}, and the input detect a 6.1V input voltage, input OVP occurs. Then the MPQ2179 stops switching, and does not resume normal operation until the input voltage drops below 6V.

Power Good Indicator

The MPQ2179 has one power good (PG) output to indicate normal operation after the soft-start time. PG is the open drain of an internal MOSFET, which has a maximum $R_{DS(ON)}$ below 400Ω. PG can be connected to VIN or an external voltage source through an external a resistor (e.g. 100kΩ).

After the input voltage is applied, the MOSFET turns on, and PG is pulled to GND before soft start is ready. After V_{FB} reaches 90% of V_{REF}, PG is pulled high by the external voltage source. When V_{FB} drops to 85% of V_{REF}, the PG voltage is pulled to GND to indicate an output failure.

If VIN and EN are not available, and PG is pulled up by an external power supply, PG will self-bias and assert. If a 100kΩ pull-up resistor is used, the voltage on the pin is below 0.7V.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage. Select a feedback resistor (R1) that reduces the V_{OUT} leakage current. Generally, it is recommended for R1 to be between 10kΩ and 100kΩ. R2 can then be calculated with Equation (3):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6} - 1} \quad (3)$$

Figure 2 shows the feedback circuit.

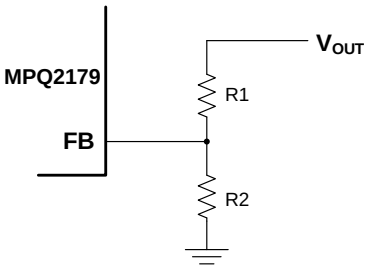


Figure 2: Feedback Network

Table 1 lists the recommended resistors value for common output voltages.

Table 1: Resistor Values for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.0	30.9 (1%)	47 (1%)
1.2	100 (1%)	100 (1%)
1.8	36 (1%)	18 (1%)
2.5	51 (1%)	16 (1%)
3.3	68 (1%)	15 (1%)

Frequency Scales Down at Low V_{IN}

At heavy loads, the voltage on the HS-FET drops while t_{ON} increases, and the duty cycle is extended. If the minimum off time is reached when there is a low input voltage under a heavy load, the frequency scales down. To maintain a constant switching frequency, a higher output voltage requires a higher V_{IN} under heavy loads. For a 1.8V output, the input voltage must exceed 3V to keep the frequency above 2MHz for 3A loads.

The input voltage when the frequency starts to scale down can be estimated with Equation (4):

$$V_{IN} = \frac{V_{OUT} + R_{DS(ON)_P} \times I_{OUT}}{1 - \frac{t_{MIN-OFF}}{400 \times 10^{-9}}} \quad (4)$$

Where the maximum $t_{MIN-OFF}$ is 125ns. (7)

Note:

7) Guaranteed by design and bench characterization. Not tested in production.

Selecting the Inductor

Most applications work best with a 0.47µH to 1.5µH inductor. Select an inductor with a DC resistance less than 25mΩ to optimize efficiency.

High-frequency, switch-mode power supplies with magnetic devices can have strong electronic magnetic inference. It is not recommended to use an unshielded power inductor, as they do not provide sufficient magnetic shielding. Shield inductors (e.g. metal alloy inductor or multiplayer chip power inductor) are recommended because they effectively reduce magnetic interference.

For most designs, estimate the inductance value can be estimated with Equation (5):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}} \quad (5)$$

Where ΔI_L is the inductor ripple current.

Choose an inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (6):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (6)$$

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current to the converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10µF capacitor is sufficient. Higher output voltages may require a 22µF capacitor to increase system stability.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

The input capacitor requires an adequate ripple current rating because it absorbs the input switching current. Estimate the RMS current in the input capacitor with Equation (7):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (7)$$

The worst case occurs at V_{IN} = $2V_{OUT}$, calculated with Equation (8):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (8)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality, ceramic 0.1µF capacitor as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (9):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

Selecting the Output Capacitor

The output capacitor (C2) stabilizes the DC output voltage. Ceramic capacitors are recommended, as well as low-ESR capacitors to limit the output voltage ripple. Estimate the output voltage ripple with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (10)$$

Where L_1 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and causes most of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (11)$$

Ceramic capacitors with X7R or X5R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

For a 3A load, a 22µF capacitor with a 0805 package (or a larger capacitor) is recommended to reduce the output voltage ripple during steady state operation and load transient. To see the detailed output voltage ripple performance, see the Typical Performance Characteristics section on page 10.

The output capacitor value can be smaller for applications with a lower current, or if a larger-value output voltage ripple is allowed. However, to ensure loop stability, the output capacitor should never be below 10µF, or smaller than a 1206 package.

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (12)$$

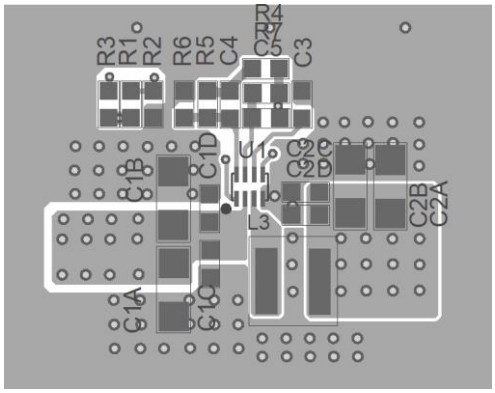
The characteristics of the output capacitor also affect the stability of the regulation system.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

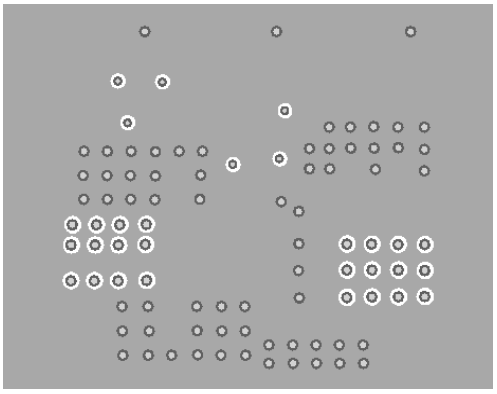
PCB Layout Guidelines

Proper layout of the switching power supplies is important, and sometimes critical for proper function. For the high-frequency switching converter, poor layout design can result in poor line or load regulation, as well as stability issues. For the best results, refer to Figure 3 and follow the guidelines below.

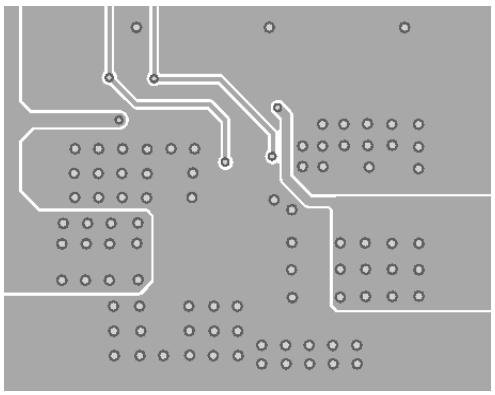
1. Place the high-current paths (GND, VIN, and SW) close to the device with short, direct, and wide traces.
2. Place the input capacitor as close as possible to the VIN and GND pins.
3. The output capacitor for GND must be close to the GND pins.
4. Place the external feedback resistors next to the FB pin.
5. Keep the switching node (SW) short, and route it away from the feedback network.
6. Keep the output voltage sense line as short as possible, and route it away from the power inductor. Do not place this line close to surrounding inductors or SW.



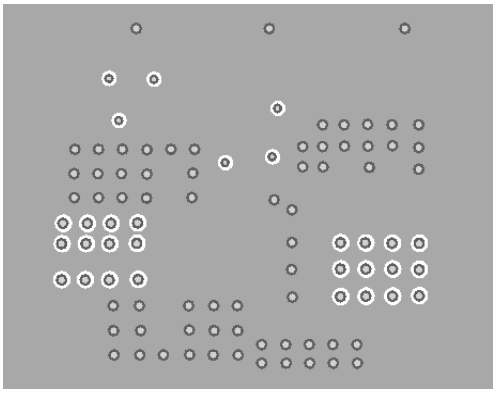
Top Layer



Inner Layer 1



Inner Layer 2



Bottom Layer

Figure 3: Recommended PCB Layout

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS

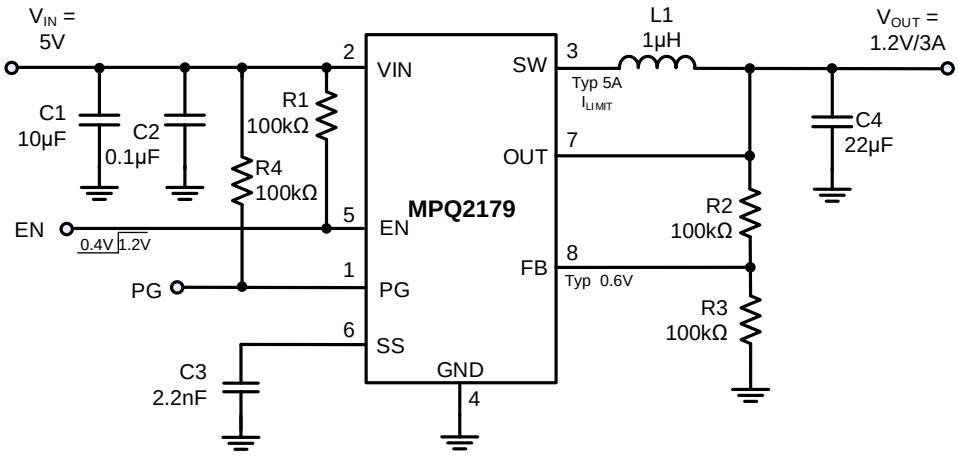


Figure 4: 1.2V Output Application Circuit for the MPQ2179

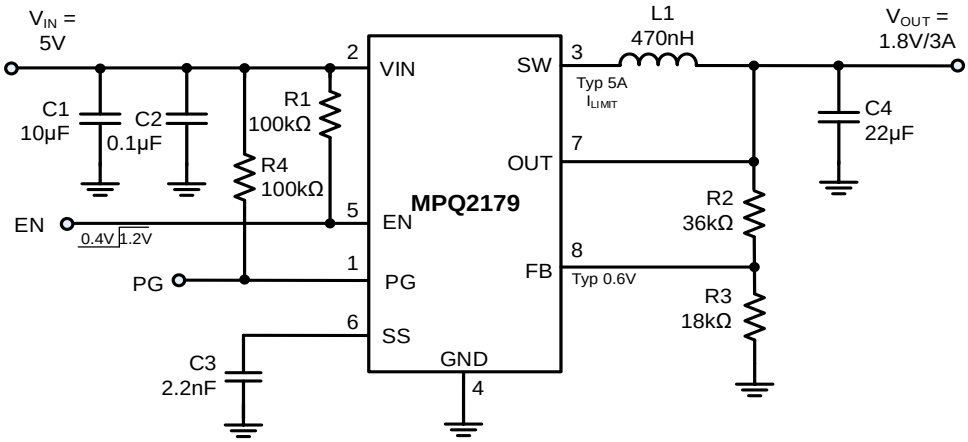


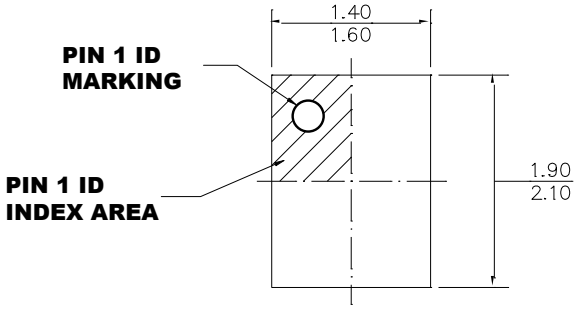
Figure 5: 1.8V Output Application Circuit for the MPQ2179

.

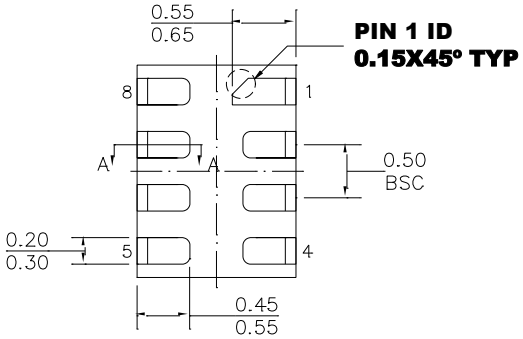
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

PACKAGE INFORMATION

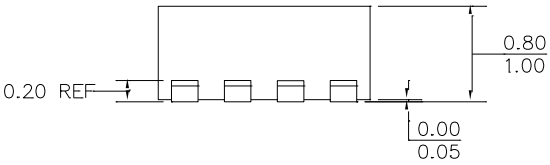
QFN-8 (1.5mmx2mm)
Wettable Flank



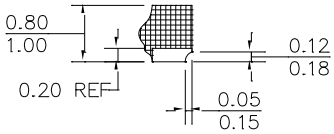
TOP VIEW



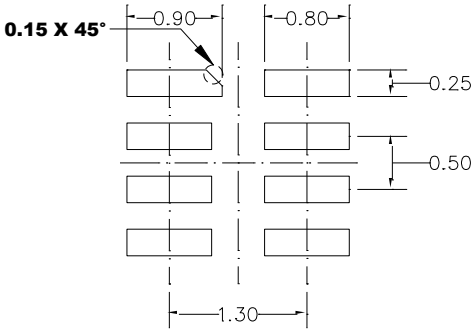
BOTTOM VIEW



SIDE VIEW



SECTION A-A



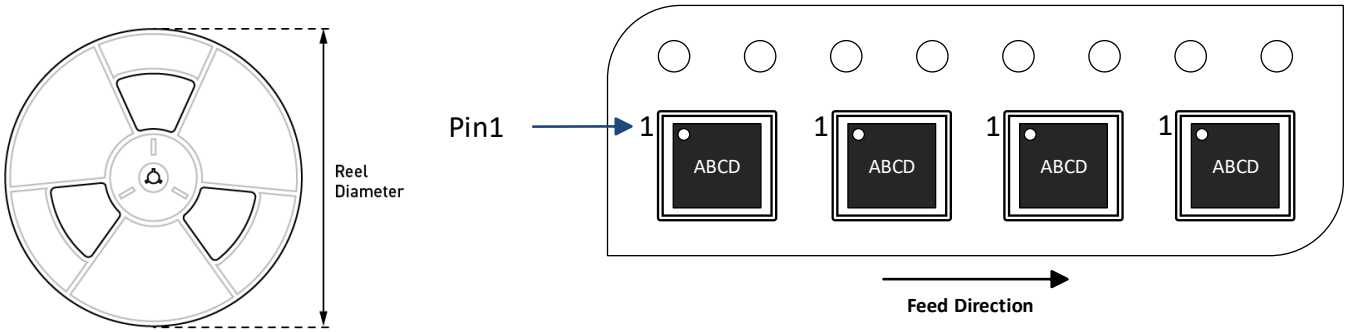
RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ2179GQHE–Z MPQ2179GQHE-AEC1–Z	QFN-8 (1.5mmx2mm)	5000	N/A	N/A	13in	8mm	4mm

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	2/23/2021	Initial Release	-

NOTICE: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.