MPQ2177F

6V, 1A, 2.5MHz, AAM Mode, Synchronous Step-Down Converter with Power Good and Soft Start, AEC-Q100 Qualified

DESCRIPTION

The MPQ2177F is a monolithic, step-down switch-mode converter with built-in internal power MOSFETs. It achieves up to 1A of continuous output current (I_{OUT}) across a 2.5V to 6V input voltage (V_{IN}) range, with excellent load and line regulation. The output voltage (V_{OUT}) can be regulated to as low as 0.6V.

The constant-on-time (COT) control scheme provides fast transient response and eases loop stabilization. Fault protections include cycle-by-cycle current limiting and thermal shutdown.

The MPQ2177F is ideal for a wide range of applications, including automotive infotainment systems, clusters, and telematics.

The MPQ2177F requires a minimal number of readily available, standard external components. It is available in an ultra-small QFN-8 (1.5mmx2mm) package, and is AEC-Q100 qualified.

FEATURES

- Designed for Automotive Applications
  - Wide 2.5V to 6V Operating Input Voltage (V_{IN}) Range
  - Up to 1A Output Current (I_{OUT})
  - 1% Feedback (FB) Accuracy
  - -40°C to +150° Operating Junction Temperature (T_J)
- Improved Battery Life
  - 21µA Sleep Mode Quiescent Current (I_Q)
  - Advanced Asynchronous Modulation (AAM) Mode Increases Efficiency During Light Loads
- High Performance for Improved Thermals
  - 60mΩ and 36mΩ Internal Power MOSFETs
- Optimized for EMC and EMI Reduction
  - 2.5MHz Switching Frequency (f_{SW})
  - MeshConnect™ Flip-Chip Package
- Optimized for Board Size and BOM
  - Built-In Internal Power MOSFETs
  - Integrated Compensation Network
  - Fixed-Output Options (1): 0.7V, 0.75V, 0.8V, 0.85V, 0.88V, 0.9V, 1.05V, 1V, 1.1V, 1.2V, 1.25V, 1.5V, 1.8V, 2.5V, 2.8V, and 3.3V
- Additional Features
  - Enable (EN) for Power Sequencing
  - Power Good (PG)
  - 100% Duty Cycle
  - External Soft Start (SS) Control
  - Output Discharge
  - Output Over-Voltage Protection (OVP)
  - Short-Circuit Protection (SCP) with Hiccup Mode
  - Available in a Compact QFN-8 (1.5mmx2mm) Package with Wettable Flanks
  - Available in AEC-Q100 Grade 1
- Functional Safety System Design Capable
  - MPSafe ™ Compatible – Functional Safety Supporting Document Available

MPSafe™ FuSa Compatible

APPLICATIONS

- Automotive Infotainment Systems
- Camera Modules
- Key Fobs
- Automotive Clusters
- Automotive Telematics
- Industrial Supplies
- Battery-Powered Devices

Note:

1) See the Ordering Information section on page 3 for additional fixed-output options.

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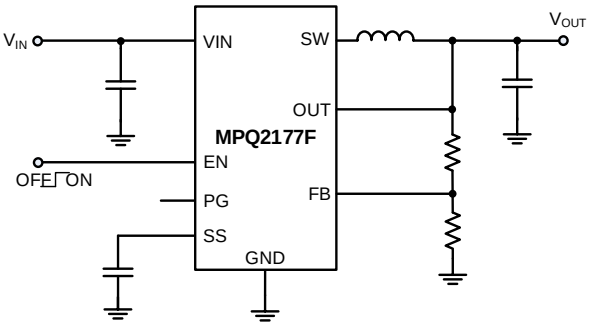
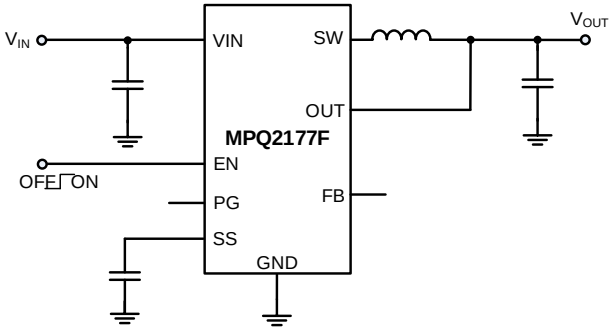
TYPICAL APPLICATION



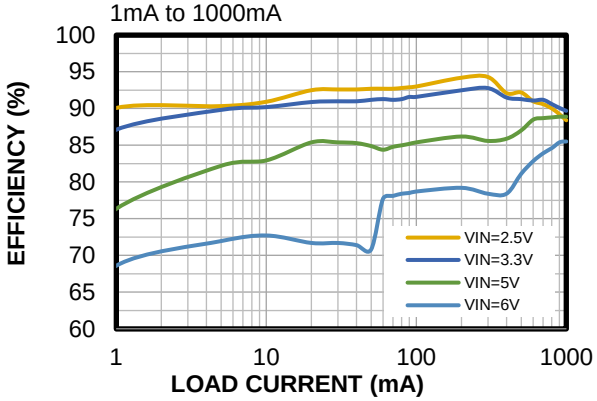
Adjustable-Output Version



Fixed-Output Versions

Efficiency vs. Load Current

AAM mode, V_{OUT} = 1.2V,
f_{SW} = 2.5MHz, L = 2.2µH (DCR = 21.35mΩ),
1mA to 1000mA



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ORDERING INFORMATION

Part Number* (2)	Output Voltage	Package	Top Marking	MSL Rating**
MPQ2177FGQHE-AEC1 ***	Adjustable	QFN-8 (1.5mmx2mm)	*See Below*	1
MPQ2177FGQHE-12-AEC1***	Fixed 1.2V			
MPQ2177FGQHE-18-AEC1***	Fixed 1.8V			

* For Tape & Reel, add suffix -Z (e.g. MPQ2177FGQHE-AEC1-Z).

** Moisture Sensitivity Level Rating

*** Wettable flank

Note:

2) Contact an MPS FAE for more details on additional fixed-output options.

TOP MARKING (MPQ2177FGQHE-AEC1)

$\overline{\text{PX}}$
LL

PX: Product code of MPQ2177FGQHE-AEC1
LL: Lot number

TOP MARKING (MPQ2177FGQHE-12-AEC1)

$\overline{\text{QB}}$
LL

QB: Product code of MPQ2177FGQHE-12-AEC1
LL: Lot number

TOP MARKING (MPQ2177FGQHE-18-AEC1)

$\overline{\text{QC}}$
LL

QC: Product code of MPQ2177FGQHE-18-AEC1
LL: Lot number

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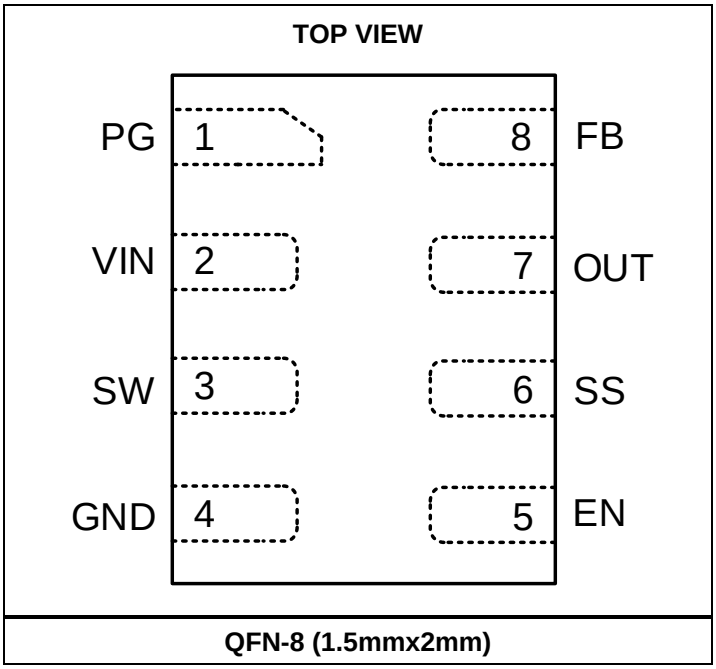
PACKAGE REFERENCE



QFN-8 (1.5mmx2mm)

PIN FUNCTIONS

Pin #	Name	Description
1	PG	**Power good indicator.** The PG pin is an open-drain output. Connect PG to a voltage source via an external resistor. If the feedback (FB) voltage (V_{FB}) exceeds 95.5% of the reference voltage (V_{REF}), then PG is pulled high. If V_{FB} drops below 90% of V_{REF}, PG is pulled low to GND. Float this pin if it is not used.
2	VIN	**Supply voltage.** The MPQ2177F operates from a 2.5V to 6V input voltage (V_{IN}) range. A decoupling capacitor is required to prevent large voltage spikes from appearing at the input.
3	SW	**Output switching node.** The SW pin is the drain of the internal P-channel high-side MOSFET (HS-FET). Connect the inductor to SW to complete the converter.
4	GND	**Ground.**
5	EN	**Enable (EN) control.** Pull the EN pin below the falling threshold (0.65V) to turn the chip off; pull EN above the rising threshold (0.9V) to turn the chip on. Connect an internal 2MΩ resistor between EN and GND. Float this pin if it is not used.
6	SS	**Soft start (SS).** Connect a capacitor (C_{SS}) between the SS pin and GND to set the soft-start time (t_{SS}) and avoid start-up inrush current. The minimum recommended soft-start capacitance is 6.8nF.
7	OUT	**Output voltage.** The OUT pin is the output voltage (V_{OUT}) for the power rail and input sense pin. Connect the load to this pin. An output capacitor (C_{OUT}) is required to reduce the V_{OUT} ripple.
8	FB	**Feedback.** Connect the FB pin to an external resistor divider between the output and GND. To set the regulation voltage, V_{FB} is compared to the internal 0.6V V_{REF}. For the fixed-output versions of the MPQ2177F, this pin can be floated.

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ABSOLUTE MAXIMUM RATINGS (3)

SW .....-0.3V (-1.5V for <10ns)
….. ..... to +6.5V (+7.5V for <10ns)
All other pins .....-0.3V to +6.5V
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Continuous power dissipation (T_A = 25°C) (4) (8)
……. 2.2W
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) .....Class 2 (5)
Charged-device model (CDM) .....Class 2b (6)

Recommended Operating Conditions

Supply voltage (V_{IN}) .....2.5V to 6V
Output voltage (V_{OUT}).....0.6V to V_{IN} - 0.5V
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-8 (1.5mmx2mm)
JESD51-7 …..84.....8.1...°C/W (7)
EVQ2177F-QH-00A .....59.....°C/W (8)

Ψ_{JT}

JESD51-7 …..2.85..°C/W (7)
EVQ2177F-QH-00A .....14....°C/W (8)

Notes:

3) Exceeding these ratings may damage the device.
4) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
5) Per AEC-Q100-002.
6) Per AEC-Q100-011.
7) Measured on a JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application, the value of θ_{JC} shows the thermal resistance from junction-to-case bottom, and the Ψ_{JT} value shows the characterization parameter from the junction-to-case top.
8) Measured on an MPS standard EVB: 6.3cmx6.3cm, 2oz. copper thickness, 4-layer PCB. The value of Ψ_{JT} shows the characterization parameter from the junction-to-case top.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6V, T_J = -40°C to +150°C, typical value tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input voltage (V_{IN}) range			2.5		6	V
Under-voltage lockout (UVLO) rising threshold				2.3	2.45	V
UVLO threshold hysteresis				200		mV
Shutdown supply current		V_{EN} = 0V, T_J = 25°C		0.01	1	µA
		V_{EN} = 0V			20	µA
Quiescent supply current		V_{EN} = 2V, V_{FB} = 0.63V, V_{IN} = 3.6V, T_J = 25°C		21	30	µA
		V_{EN} = 2V, V_{FB} = 0.63V, V_{IN} = 3.6V			72	µA
Feedback voltage	V_{FB}	T_J = 25°C, 2.5V ≤ V_{IN} ≤ 5.5V	594	600	606	mV
		2.5V ≤ V_{IN} ≤ 5.5V	591	600	609	
Feedback current	I_{FB}	V_{FB} = 0.63V, adjustable output		50	100	nA
		V_{FB} = 0.63V, 1.2V fixed output		3	8	µA
		V_{FB} = 0.63V, 1.8V fixed output		5	10	µA
Output regulation voltage (fixed-output versions)	V_{OUT_REG}	1.2V fixed output	1.188	1.2	1.212	V
		1.8V fixed output	1.773	1.8	1.827	V
P-channel MOSFET on resistance	$R_{DS(ON)\_P}$	V_{IN} = 5V		60	110	mΩ
N-channel MOSFET on resistance	$R_{DS(ON)\_N}$	V_{IN} = 5V		36	70	mΩ
Zero-current detection (ZCD)				50		mA
Switch leakage		V_{EN} = 0V, V_{IN} = 6V, V_{SW} = 0V or 6V, T_J = 25°C		0	1	µA
		V_{EN} = 0V, V_{IN} = 6V, V_{SW} = 0V or 6V			40	µA
Switching frequency	f_{SW}	V_{IN} = 5V, V_{OUT} = 1.2V, operating in CCM	2000	2500	2800	kHz
Minimum on time (10)	t_{MIN_ON}	V_{IN} = 5V		50		ns
Minimum off time (10)	t_{MIN_OFF}	V_{IN} = 5V		80		ns
P-channel MOSFET peak current limit			1.6	2.5	3.4	A
N-channel MOSFET valley current limit			0.4	1	1.6	A
Soft-start current	I_{SS_ON}		11	21	31	µA
Maximum duty cycle				100		%
Power good (PG) rising threshold		FB rising edge	93	95.5	98	%
PG falling threshold		FB falling edge	86	90	93	%
PG delay	t_{PGD}	PG rising/falling edge		70		µs
PG sink current capability	V_{PG_L}	Sink 1mA			0.4	V
PG logic high voltage	V_{PG_H}	V_{IN} = 5V, V_{FB} = 0.6V	4.9			V
Self-biased PG (9)					0.7	V
PG leakage current/logic high		5V logic high			100	nA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_J = -40°C to +150°C, typical value tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Enable (EN) turn-on delay		EN on to SW active		100		µs
EN turn-off delay		EN off to stop switching		11		µs
EN input logic low voltage			0.4	0.65		V
EN input logic high voltage				0.9	1.2	V
EN pull-down resistor				2		MΩ
Output discharge resistor	R_{DIS}	V_{EN} = 0V, V_{OUT} = 1.2V		120		Ω
EN input current		V_{EN} = 2V		1.2		µA
		V_{EN} = 0V		0		µA
Output over-voltage (OV) rising threshold	V_{OVP}		110	115	120	% of V_{FB}
Output OV hysteresis	V_{OVP_HYS}			10		% of V_{FB}
Output OV delay				2		µs
Low-side (LS) current limit		Current flowing from SW to GND		1.2		A
Absolute V_{IN} over-voltage protection (OVP)		After V_{OUT} OVP is enabled		6.1		V
Absolute V_{IN} OVP hysteresis				160		mV
Thermal shutdown (10)				170		°C
Thermal shutdown hysteresis (10)				20		°C

Notes:

9) V_{IN} = 0V, EN = 0V, PG pulled up from 3V to 6V via a 100kΩ resistor.
10) Guaranteed by design and bench characterization. Not tested in production.

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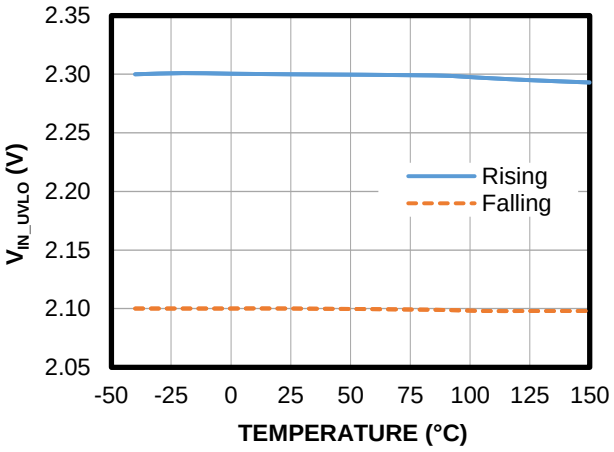
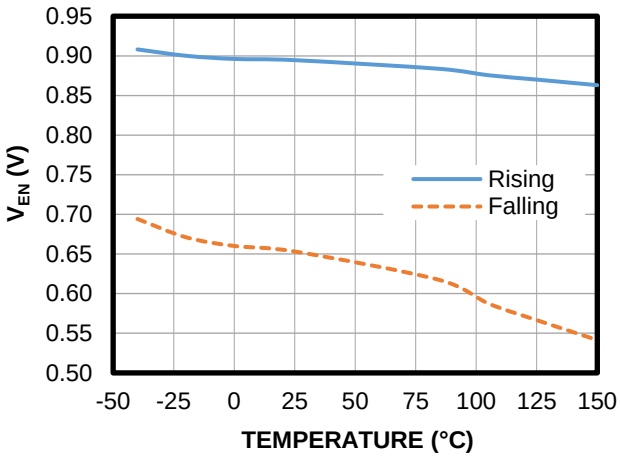
TYPICAL CHARACTERISTICS

V_{IN} = 3.6V, T_J = -40°C to +150°C, unless otherwise noted.

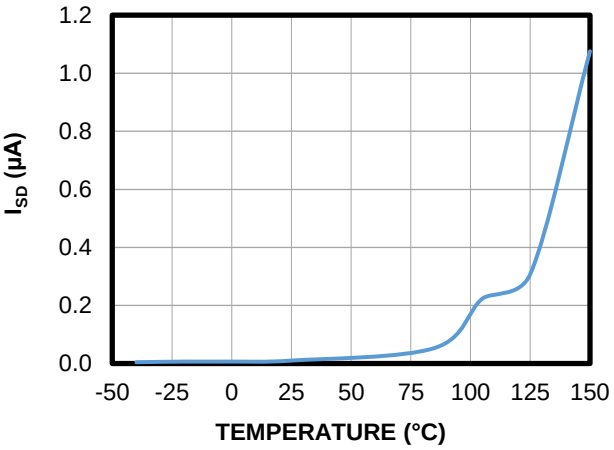
V_{IN} UVLO Threshold vs. Temperature



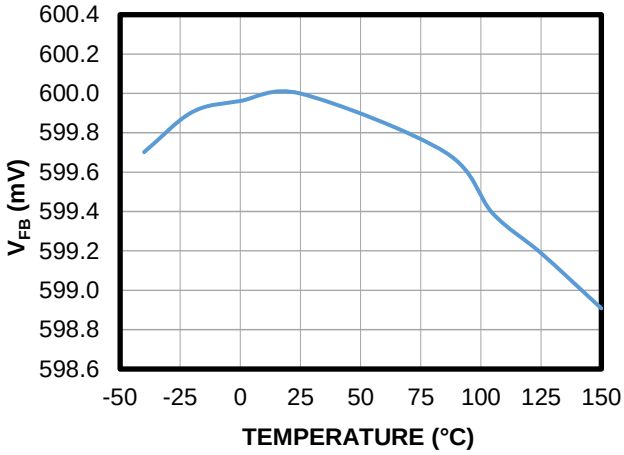
EN Rising and Falling Threshold vs. Temperature



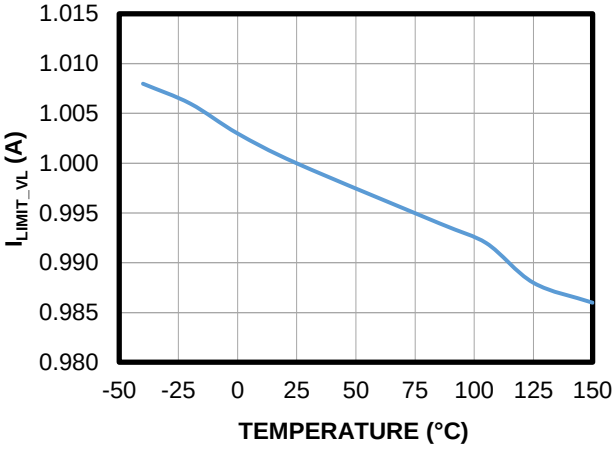
Shutdown Current vs. Temperature



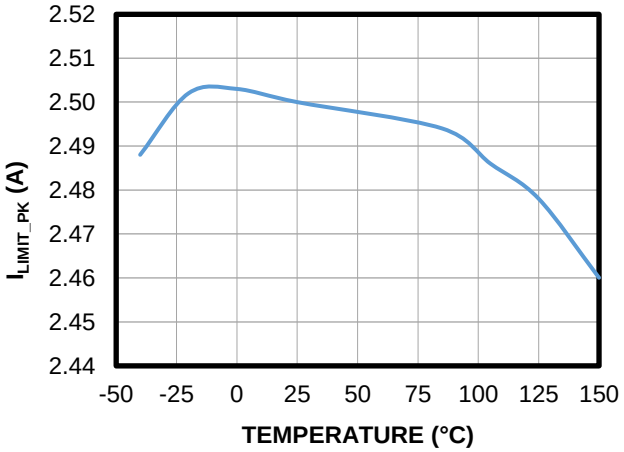
FB Voltage vs. Temperature



N-Channel MOSFET Valley Current Limit vs. Temperature



P-Channel MOSFET Peak Current Limit vs. Temperature



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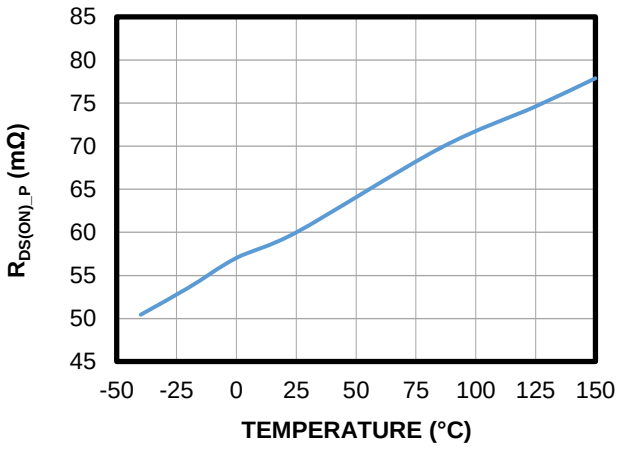
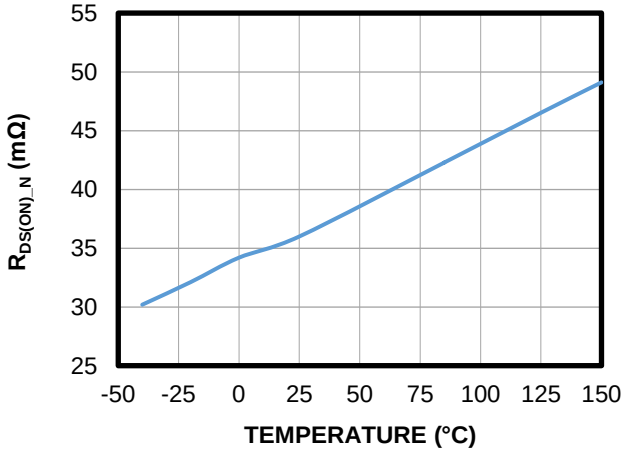
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_J = -40°C to +150°C, unless otherwise noted.

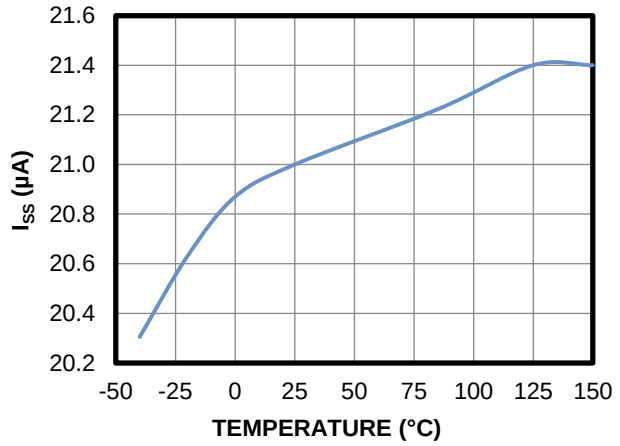
P-Channel MOSFET $R_{DS(ON)}$ vs. Temperature (11)



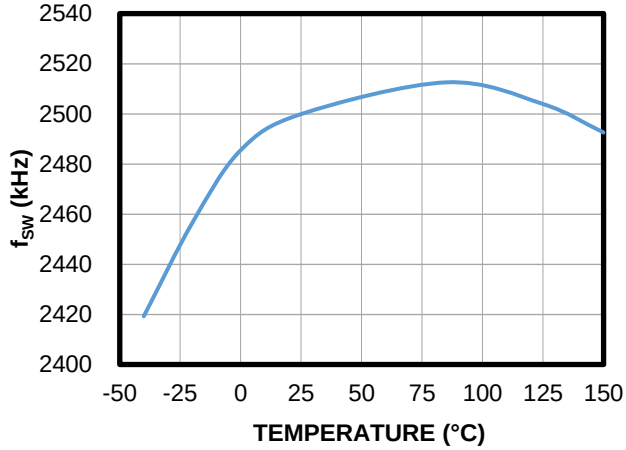
N-Channel MOSFET $R_{DS(ON)}$ vs. Temperature (11)



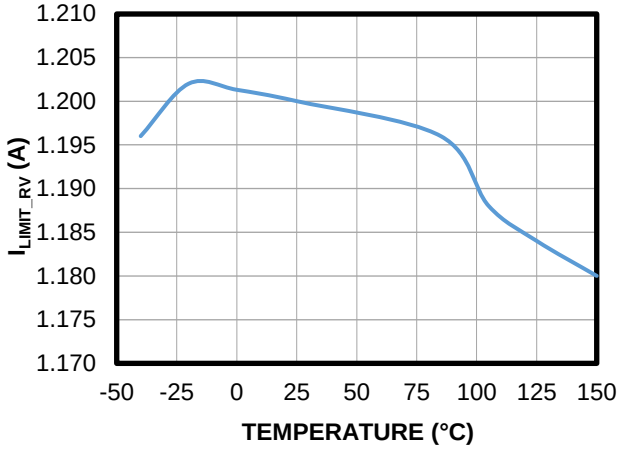
Soft-Start Current vs. Temperature



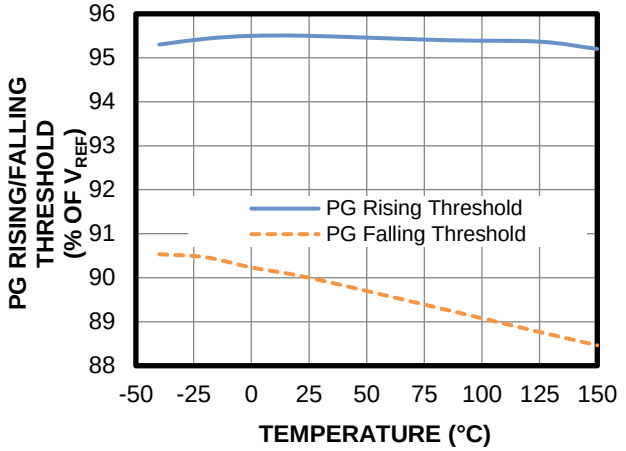
Switching Frequency vs. Temperature (11)



Low-Side Reverse Current Limit vs. Temperature



PG Rising and Falling Threshold vs. Temperature



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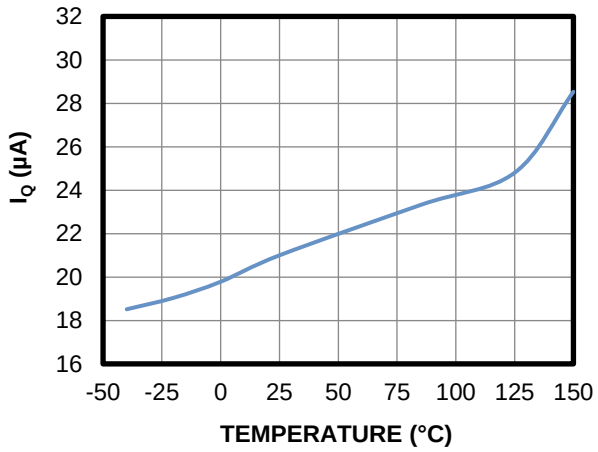
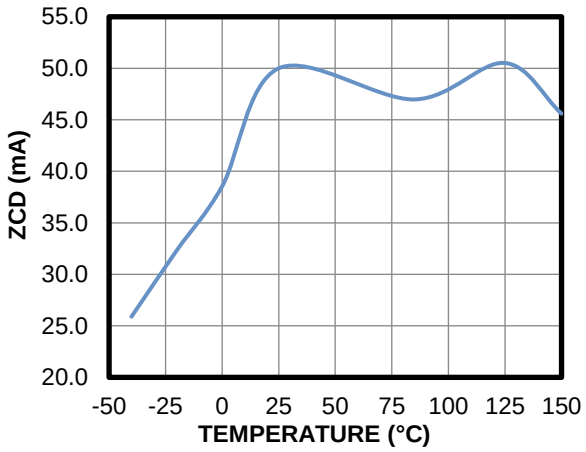
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_J = -40°C to +150°C, unless otherwise noted.

Quiescent Current vs. Temperature



Zero-Current Detection vs. Temperature



Note:

11) The results are tested at V_{IN} = 5V.

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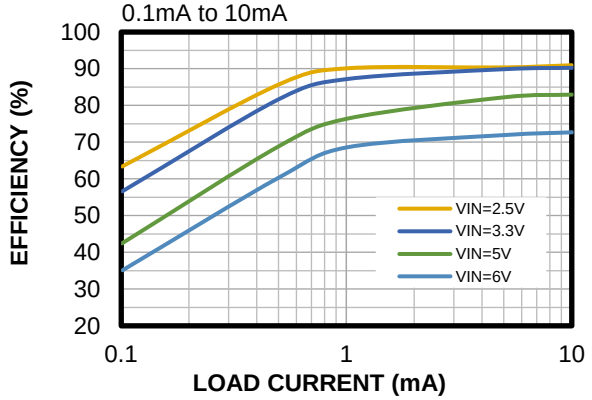
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3V, V_{OUT} = 1.2V, L = 2.2µH, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

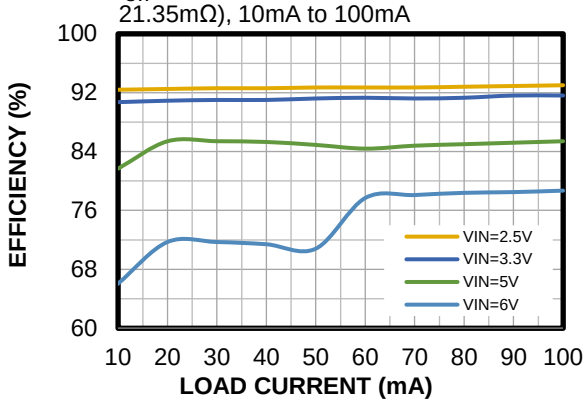
Efficiency vs. Load Current

AAM mode, V_{OUT} = 1.2V, f_{SW} = 2.5MHz, L = 2.2µH (DCR = 21.35mΩ), 0.1mA to 10mA



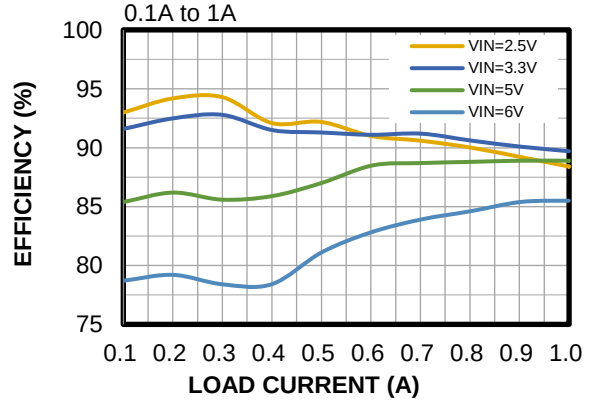
Efficiency vs. Load Current

AAM mode, V_{OUT} = 1.2V, f_{SW} = 2.5MHz, L = 2.2µH (DCR = 21.35mΩ), 10mA to 100mA



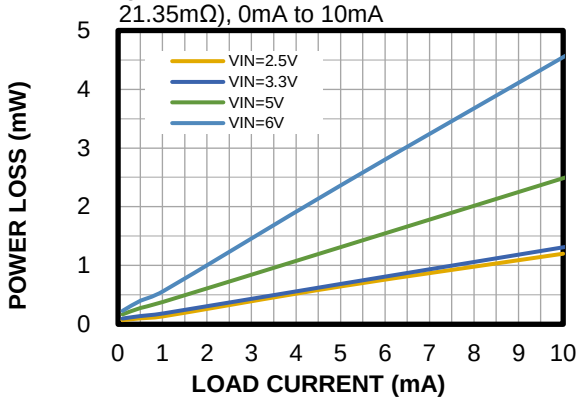
Efficiency vs. Load Current

AAM mode, V_{OUT} = 1.2V, f_{SW} = 2.5MHz, L = 2.2µH (DCR = 21.35mΩ), 0.1A to 1A



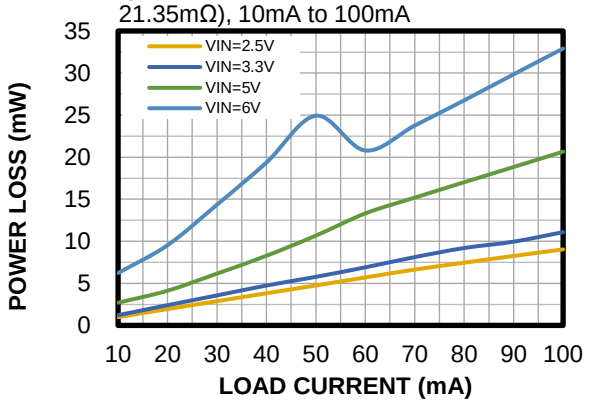
Power Loss vs. Load Current

AAM mode, V_{OUT} = 1.2V, f_{SW} = 2.5MHz, L = 2.2µH (DCR = 21.35mΩ), 0mA to 10mA



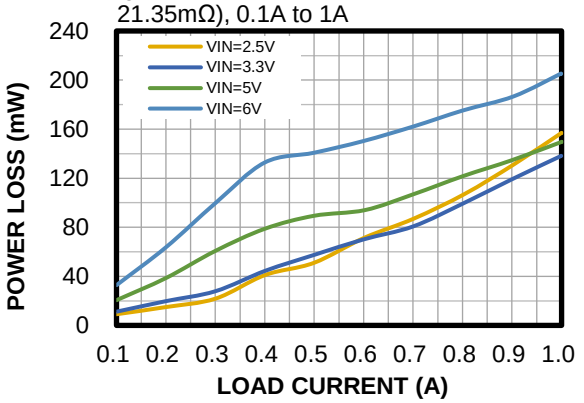
Power Loss vs. Load Current

AAM mode, V_{OUT} = 1.2V, f_{SW} = 2.5MHz, L = 2.2µH (DCR = 21.35mΩ), 10mA to 100mA



Power Loss vs. Load Current

AAM mode, V_{OUT} = 1.2V, f_{SW} = 2.5MHz, L = 2.2µH (DCR = 21.35mΩ), 0.1A to 1A



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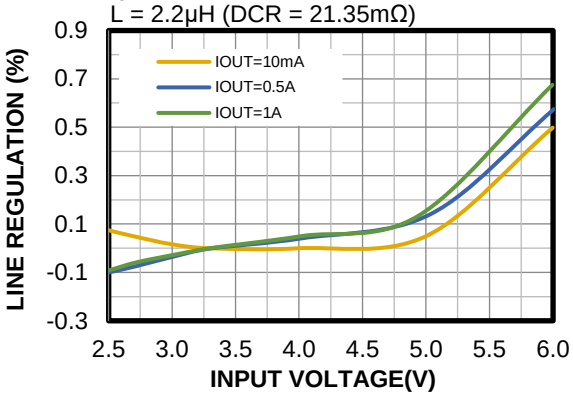
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 1.2V, L = 2.2µH, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

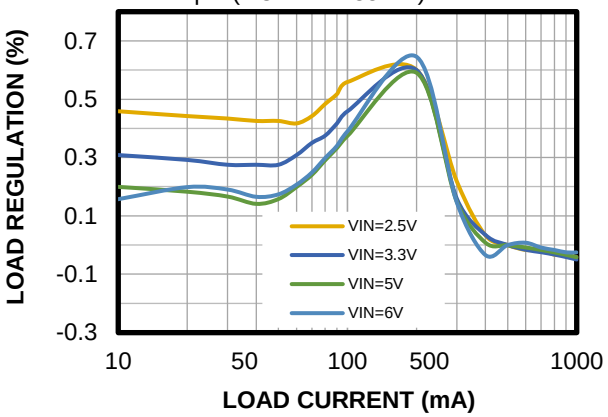
Line Regulation

AAM mode, V_{OUT} = 1.2V,
f_{SW} = 2.5MHz,
L = 2.2µH (DCR = 21.35mΩ)



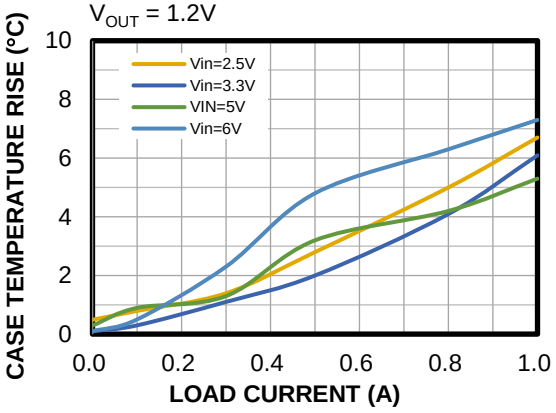
Load Regulation

AAM mode, V_{OUT} = 1.2V,
f_{SW} = 2.5MHz,
L = 2.2µH (DCR = 21.35mΩ)



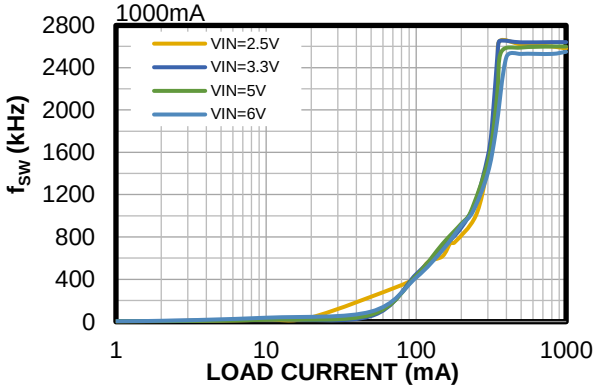
Case Temperature Rise

V_{OUT} = 1.2V



Switching Frequency vs. Load Current

AAM mode, V_{OUT} = 1.2V, f_{SW} = 2.5MHz,
L = 2.2µH (DCR = 21.35mΩ), 1mA to 1000mA



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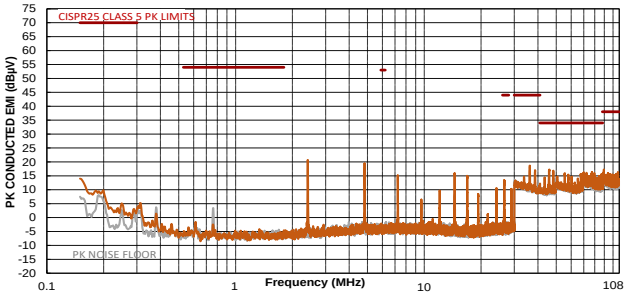
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 6V, V_{OUT} = 1.2V, L = 2.2µH [12], C_{OUT} = 22µF, I_{OUT} = 1A, T_A = 25°C, unless otherwise noted. [13]

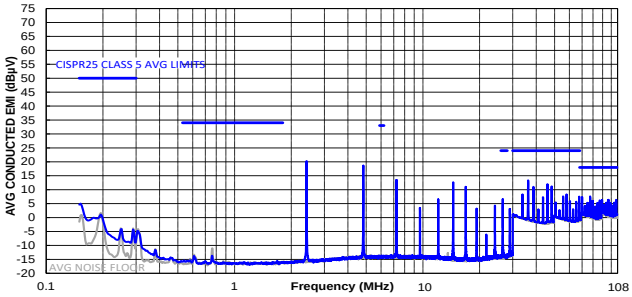
CISPR 25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



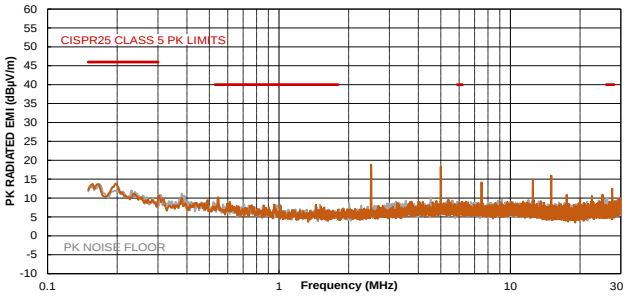
CISPR 25 Class 5 Average Conducted Emissions

150kHz to 108MHz



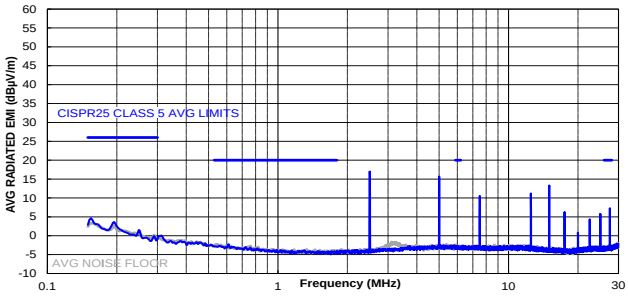
CISPR 25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



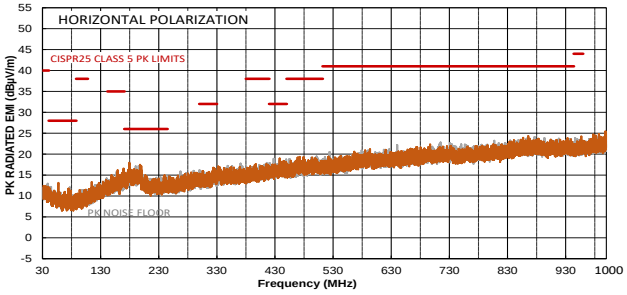
CISPR 25 Class 5 Average Radiated Emissions

150kHz to 30MHz



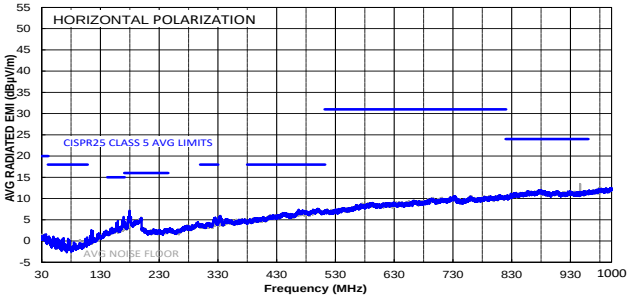
CISPR 25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



CISPR 25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz



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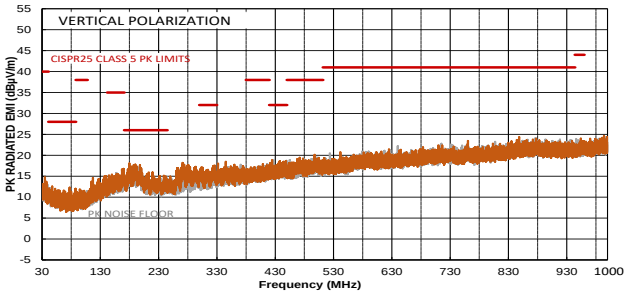
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 6V, V_{OUT} = 1.2V, L = 2.2µH (12), C_{OUT} = 22µF, I_{OUT} = 1A, T_A = 25°C, unless otherwise noted. (13)

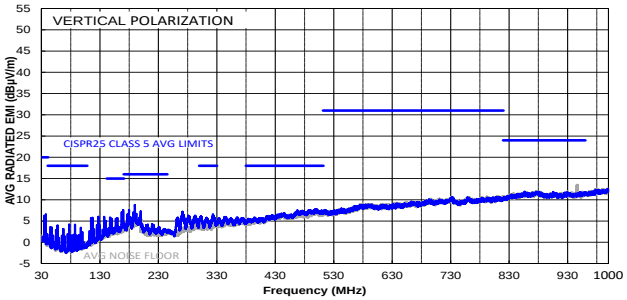
CISPR 25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR 25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



Notes:

12) Inductor part number: XFL4020-222MEB, DCR = 21.35mΩ.

13) The EMC test results are based on the typical application circuit with EMI filters (see Figure 15 on page 29).

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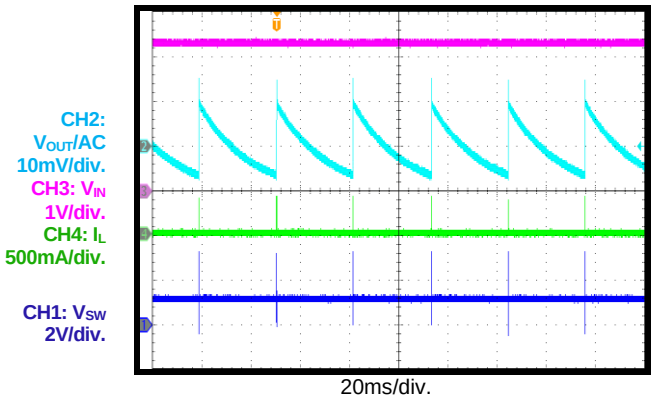
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 1.2V, L = 2.2µH, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

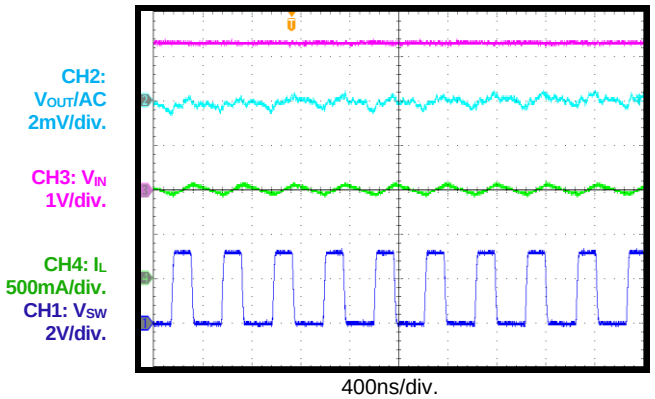
Steady State

I_{OUT} = 0A



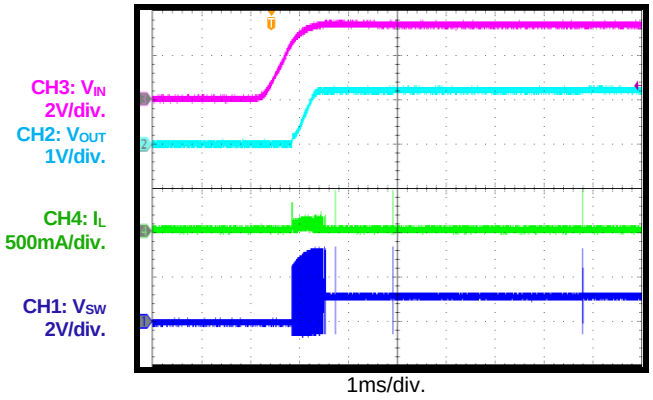
Steady State

I_{OUT} = 1A



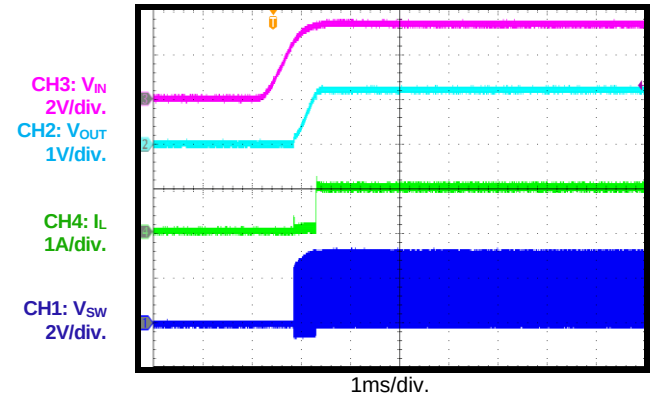
Start-Up through VIN

I_{OUT} = 0A



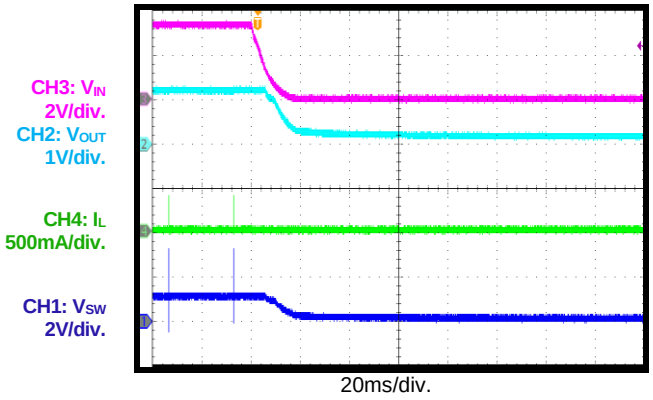
Start-Up through VIN

I_{OUT} = 1A



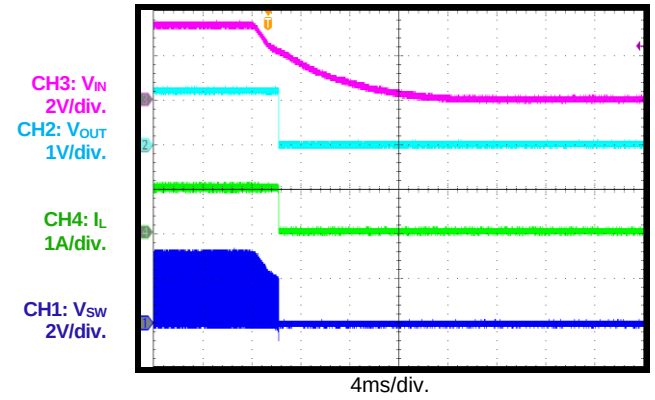
Shutdown through VIN

I_{OUT} = 0A



Shutdown through VIN

I_{OUT} = 1A



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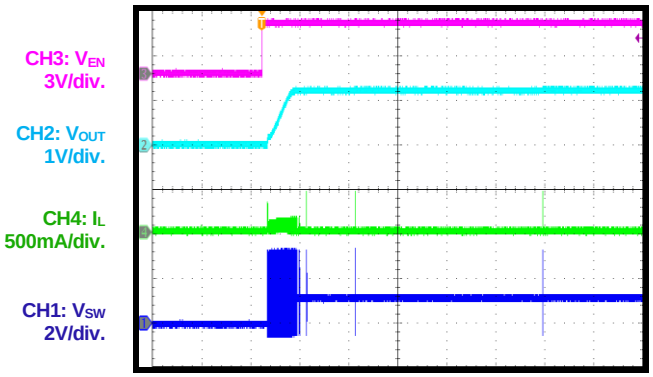
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 1.2V, L = 2.2µH, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

Start-Up through EN

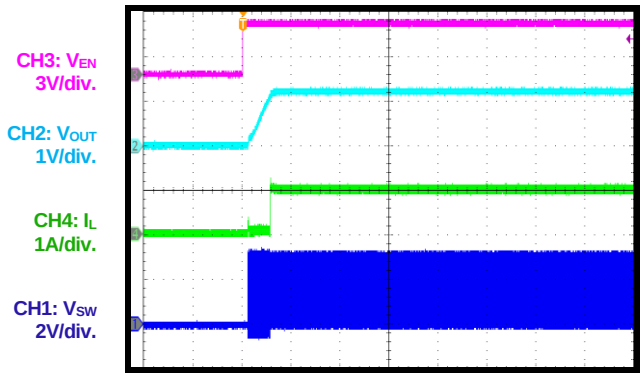
I_{OUT} = 0A



1ms/div.

Start-Up through EN

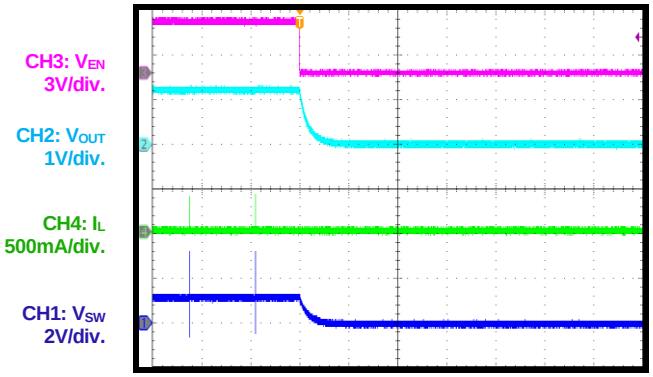
I_{OUT} = 1A



1ms/div.

Shutdown through EN

I_{OUT} = 0A



20ms/div.

Shutdown through EN

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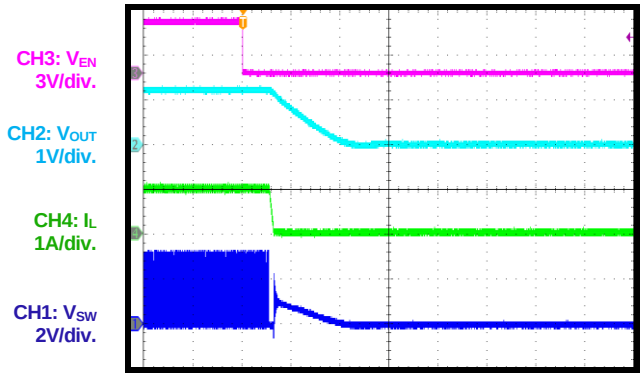
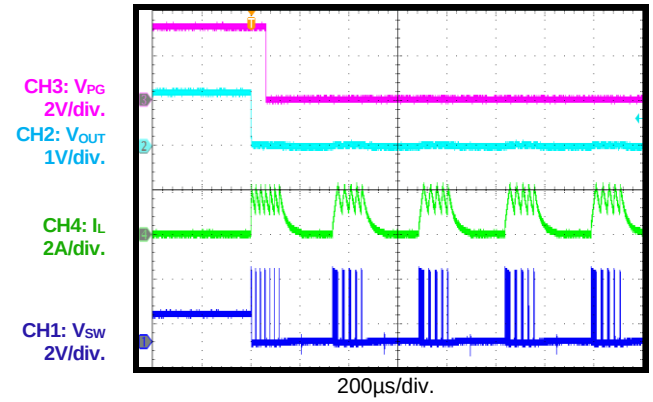


20µs/div.

SCP Entry

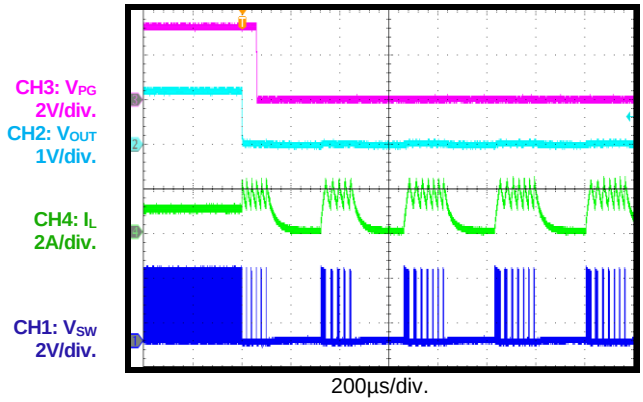
I_{OUT} = 0A



200µs/div.

SCP Entry

I_{OUT} = 1A



200µs/div.

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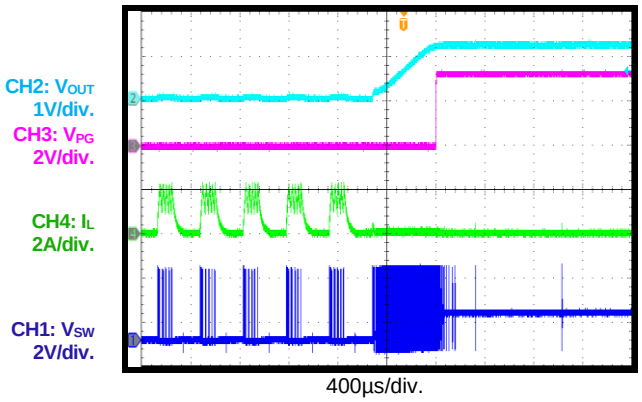
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 1.2V, L = 2.2µH, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

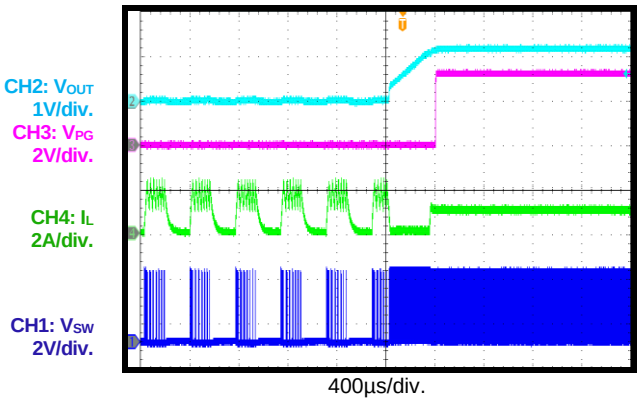
SCP Recovery

I_{OUT} = 0A

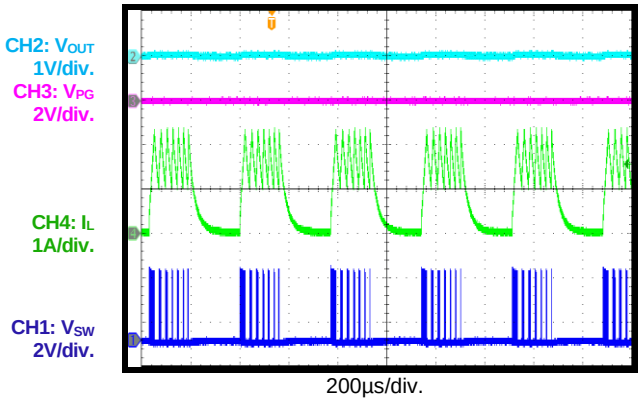


SCP Recovery

I_{OUT} = 1A

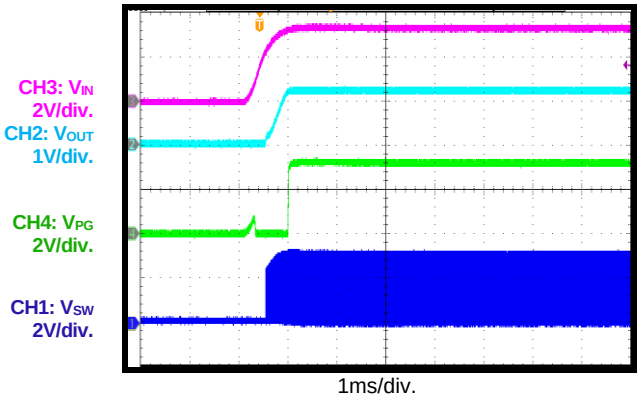


Short-Circuit Protection (SCP)



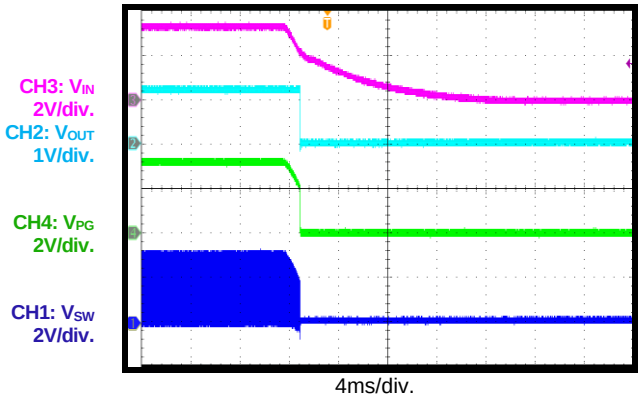
PG in Start-Up through VIN

I_{OUT} = 1A



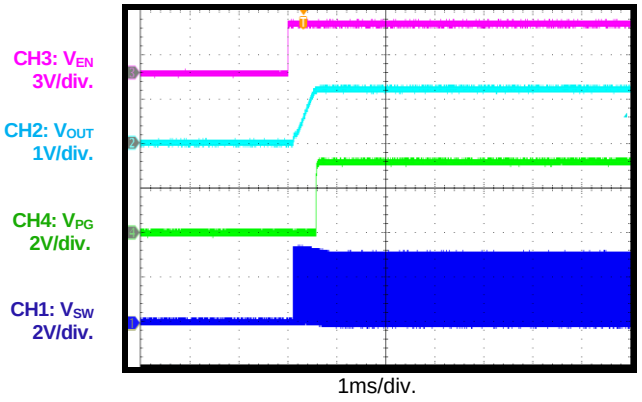
PG in Shutdown through VIN

I_{OUT} = 1A



PG in Start-Up through EN

I_{OUT} = 1A



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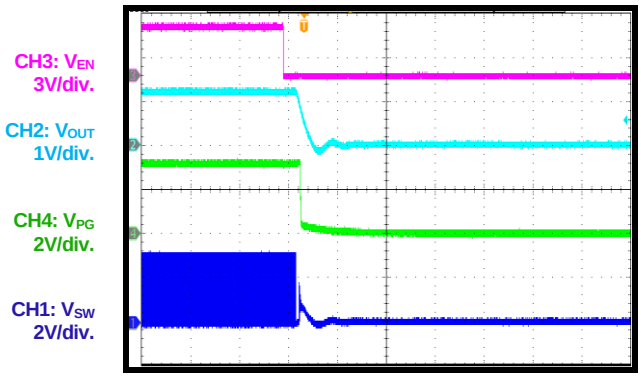
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 1.2V, L = 2.2µH, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

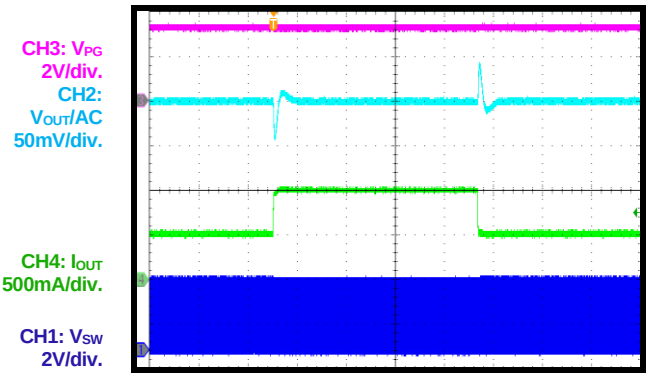
PG in Shutdown through EN

I_{OUT} = 1A



Load Transient Response

I_{OUT} = 0.5A to 1A, 1A/µs



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FUNCTIONAL BLOCK DIAGRAM

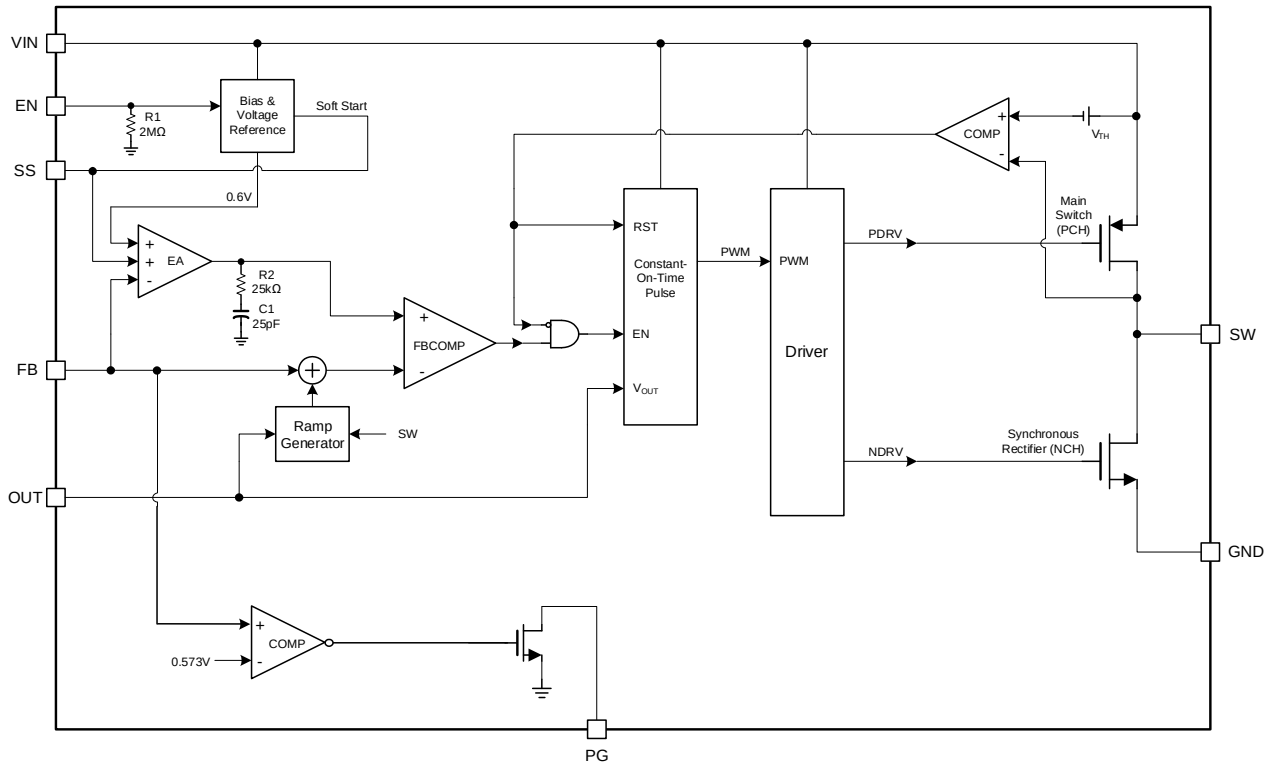

Figure 1: Functional Block Diagram for the Adjustable-Output Version

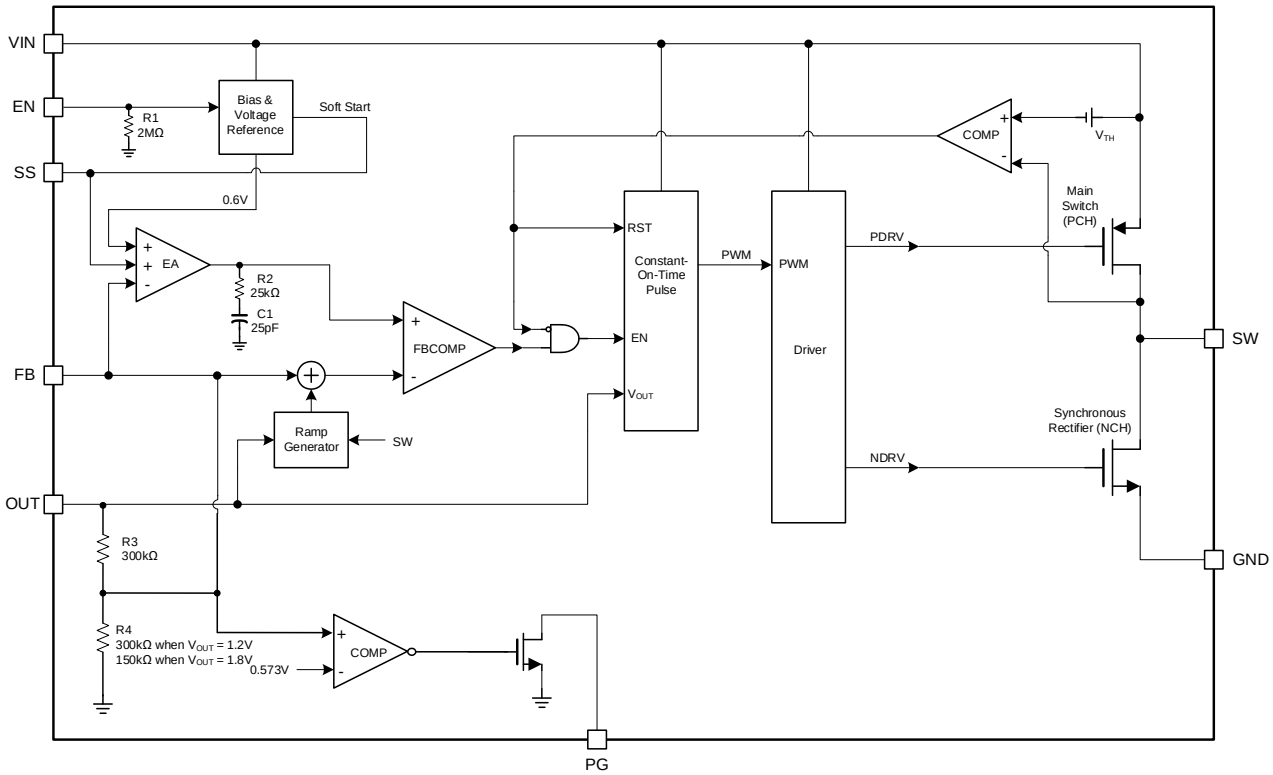

Figure 2: Functional Block Diagram for the Fixed-Output Versions

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OPERATION

The MPQ2177F employs constant-on-time (COT) control with input voltage (V_{IN}) feed-forward to stabilize the switching frequency (f_{SW}) across the entire V_{IN} range. The device achieves up to 1A of continuous output current (I_{OUT}) across a 2.5V to 6V V_{IN} range, with excellent load and line regulation. For the adjustable-output version, the output voltage (V_{OUT}) can be regulated to as low as 0.6V. When V_{IN} falls below 3V in low-dropout (LDO) mode, the MPQ2177F can reach a 100% maximum duty cycle.

Constant-On-Time (COT) Control

Constant-on-time (COT) control offers simpler control loop and faster transient response compared to fixed-frequency pulse-width modulation (PWM) control. To prevent inductor current (I_L) runaway during load transient, the MPQ2177F's MOSFET has a fixed minimum off time (t_{MIN_OFF}). When the N-channel low-side MOSFET (LS-FET) turns on, it remains on for at least t_{MIN_OFF}. Once the feedback (FB) voltage (V_{FB}) drops below the reference voltage (V_{REF}), the P-channel high-side MOSFET (HS-FET) turns on. This indicates an insufficient V_{OUT}. By using V_{IN} feed-forward, the MPQ2177F maintains a nearly constant f_{SW} across V_{IN} and load ranges. The on time (t_{ON}) can be estimated with Equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 400ns \quad (1)$$

Frequency Scaling at Low Input Voltages

Under heavy-load conditions, the HS-FET voltage drops as t_{ON} increases and the duty cycle is extended. If t_{MIN_OFF} is reached at a low V_{IN} and under heavy-load conditions, f_{SW} scales down. To maintain a constant f_{SW}, a higher I_{OUT} requires a higher V_{IN} under heavy loads. For a 1.8V V_{OUT}, V_{IN} should be above 2.7V to keep f_{SW} above 2MHz for 1A loads.

When f_{SW} starts to scale down, V_{IN} can be estimated with Equation (2):

$$V_{IN} = \frac{V_{OUT} + R_{DS(ON)\_P} \times I_{OUT}}{1 - \frac{t_{MIN\_OFF}}{400 \times 10^{-9}}} \quad (2)$$

Where the maximum t_{MIN_OFF} is 125ns. (14)

Note:

14) Guaranteed by design and bench characterization. Not tested in production.

Sleep Mode Operation

To achieve high efficiency at extremely light loads, the MPQ2177F employs sleep mode. In sleep mode, most of the circuit block input currents are decreased, especially the error amplifier (EA) and PWM comparator.

When the load gets lighter, f_{SW} slows down. If the load is further decreased and the off time is longer than 3.5µs, the MPQ2177F enters sleep mode and consumes very low quiescent current (I_Q) to further improve light-load efficiency.

The MPQ2177F exits sleep mode when a high-side (HS) pulse occurs.

Advanced Asynchronous Modulation (AAM) Mode

Under light loads, the MPQ2177F employs advanced asynchronous modulation (AAM) mode, a power-saving mode that works with zero-current detection (ZCD) circuits.

Figure 3 shows the simplified AAM mode control theory. The AAM mode current (I_{AAM}) is set internally. The SW pulse-on time is determined by the on-timer generator and AAM mode comparator.

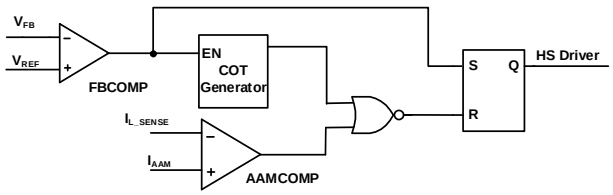

Figure 3: Simplified AAM Mode Control Logic

Under light loads, the SW pulse-on time is the longer pulse. When the AAM mode comparator pulse is longer than the on-timer generator, the AAM mode comparator controls t_{ON} (see Figure 4 on page 21).

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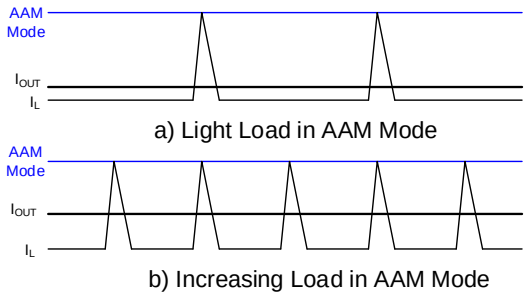

Figure 4: AAM Comparator Controls t_{ON}

When using a lower-value inductor, the AAM mode comparator pulse is shorter than the on-timer generator. Because the HS-FET depends on the on-time generator, the on-timer controls t_{ON} (see Figure 5).

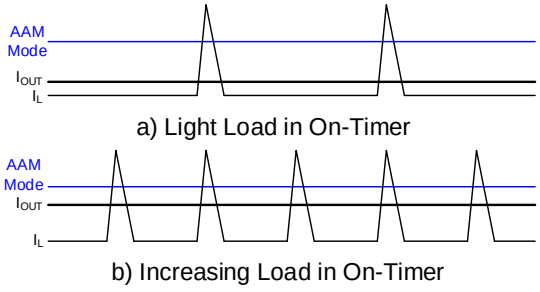

Figure 5: On-Timer Controls t_{ON}

In addition to the on-timer methods above, the AAM mode circuit has another 150ns blanking time in sleep mode. If the on-timer is shorter than 150ns, the HS-FET may turn off after the on-timer generator pulse, without AAM mode control.

The pulse on time in sleep mode is about 40% longer than the pulse in discontinuous conduction mode (DCM) or continuous conduction mode (CCM). In this scenario, I_L may not reach the AAM mode threshold (see Figure 6).

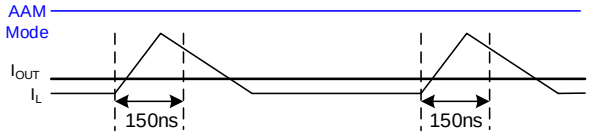

Figure 6: AAM Mode Blanking Time in Sleep Mode

Figure 7 shows how the AAM mode threshold decreases as t_{ON} increases. During CCM, I_{OUT} should exceed half of the AAM mode threshold.

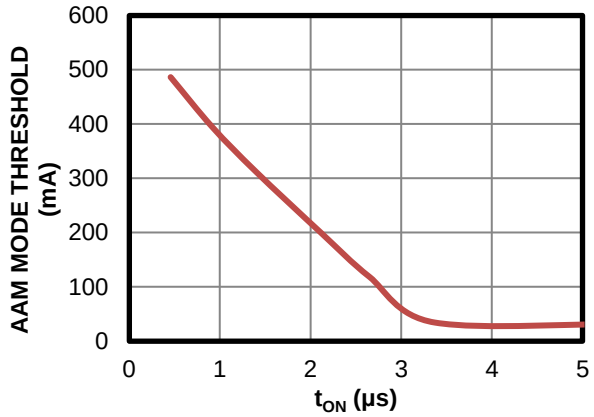

Figure 7: AAM Mode Threshold Decreases as t_{ON} Increases

The MPQ2177F has a ZCD circuit to detect when I_L starts to reverse. Once I_L reaches the ZCD threshold, the LS-FET turns off.

By pairing AAM mode with the ZCD circuit, the MPQ2177F always operates in DCM under light loads conditions, even if V_{OUT} is almost equal to V_{IN}.

Output Discharge

When the device is disabled, the part automatically enters output discharge mode. The internal discharge MOSFET provides a resistive discharge path between OUT and GND for the output capacitor (C_{OUT}). For the adjustable-output version, output discharge mode can be blocked by adding an external capacitor between the output and OUT. See the Output Discharge Blocking section on page 25 for more details.

Peak and Valley Current Limit

Both the HS-FET and LS-FET feature current-limit protection. When I_L reaches the HS-FET's peak current limit (typically 2.5A) during the HS-FET on time, the HS-FET turns off immediately to prevent I_L from exceeding the limit. Then the LS-FET turns on to discharge the energy. The HS-FET does not turn on again until I_L drops below the valley current limit threshold (typically 1A). This current limit scheme helps prevent current runaway during overload and short circuit events.

Short-Circuit Protection (SCP) and Recovery

If a V_{OUT} short to ground occurs and the MPQ2177F reaches its current limit, short-

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circuit protection (SCP) is triggered and the device tries to recover via hiccup mode.

During SCP, the MPQ2177F disables the output power (P_{OUT}) stage, then begins discharging the SS voltage (V_{SS}). Once V_{SS} is fully discharged, soft start (SS) is initiated and the device restarts. This hiccup process repeats until the fault condition is removed.

Over-Voltage Protection (OVP)

The MPQ2177F monitors a resistor-divided V_{FB} to detect over-voltage (OV) conditions. If V_{FB} exceeds 115% of V_{REF}, the controller enters a dynamic regulation period. During this period, the LS-FET remains on until the LS-FET current reaches -1.2A. This process discharges V_{OUT} and keeps it within the normal range.

If the OV condition still remains, the LS-FET turns on again after a 1.5µs delay. Once V_{FB} falls below 105% of V_{REF}, the MPQ2177F exits the regulation period. If the dynamic regulation period cannot prevent V_{OUT} from increasing and a $6.1V_{IN}$ is detected, over-voltage protection (OVP) occurs, and the MPQ2177F stops switching. Once V_{IN} drops below 6V, the device restarts and resumes normal operation.

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APPLICATION INFORMATION

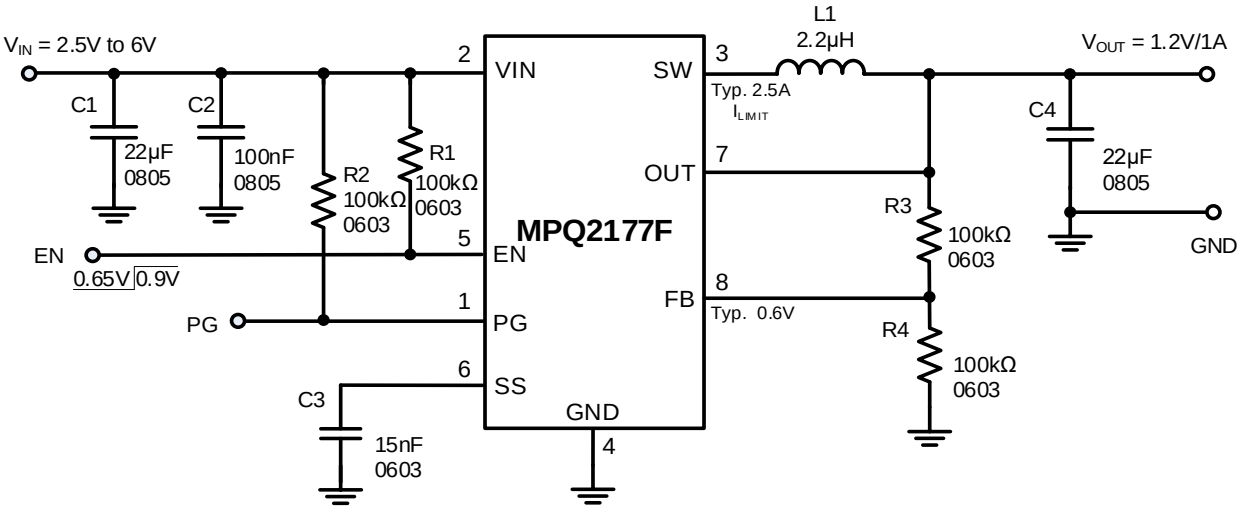

Figure 8: Typical Application Circuit (V_{OUT} = 1.2V, f_{SW} = 2.5MHz)

Table 1: Design Guide Index and Recommended Values

Pin #	Name	Component	Design Guide Index	Value
1	PG	R2	Power Good Indicator (PG, Pin 1)	100kΩ
2	VIN	C1, C2	Selecting the Input Capacitor (VIN, Pin 2)	22µF, 100nF
3	SW	L1, C4	Selecting the Inductor and Output Capacitor (SW, Pin 3)	2.2µH, 22µF
4	GND	-	GND Connection (GND, Pin 4)	-
5	EN	R1	Enable (EN, Pin 5)	100kΩ
6	SS	C3	Soft Start (SS, Pin 6)	15nF
7	OUT	-	Output Discharging Blocking (OUT, Pin 7)	-
8	FB	R3, R4	Setting the Output Voltage (FB, Pin 8)	100kΩ, 100kΩ

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Power Good Indicator (PG, Pin 1)

The MPQ2177F has a power good (PG) output to indicate whether the device is operating normally after soft start (SS). The PG pin is the open-drain output of an internal MOSFET. It is recommended for the MOSFET's maximum on resistance ($R_{DS(ON)}$) to remain below 400Ω. PG can connect to V_{IN} or an external voltage source via an external resistor (e.g. 100kΩ). After V_{IN} is applied, the MOSFET turns on and PG is pulled to GND before SS is complete. After V_{FB} reaches 95.5% of V_{REF}, PG is pulled high via the external voltage source. If V_{FB} drops to 90% of V_{REF}, the PG voltage (V_{PG}) is pulled to GND to indicate an output failure.

If V_{IN} and EN are not available and PG is pulled up via an external power supply, then PG self-biases and asserts. If a 100kΩ pull-up resistor is used, V_{PG} should be below 0.7V.

Selecting the Input Capacitor (VIN, Pin 2)

The step-down converter has a discontinuous input current (I_{IN}), and requires a capacitor to supply AC current to the converter while maintaining the DC V_{IN}. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10µF capacitor is sufficient. Higher output voltages may require a 22µF capacitor for better system stability.

The input capacitor (C_{IN}) requires an adequate ripple current rating to absorb the input switching current. The RMS current (I_{C1}) in C_{IN} can be estimated with Equation (3):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (3)$$

The worst-case scenario occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (4):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (4)$$

For simplification, choose C_{IN} to have an RMS current rating greater than half of the maximum load current.

C_{IN} can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality, ceramic 0.1µF capacitor, placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to prevent an excessive V_{IN} ripple (ΔV_{IN}). ΔV_{IN} can be estimated with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

Selecting the Inductor and Output Capacitor (SW, Pin 3)

Selecting the Inductor

A 0.47µH to 2.2µH inductor is recommended for most applications. Select an inductor with a DC resistance below 25mΩ to optimize efficiency.

High-frequency, switch-mode power supplies with magnetic devices, such as the MPQ2177F, can have strong electromagnetic inference (EMI). Avoid using unshielded power inductors as they provide poor magnetic shielding. To effectively reduce EMI, it is recommended to use shielded inductors, such as metal alloy or multiplayer chip power inductors.

For most designs, the inductance (L) can be estimated with Equation (6):

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}} \quad (6)$$

Where ΔI_L is the inductor ripple current.

Choose an inductor ripple current that is approximately 30% of the maximum load current. The maximum peak inductor current ($I_{L(MAX)}$) can be calculated with Equation (7):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (7)$$

Selecting the Output Capacitor

The output capacitor (C_{OUT}) stabilizes the DC V_{OUT}. Ceramic capacitors are recommended. Low-ESR capacitors are ideal because they effectively limit the V_{OUT} ripple (ΔV_{OUT}). ΔV_{OUT} can be calculated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (8)$$

Where L is the inductance, and R_{ESR} is the equivalent series resistance (ESR) of C_{OUT}.

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When using ceramic capacitors, the capacitance dominates the impedance at f_{SW} and causes the majority of ΔV_{OUT}.

For simplification, ΔV_{OUT} can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

Ceramic capacitors with X7R or X5R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

For a 1A load, a 22µF capacitor with a 0805 package or a larger-value capacitor is recommended to reduce ΔV_{OUT} during steady state operation and load transient. For the detailed ΔV_{OUT} performance, see the Typical Performance Characteristics section on page 15.

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (10)$$

The characteristics of C_{OUT} also affect the regulation system stability.

GND Connection (GND, Pin 4)

See the PCB Layout Guidelines section on Page 27 for more details.

Enable (EN, Pin 5)

The EN pin turns the regulator on and off. Pull EN below its falling threshold (0.65V) to turn the MPQ2177F off; pull EN above its rising threshold voltage (0.9V) to turn the chip on. Leave EN floating or pull it down to ground to disable the MPQ2177F. There is an internal 2MΩ resistor connected from EN to ground.

Soft Start (SS, Pin 6)

To avoid overshoot during start-up, the MPQ2177F has an external SS pin that increases V_{OUT} at a controlled slew rate. The SS pin's charge current is typically 21µA. The soft-start time (t_{SS}) is determined via the SS capacitor (C_{SS}). t_{SS} can be calculated with Equation (11):

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times 0.6V}{I_{SS}(\mu A)} \quad (11)$$

Where C_{SS} is the external SS capacitor, and I_{SS} is the internal 21µA SS charge current.

It is recommended for C_{SS} to be 6.8nF at minimum.

The device has a pre-biased start-up function. Once EN is pulled above 0.9V, the converter starts up even if there is a pre-biased voltage on V_{OUT}. Pre-biased start-up works even while the output discharge path is blocked.

Output Discharge Blocking (OUT, Pin 7)

When the device is disabled, an internal resistive discharge path between OUT and GND is enabled to discharge C_{OUT}. The discharge path can be blocked via adding an external capacitor between V_{OUT} and OUT (see Figure 9).

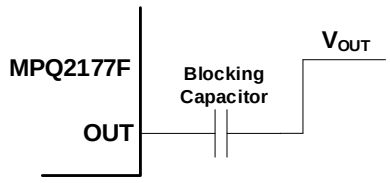

Figure 9: Circuit with V_{OUT} Discharge Blocking Capacitor

To avoid influencing the loop and load transient, it is recommended that the blocking capacitor be at least 10nF. Larger-value blocking capacitors do not impact loop performance, but are not required and may be more costly. A 10nF and 100nF capacitance is recommended.

Setting the Output Voltage (FB, Pin 8)

To set V_{OUT} for the adjustable-output version, the MPQ2177F uses an external resistor divider.

Select a feedback (FB) resistor (R1) that reduces the V_{OUT} leakage current (typically between 10kΩ and 100kΩ). R2 can be calculated with Equation (12):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6} - 1} \quad (12)$$

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Figure 10 shows the feedback (FB) circuit.

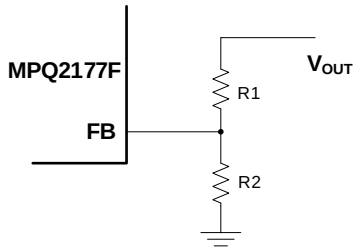

Figure 10: Feedback Network

Table 2 lists the recommended resistances for common output voltages.

Table 2: Resistances for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1	30.9 (1%)	47 (1%)
1.2	100 (1%)	100 (1%)
1.8	36 (1%)	18 (1%)
2.5	51 (1%)	16 (1%)
3.3	68 (1%)	15 (1%)

For the fixed-output versions, float the FB pin; the internal resistor dividers regulate V_{OUT}.

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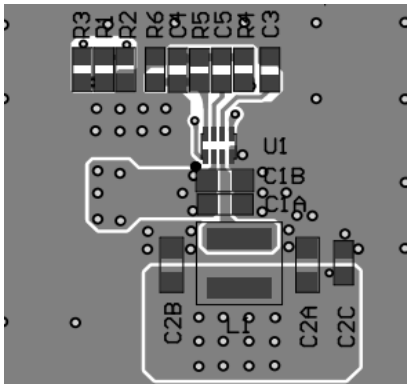
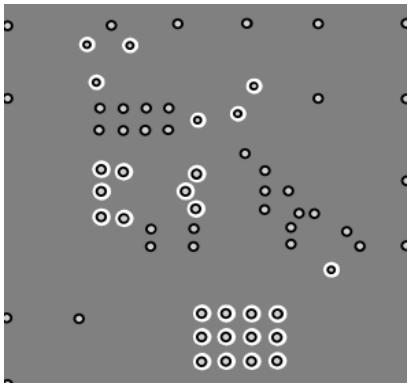
PCB Layout Guidelines

Efficient PCB layout is critical for proper function. Poor layout design can result in poor line or load regulation and stability issues. For the best results, refer to Figure 11 and follow the guidelines below:

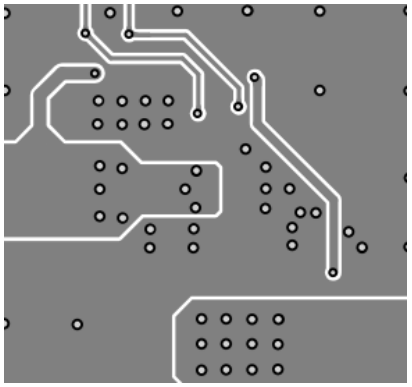
1. Place the high-current paths (GND, VIN, and SW) as close to the device as possible with short, direct, and wide traces.
2. Place the input capacitor (C1) as close as possible to the VIN and GND pins.
3. Place the GND output capacitor close to the GND pin.
4. For the adjustable-output version, place the external feedback (FB) resistors next to the FB pin.
5. Keep the switching node (SW) short and route it away from the feedback network.
6. Keep the V_{OUT} sense line as short as possible, and place it as far away from the power inductor as possible. The sense line must not surround the inductor or be close to SW.



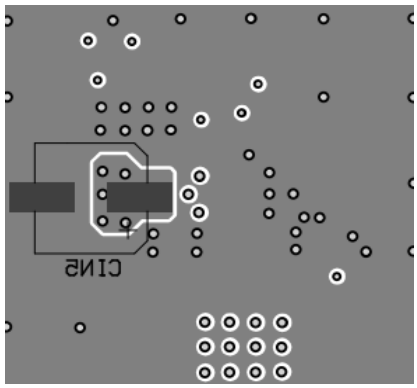
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 11: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

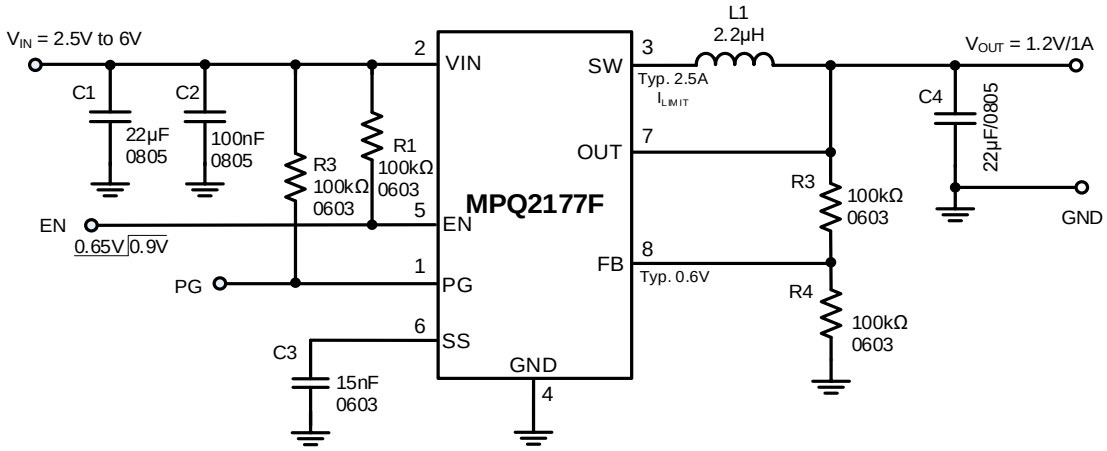

Figure 12: Typical Application Circuit for the Adjustable-Output Version (1.2V Output)

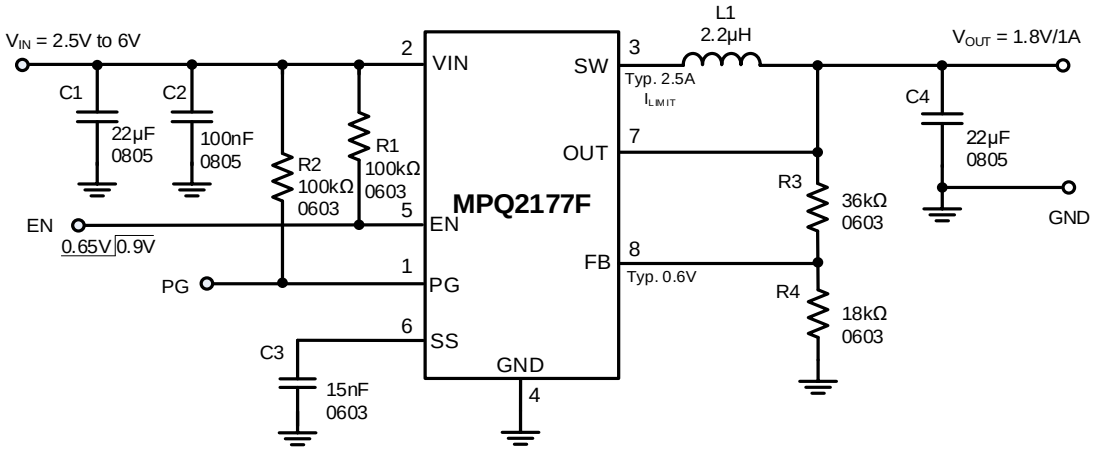

Figure 13: Typical Application Circuit for the Adjustable-Output Version (1.8V Output)

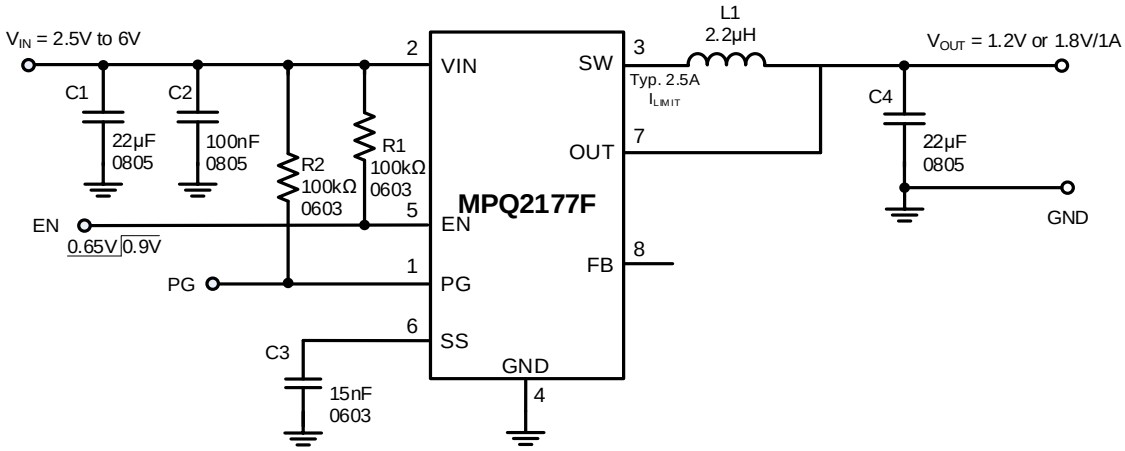

Figure 14: Typical Application Circuit for the Fixed-Output Versions

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TYPICAL APPLICATION CIRCUITS *(continued)*

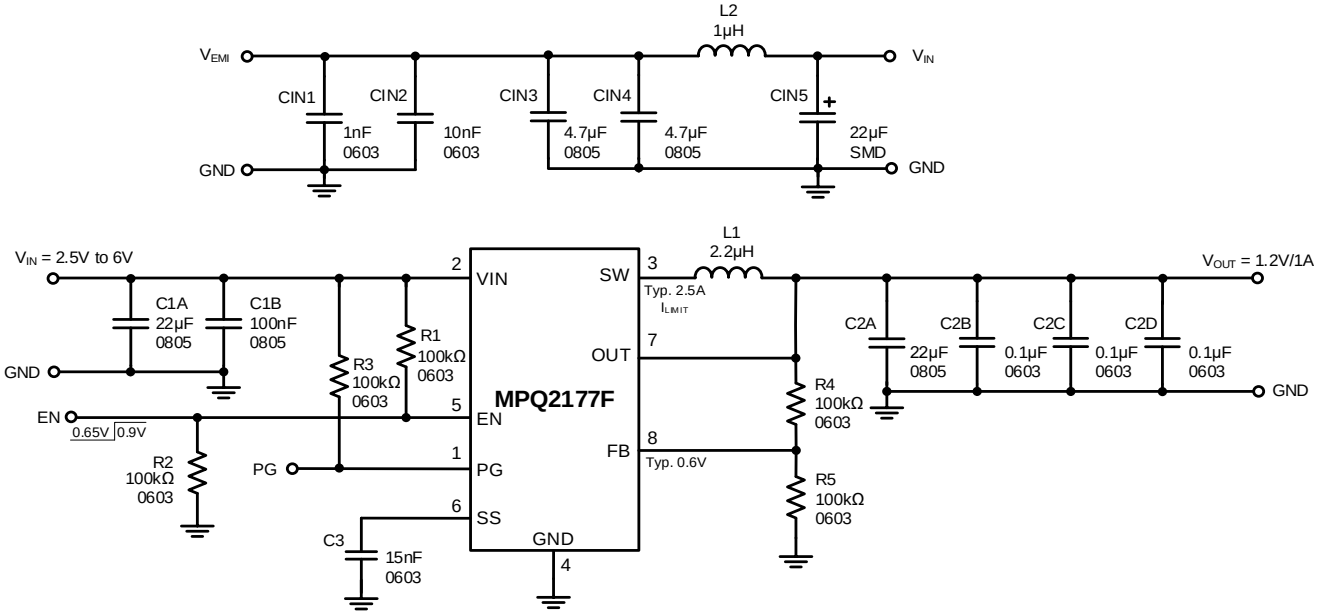

Figure 15: Typical Application Circuit with EMI Filter (1.2V Adjustable-Output Version)

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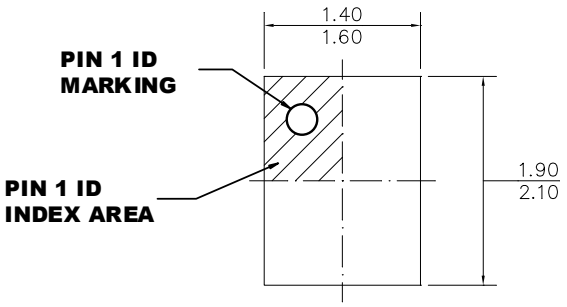
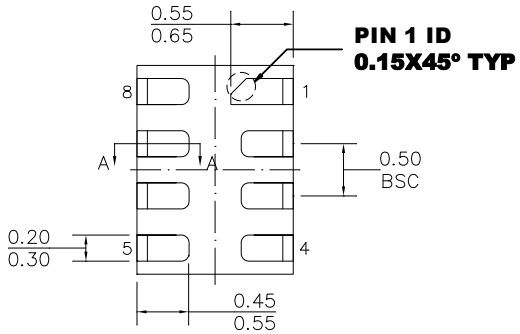
PACKAGE INFORMATION

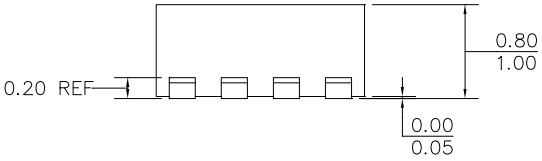
QFN-8 (1.5mmx2mm)
Wettable Flank



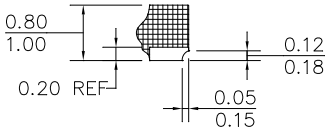
TOP VIEW



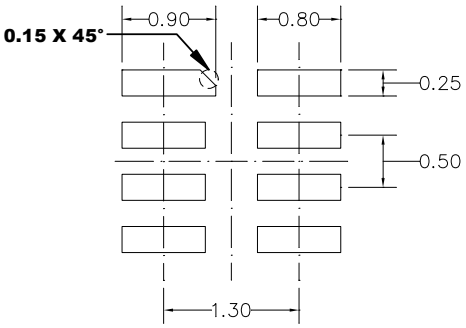
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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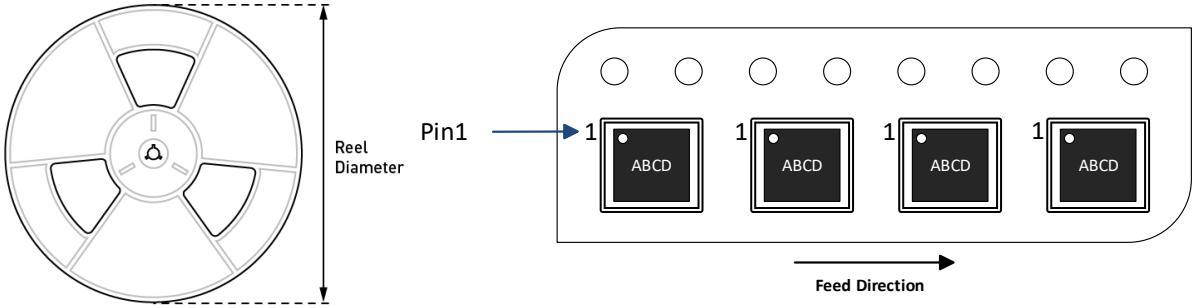
CARRIER INFORMATION



Part Number	Package Description	Quantity /Reel	Quantity /Tube	Quantity /Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ2177FGQHE-AEC1-Z	QFN-8 (1.5mmx2mm)	5000	N/A	N/A	13in	8mm	4mm
MPQ2177FGQHE-12-AEC1-Z							
MPQ2177FGQHE-18-AEC1-Z							

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/21/2024	Initial Release	-

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