MPQ2166B

6V, Dual 2A/2A or 3A/1A, Low-I_Q, Synchronous Buck with PG and SS, AEC-Q100 Qualified

DESCRIPTION

The MPQ2166B is an internally compensated, dual, pulse-width modulation (PWM), synchronous step-down regulator that operates from a 2.7V to 6V input voltage (V_{IN}) and generates an output voltage (V_{OUT}) as low as 0.6V. The MPQ2166B can be configured as a 2A/2A or 3A/1A output current (I_{OUT}) regulator, and is ideal for a wide range of applications, including automotive infotainment, clusters, and telematics, as well as portable instruments.

The MPQ2166B integrates dual, 55mΩ, high-side MOSFETs (HS-FETs) and 20mΩ synchronous rectifiers to achieve high efficiency without an external Schottky diode. The MPQ2166B offers peak current mode control and internal compensation, and is capable of low-dropout configurations. Both channels can operate at 100% duty cycle.

Full protection features include cycle-by-cycle current limiting and thermal shutdown.

The MPQ2166B requires a minimal number of readily available, standard external components, and is available in a QFN-18 (2.5mmx3.5mm) package.

FEATURES

- **Cooler Thermals:**
  - Below 20°C Operating Junction Temperature (T_J) Rise at 2A/2A, 2.3MHz
  - 90% Efficiency (5V to 1.8V, 2A, 2.3MHz)
  - Low-Ohmic BCD FET Technology
- **Low-Noise EMI and EMC:**
  - MeshConnect™ Flip-Chip Package
  - Operates Outside of AM Radio Band
- **Reduces Board Size and BOM:**
  - Integrated Compensation Network
  - Available in a Small QFN-18 (2.5mmx3.5mm) Package
- **Additional Features:**
  - Power Good (PG) Output
  - External Soft Start (SS) and Tracking
  - Over-Current Protection (OCP) with Hiccup Mode
  - External Sync Clock
  - 100% Duty Cycle Operation
  - Available in AEC-Q100 Grade 1

APPLICATIONS

- Automotive Infotainment
- Automotive Clusters
- Automotive Telematics
- Battery-Powered Devices
- Portable Instruments

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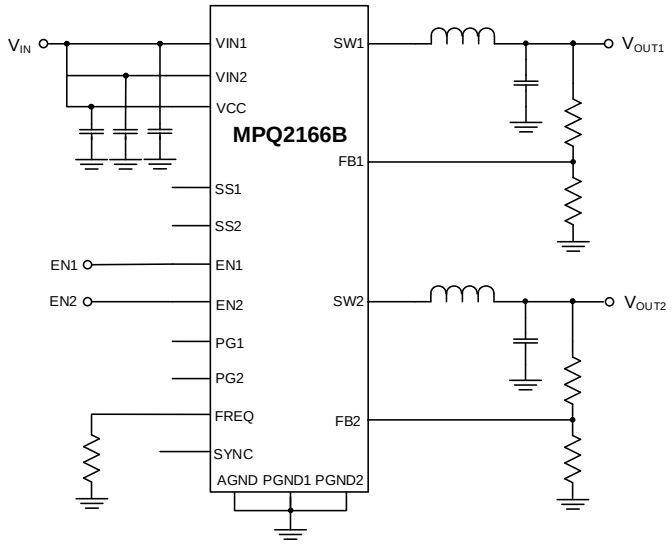
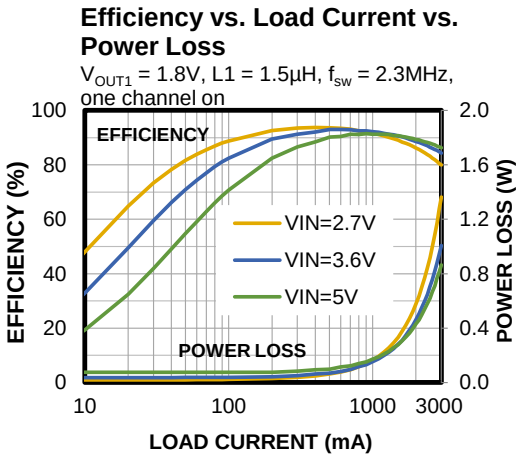
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ2166BGRHE-AEC1***	QFN-18 (2.5mmx3.5mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ2166BGRHE-AEC1-Z).
** Moisture Sensitivity Level Rating
*** Wettable Flank

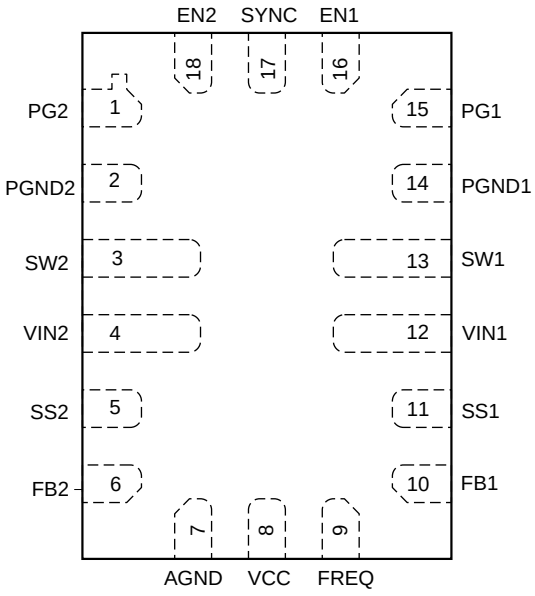
TOP MARKING

BQU
YWW
LLL

BQU: Product code of MPQ2166BGRHE-AEC1
Y: Year code
WW: Week code
LLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-18 (2.5mmx3.5mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	PG2	**Power good for channel 2.** The output of PG2 is an open drain. A pull-up resistor to the power source is required if this pin used. When V_{FB2} reaches 90% of the reference voltage (V_{REF}), PG2 is pulled high. When V_{FB2} drops to 82% of V_{REF}, it is pulled low to GND.
2	PGND2	**Power ground for channel 2.** Connect PGND2 to the negative terminals of the input and output capacitors with larger copper areas. PGND2 must be connected to PGND1 externally on the board.
3	SW2	**Switch-node connection to the inductor for channel 2.** Connect SW2 to the internal high-side MOSFETs (HS-FETs) and low-side MOSFETs (LS-FETs) of the channel 2 buck converter.
4	VIN2	**Input supply for channel 2.** Place a decoupling capacitor to ground, close to VIN2, to reduce switching spikes.
5	SS2	**Soft start for channel 2.** Place a capacitor from SS2 to GND to set the soft-start time (t_{SS}) externally. Floating this pin activates the internal default 0.5ms soft-start setting.
6	FB2	**Feedback for channel 2.** FB2 is the input to channel 2's error amplifier (EA). An external resistor divider connects FB2 between the output and ground. The voltage on FB2 is compared to the internal 0.6V V_{REF} to set the regulation voltage for channel 2.
7	AGND	**Analog ground.** Connect AGND to PGND1 and PGND2 externally on the board.
8	VCC	**Power supply to the internal regulator for both channels.** Decouple VCC with a 0.1µF to 1µF capacitor, placed between VCC and AGND. Connect VIN1, VIN2, and VCC together externally. It is not recommended to power VIN1, VIN2, and VCC from a separate power supply.
9	FREQ	**Frequency set.** Connect a resistor to GND to set the switching frequency (f_{SW}).
10	FB1	**Feedback for channel 1.** FB1 is the input to channel 1's EA. An external resistor divider connects FB1 between the output and GND. The voltage on FB1 is compared to the internal 0.6V V_{REF} to set the regulation voltage for channel 1.
11	SS1	**Soft start for channel 1.** Place a capacitor from SS1 to GND to set t_{SS} externally. Floating this pin activates the internal default 0.5ms soft-start setting.
12	VIN1	**Input supply for channel 1.** Place a decoupling capacitor to ground, close to VIN1, to reduce switching spikes.
13	SW1	**Switch-node connection to the inductor for channel 1.** SW1 connects to the internal HS-FETs and LS-FETs of the channel 1 buck converter.
14	PGND1	**Power ground for channel 1.** Connect PGND1 to the negative terminals of the input and output capacitors with larger copper areas. PGND1 must be connected to PGND2 externally on the board.
15	PG1	**Power good for channel 1.** The output of PG1 is an open drain. A pull-up resistor to the power source is required if this pin used. When V_{FB1} reaches 90% of V_{REF}, PG1 is pulled high. When V_{FB1} drops to 82% of V_{REF}, it is pulled low to GND.
16	EN1	**Enable control for channel 1.** Pull EN1 below the specified threshold (0.8V) to shut down the chip. Pull EN above the threshold (0.9V) to enable the chip. Do not float EN1.
17	SYNC	**Frequency sync.** f_{SW} can be synchronized by an external clock via the SYNC pin.
18	EN2	**Enable control for channel 2.** Pull EN2 below the specified threshold (0.8V) to shut down the chip. Pull EN above the threshold (0.9V) to enable the chip. Do not float EN2.

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 6.5V
V_{SW} .....-0.3V to V_{IN} + 0.3V
All other pins..... -0.3V to +6.5V
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature..... -65°C to +150°C
Continuous power dissipation (T_A = 25°C) (2) (7)
QFN-18 (2.5mmx3.5mm) 3.6W

ESD Ratings

Human body model (HBM).....Class 2 (3)
Charged device model (CDM).....Class C2b (4)

Recommended Operating Conditions

Supply voltage (V_{IN}) ..... 2.7V to 6V
Output voltage (V_{OUT})..... 0.6V to 5.5V
Operating junction temp (5) ..... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-18 (2.5mmx3.5mm)
JESD51-7 (6).....50……12….°C/W
EVQ2166B-RH-00A (7).....34.8….2.7….°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per AEC-Q100-002.
4) Per AEC-Q100-011.
5) Operating devices at junction temperatures exceeding 125°C is possible. Contact MPS for details.
6) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.
7) Measured on a MPS standard EVB: a 4-layer, 6.35cmx6.35cm PCB with 2oz thick copper.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Quiescent supply current	I_Q	V_{IN} = 5V, V_{EN} = 2V, V_{FB} = 0.65V, no switching		65	100	µA
Shutdown current	I_{SHDN}	V_{EN} = 0V, T_J = 25°C		0	0.2	µA
		V_{EN} = 0V			30	µA
Input under-voltage lockout (UVLO) threshold	V_{UVLO}	V_{IN1}, V_{IN2}, V_{CC} rising		2.4	2.55	V
Input UVLO hysteresis	V_{UVLO_HYS}	V_{IN1}, V_{IN2}, V_{CC} UVLO hysteresis		230		mV
Regulated feedback (FB) voltage	V_{FB}	T_J = 25°C	0.593	0.6	0.607	V
		T_J = -40°C to +150°C	0.585	0.6	0.612	V
FB input current	I_{FB}	V_{FB} = 0.65V		0	150	nA
EN high threshold	V_{EN_H}		0.7	0.9	1.1	V
EN low threshold	V_{EN_L}		0.6	0.8	1	V
EN threshold hysteresis	V_{EN_HYS}			100		mV
EN input current	I_{EN}	V_{EN} = 2V		0	150	nA
		V_{EN} = 0V		0	100	
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)_P}$	V_{IN} = 5V		55	100	mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)_N}$	V_{IN} = 5V		20	50	mΩ
SW leakage current	I_{SW_LK}	V_{EN} = 0V, V_{IN} = 6V, V_{SW} = 0V and 6V, T_J = 25°C	-1	0	+1	µA
HS-FET current limit (8)	I_{HS_LIMIT}	Source	3.4	4.8	6.2	A
Low-side (LS) valley current limit (8)	I_{VALLEY}			3.9		A
LS-FET current limit	I_{LS_LIMIT}	Sink	1			A
Switching frequency	f_{SW}	R_{FREQ} = 560kΩ	350	410	470	kHz
		R_{FREQ} = 75kΩ	1990	2290	2590	kHz
SYNC frequency range	f_{SYNC}		0.35		3	MHz
SYNC rising threshold	V_{SYNC_R}		1.95	2.15	2.35	V
SYNC falling threshold	V_{SYNC_F}		1.5	1.7	1.9	V
SYNC threshold hysteresis	V_{SYNC_HYS}			450		mV
SYNC input current	I_{SYNC}	V_{SYNC} = 5V		13		µA
Phase shift				180		degrees
Minimum on time (8)	t_{ON_MIN}			55		ns
Minimum off time (8)	t_{OFF_MIN}			50		ns
Maximum duty cycle	D_{MAX}			100		%
Thermal shutdown threshold (8)	T_D			175		°C
Thermal shutdown hysteresis (8)	T_{D_HYS}			40		°C
Soft start charge current	I_{SS}	V_{SS} = 0V	2	3.2	5	µA
Power good (PG) rising threshold	$PGOOD_{VTH-HI}$		0.85	0.9	0.95	V_{FB}
PG falling threshold	$PGOOD_{VTH-LO}$		0.77	0.82	0.87	V_{FB}
PG rising deglitch time	t_{PGOOD_R}			30		µs
PG falling deglitch time	t_{PGOOD_F}			40		µs

Note:

8) Not tested in production. Guaranteed by design and characterization.

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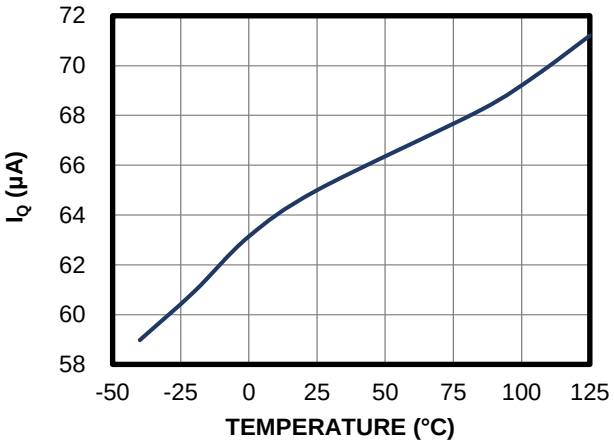
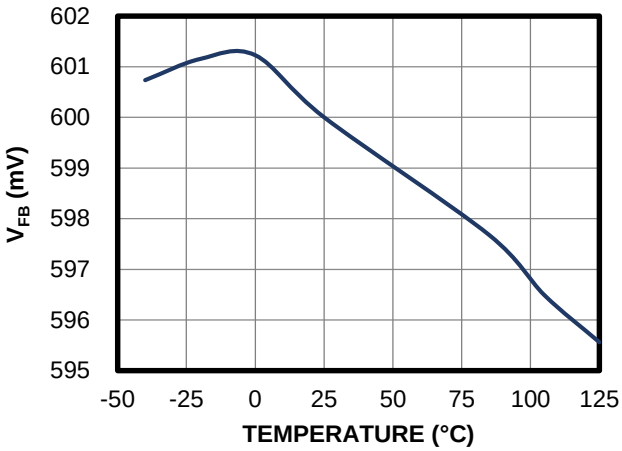
TYPICAL CHARACTERISTICS

V_{IN} = 5V, T_J = -40°C to +125°C, unless otherwise noted.

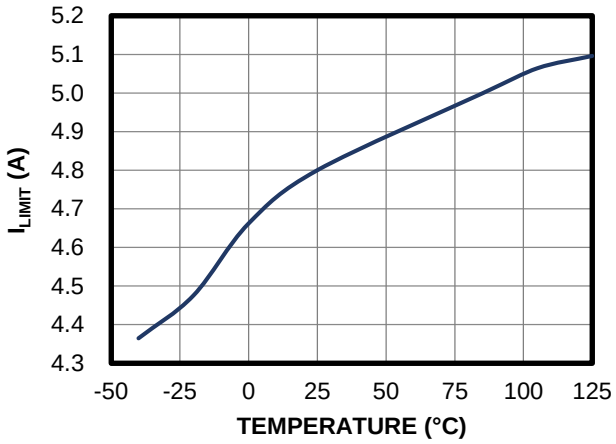
Quiescent Supply Current vs. Temperature



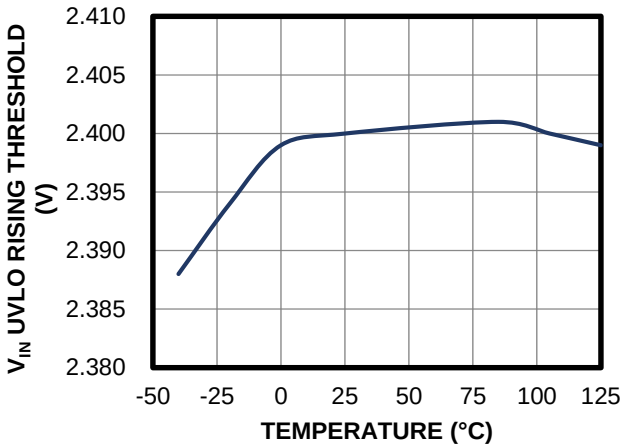
Regulated FB Voltage vs. Temperature



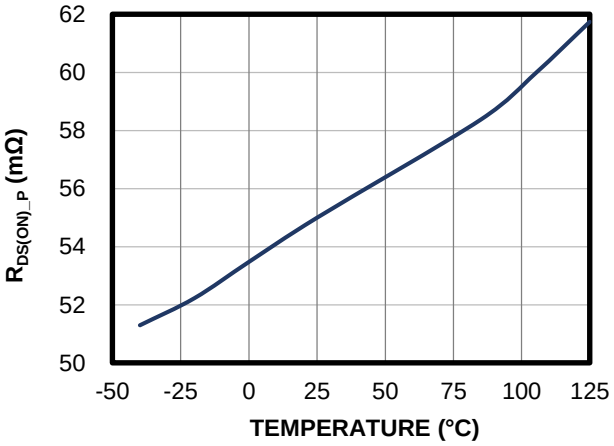
Switch Current Limit vs. Temperature



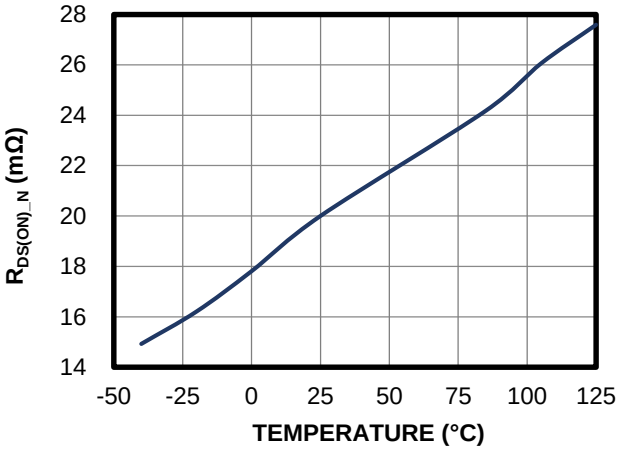
V_{IN} UVLO Rising Threshold vs. Temperature



HS-FET On Resistance vs. Temperature



LS-FET On Resistance vs. Temperature



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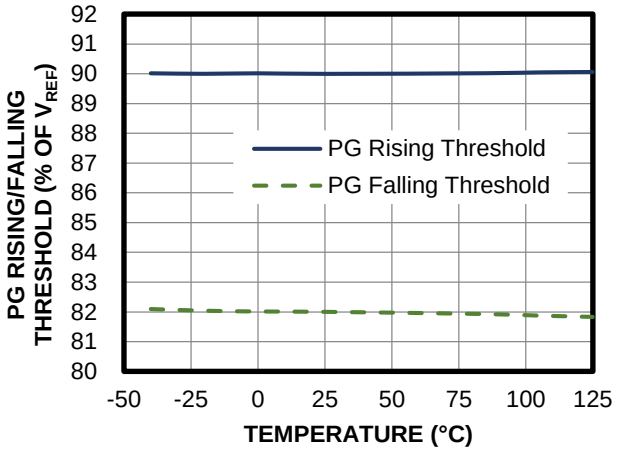
TYPICAL CHARACTERISTICS *(continued)*

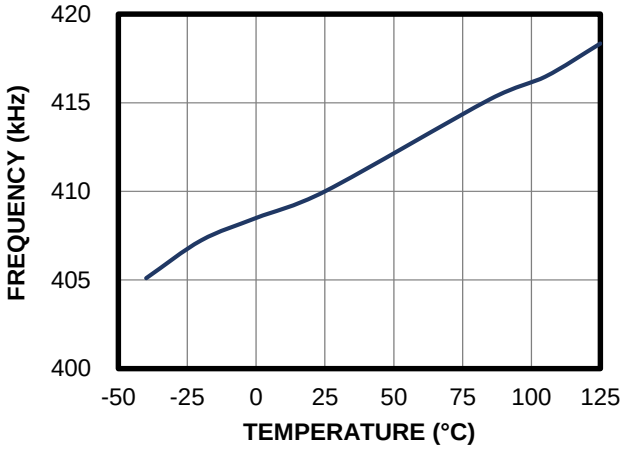
V_{IN} = 5V, T_J = -40°C to +125°C, unless otherwise noted.

PG Rising/Falling Threshold vs. Temperature



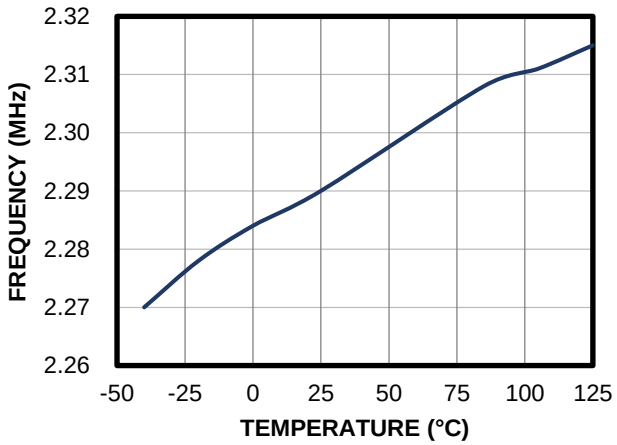
Frequency vs. Temperature

f_{SW} = 410kHz



Frequency vs. Temperature

f_{SW} = 2.29MHz



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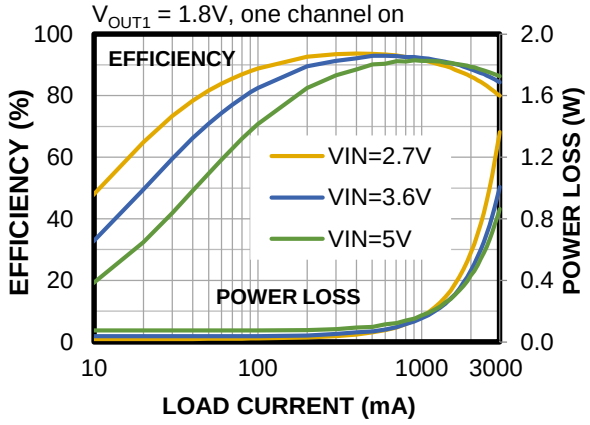
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L1 = L2 = 1.5µH, f_{SW} = 2.3MHz, T_A = 25°C, unless otherwise noted.

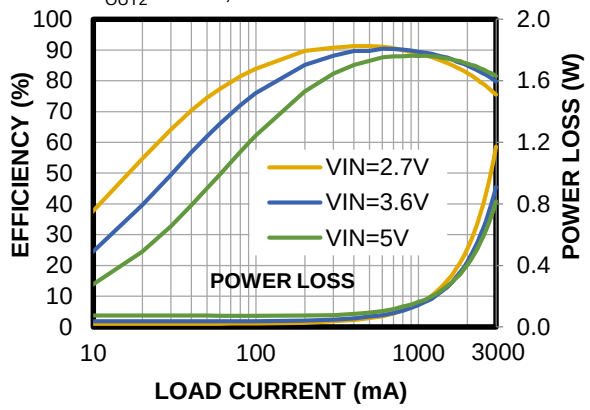
Efficiency vs. Load Current vs. Power Loss

V_{OUT1} = 1.8V, one channel on



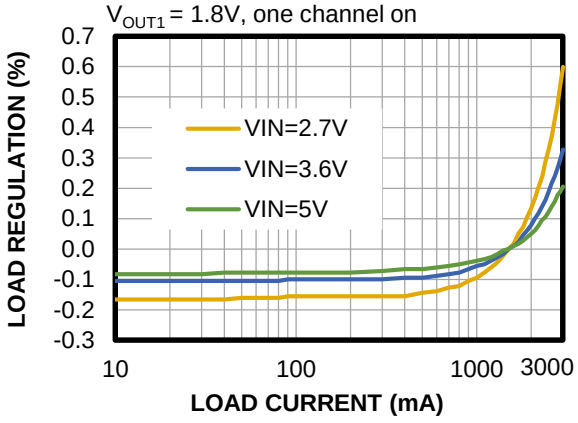
Efficiency vs. Load Current vs. Power Loss

V_{OUT2} = 1.2V, one channel on



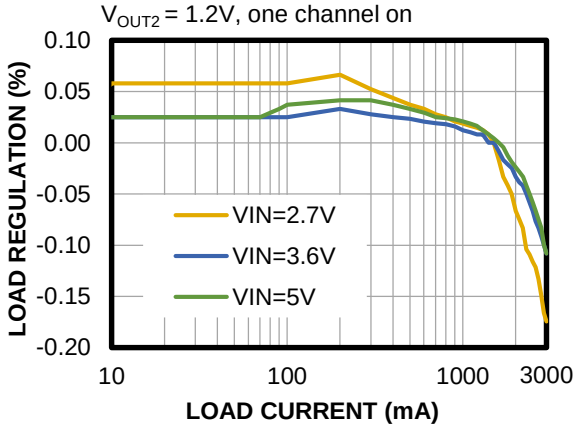
Load Regulation

V_{OUT1} = 1.8V, one channel on



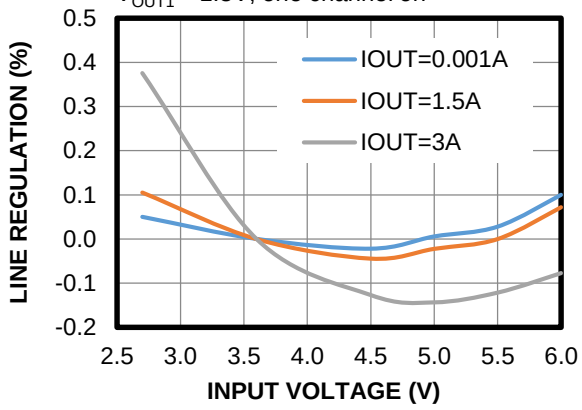
Load Regulation

V_{OUT2} = 1.2V, one channel on



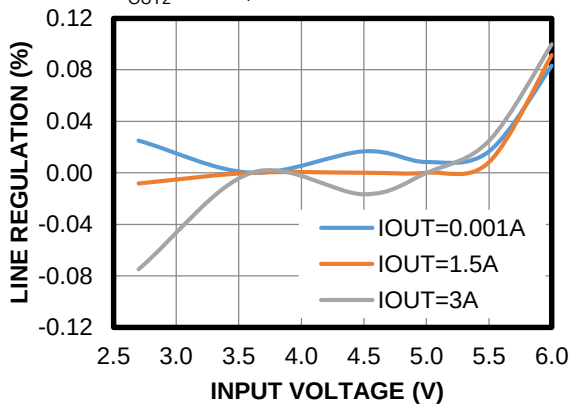
Line Regulation

V_{OUT1} = 1.8V, one channel on



Line Regulation

V_{OUT2} = 1.2V, one channel on



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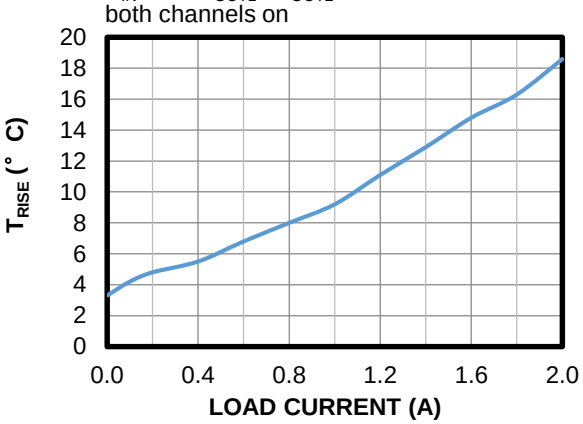
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L1 = L2 = 1.5µH, f_{SW} = 2.3MHz, T_A = 25°C, unless otherwise noted.

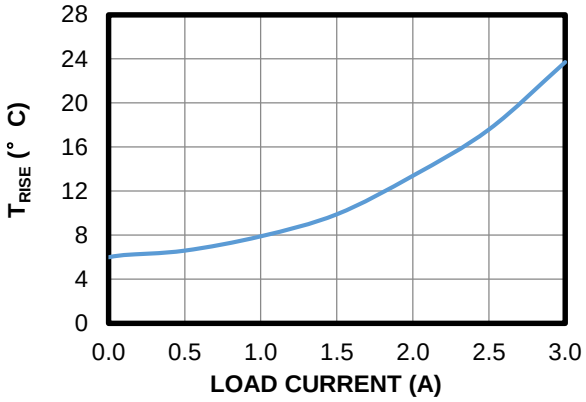
Case Temperature Rise

V_{IN} = 5V, I_{OUT1} = I_{OUT2} = 0A to 2A, both channels on



Case Temperature Rise

V_{IN} = 5V, I_{OUT1} = 0A to 3A, I_{OUT2} = 1A, both channels on



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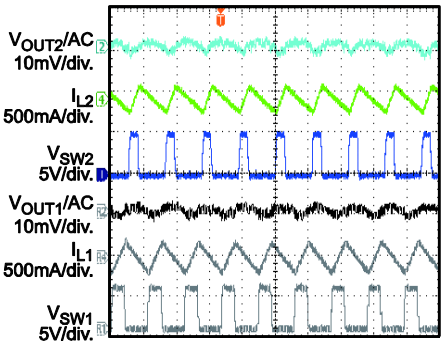
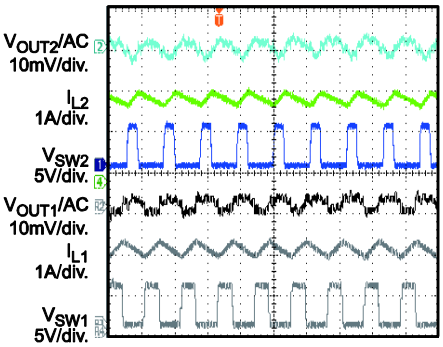
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L1 = L2 = 1.5µH, f_{SW} = 2.3MHz, T_A = 25°C, unless otherwise noted.

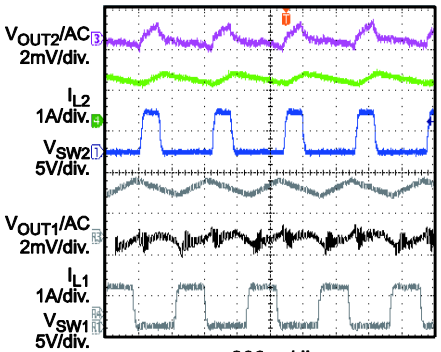
Steady State
$I_{OUT1} = I_{OUT2}$ = 0A



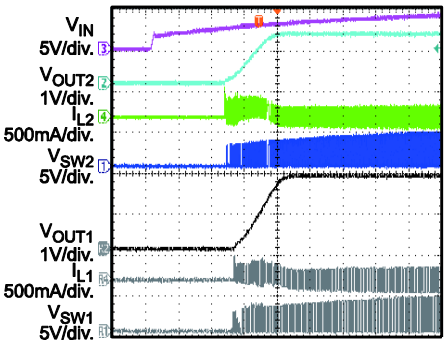
Steady State
$I_{OUT1} = I_{OUT2}$ = 2A



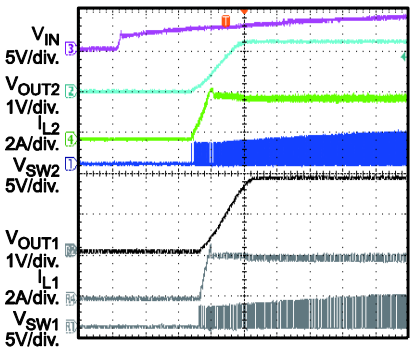
Steady State
I_{OUT1} = 3A, I_{OUT2} = 1A



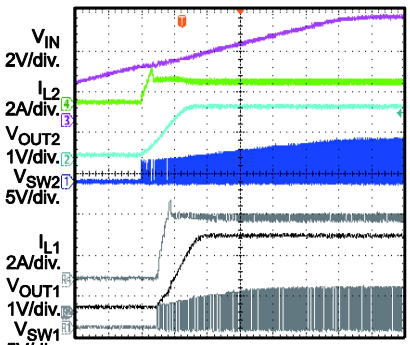
Start-Up through VIN
$I_{OUT1} = I_{OUT2}$ = 0A



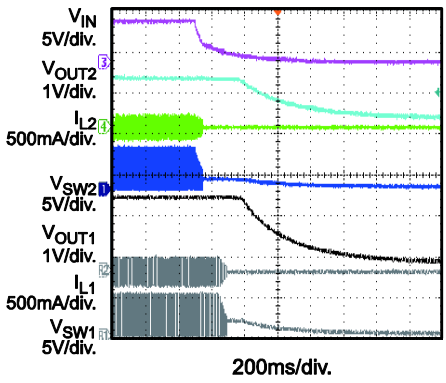
Start-Up through VIN
$I_{OUT1} = I_{OUT2}$ = 2A



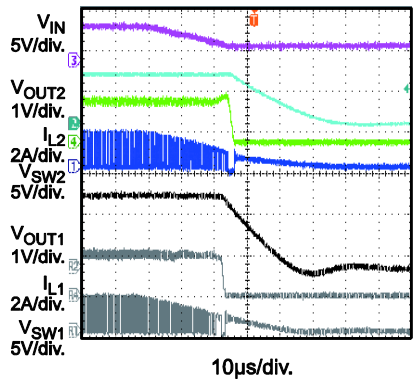
Start-Up through VIN
I_{OUT1} = 3A, I_{OUT2} = 1A



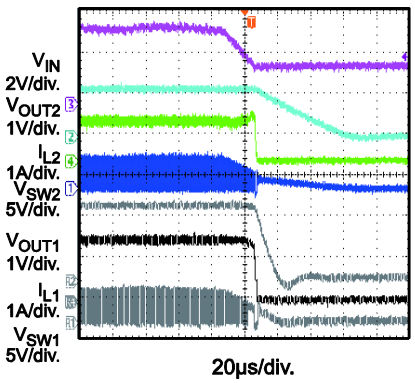
Shutdown through VIN
$I_{OUT1} = I_{OUT2}$ = 0A



Shutdown through VIN
$I_{OUT1} = I_{OUT2}$ = 2A



Shutdown through VIN
I_{OUT1} = 3A, I_{OUT2} = 1A



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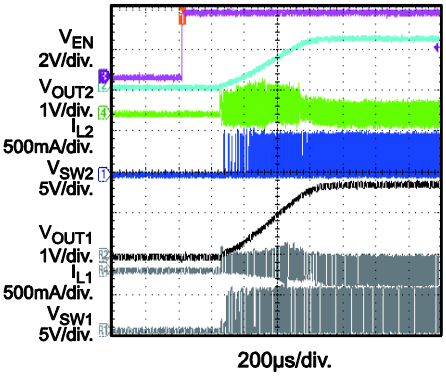
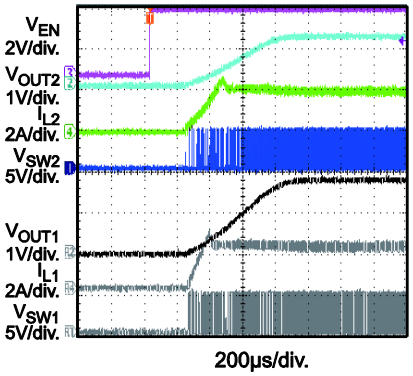
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L1 = L2 = 1.5µH, f_{SW} = 2.3MHz, T_A = 25°C, unless otherwise noted.

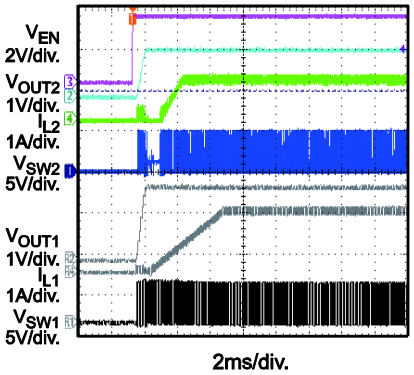
Start-Up through EN
I_{OUT1} = I_{OUT2} = 0A



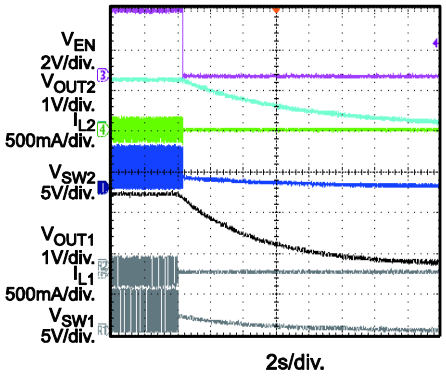
Start-Up through EN
I_{OUT1} = I_{OUT2} = 2A



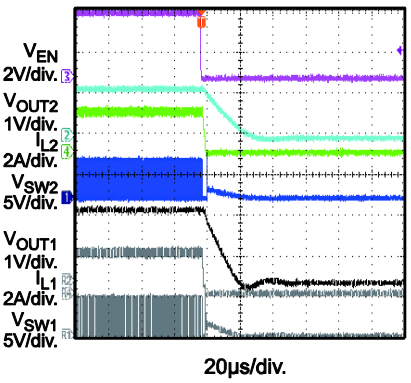
Start-Up through EN
I_{OUT1} = 3A, I_{OUT2} = 1A



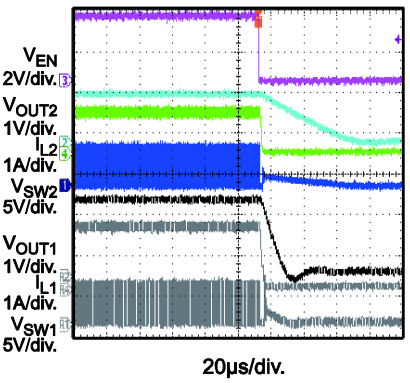
Shutdown through EN
I_{OUT1} = I_{OUT2} = 0A



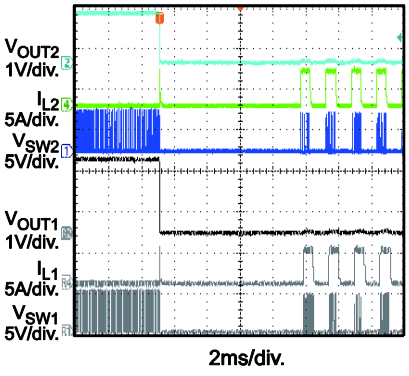
Shutdown through EN
I_{OUT1} = I_{OUT2} = 2A



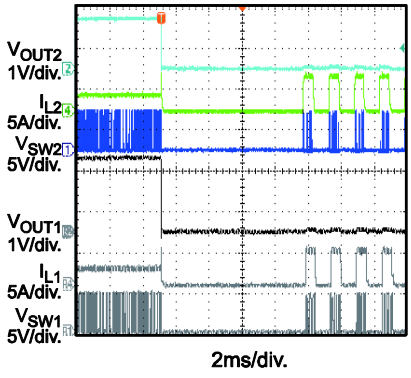
Shutdown through EN
I_{OUT1} = 3A, I_{OUT2} = 1A



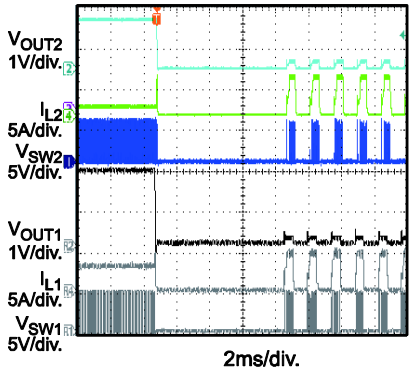
SCP Entry
I_{OUT1} = I_{OUT2} = 0A



SCP Entry
I_{OUT1} = I_{OUT2} = 2A



SCP Entry
I_{OUT1} = 3A, I_{OUT2} = 1A



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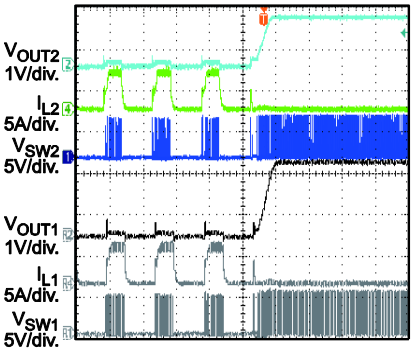
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L1 = L2 = 1.5µH, f_{SW} = 2.3MHz, T_A = 25°C, unless otherwise noted.

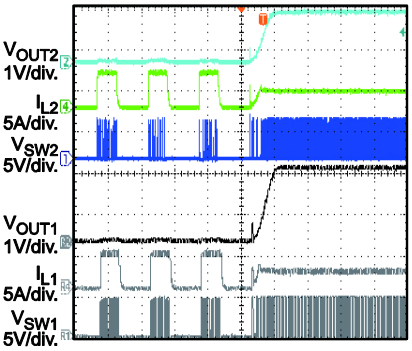
SCP Recovery

I_{OUT1} = I_{OUT2} = 0A



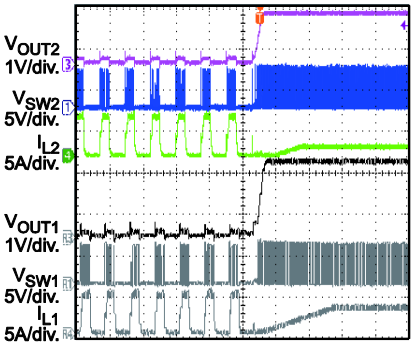
SCP Recovery

I_{OUT1} = I_{OUT2} = 2A

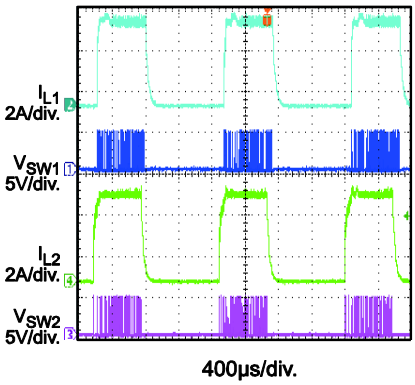


SCP Recovery

I_{OUT1} = 3A, I_{OUT2} = 1A

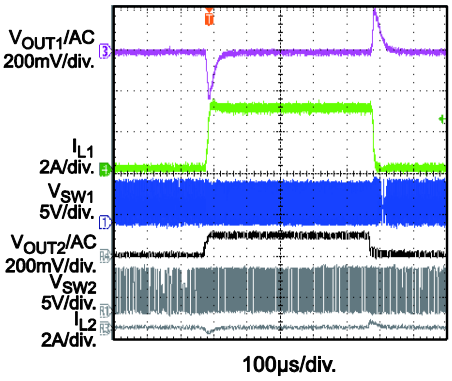


SCP Steady State



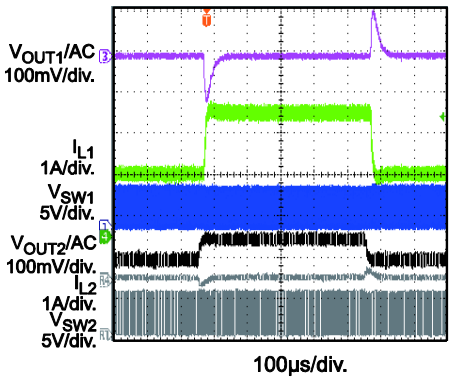
Load Transient

I_{OUT1} = 0A to 3A, I_{OUT2} = 0A to 1A, 1.6A/µs speed



Load Transient

I_{OUT1} = 1.5A to 3A, I_{OUT2} = 0.5A to 1A, 1.6A/µs speed



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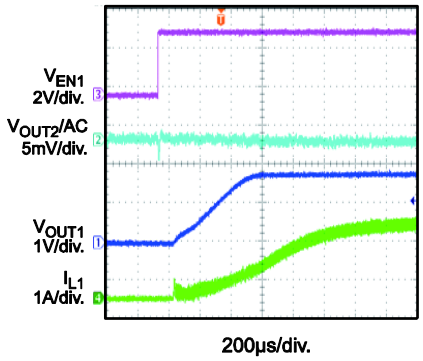
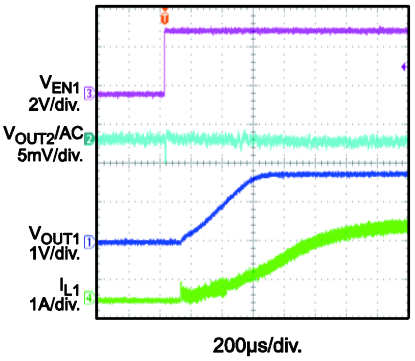
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L1 = L2 = 1.5µH, f_{SW} = 2.3MHz, T_A = 25°C, unless otherwise noted.

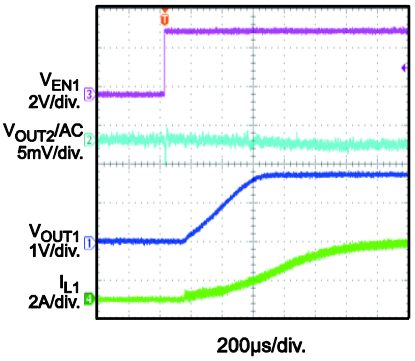
CH1 EN On, CH2 Steady State
I_{OUT1} = 2A, I_{OUT2} = 0A



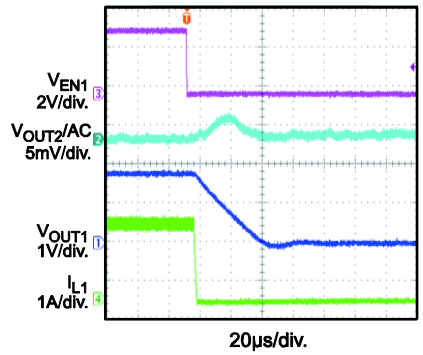
CH1 EN On, CH2 Steady State
I_{OUT1} = 2A, I_{OUT2} = 2A



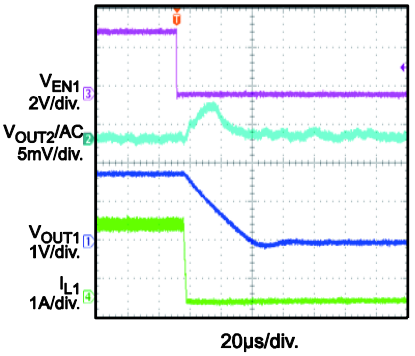
CH1 EN On, CH2 Steady State
I_{OUT1} = 3A, I_{OUT2} = 1A



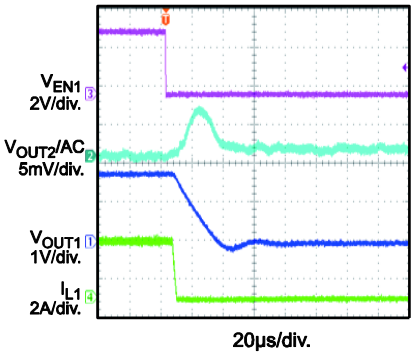
CH1 EN Off, CH2 Steady State
I_{OUT1} = 2A, I_{OUT2} = 0A



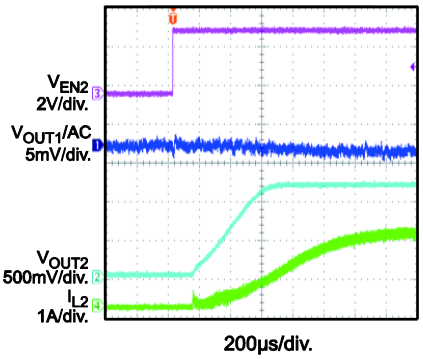
CH1 EN Off, CH2 Steady State
I_{OUT1} = 2A, I_{OUT2} = 2A



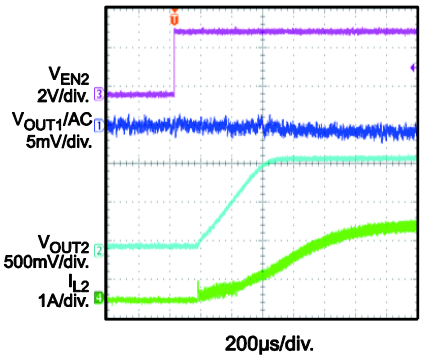
CH1 EN Off, CH2 Steady State
I_{OUT1} = 3A, I_{OUT2} = 1A



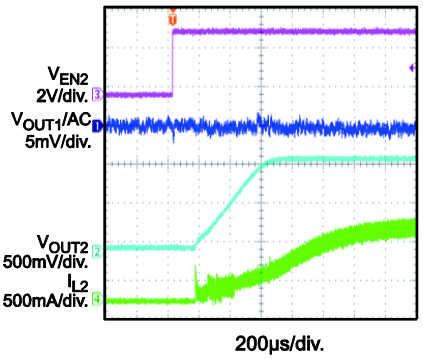
CH1 Steady State, CH2 EN On
I_{OUT1} = 0A, I_{OUT2} = 2A



CH1 Steady State, CH2 EN On
I_{OUT1} = 2A, I_{OUT2} = 2A



CH1 Steady State, CH2 EN On
I_{OUT1} = 3A, I_{OUT2} = 1A



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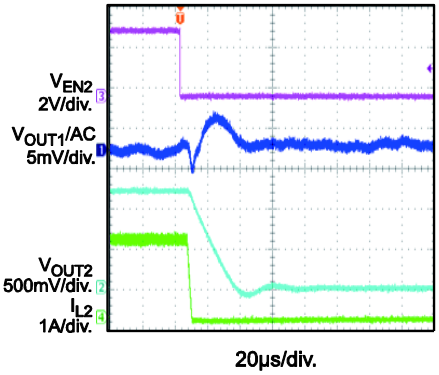
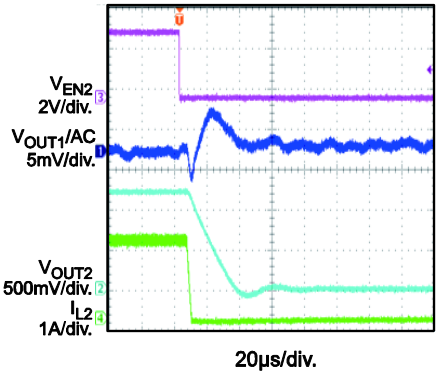
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L1 = L2 = 1.5µH, f_{SW} = 2.3MHz, T_A = 25°C, unless otherwise noted.

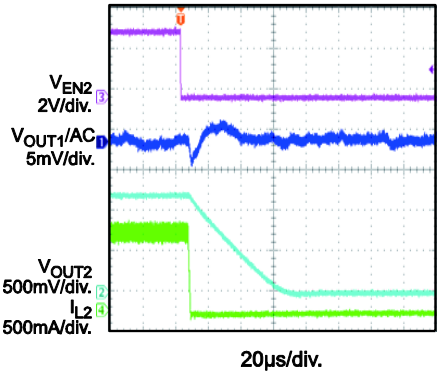
CH1 Steady State, CH2 EN Off
I_{OUT1} = 0A, I_{OUT2} = 2A



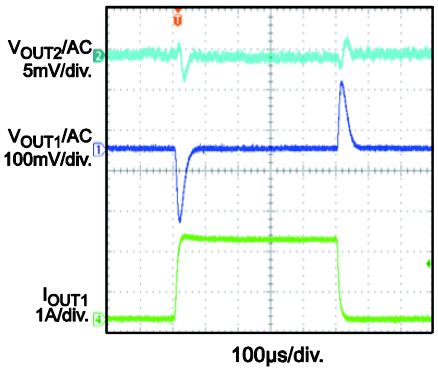
CH1 Steady State, CH2 EN Off
I_{OUT1} = 2A, I_{OUT2} = 2A



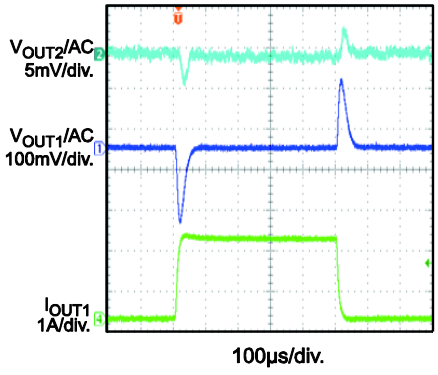
CH1 Steady State, CH2 EN Off
I_{OUT1} = 3A, I_{OUT2} = 1A



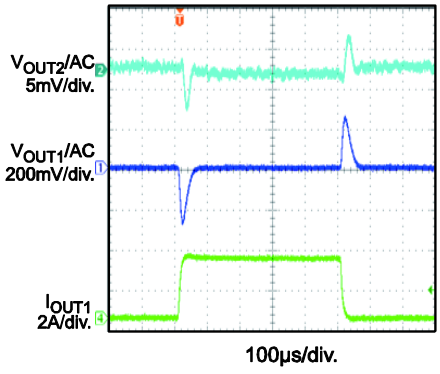
CH1 Load Transient, CH2 Steady State
I_{OUT1} = 0A to 2A, 1.6A/µs speed, I_{OUT2} = 0A



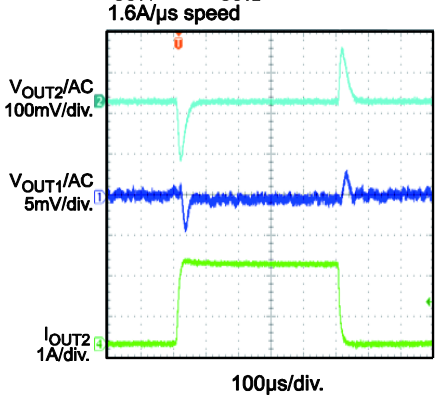
CH1 Load Transient, CH2 Steady State
I_{OUT1} = 0A to 2A, 1.6A/µs speed, I_{OUT2} = 2A



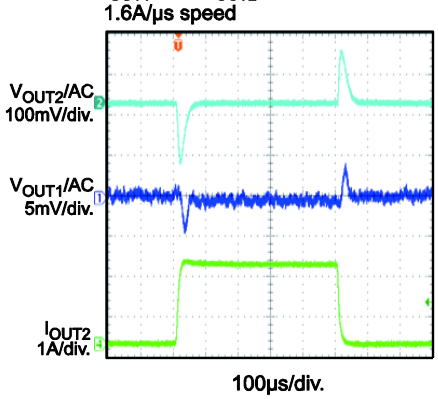
CH1 Load Transient, CH2 Steady State
I_{OUT1} = 0A to 3A, 1.6A/µs speed, I_{OUT2} = 1A



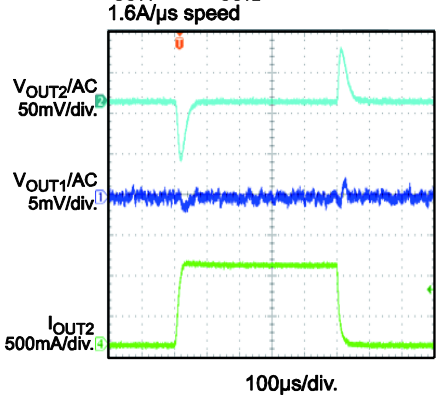
CH1 Steady State, CH2 Load Trasient
I_{OUT1} = 0A, I_{OUT2} = 0A to 2A, 1.6A/µs speed



CH1 Steady State, CH2 Load Trasient
I_{OUT1} = 2A, I_{OUT2} = 0A to 2A, 1.6A/µs speed



CH1 Steady State, CH2 Load Trasient
I_{OUT1} = 3A, I_{OUT2} = 0A to 1A, 1.6A/µs speed



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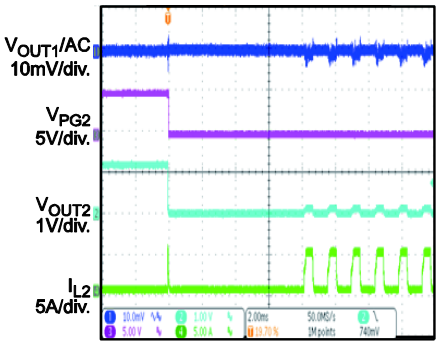
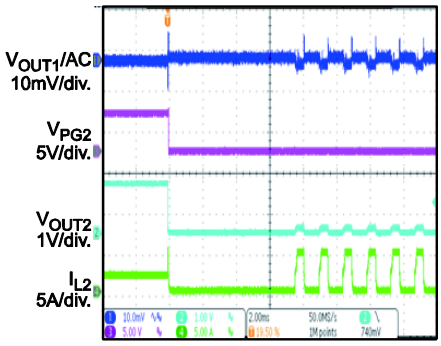
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L1 = L2 = 1.5µH, f_{SW} = 2.3MHz, T_A = 25°C, unless otherwise noted.

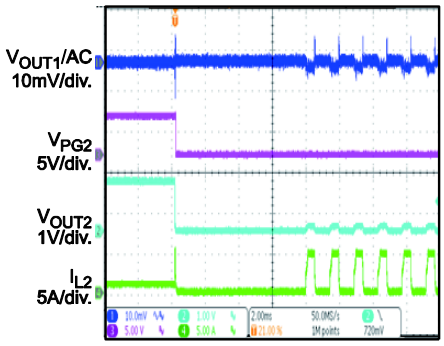
CH1 Steady State, CH2 SCP Entry
I_{OUT1} = I_{OUT2} = 0A



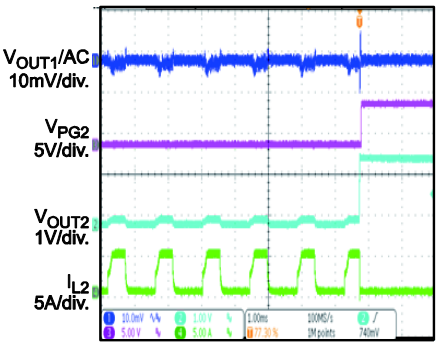
CH1 Steady State, CH2 SCP Entry
I_{OUT1} = I_{OUT2} = 2A



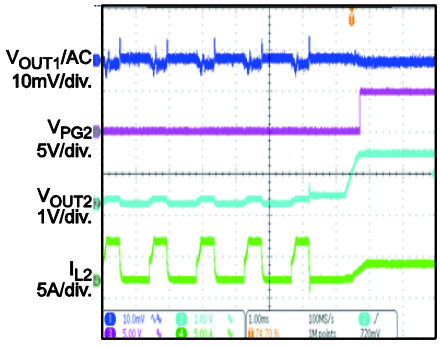
CH1 Steady State, CH2 SCP Entry
I_{OUT1} = 3A, I_{OUT2} = 1A



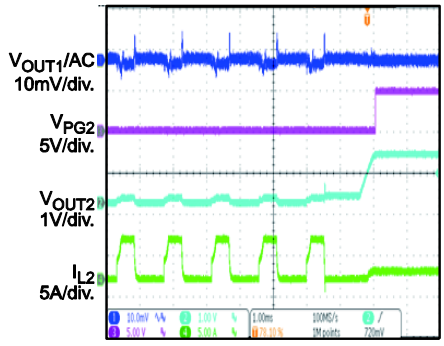
CH1 Steady State, CH2 SCP Recovery
I_{OUT1} = I_{OUT2} = 0A



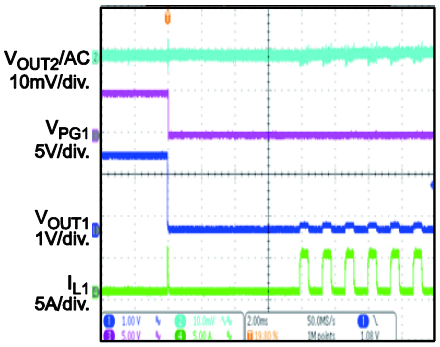
CH1 Steady State, CH2 SCP Recovery
I_{OUT1} = I_{OUT2} = 2A



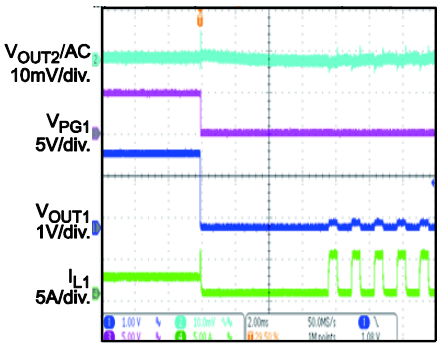
CH1 Steady State, CH2 SCP Recovery
I_{OUT1} = 3A, I_{OUT2} = 1A



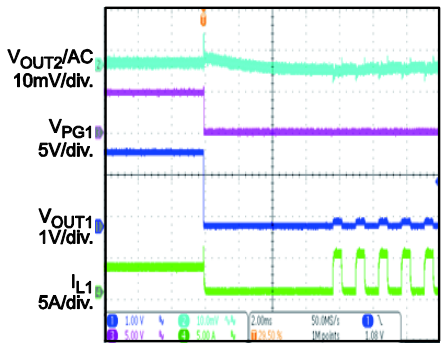
CH1 SCP Entry, CH2 Steady State
I_{OUT1} = I_{OUT2} = 0A



CH1 SCP Entry, CH2 Steady State
I_{OUT1} = I_{OUT2} = 2A



CH1 SCP Entry, CH2 Steady State
I_{OUT1} = 3A, I_{OUT2} = 1A



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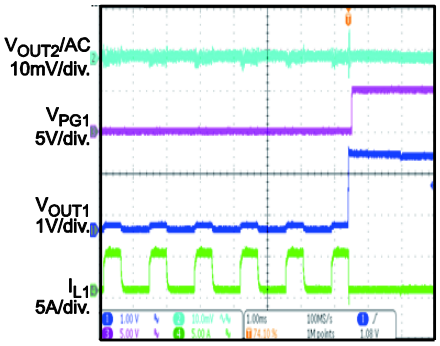
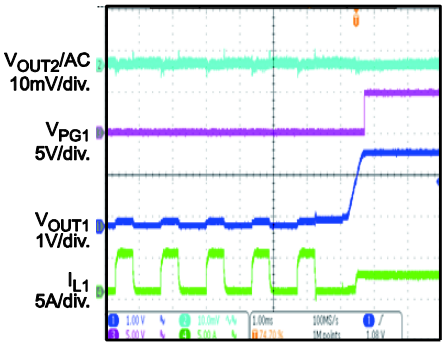
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L1 = L2 = 1.5µH, f_{SW} = 2.3MHz, T_A = 25°C, unless otherwise noted.

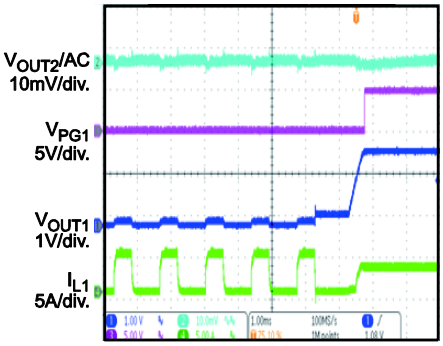
CH1 SCP Recovery, CH2 Steady State
I_{OUT1} = I_{OUT2} = 0A



CH1 SCP Recovery, CH2 Steady State
I_{OUT1} = I_{OUT2} = 2A



CH1 SCP Recovery, CH2 Steady State
I_{OUT1} = 3A, I_{OUT2} = 1A



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FUNCTIONAL BLOCK DIAGRAM

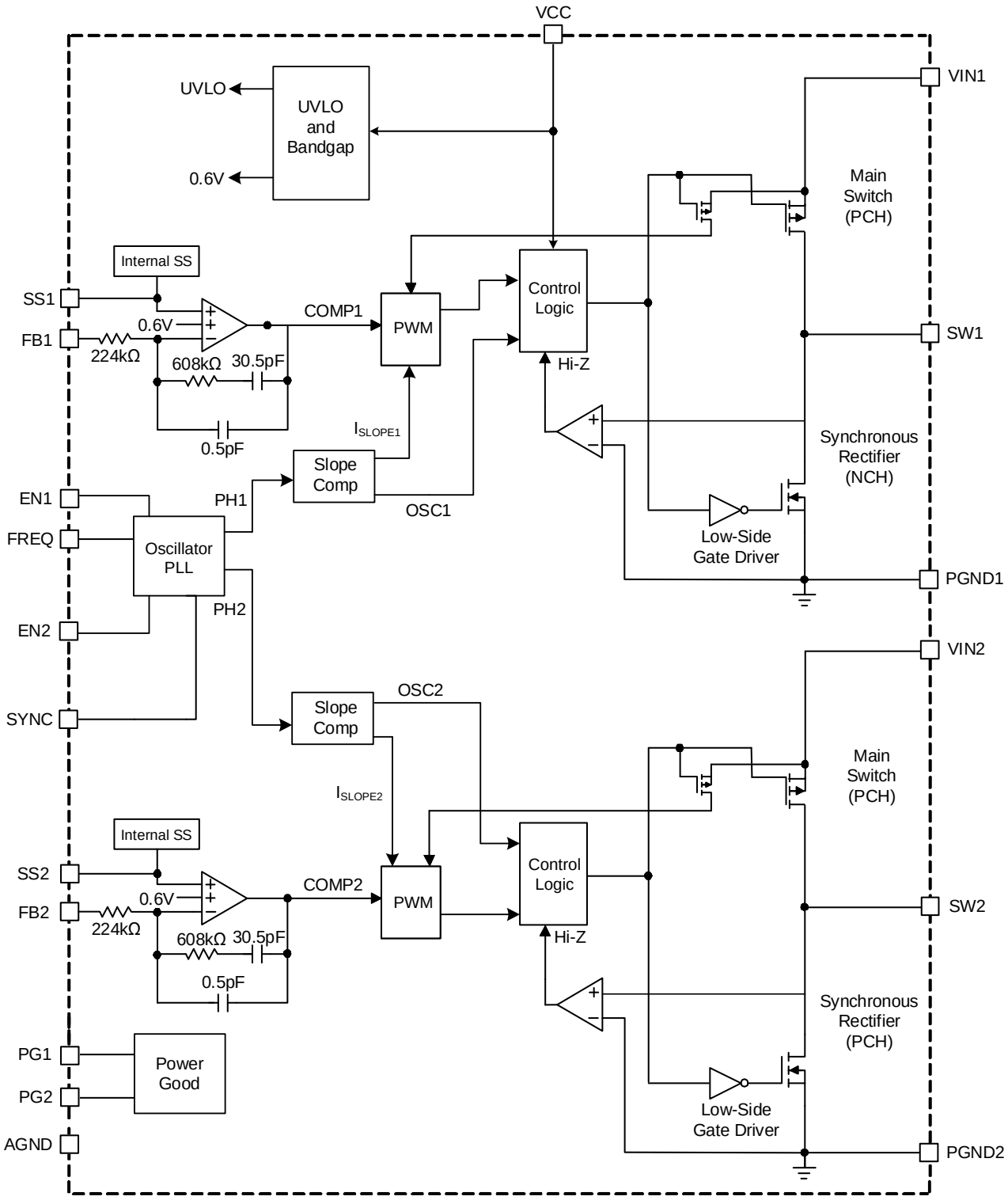

Figure 1: Functional Block Diagram

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OPERATION

The MPQ2166B is a fully integrated, dual-channel, synchronous step-down converter. Both channels use peak current mode control with internal compensation for fast transient response and cycle-to-cycle current limiting.

The MPQ2166B is optimized for low-voltage, portable applications where efficiency and small size are critical.

180° Out-of-Phase Operation

The MPQ2166B operates the two channels 180° out of phase to reduce input current ripple. This allows for a smaller input bypass capacitor to be used. When both channels operate in continuous conduction mode (CCM), two internal clocks are used (see Figure 2). The high-side MOSFET (HS-FET) turns on at the clock's rising edge for the corresponding channel.

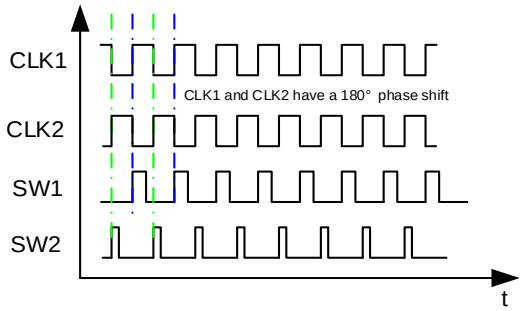

Figure 2: 180° Out-of-Phase Operation

If the switching frequency (f_{SW}) is stretched out for each channel during low-dropout mode, then the MPQ2166B runs with a fixed off time and an independent f_{SW}. After the input voltage (V_{IN}) rises high again, frequency stretch mode ends. Subsequently, pulse-width modulation (PWM) mode resumes and synchronizes with the master oscillator for 180° out-of-phase operation.

Forced Continuous Conduction Mode (FCCM)

The MPQ2166B works in forced continuous conduction mode (FCCM) with a fixed frequency from no load to full load (see Figure 3). The advantages of FCCM are its controllable frequency and lower output ripple under light-load conditions.

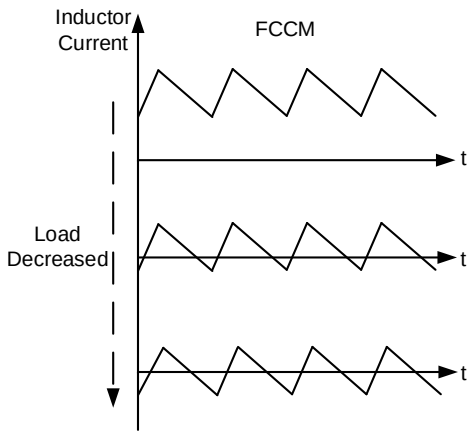

Figure 3: FCCM

Enable (EN)

EN is a digital control pin that turns the regulator on and off.

When EN is pulled below the falling threshold voltage (typically 0.8V), the chip shuts down. Pulling EN above the rising threshold voltage (typically 0.9V) turns on the part. Do not float the EN pin, since there is no internal resistor from EN to GND. If EN is floated, the part's status is uncertain, which may lead to unexpected behavior.

Soft Start (SS)

The MPQ2166B has a built-in soft start (SS) that ramps up the output voltage (V_{OUT}) at a controlled slew rate, preventing overshoot during start-up. The soft-start time (t_{SS}) is typically about 0.5ms.

t_{SS} can also be configured by an external capacitor connected to the SS pin, and can be calculated using Equation (1):

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}(V)}{I_{SS}(\mu A)} \quad (1)$$

Where C_{SS} is the external SS capacitor, V_{REF} is the internal reference voltage (0.6V), and I_{SS} is the 3.2μA SS charge current.

Oscillator and SYNC Function

The internal oscillator frequency is set by a single external resistor (R_{FREQ}) connected between FREQ and ground. The frequency-setting resistor should be placed close to the device.

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Figure 4 shows the relationship between f_{SW} and R_{FREQ}.

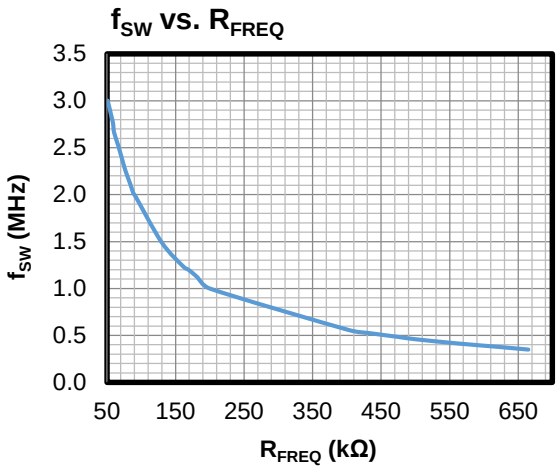

Figure 4: f_{SW} vs. R_{FREQ}

Table 1 shows the f_{SW} and R_{FREQ} values.

Table 1: f_{SW} vs. R_{FREQ}

R_{FREQ} (kΩ)	f_{SW} (kHz)	R_{FREQ} (kΩ)	f_{SW} (kHz)
665	350	90	2000
499	460	84.5	2100
200	1000	78.7	2200
169	1200	75	2300
130	1500	51	3000

The internal f_{SW} can also be synchronized to an external clock applied at the SYNC pin. The rising edge of channel 1's clock is synchronized to the external clock's rising edge, while channel 2's clock remains 180° out-of-phase from channel 1. The recommended external SYNC frequency range is 350kHz to 3MHz. While there is no pulse width requirement, note that there is always parasitic capacitance on the pad. If the pulse width is too short, a clear rising and falling edge may not be seen. It is recommended to make the pulse longer than 100ns.

Power Good (PG)

The MPQ2166B has one power good (PG) output to indicate normal operation after SS. PG is the open drain of an internal MOSFET. It should be connected to VIN, VCC, or an external voltage source through a resistor (e.g. 100kΩ). After V_{IN} is applied, the MOSFET turns on and PG is pulled to GND before SS is ready. Once the FB voltage (V_{FB}) reaches 90% of the reference voltage (V_{REF}), the MOSFET turns off and PG is pulled high by an external voltage source. If V_{FB} drops to 82% of V_{REF}, then the PG voltage is pulled to GND to indicate an output failure.

Current Limit and Short Circuit

Each channel of the MPQ2166B has a typical 4.8A current limit for the HS-FET. If V_{FB} drops to 60% of V_{REF} and SS has finished, then the MPQ2166B treats this as a short fault and attempts to recover with hiccup mode.

In hiccup mode, the MPQ2166B disables the output power stage, slowly discharges the soft-start capacitor (C_{SS}), and soft starts automatically. If the short-circuit condition still remains, the MPQ2166B repeats this operation cycle until the short circuit is removed and the output rises back to regulation levels.

Low-Dropout (LDO) Mode

The MPQ2166B allows the HS-FET to remain on for more than one switching cycle, and increases the duty cycle while V_{IN} drops down to V_{OUT}. When the duty cycle reaches 100%, the HS-FET turns on to deliver current to the output up to its current limit. The voltage drop between V_{IN} and V_{OUT} is determined by the main switch and the inductor.

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets V_{OUT}. The feedback resistor (R1) also sets the feedback (FB) loop bandwidth with the internal compensation. Figure 5 shows the feedback network.

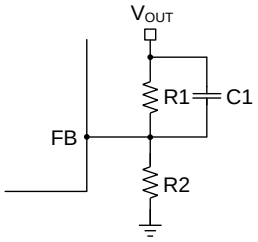

Figure 5: Feedback Network

If R1 is estimated to be 100kΩ, R2 can then be calculated using Equation (2):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6V} - 1} \quad (2)$$

Table 2 lists the recommended feedback resistor values for common output voltages.

Table 2: Resistor Selection vs. Output Voltage Setting

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C1 (pF)
1.2	100	100	22
1.5	100	66.5	22
1.8	100	49.9	22
2.5	100	31.6	22
3.3	100	22.1	22

Selecting the Inductor

It is recommended to use an inductor with a DC current rating at least 25% greater than the maximum load current for most applications. For the best efficiency, the inductor DC resistance should be below 20mΩ. For most designs, the inductance can be estimated with Equation (3):

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}} \quad (3)$$

Where ΔI_L is inductor ripple current.

Choose ΔI_L to be approximately 30% of the maximum load current. The maximum inductor peak current ($I_{L(MAX)}$) can be calculated using Equation (4):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (4)$$

Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input and the switching noise from the device. The input capacitor impedance at f_{SW} should be below the input source impedance to prevent high-frequency switching current from passing to the input source. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 22µF capacitor is sufficient.

Selecting the Output Capacitor

The output capacitor (C_O) keeps the output voltage ripple small and ensures a stable regulation loop. The C_O impedance should be low at f_{SW}. It is recommended to use ceramic capacitors with X5R or X7R dielectrics. If an electrolytic capacitor is used, pay close attention to the output ripple voltage, extra heating, and the selection of the upper feedback resistor due to the large ESR of electrolytic capacitors (see the Setting the Output Voltage section above).

The output ripple (ΔV_{OUT}) can be estimated using Equation (5):

$$\Delta V_{OUT} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times L \times f_{SW}} \times (ESR + \frac{1}{8 \times f_{SW} \times C_O}) \quad (5)$$

Power Dissipation

IC power dissipation is important in circuit design, not only because of efficiency concerns, but also because of the chip's thermal requirements. Several parameters influence power dissipation, such as conduction loss (P_{COND}), dead time (DT), switching loss (P_{SW}), MOSFET driver current (P_{DR}), and supply current (P_S).

Based on these parameters, the power loss (P_{LOSS}) can be calculated using Equation (6):

$$P_{LOSS} = P_{COND} + P_{DT} + P_{SW} + P_{DR} + P_S \quad (6)$$

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Thermal Regulation

Changes in the IC temperature can change the electrical characteristics, especially when the temperature exceeds the IC's recommended operating range. Managing the IC's temperature requires additional considerations to ensure that the IC runs within the maximum allowable temperature junction. Specific layout designs can improve the thermal profile while limiting losses to the efficiency or operating range.

For the MPQ2166B, connect the ground pin on the package to a ground plane on top of the PCB, and use this plane as a heatsink. Connect this ground plane to the ground planes beneath the IC using vias to improve heat dissipation. Given that these ground planes can introduce unwanted EMI noise and occupy valuable PCB space, design their size and shape to match the thermal resistance requirements.

Connecting the ground pin to a heatsink does not guarantee that the IC remains within its recommended temperature limits (e.g. the ambient temperature may exceed the IC's temperature limits). If the ambient air temperature approaches the IC's temperature limit, then the IC can be derated to operate using less power, which helps prevent thermal damage and unwanted electrical characteristics.

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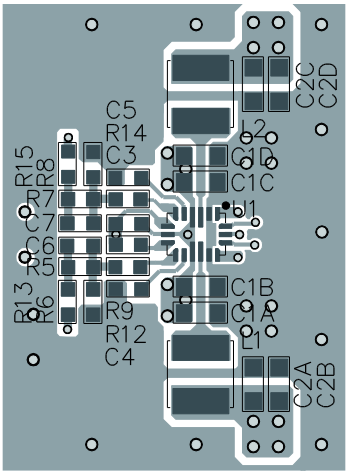
PCB Layout Guidelines [9]

Efficient PCB layout is critical for stable operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 6 and follow the guidelines below:

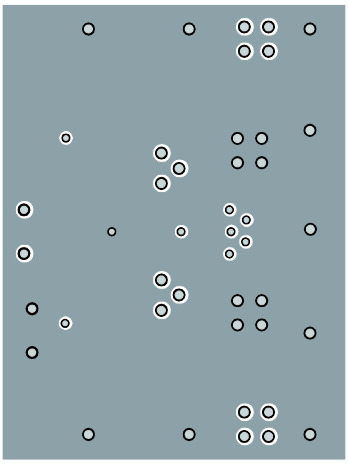
1. Connect PGND1 and PGND2 together at PGND.
2. Place the high-current paths (PGND, VIN, and SW) very close to the device with short, direct, and wide traces.
3. Place input capacitors on both sides of VIN, as close to VIN and PGND as possible.
4. Place the decoupling capacitor as close to VCC and AGND as possible.
5. Keep the switching node (SW) short, and route it away from the feedback network.
6. Place the external feedback resistors next to FB.
7. Do not place vias on the FB trace.
8. Connect PGND to a large copper area to improve thermal performance.

Note:

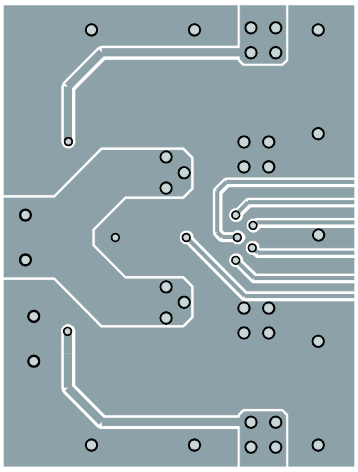
9) The recommended PCB layout is based on Figure 7 on page 24.



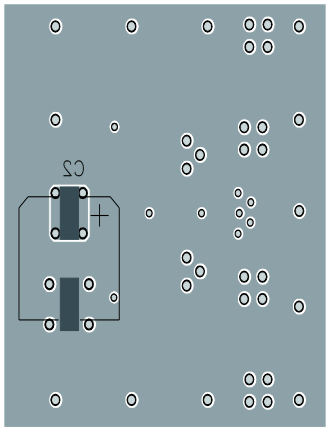
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 6: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUIT

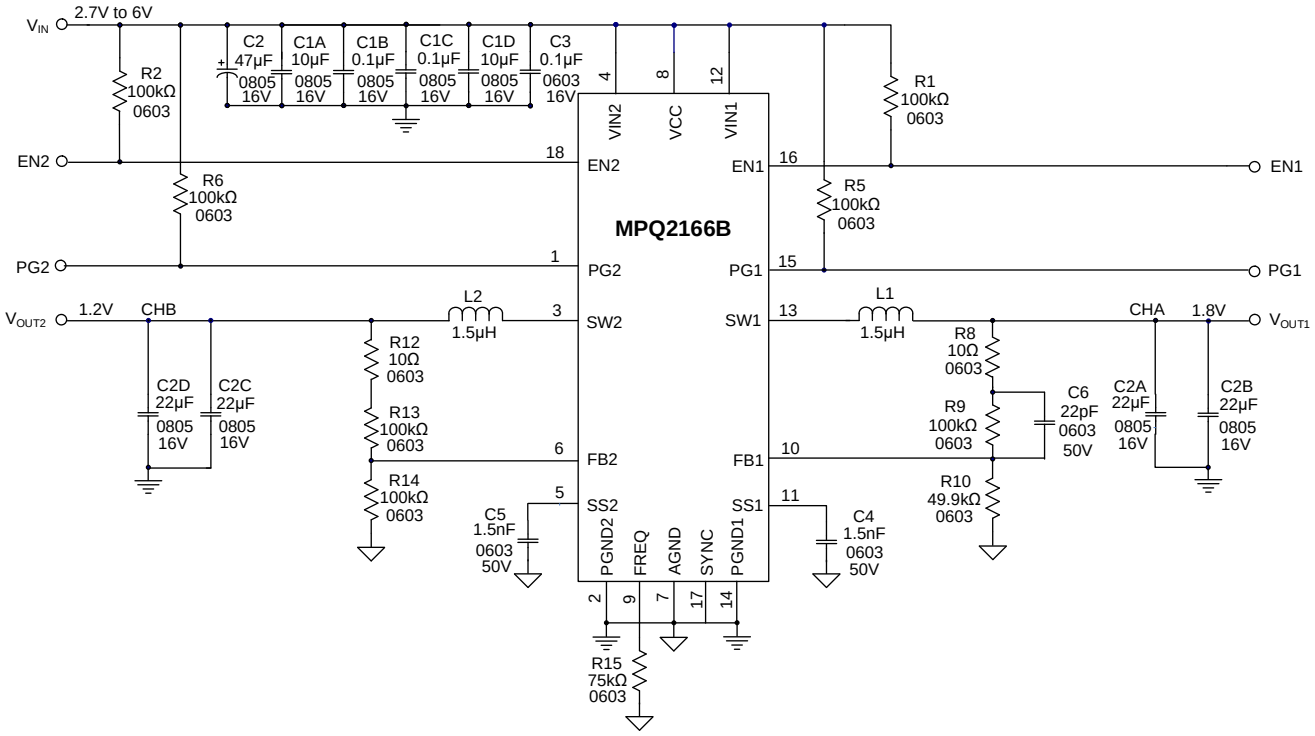

Figure 7: Typical Application Circuit (1.8V/1.2V V_{OUT})

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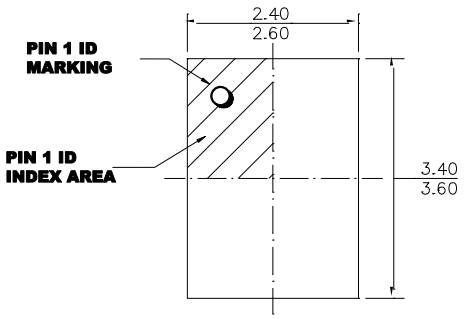
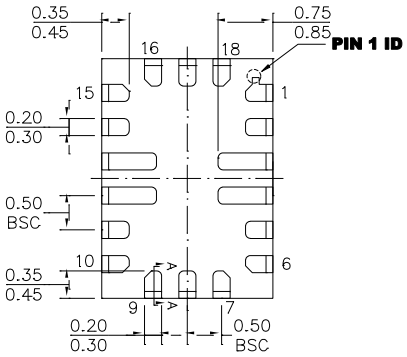
PACKAGE INFORMATION

QFN-18 (2.5mmx3.5mm)

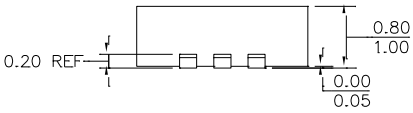
Wettable Flank



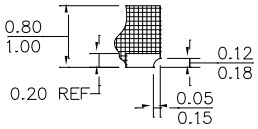
TOP VIEW



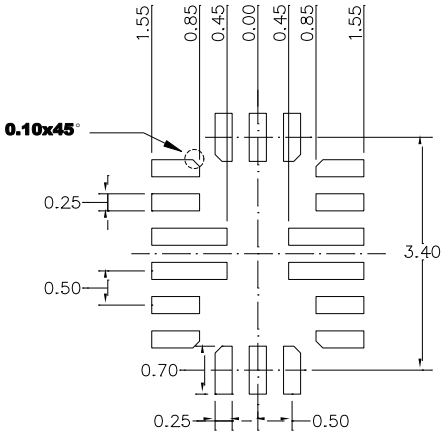
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) LAND PATTERNS OF PIN3, 4, 12 AND 13 HAVE THE SAME LENGTH AND WIDTH.
3) ALL DIMENSIONS ARE IN MILLIMETERS.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.

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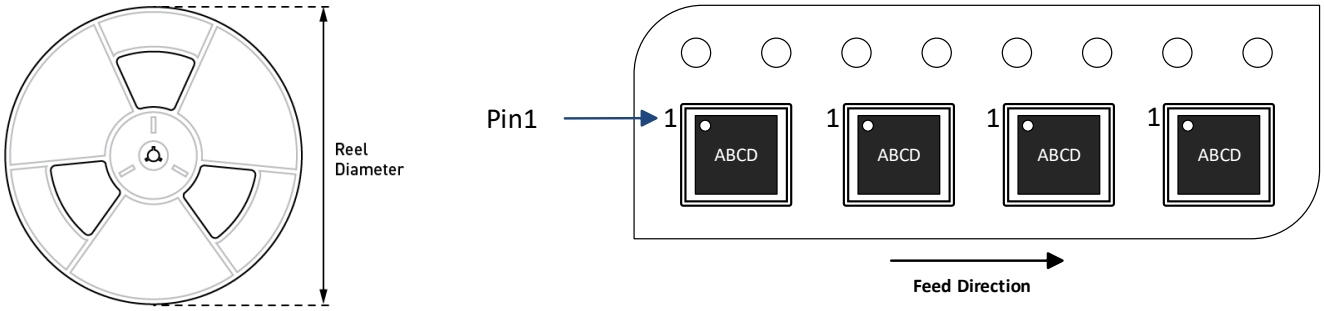
CARRIER INFORMATION



Part Number	Package Description	Quantity /Reel	Quantity /Tube	Quantity /Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ2166BGRHE-AEC1-Z	QFN-18 (2.5mmx3.5mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	1/18/2022	Initial Release	-

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