MPQ2024A

40V, 300mA, Phantom Antenna LDO with Pre-Boost, I²C, and ADC for Digital Diagnosis and Protection, AEC-Q100 Qualified

DESCRIPTION

The MPQ2024A is a low-dropout (LDO) regulator that contains a boost pre-regulator operating at either 400kHz or 2.2MHz with I²C interface and one-time programmable (OTP) memory. The device provides phantom power to low-noise amplifiers (LNAs) for active antennas in automotive systems from a cold crank through load dump (3V to 40V) input voltage (V_{IN}) conditions.

It delivers up to 300mA of load current, with excellent load and line regulation. During normal operation, when the battery is healthy, the pre-boost is completely turned off to reduce the quiescent current (I_Q), which makes the device suitable for always-on power supplies.

The MPQ2024A also integrates a MOSFET in the pre-boost to further reduce the external component count and EMI. Both the LDO and boost outputs are configurable through I²C interface. The pre-boost output voltage ($V_{OUT-BOOST}$) is adjustable from 6.5V to 15.9V. The LDO output voltage (V_{OUT}) is adjustable from 1V to 13.6V. The LDO output is protected during load dump conditions.

During bench evaluations, different configurations can be easily obtained via the I²C interface instead of reworking external components. Once the desired setting has been reached, a one-time programmable (OTP) memory allows the settings to be permanently stored.

The MPQ2024A is available in a QFN-16 (4mmx4mm) package with wettable flanks, and is AEC-Q100 qualified.

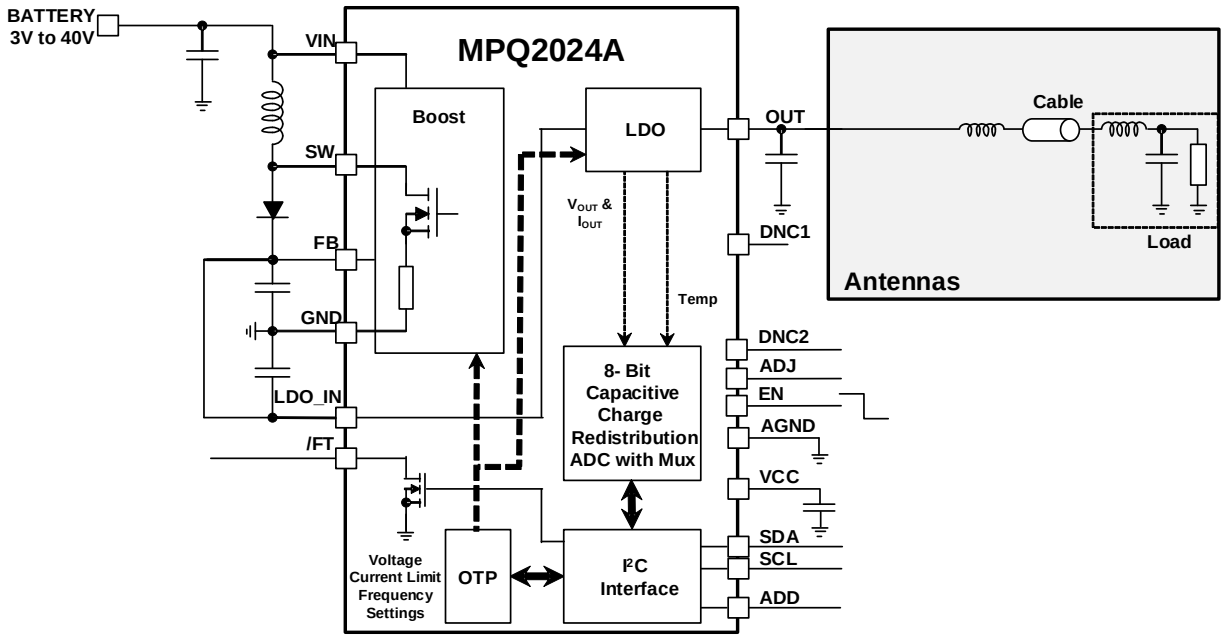
FEATURES

- Powerful Digital Functions:
  - No External Resistor Network for Output Voltage Settings
  - Configurable LDO
    - 300mA Continuous Output Current (I_{OUT})
    - 1V to 13.6V Output Voltage (V_{OUT}) Range
    - Over-Temperature Protection
  - Configurable Asynchronous Pre-Boost Regulator
    - 4A/40V Internal MOSFET
    - 6.5V to 15.9V Output Voltage ($V_{OUT-BOOST}$) Range with 100mV Adjustable Steps
    - Switching Frequency (f_{SW}) Configurable to 400kHz or 2.2MHz
    - Over-Temperature Protection
  - I²C Interface
  - Analog-to-Digital Converter (ADC) for LDO V_{OUT} and Load Current
  - One-Time Programmable (OTP) Memory
- Optimized for EMC/EMI:
  - Frequency Dithering for Low EMI
- Additional Features:
  - Wide 3V to 40V V_{IN} Range
  - 35µA Low Quiescent Current (I_Q)
  - LDO Short-to-Battery Detection
  - Soft Start for Both Regulator Outputs
  - Open-Load Detection
  - Available in a QFN-16 (4mmx4mm) Package
  - Available in a Wettable Flank Package
  - Available in AEC-Q100 Grade 1

APPLICATIONS

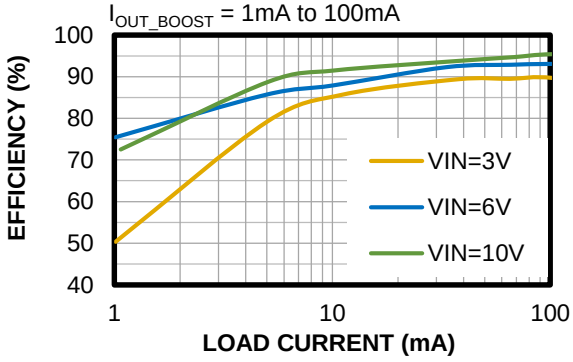
- Automotive Antenna Phantom Power
- Automotive Cameras
- Automotive ADAS Systems with Functional Safety and ASIL Requirements

TYPICAL APPLICATION



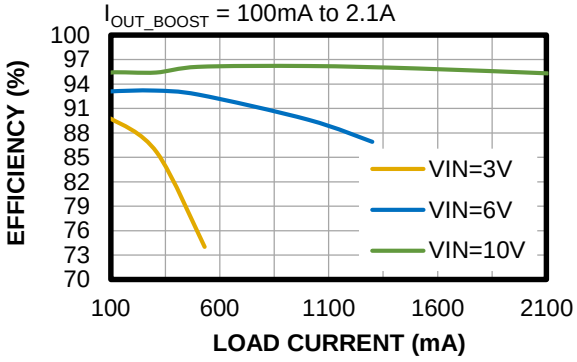
Boost Efficiency vs. Load Current

LDO disabled, V_{OUT_BOOST} = 12V,
f_{SW} = 400kHz, L = 10µH (DCR = 45mΩ),
B350A-13-F rectifier diode, FSS on,
I_{OUT_BOOST} = 1mA to 100mA



Boost Efficiency vs. Load Current

LDO disabled, V_{OUT_BOOST} = 12V,
f_{SW} = 400kHz, L = 10µH (DCR = 45mΩ),
B350A-13-F rectifier diode, FSS on,
I_{OUT_BOOST} = 100mA to 2.1A



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating***
MPQ2024AGRE-xxxx-AEC1**	QFN-16 (4mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ2024AGRE-xxxx-AEC1-Z).

** “xxxx” is the configuration code identifier for the register settings stored in the OTP register. Each “x” can be a hexadecimal value between 0 and F. The default code is “0000.” Please contact an MPS FAE to create this unique number.

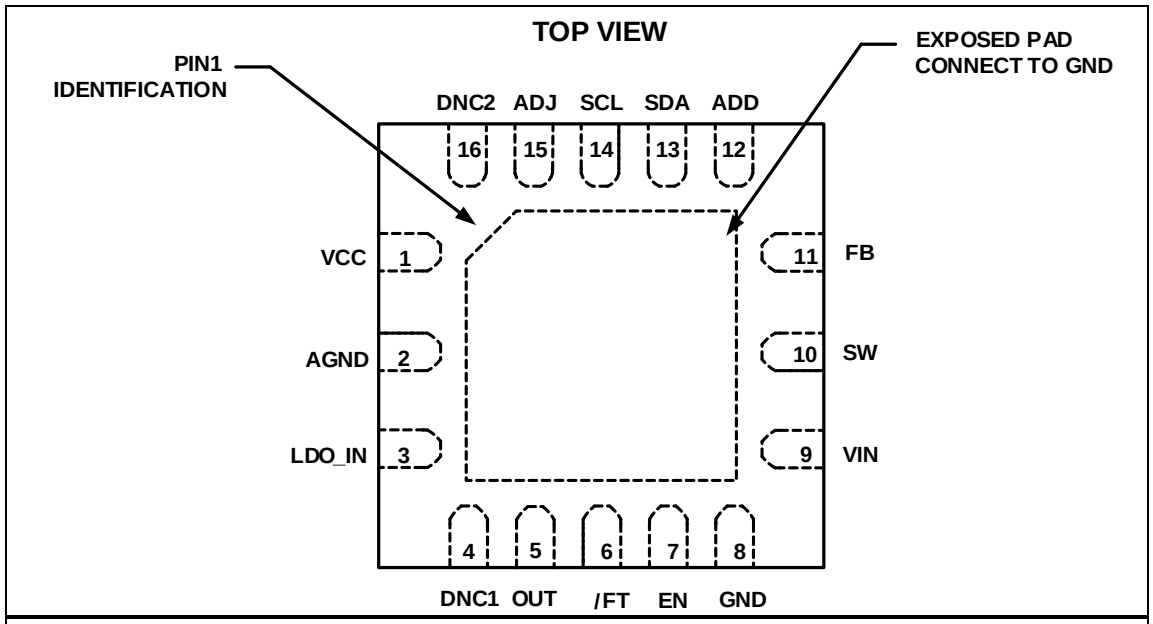
*** Moisture Sensitivity Level Rating

TOP MARKING

MPSYWW
M2024A
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
M2024A: Part number
LLLLLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



QFN-16 (4mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1	VCC	**Bias supply.** This 5V internal regulator output supplies power to the I^2C interface, internal control circuit, and gate drivers. Place an external, low-ESR decoupling capacitor connected to ground close to this pin. A 1µF to 10µF ceramic capacitor is recommended.
2	AGND	**Analog ground.** Ground for internal logic and signal control blocks.
3	LDO_IN	**LDO supply input.** In addition to the capacitors for the boost converter on the FB pin, place a 1µF to 10µF ceramic between LDO_IN and ground.
4	DNC1	**Do not connect.** Leave this pin floating.
5	OUT	**LDO output.** Only a low-value ceramic capacitor is required as an output capacitor for stability. A 10µF ceramic capacitor is recommended for most applications.
6	/FT	**Fault pin output.** This pin is an open-drain status pin. Connect this pin to a ≤5V voltage source using a resistor (e.g. 100kΩ). If this pin is not used, leave it floating or connect it to ground.
7	EN	**Enable.** Pull this pin below the falling threshold (2.2V) to shut down the chip. Pull it above the rising threshold (2.4V) or connect it to VIN via a pull-up resistor (e.g. 100kΩ) to enable the chip. There is an internal 3.3MΩ pull-down resistor. Leaving EN floating disables the chip.
8	GND	**Power ground.** This pin is the reference ground for the regulated output voltage. Connect this pin to larger copper areas for the best thermal performance.
9	VIN	**Input supply.** VIN supplies power to all of the internal control circuitries and the power MOSFET that is connected to SW. Place a decoupling capacitor to ground as close to this pin as possible.
10	SW	**Switching node.** This pin is the switching node of the asynchronous pre-boost converter.
11	FB	**Boost converter feedback.** An internal resistor divider is connected between this pin and ground. Connect this pin to the rectifier diode of the asynchronous pre-boost converter. The boost converter output capacitors should be placed as close to this pin as possible, with a short return path to the ground plane.
12	ADD	**I^2C address setting.** Connect a resistor between this pin and ground to set the I^2C address. If not used, float this pin.
13	SDA	**I^2C serial data.** This pin is an open-drain port, and cannot be floated. An external pull-up resistor is required to connect this pin to the I^2C bus supply rail. If SDA is not used, it is recommend to connect SDA to the VCC pin through a resistor (e.g. 100kΩ).
14	SCL	**I^2C serial clock.** This pin is an open-drain port, and cannot be floated. An external pull-up resistor is required to connect this pin to the I^2C bus supply rail. If SCL is not used, it is recommend to connect SCL to the VCC pin through a resistor (e.g. 100kΩ).
15	ADJ	**LDO reference voltage input.** In LDO output voltage tracking mode, connect this pin directly to the voltage reference or with a voltage divider for lower output voltages. If this pin is not used, leave it floating or connect it to ground.
16	DNC2	**Do not connect.** Connect this pin to ground or leave it floating.
-	Exposed pad	**Exposed thermal power pad.** Connect the exposed pad to the ground plane for optimal heat dissipation. Do not use the exposed pad as the primary electrical ground connection.

ABSOLUTE MAXIMUM RATINGS (1)

VIN, SW, FB, LDO_IN.....-0.3V to +45V
DNC1, OUT .....-0.3V to +18V
DNC2, ADJ .....-0.3V to +15V
All other pins .....-0.3V to +5.5 V
Continuous power dissipation (T_A = 25°C) (2) (6)
QFN-16 (4mmx4mm)..... 4W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM)
VCC-VIN ..... Class 1C (3)
Other pins .....Class 2 (3)
Charged-device model (CDM) ..... Class C2b (4)

Recommended Operating Conditions

Input voltage (V_{IN}) .....3V to 40V
Pre-boost output voltage ($V_{OUT-BOOST}$) .....
.....6.5V to 15.9V
LDO output voltage (V_{OUT}) .....1V to 13.6V
LDO load current range (I_{OUT}) 300mA
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-16 (4mmx4mm)
JESD51-5,7 .....40.4 .....6 ..°C/W (5)
EVQ2024A-R-00A ..... 31.....5.5. °C/W (6)

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per AEC-Q100-002.
4) Per AEC-Q100-011.
5) Measured on a JESD51-5,7, 4-layer PCB, where a thermal via array under the exposed pad. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-5,7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application, the value of θ_{JC} shows the thermal resistance from junction-to-case bottom.
6) Measured on the EVQ2024A-R-00A, a 4-layer, 2oz, 9cmx9cm, PCB. The value of θ_{JC} shows the thermal resistance from junction-to-case top.

ELECTRICAL CHARACTERISTICS

Typical values are at V_{IN} = 13.5V, V_{EN} = 3V, T_J = 25°C, all voltages with respect to ground, unless otherwise noted. Minimum and maximum values are at V_{IN} = 13.5V, V_{EN} = 3V, T_J = -40°C to +150°C, all voltages with respect to ground, guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input Voltage-Current Parameters						
Input voltage	V_{IN}		3		40	V
Quiescent supply current	I_Q	LDO enabled, boost disabled, V_{OUT} = 9V, ADC disabled, no load, T_J = 25°C		35		µA
		LDO enabled, boost disabled, V_{OUT} = 9V, ADC disabled, no load, T_J = -40°C to +150°C			135	µA
Shutdown supply current	I_{SD}	V_{EN} = 0V			5	µA
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_RISING}$	Boost enabled	2.6	2.8	3	V
		Boost disabled		4.2		
V_{IN} UVLO falling threshold	$V_{IN\_UVLO\_FALLING}$	Boost enabled	1.8	2	2.2	V
		Boost disabled		3.8		V
Pre-boost under-voltage (UV) filtering time	t_{BST-UV}	Time after V_{IN} falls below the boost turn-on threshold to generate the first switching pulse	10		200	µs
Thermal Shutdown and Over-Temperature Protection						
Thermal shutdown (7)	T_{SD}	Junction temperature rising		170		°C
Thermal shutdown hysteresis (7)	T_{SD-HYS}			20		°C
/FT						
/FT sink current capacity	$V_{FT-SINK}$	Sink 4mA			300	mV
/FT delay time	$t_{FT-DELAY}$	Rising edge		40		µs
		Falling edge		40		µs
/FT leakage current	I_{FT-LKG}			10	100	nA
Enable (EN)						
EN rising threshold	$V_{EN\_TH\_R}$	Level sensitive input	2.1	2.4	2.7	V
EN falling threshold	$V_{EN\_TH\_F}$	Level sensitive input	1.9	2.2	2.5	V
EN threshold hysteresis	V_{EN-HYS}			200		mV
EN input current	I_{EN}	V_{EN} = 2V		0.6	1.2	µA
Internal VCC						
VCC regulator	V_{CC}	I_{CC} = 0mA	4.8	5	5.2	V
Fault Detection						
Start-up short-to-battery (STB) detection window	t_{BLK-RC}	Default setting: Reg0x0F, bits[7:6] = 00		15		ms
		Reg0x0F, bits [7:6] = 01		7		
		Reg0x0F, bits [7:6] = 10		3		
		Reg0x0F, bits [7:6] = 11		1		
Short to battery threshold	V_{STB}	V_{OUT} - V_{IN} , check during start-up sequence		-80	-10	mV
Linear Regulator (LDO)						
Regulated output range	V_{OUT}	Configurable range	1		13.6	V
		Default setting		9		V
Output voltage accuracy	Acc_{VOUT}	Default setting V_{OUT} = 9V, T_J = 25°C	-2		+2	%
		Default setting V_{OUT} = 9V, T_J = -40°C to +150°C	-3		+3	
		V_{OUT} = 1V to 13.6V, T_J = 25°C	-3		+3	
		V_{OUT} = 1V to 13.6V, T_J = -40°C to +150°C	-4		+4	

ELECTRICAL CHARACTERISTICS *(continued)*

Typical values are at V_{IN} = 13.5V, V_{EN} = 3V, T_J = 25°C, all voltages with respect to ground, unless otherwise noted. Minimum and maximum values are at V_{IN} = 13.5V, V_{EN} = 3V, T_J = -40°C to +150°C, all voltages with respect to ground, guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Linear Regulator (LDO)						
Line regulation	dV_{A_LINE}	V_{IN} = 3V to 40V, 5mA load current, V_{OUT} = 9V	-10	1	+10	mV
Load regulation	dV_{A_LOAD}	I_{LOAD} = 5mA to 300mA, V_{OUT} = 9V, T_J = 25°C		30	50	mV
Power supply rejection ratio (7)	PSRR	I_{LOAD} = 100mA at 100Hz, V_{OUT} = 9V		60		dB
Dropout voltage	$V_{DROPOUT}$	I_{LOAD} = 100mA, measured between LDO_IN and OUT, T_J = 25°C		250	400	mV
		I_{LOAD} = 100mA, measured between LDO_IN and OUT, T_J = -40°C to +150°C			700	
Over-current (OC) limit	$I_{LDO-LIMIT}$	Configurable range	100		500	mA
		Default value		400		mA
Current limit accuracy	$Acc_{ILDO-LIMIT}$	LDO_IN - OUT > $V_{DROPOUT}$, 500mA ≥ $I_{LDO-LIMIT}$ > 200mA, T_J = 25°C	-10		+10	%
		LDO_IN - OUT > $V_{DROPOUT}$, 500mA ≥ $I_{LDO-LIMIT}$ > 200mA, T_J = -40°C to +150°C	-15		+15	
		LDO_IN - OUT > $V_{DROPOUT}$, 100mA ≤ $I_{LDO-LIMIT}$ ≤ 200mA, T_J = 25°C	-15		+15	
		LDO_IN - OUT > $V_{DROPOUT}$, 100mA ≤ $I_{LDO-LIMIT}$ ≤ 200mA, T_J = -40°C to +150°C	-20		+20	
Pre-Boost Regulator						
Boost turn-on threshold	V_{BST_TH}	Configurable range	6.5		15	V
		Default value		11		V
Boost turn-on threshold hysteresis	V_{BST_TH-HYS}			200		mV
Boost regulated output range	$V_{OUT-BOOST}$	V_{IN} - V_{OUT} > 0.5V	6.5		15.9	V
		Default setting		12		V
Boost output voltage accuracy	$Acc_{VOUT-BOOST}$	Default setting $V_{OUT-BOOST}$ = 12V, T_J = 25°C	-2		+2	%
		Default setting $V_{OUT-BOOST}$ = 12V, T_J = -40°C to +150°C	-3		+3	
		$V_{OUT-BOOST}$ = 6.5V to 15.9V, T_J = 25°C	-3		+3	
		$V_{OUT-BOOST}$ = 6.5V to 15.9V, T_J = -40°C to +150°C	-4		+4	
Internal N-channel MOSFET current limit	$I_{LS-LIMIT}$	Peak	3	4		A
FB input current	I_{FB}	V_{FB} = 0.85V, T_J = 25°C		1	50	nA
Low-side MOSFET (LS-FET) on resistance (N-channel)	$R_{DS(ON)\_BOOST}$			180		mΩ

ELECTRICAL CHARACTERISTICS *(continued)*

Typical values are at V_{IN} = 13.5V, V_{EN} = 3V, T_J = 25°C, all voltages with respect to ground, unless otherwise noted. Minimum and maximum values are at V_{IN} = 13.5V, V_{EN} = 3V, T_J = -40°C to +150°C, all voltages with respect to ground, guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Pre-Boost Regulator						
LS-FET leakage current (N-channel)	I_{N-LKG}	V_{SW} = 13.5V, V_{OUT} = 0V, T_J = 25°C		20	150	nA
		V_{SW} = 13.5V, V_{OUT} = 0V, T_J = -40°C to +150°C			1500	
Switching frequency	f_{SW}	Boost switching frequency, 400kHz/2.2MHz configurable	0.3	0.4	0.5	MHz
			1.8	2.2	2.6	
Minimum on time	t_{ON-MIN}			60		ns
Minimum off time	$t_{OFF-MIN}$			40		ns
Boost soft-start time	t_{SS}	V_{IN} = 5V, V_{OUT_BST} = 12V		1		ms

Note:

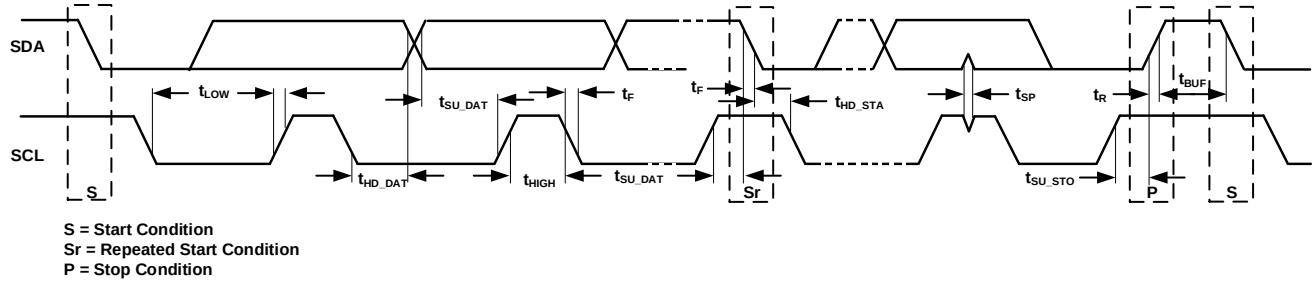
7) Not tested in production. Guaranteed by design and characterization.

I²C PORT SIGNAL CHARACTERISTICS

Typical values are at V_{IN} = 13.5V, V_{EN} = 3V, T_J = 25°C, all voltages with respect to ground, unless otherwise noted. Minimum and maximum values are at V_{IN} = 13.5V, V_{EN} = 3V, T_J = -40°C to +150°C, all voltages with respect to ground, guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
I²C Interface Specifications						
Input logic low	V_{IL}		0		0.4	V
Input logic high	V_{IH}		1.3			V
Output logic low	V_{OL}	I_{LOAD} = 3mA			0.4	V
SCL clock frequency	f_{SCL}				400	kHz
SCL high time	t_{HIGH}		0.6			µs
SCL low time	t_{LOW}		1.3			µs
Data set-up time	$t_{SU,DAT}$		100			ns
Data hold time	$t_{HD,DAT}$		0		0.9	µs
Set-up time for a repeated start condition	$t_{SU,STA}$		0.6			µs
Hold time for a start condition	$t_{HD,STA}$		0.6			µs
Bus free time between a start and a stop condition	t_{BUF}		1.3			µs
Set-up time for a stop condition	$t_{SU,STO}$		0.6			µs
SCL and SDA rising time	t_R		20 + 0.1 x C_B		120	ns
SCL and SDA falling time	t_F		20 + 0.1 x C_B		120	ns
Pulse width of suppressed spike	t_{SP}		0		50	ns
Capacitance bus for each bus line	C_B				400	pF

I²C TIMING DIAGRAM



S = Start Condition
Sr = Repeated Start Condition
P = Stop Condition

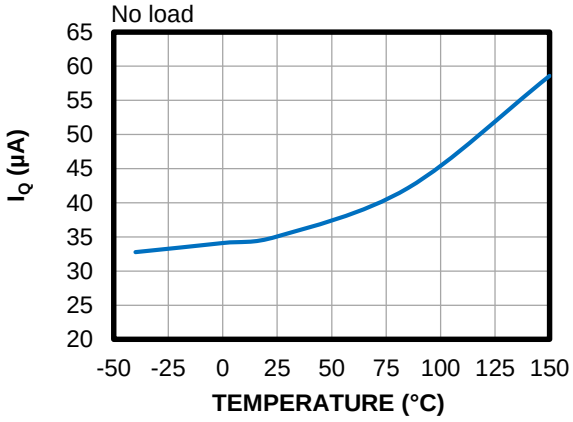
Figure 1: I²C-Compatible Interface Timing Diagram

TYPICAL CHARACTERISTICS

V_{IN} = 13.5V, V_{OUT} = 9V, V_{EN} = 3V, T_J = -40°C to +150°C, unless otherwise noted.

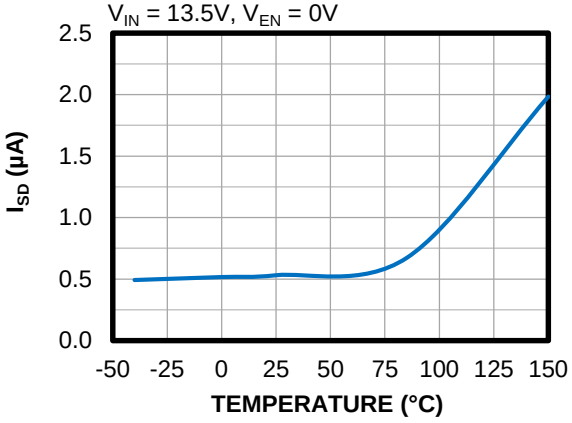
Quiescent Current vs. Temperature

No load



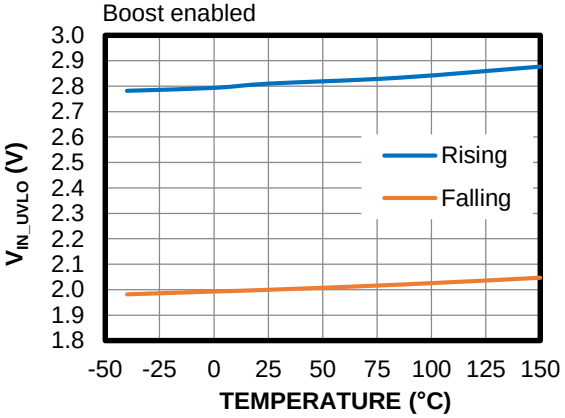
Shutdown Current vs. Temperature

V_{IN} = 13.5V, V_{EN} = 0V



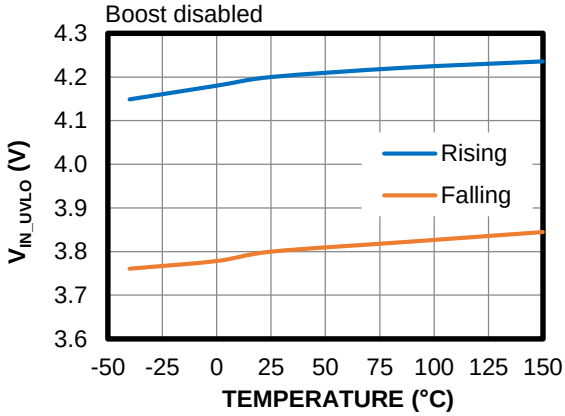
V_{IN} UVLO Threshold vs. Temperature

Boost enabled

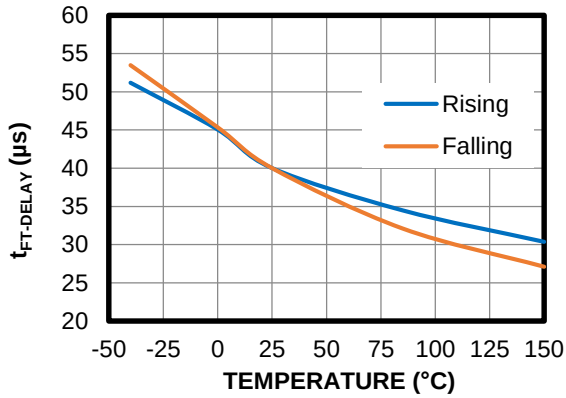


V_{IN} UVLO Threshold vs. Temperature

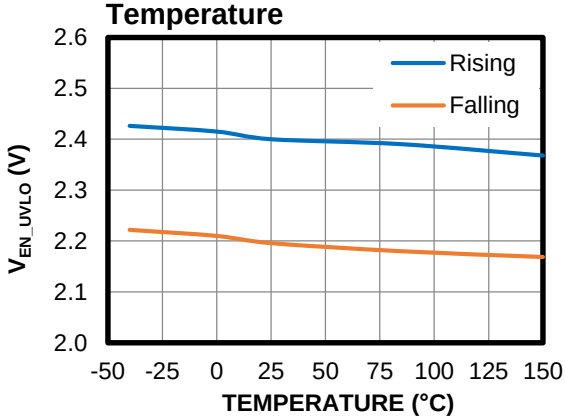
Boost disabled



/FT Delay Time vs. Temperature



EN UVLO Threshold vs. Temperature

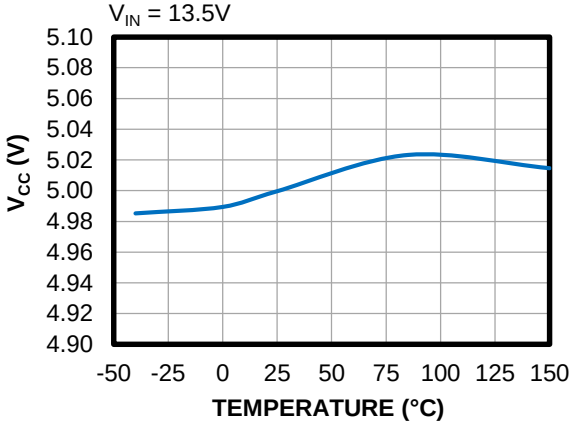


TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 13.5V, V_{OUT} = 9V, V_{EN} = 3V, T_J = -40°C to +150°C, unless otherwise noted.

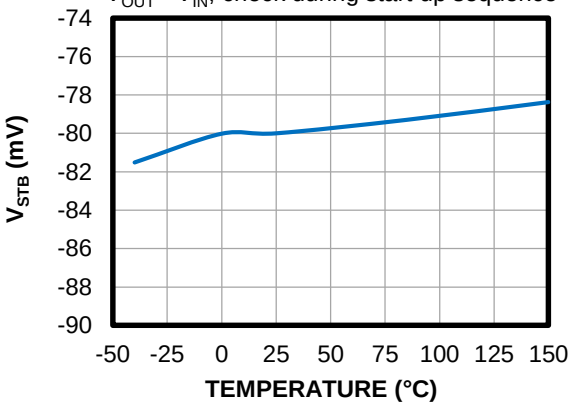
V_{CC} vs. Temperature

V_{IN} = 13.5V



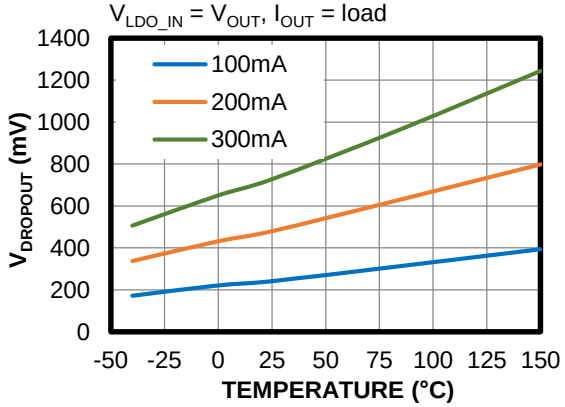
Short-to-Battery Threshold vs. Temperature

V_{OUT} - V_{IN}, check during start-up sequence



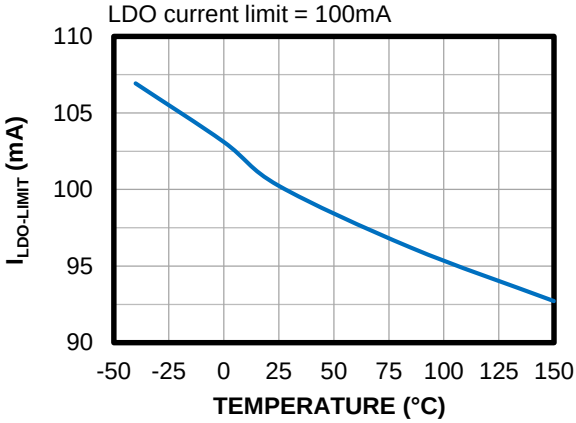
Dropout Voltage vs. Ambient Temperature

V_{LDO_IN} = V_{OUT}, I_{OUT} = load



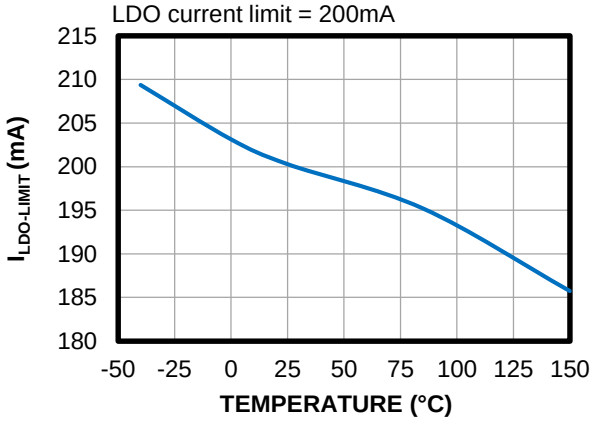
LDO Current Limit vs. Temperature

LDO current limit = 100mA



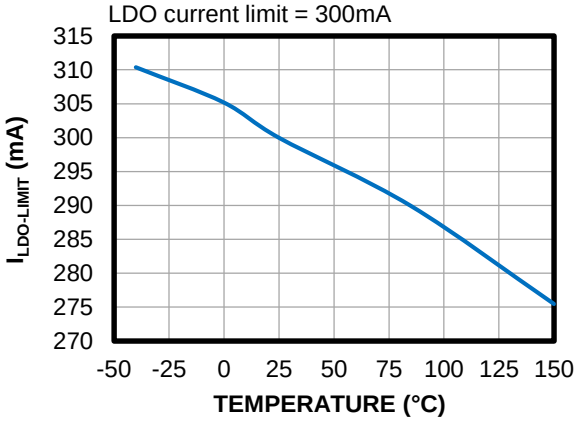
LDO Current Limit vs. Temperature

LDO current limit = 200mA



LDO Current Limit vs. Temperature

LDO current limit = 300mA

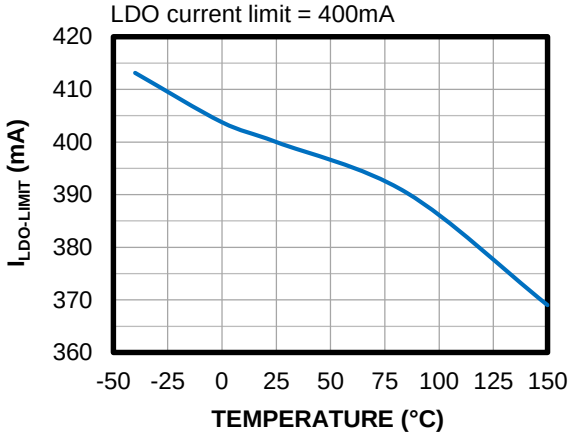


TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 13.5V, V_{OUT} = 9V, V_{EN} = 3V, T_J = -40°C to +150°C, unless otherwise noted.

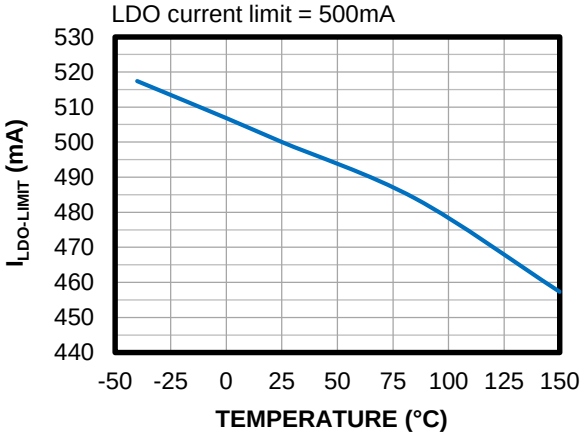
LDO Current Limit vs. Temperature

LDO current limit = 400mA

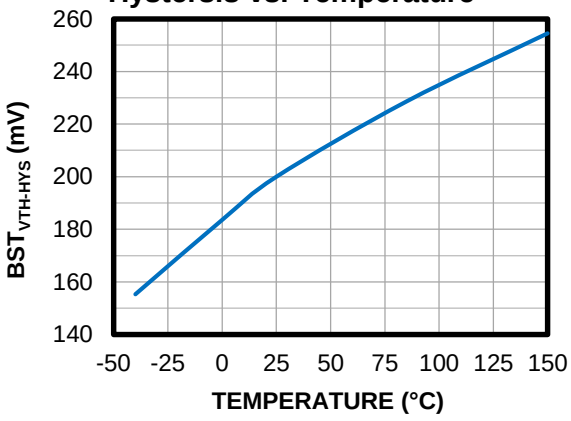


LDO Current Limit vs. Temperature

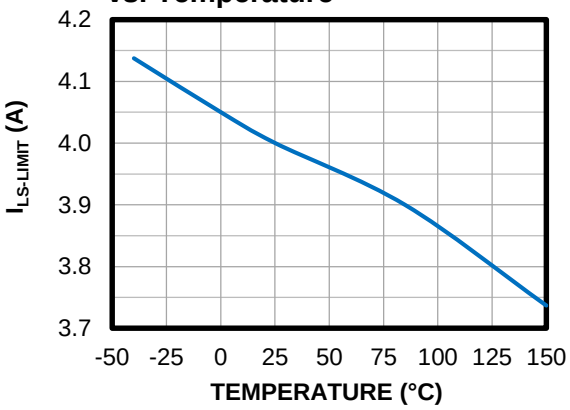
LDO current limit = 500mA



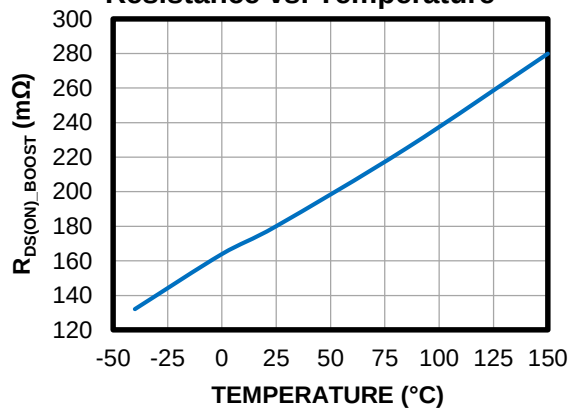
Boost Turn-On Threshold Hystersis vs. Temperature



Low-Side MOSFET Current Limit vs. Temperature

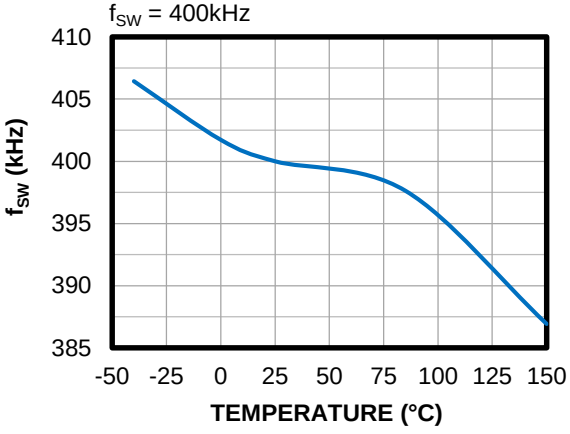


Low-Side MOSFET On Resistance vs. Temperature



Switching Frequency vs. Temperature

f_{SW} = 400kHz

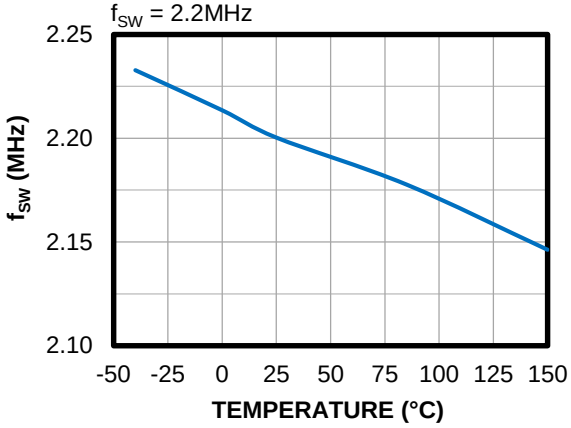


TYPICAL CHARACTERISTICS *(continued)*

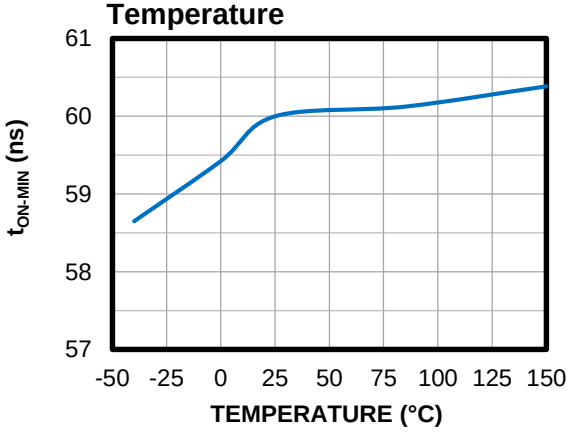
V_{IN} = 13.5V, V_{OUT} = 9V, V_{EN} = 3V, T_J = -40°C to +150°C, unless otherwise noted.

Switching Frequency vs. Temperature

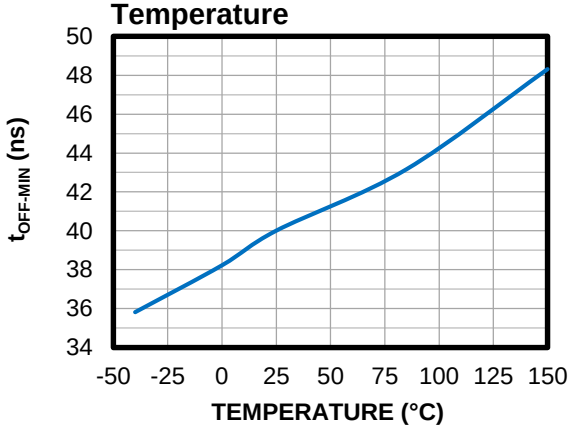
f_{SW} = 2.2MHz



Minimum On Time vs. Temperature

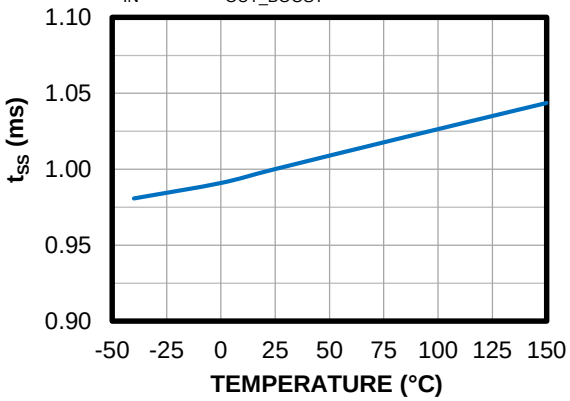


Minimum Off Time vs. Temperature



Boost Soft-Start Time vs. Temperature

V_{IN} = 5V, V_{OUT_BOOST} = 12V

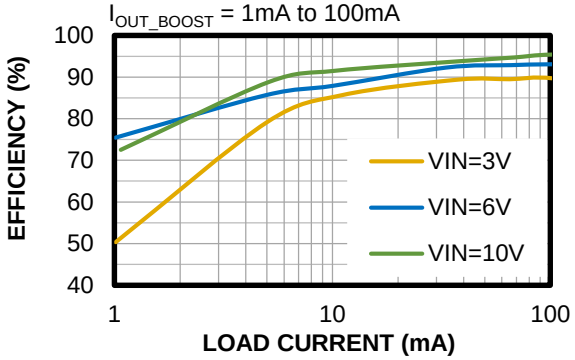


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 6V, V_{OUT} = 9V, V_{OUT_BOOST} = 12V, C_{OUT_BOOST} = 40µF, C_{OUT} = 10µF, V_{EN} = 3V, T_A = 25°C, unless otherwise noted.

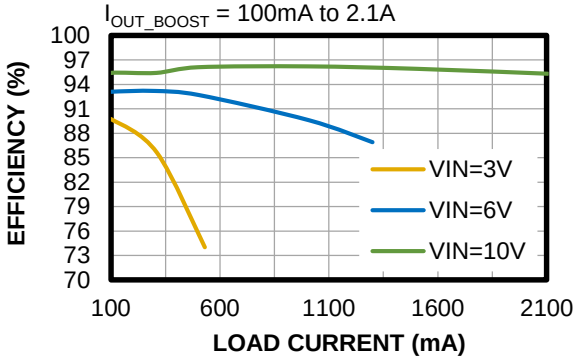
Boost Efficiency vs. Load Current

LDO disabled, V_{OUT_BOOST} = 12V, f_{SW} = 400kHz, L = 10µH (DCR = 45mΩ), B350A-13-F rectifier diode, FSS on, I_{OUT_BOOST} = 1mA to 100mA



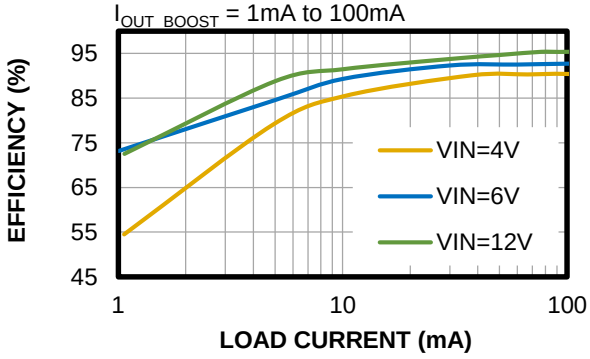
Boost Efficiency vs. Load Current

LDO disabled, V_{OUT_BOOST} = 12V, f_{SW} = 400kHz, L = 10µH (DCR = 45mΩ), B350A-13-F rectifier diode, FSS on, I_{OUT_BOOST} = 100mA to 2.1A



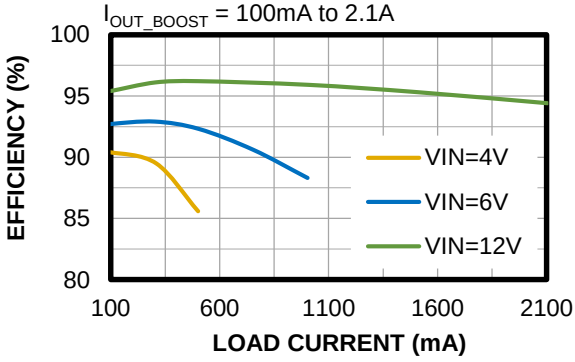
Boost Efficiency vs. Load Current

LDO disabled, V_{OUT_BOOST} = 14V, f_{SW} = 400kHz, L = 10µH (DCR = 45mΩ), B350A-13-F rectifier diode, FSS on, I_{OUT_BOOST} = 1mA to 100mA



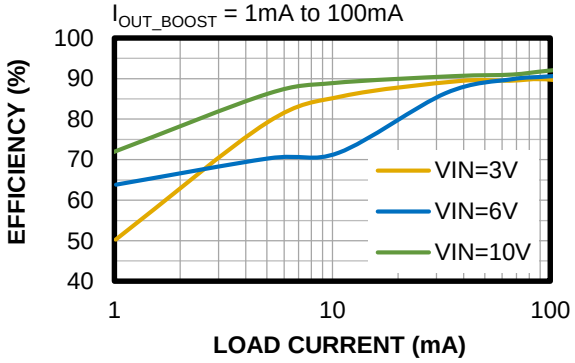
Boost Efficiency vs. Load Current

LDO disabled, V_{OUT_BOOST} = 14V, f_{SW} = 400kHz, L = 10µH (DCR = 45mΩ), B350A-13-F rectifier diode, FSS on, I_{OUT_BOOST} = 100mA to 2.1A



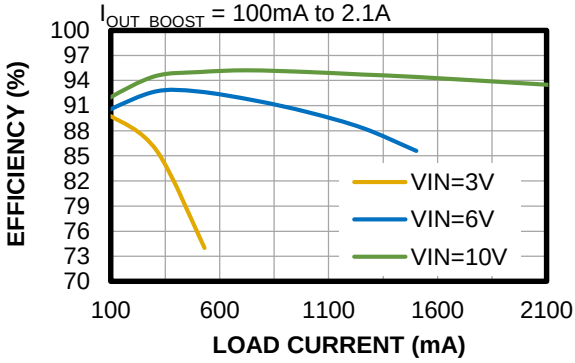
Boost Efficiency vs. Load Current

LDO disabled, V_{OUT_BOOST} = 12V, f_{SW} = 2.2MHz, L = 2.2µH (DCR = 35.2mΩ), B350A-13-F rectifier diode, FSS on, I_{OUT_BOOST} = 1mA to 100mA



Boost Efficiency vs. Load Current

LDO disabled, V_{OUT_BOOST} = 12V, f_{SW} = 2.2MHz, L = 2.2µH (DCR = 35.2mΩ), B350A-13-F rectifier diode, FSS on, I_{OUT_BOOST} = 100mA to 2.1A

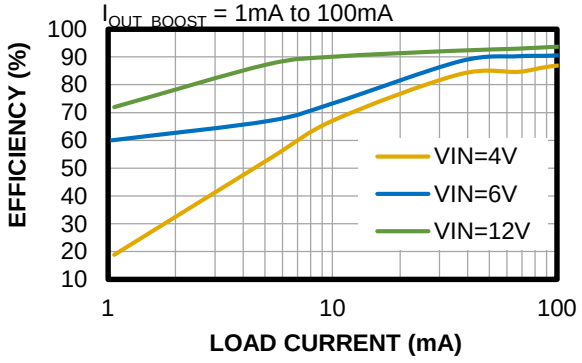


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 6V, V_{OUT} = 9V, V_{OUT_BOOST} = 12V, C_{OUT_BOOST} = 40µF, C_{OUT} = 10µF, V_{EN} = 3V, T_A = 25°C, unless otherwise noted.

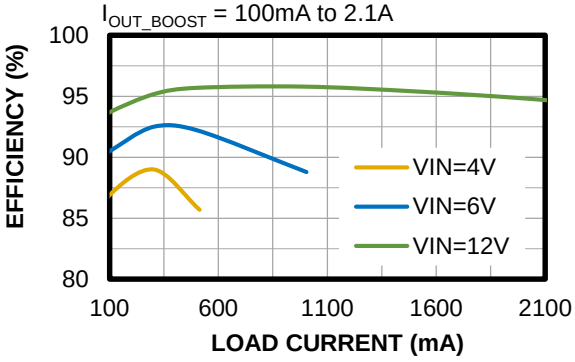
Boost Efficiency vs. Load Current

LDO disabled, V_{OUT_BOOST} = 14V, f_{SW} = 2.2MHz, L = 2.2µH (DCR = 35.2mΩ), B350A-13-F rectifier diode, FSS on, I_{OUT_BOOST} = 1mA to 100mA



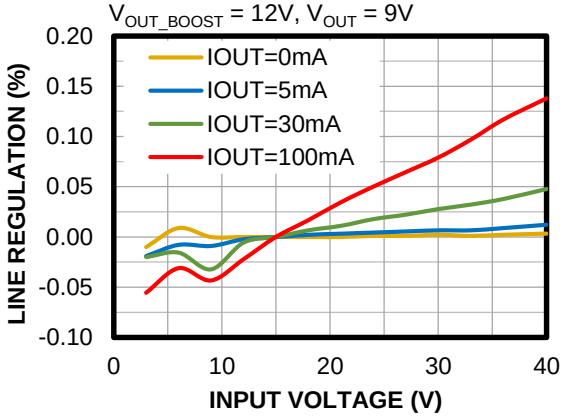
Boost Efficiency vs. Load Current

LDO disabled, V_{OUT_BOOST} = 14V, f_{SW} = 2.2MHz, L = 2.2µH (DCR = 35.2mΩ), B350A-13-F rectifier diode, FSS on, I_{OUT_BOOST} = 100mA to 2.1A



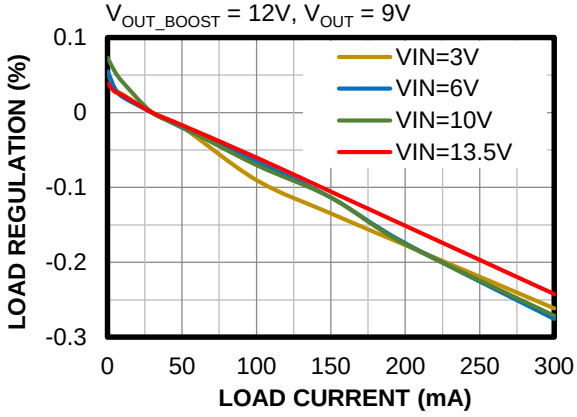
LDO Line Regulation

V_{OUT_BOOST} = 12V, V_{OUT} = 9V



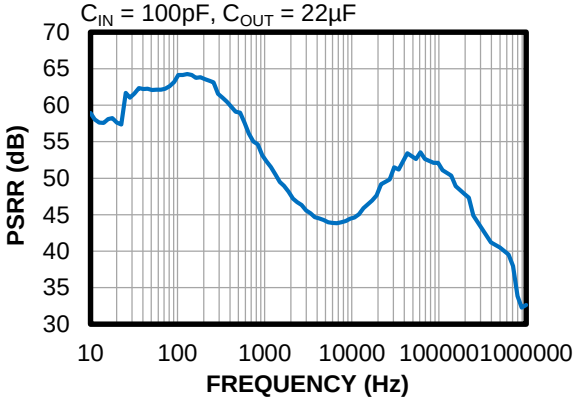
LDO Load Regulation

V_{OUT_BOOST} = 12V, V_{OUT} = 9V



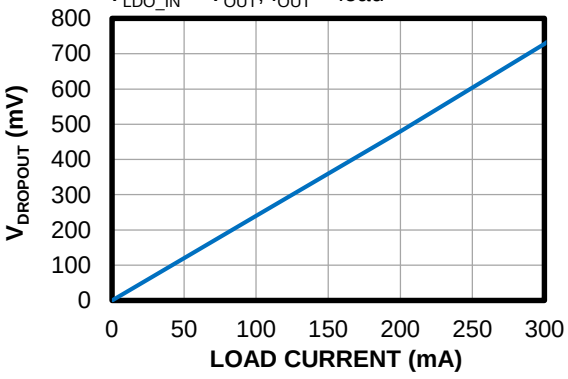
PSRR

V_{IN} = 13.5V, V_{OUT} = 9V, I_{OUT} = 5mA, C_{IN} = 100pF, C_{OUT} = 22µF



Dropout Voltage vs. Load Current

V_{LDO_IN} = V_{OUT}, I_{OUT} = load

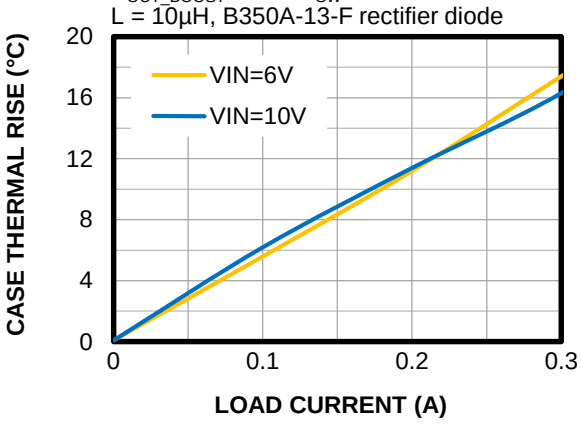


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 6V, V_{OUT} = 9V, V_{OUT_BOOST} = 12V, C_{OUT_BOOST} = 40µF, C_{OUT} = 10µF, V_{EN} = 3V, T_A = 25°C, unless otherwise noted.

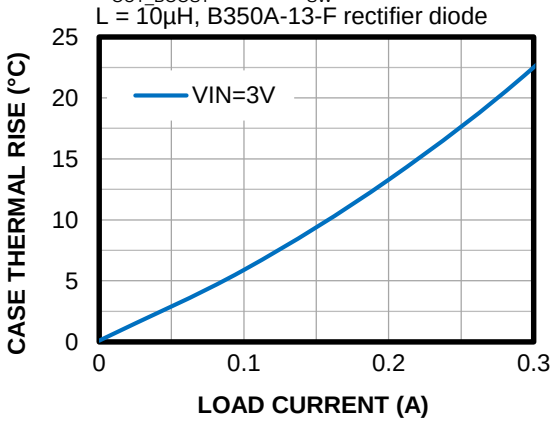
Case Thermal Rise

V_{OUT} = 9V, I_{OUT} = load,
V_{OUT_BOOST} = 12V, f_{SW} = 400kHz,
L = 10µH, B350A-13-F rectifier diode



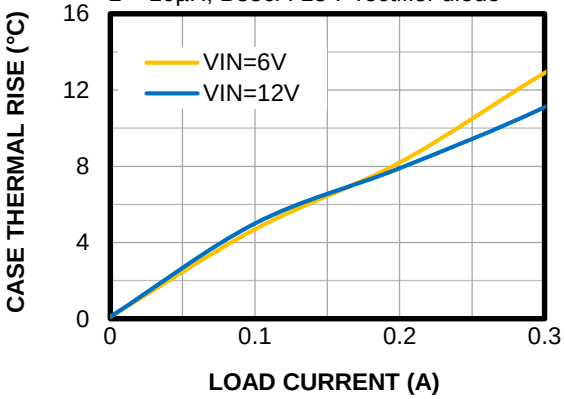
Case Thermal Rise

V_{OUT} = 5V, I_{OUT} = load,
V_{OUT_BOOST} = 6.5V, f_{SW} = 400kHz,
L = 10µH, B350A-13-F rectifier diode



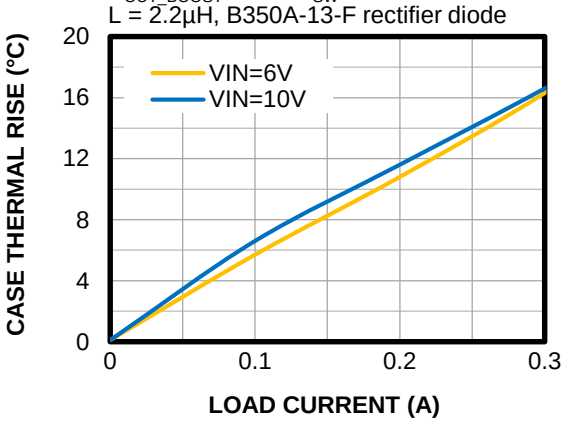
Case Thermal Rise

V_{OUT} = 12V, I_{OUT} = load,
V_{OUT_BOOST} = 14V, f_{SW} = 400kHz,
L = 10µH, B350A-13-F rectifier diode



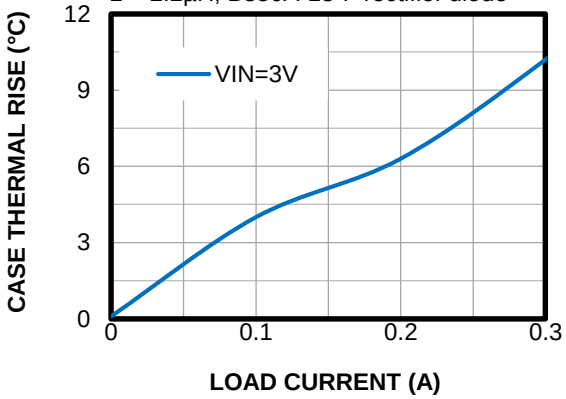
Case Thermal Rise

V_{OUT} = 9V, I_{OUT} = load,
V_{OUT_BOOST} = 12V, f_{SW} = 2.2MHz,
L = 2.2µH, B350A-13-F rectifier diode



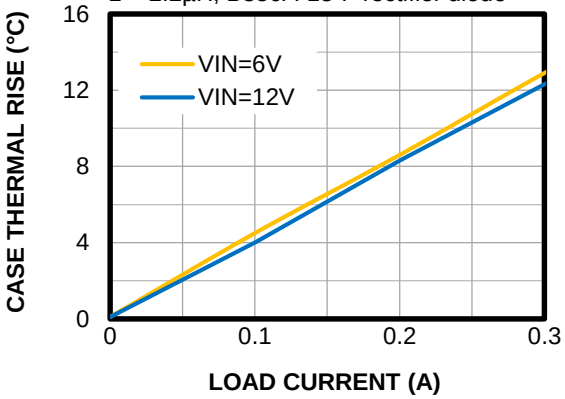
Case Thermal Rise

V_{OUT} = 5V, I_{OUT} = load,
V_{OUT_BOOST} = 6.5V, f_{SW} = 2.2MHz,
L = 2.2µH, B350A-13-F rectifier diode



Case Thermal Rise

V_{OUT} = 12V, I_{OUT} = load,
V_{OUT_BOOST} = 14V, f_{SW} = 2.2MHz,
L = 2.2µH, B350A-13-F rectifier diode

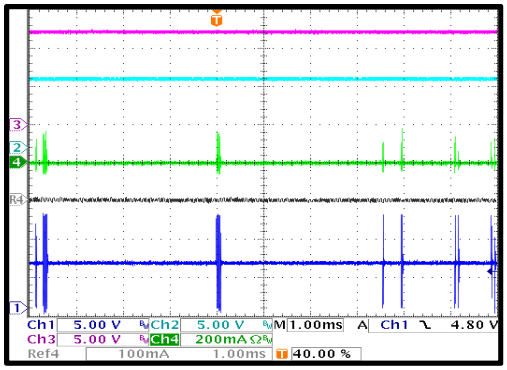


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 6V, V_{OUT} = 9V, V_{OUT_BOOST} = 12V, C_{OUT_BOOST} = 40µF, C_{OUT} = 10µF, V_{EN} = 3V, B350A-13-F rectifier diode, T_A = 25°C, unless otherwise noted.

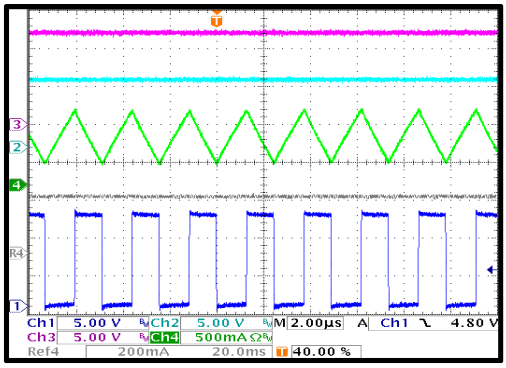
Steady State
I_{OUT} = 0A

CH3: V_{OUT_BOOST}
CH2: V_{OUT}
CH4: I_L
R4: I_{OUT} 100mA/div.
CH1: V_{SW}



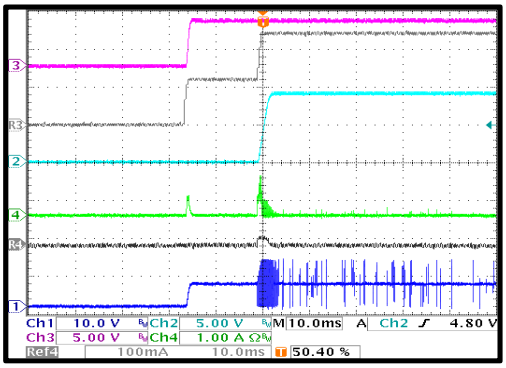
Steady State
I_{OUT} = 0.3A

CH3: V_{OUT_BOOST}
CH2: V_{OUT}
CH4: I_L
R4: I_{OUT} 200mA/div.
CH1: V_{SW}



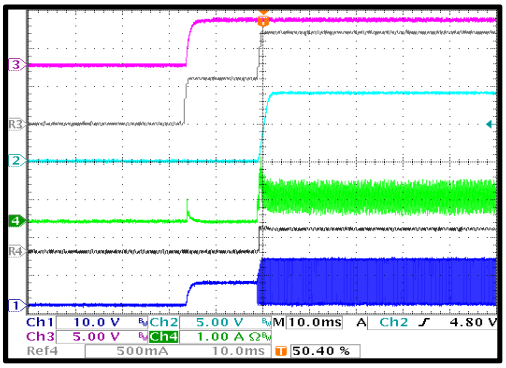
Start-Up through VIN
I_{OUT} = 0A

CH3: V_{IN}
R3: V_{OUT_BOOST} 5V/div.
CH2: V_{OUT}
CH4: I_L
R4: I_{OUT} 100mA/div.
CH1: V_{SW}



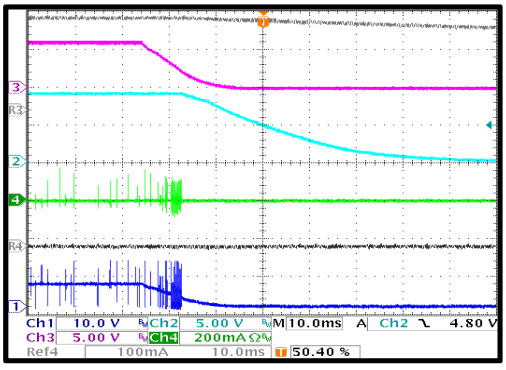
Start-Up through VIN
I_{OUT} = 0.3A

CH3: V_{IN}
R3: V_{OUT_BOOST} 5V/div.
CH2: V_{OUT}
CH4: I_L
R4: I_{OUT} 500mA/div.
CH1: V_{SW}



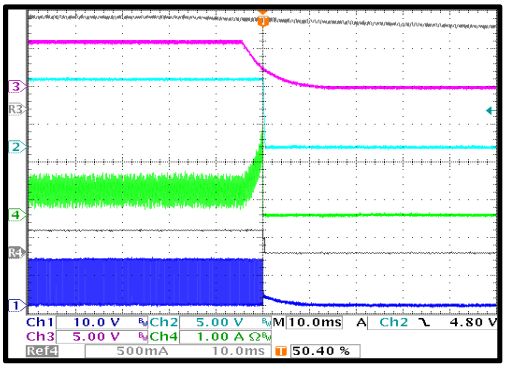
Shutdown through VIN
I_{OUT} = 0A

CH3: V_{IN}
R3: V_{OUT_BOOST} 5V/div.
CH2: V_{OUT}
CH4: I_L
R4: I_{OUT} 100mA/div.
CH1: V_{SW}



Shutdown through VIN
I_{OUT} = 0.3A

CH3: V_{IN}
R3: V_{OUT_BOOST} 5V/div.
CH2: V_{OUT}
CH4: I_L
R4: I_{OUT} 500mA/div.
CH1: V_{SW}

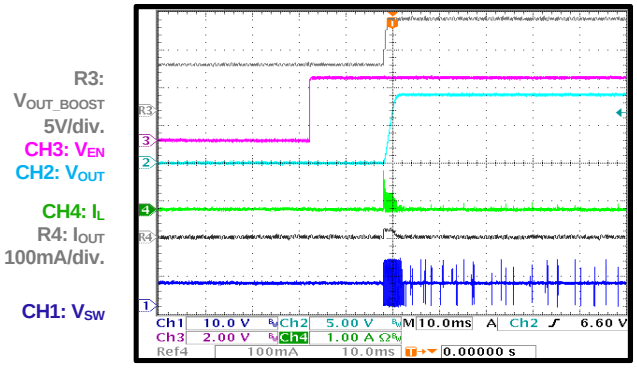


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 6V, V_{OUT} = 9V, V_{OUT_BOOST} = 12V, C_{OUT_BOOST} = 40µF, C_{OUT} = 10µF, V_{EN} = 3V, B350A-13-F rectifier diode, T_A = 25°C, unless otherwise noted.

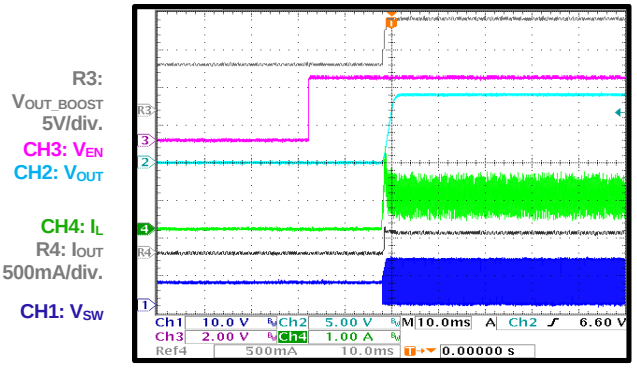
Start-Up through EN

I_{OUT} = 0A



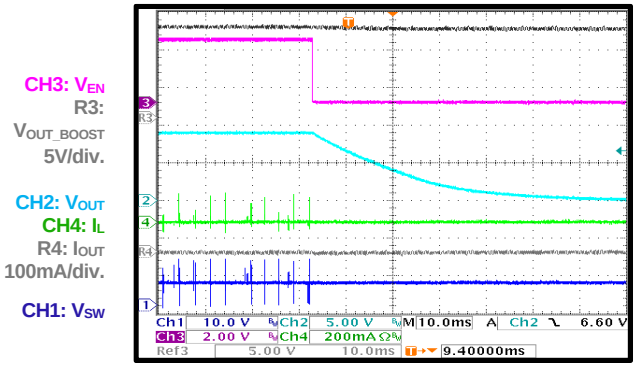
Start-Up through EN

I_{OUT} = 0.3A



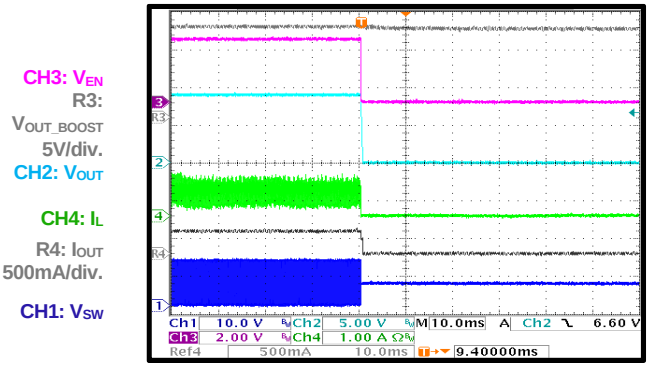
Shutdown through EN

I_{OUT} = 0A



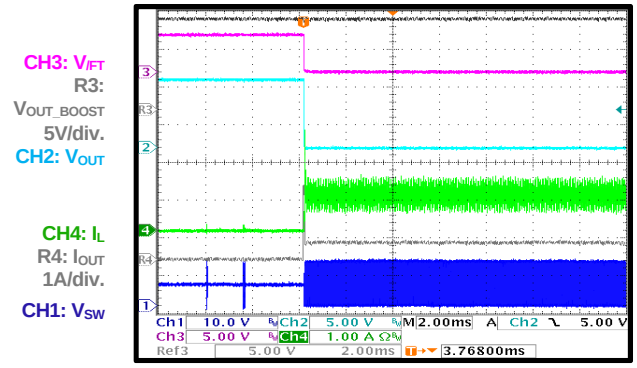
Shutdown through EN

I_{OUT} = 0.3A



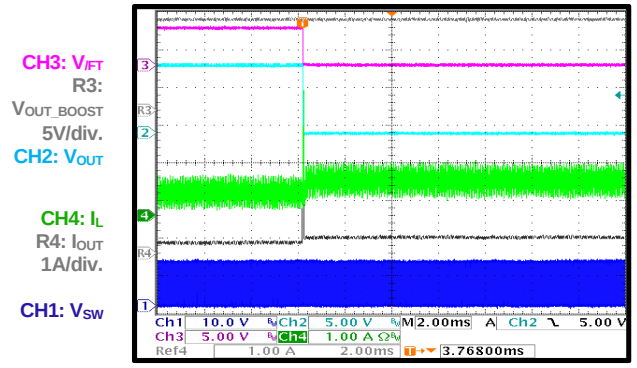
SCP Entry

I_{OUT} = 0A short to circuit



SCP Entry

I_{OUT} = 0.3A short to circuit



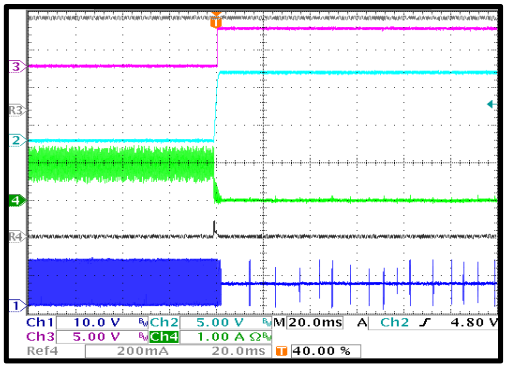
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 6V, V_{OUT} = 9V, V_{OUT_BOOST} = 12V, C_{OUT_BOOST} = 40µF, C_{OUT} = 10µF, V_{EN} = 3V, B350A-13-F rectifier diode, T_A = 25°C, unless otherwise noted.

SCP Recovery

short circuit to I_{OUT} = 0A

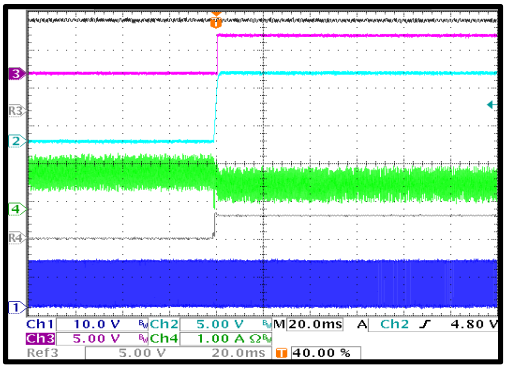
CH3: V_{IFT}
R3: V_{OUT_BOOST} 5V/div.
CH2: V_{OUT}
CH4: I_L
R4: I_{OUT} 200mA/div.
CH1: V_{SW}



SCP Recovery

short circuit to I_{OUT} = 0.3A

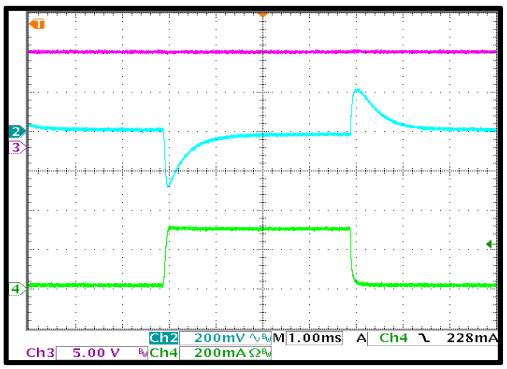
CH3: V_{IFT}
R3: V_{OUT_BOOST} 5V/div.
CH2: V_{OUT}
CH4: I_L
R4: I_{OUT} 500mA/div.
CH1: V_{SW}



Load Transient

I_{OUT} = 10mA to 300mA, 1.6A/µs

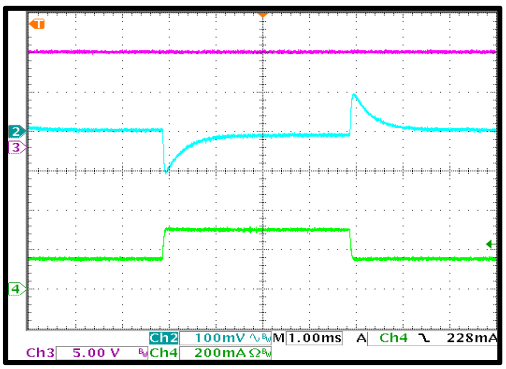
CH2: V_{OUT}/AC
CH3: V_{OUT_BOOST}
CH4: I_{OUT}



Load Transient

I_{OUT} = 150mA to 300mA, 1.6A/µs

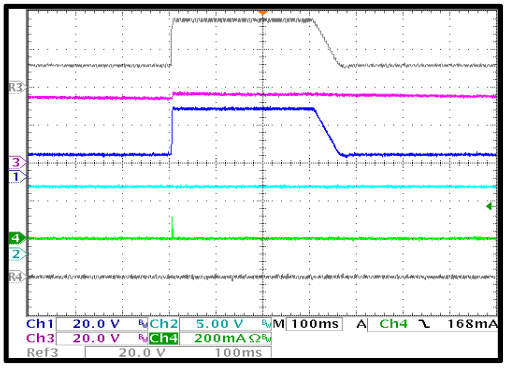
CH2: V_{OUT}/AC
CH3: V_{OUT_BOOST}
CH4: I_{OUT}



Load Dump

I_{OUT} = 0A

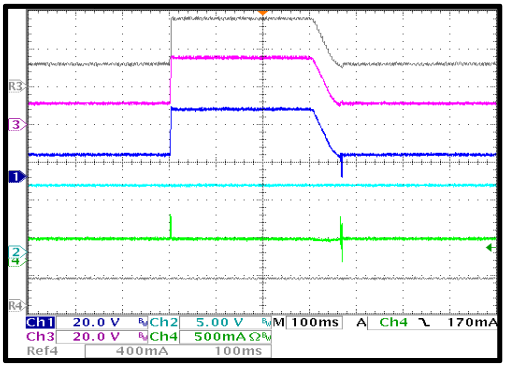
R3: V_{IN} 20V/div.
CH3: V_{OUT_BOOST}
CH1: V_{SW}
CH4: I_L
CH2: V_{OUT}
R4: I_{OUT} 100mA/div.



Load Dump

I_{OUT} = 0.3A

R3: V_{IN} 20V/div.
CH3: V_{OUT_BOOST}
CH1: V_{SW}
CH2: V_{OUT}
CH4: I_L
R4: I_{OUT} 400mA/div.

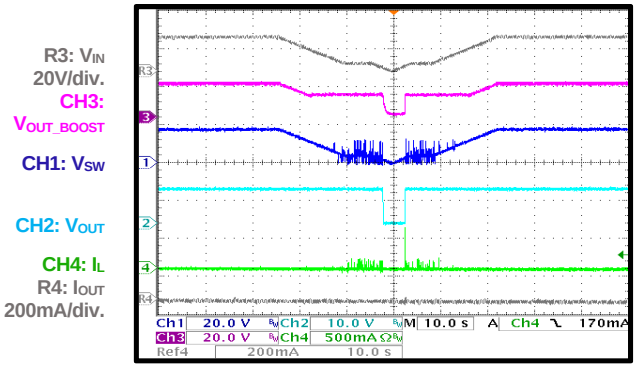


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 6V, V_{OUT} = 9V, V_{OUT_BOOST} = 12V, C_{OUT_BOOST} = 40µF, C_{OUT} = 10µF, V_{EN} = 3V, B350A-13-F rectifier diode, T_A = 25°C, unless otherwise noted.

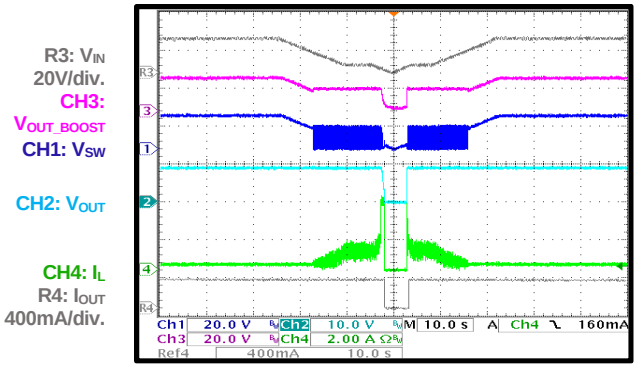
V_{IN} Ramping Down and Up

I_{OUT} = 0A



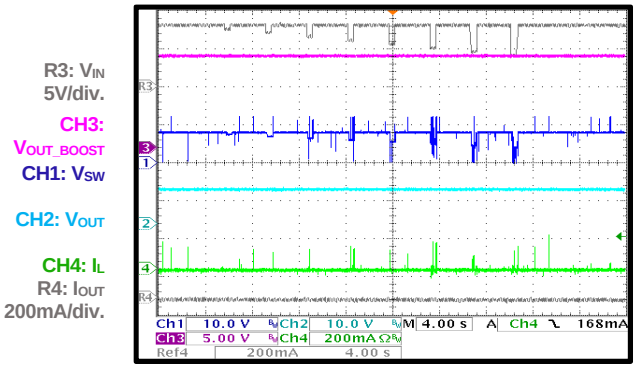
V_{IN} Ramping Down and Up

I_{OUT} = 0.3A



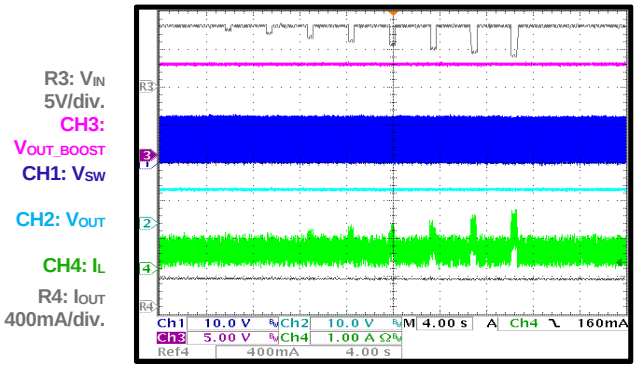
Reset Behavior

I_{OUT} = 0A



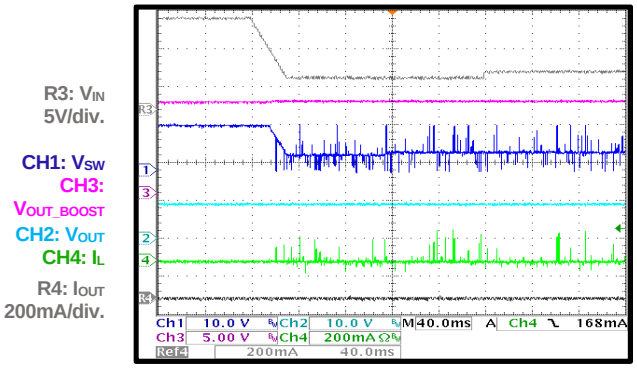
Reset Behavior

I_{OUT} = 0.3A



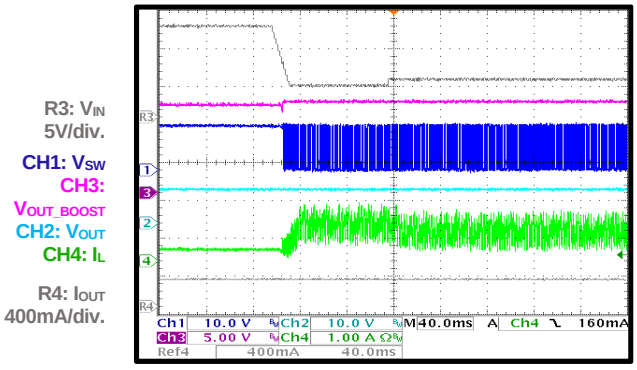
Cold Crank

I_{OUT} = 0A



Cold Crank

I_{OUT} = 0.3A

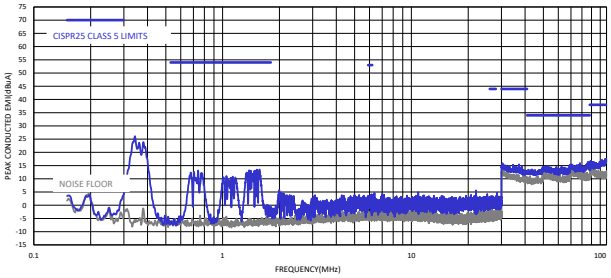


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 6V, V_{OUT} = 9V, V_{OUT_BOOST} = 12V, I_{OUT} = 0.3A, f_{SW} = 400kHz, L = 10µH, C_{OUT_BOOST} = 40µF, C_{OUT} = 10µF, V_{EN} = 3V, DFLS240-7 rectifier diode, with EMI filters and FSS enabled, T_A = 25°C, unless otherwise noted. (8)

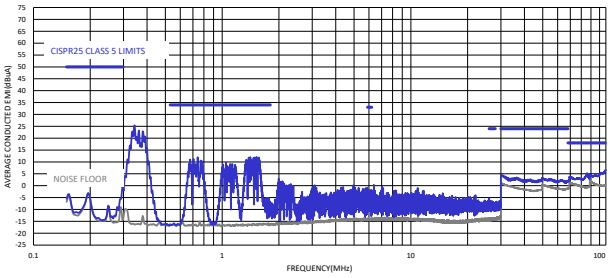
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



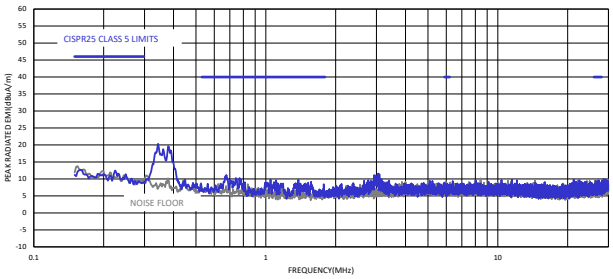
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



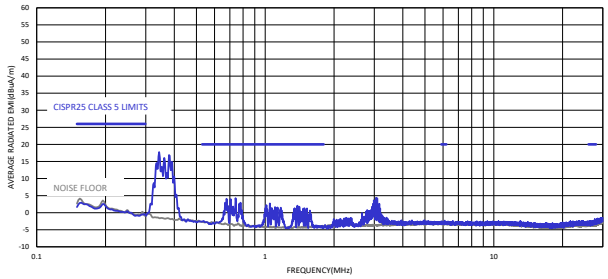
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



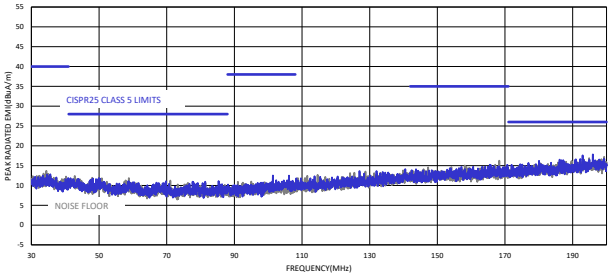
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



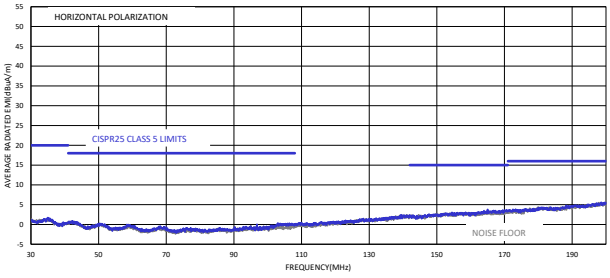
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 200MHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 200MHz

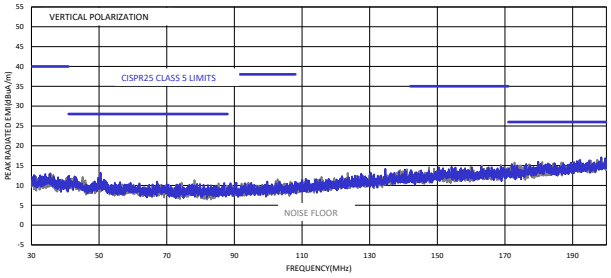


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 6V, V_{OUT} = 9V, V_{OUT_BOOST} = 12V, I_{OUT} = 0.3A, f_{SW} = 400kHz, L = 10µH, C_{OUT_BOOST} = 40µF, C_{OUT} = 10µF, V_{EN} = 3V, DFLS240-7 rectifier diode, with EMI filters and FSS enabled, T_A = 25°C, unless otherwise noted. (8)

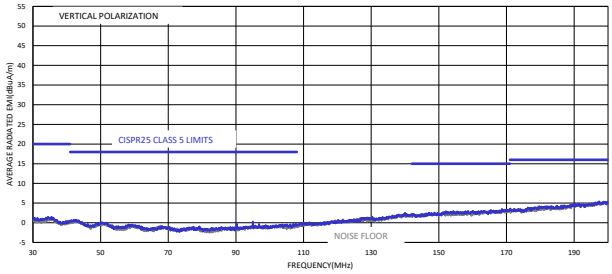
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 200MHz



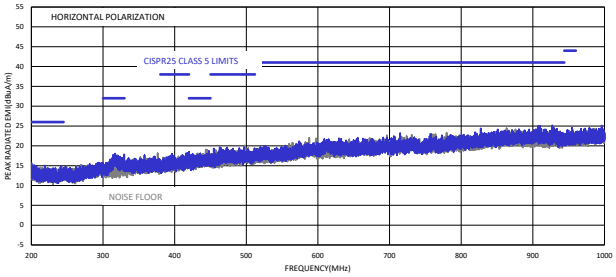
CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 200MHz



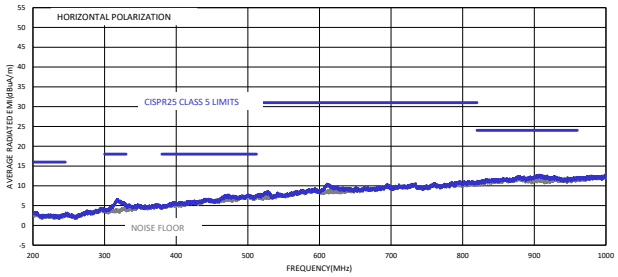
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 200MHz to 1GHz



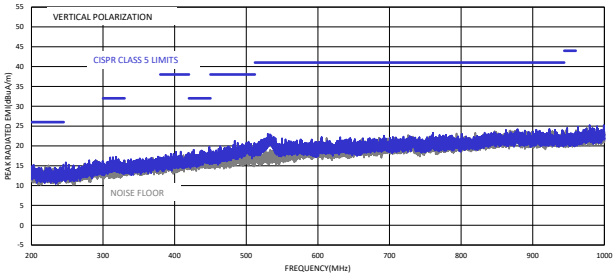
CISPR25 Class 5 Average Radiated Emissions

Horizontal, 200MHz to 1GHz



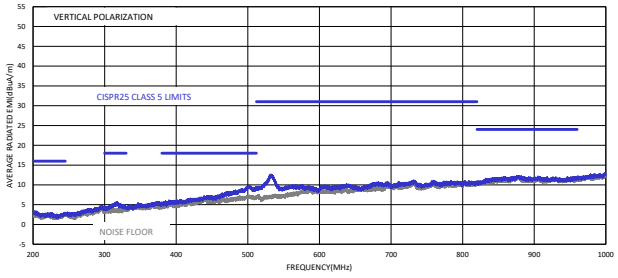
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 200MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 200MHz to 1GHz



Note:

8) All EMC test results are based on the typical application circuit with EMI filters (see Figure 17 on page 48).

FUNCTIONAL BLOCK DIAGRAM

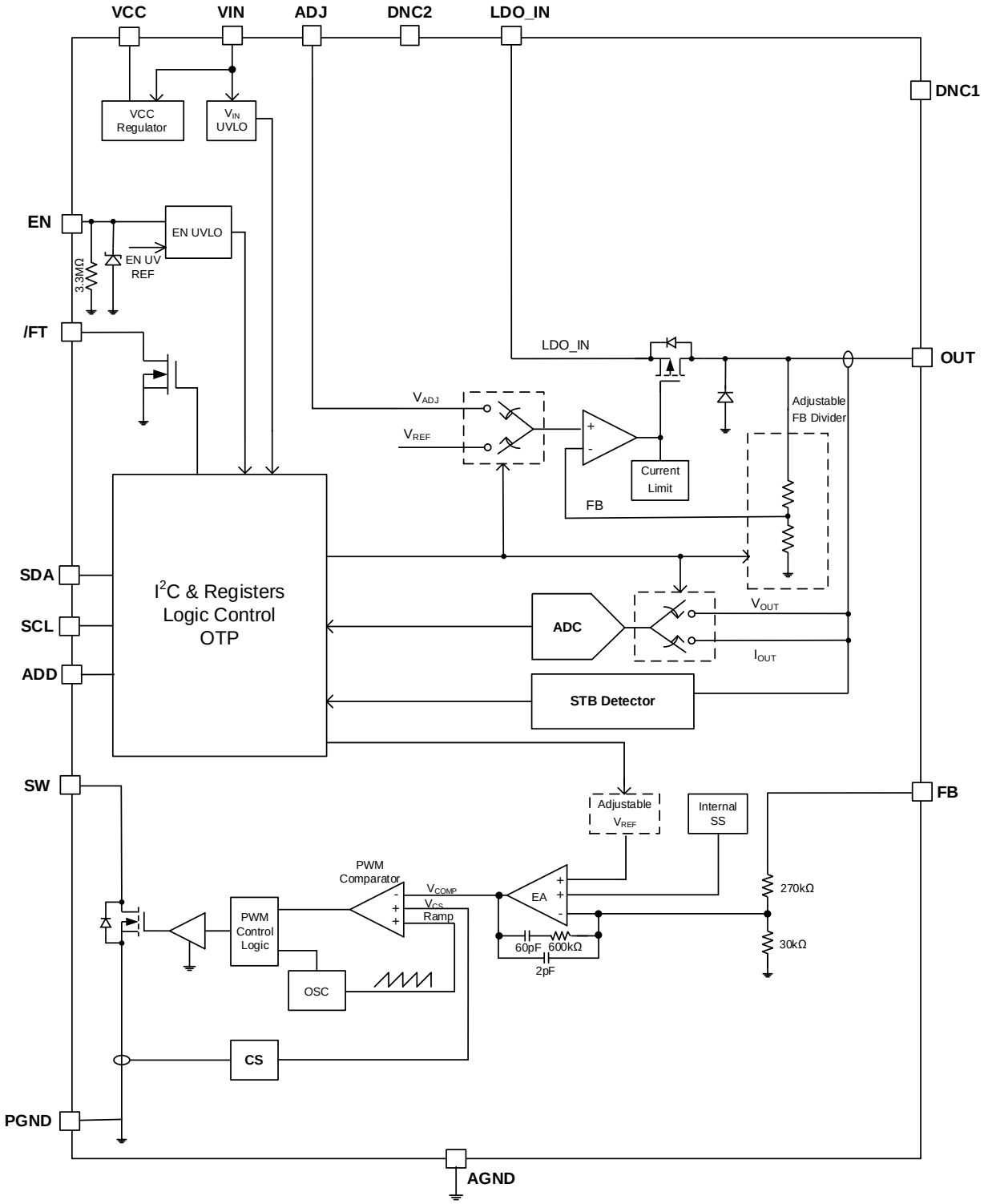


Figure 2: Functional Block Diagram

TIMING SEQUENCE

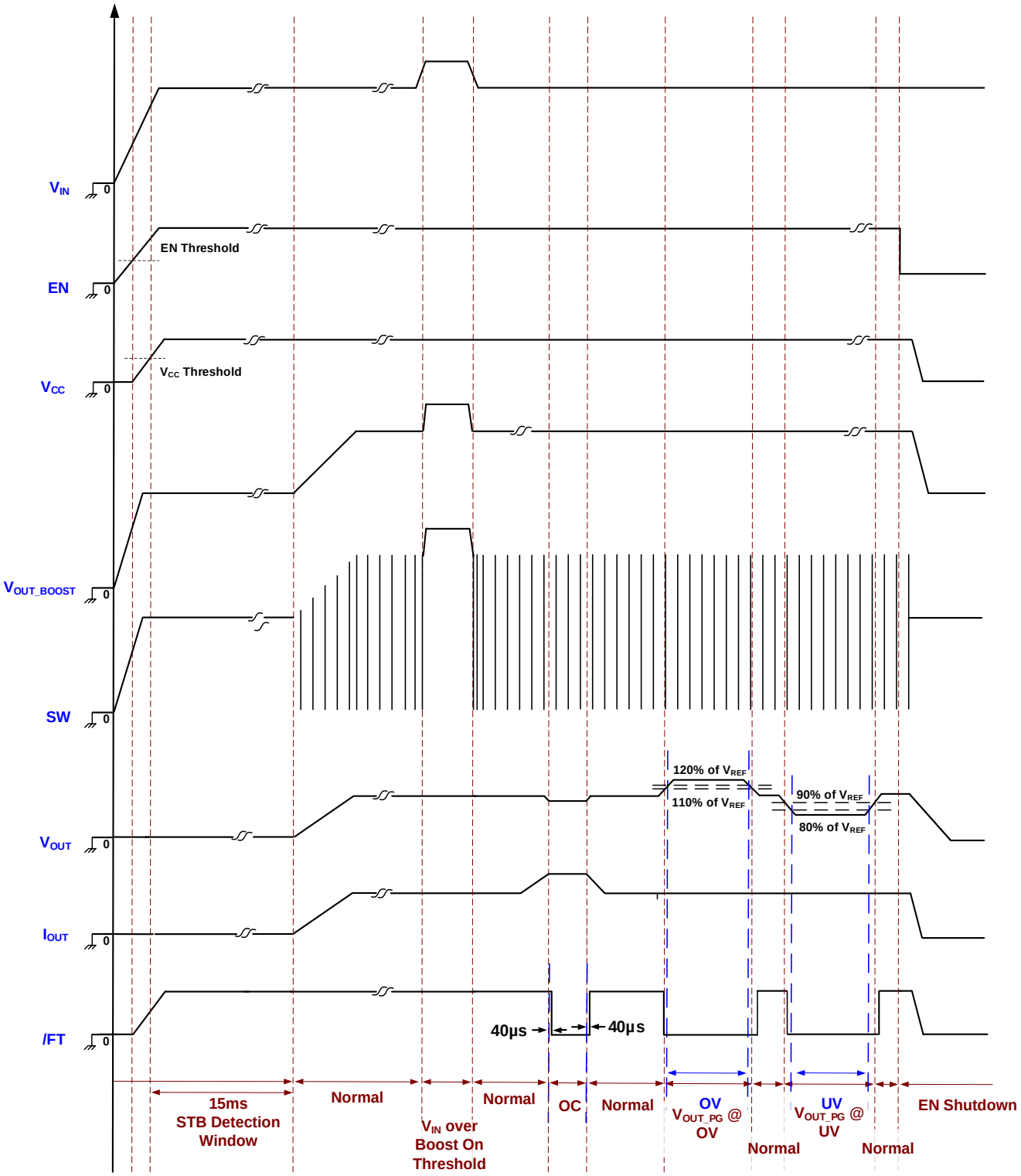


Figure 3: Timing Sequence

TIMING SEQUENCE *(continued)*

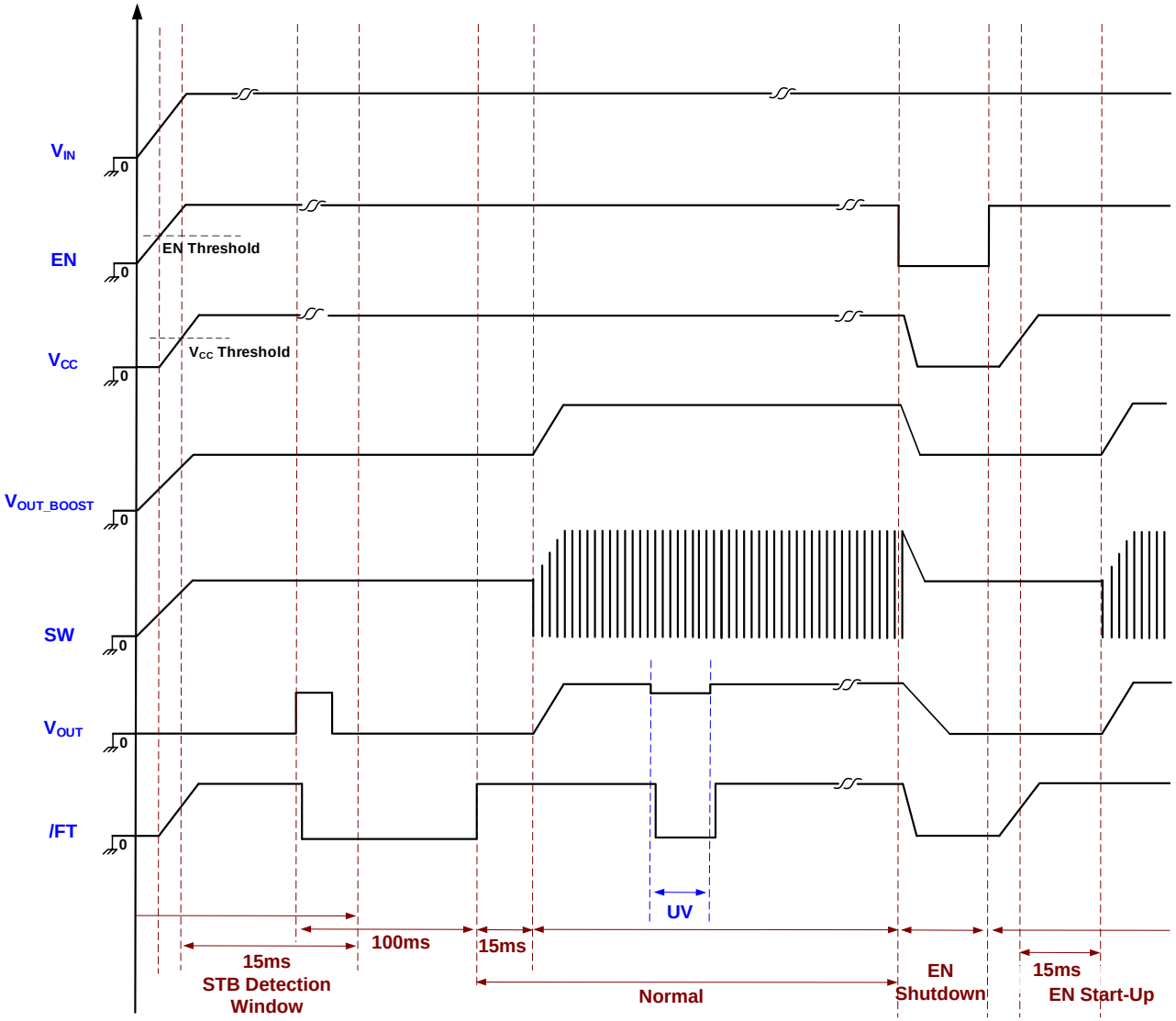


Figure 4: STB Occurs within the STB Detection Window and out of the STB Detection Window

TIMING SEQUENCE *(continued)*

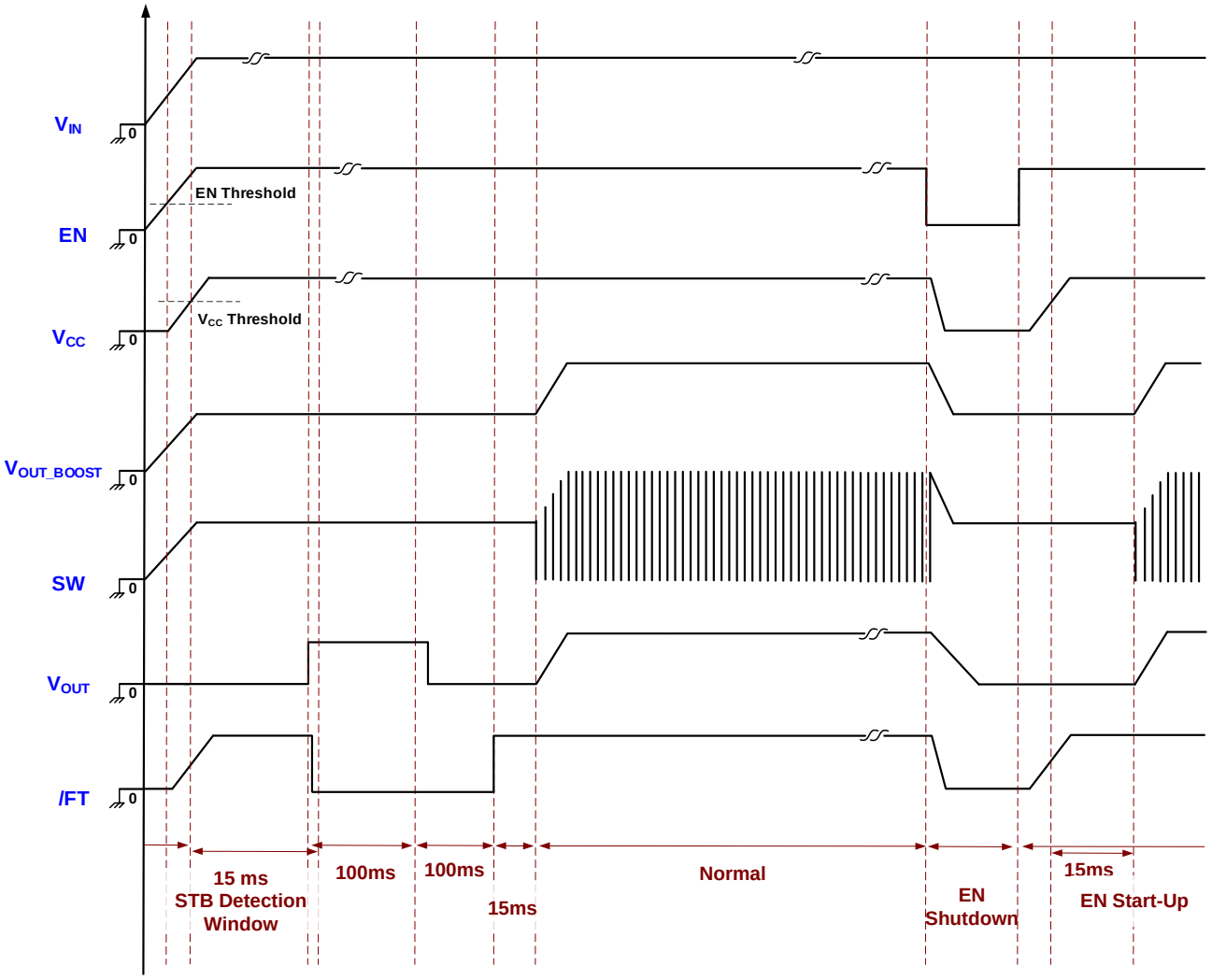


Figure 5: STB Occurs with Hiccup Protection

TIMING SEQUENCE *(continued)*

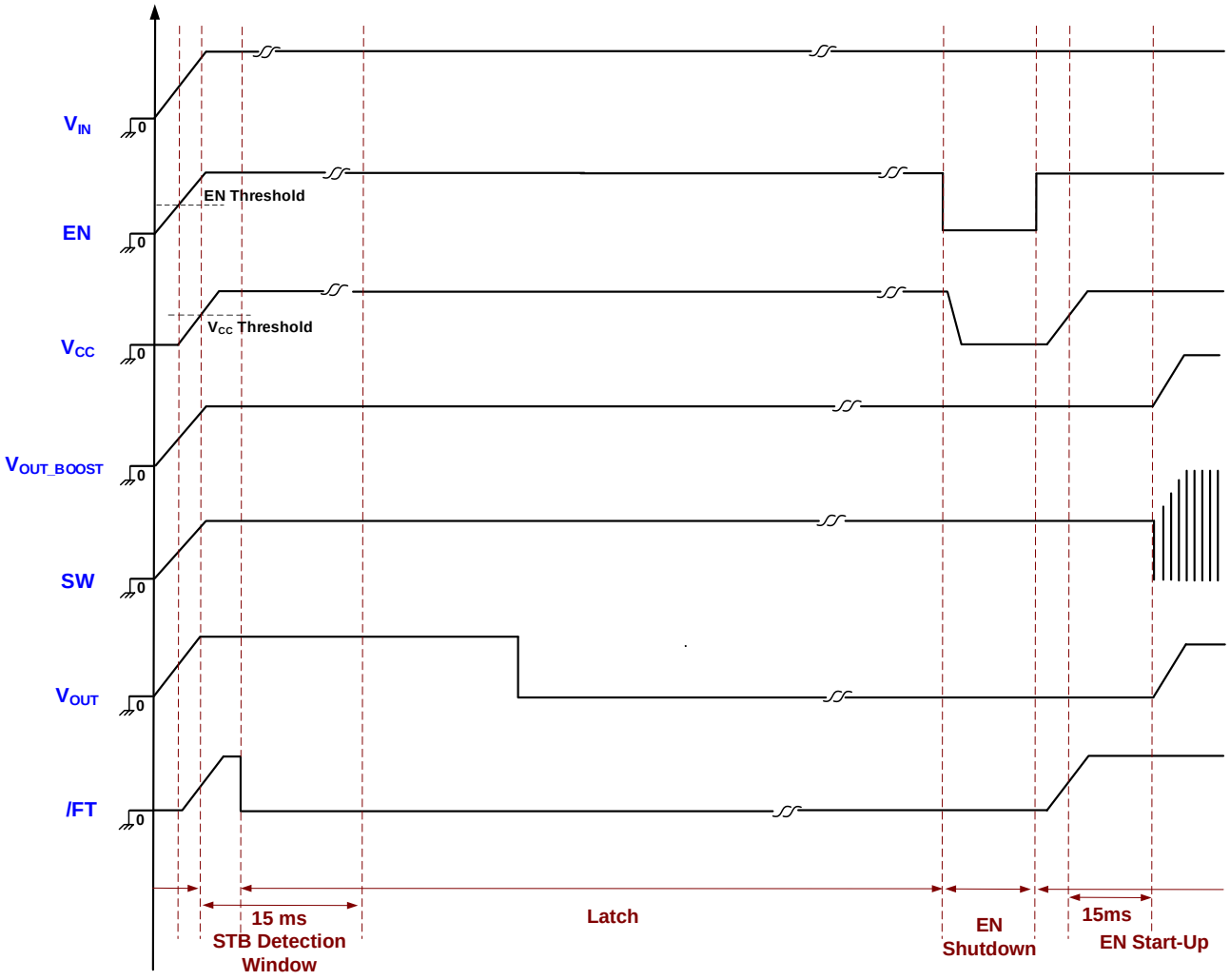


Figure 6: STB Occurs with Latch Protection

OPERATION

The MPQ2024A is a phantom antenna linear regulator with pre-boost regulator and I²C interface. It supplies power to systems with high-voltage batteries. The device features a wide 3V to 40V input voltage (V_{IN}) range, low dropout voltage ($V_{DROPOUT}$), and a low quiescent supply current (I_Q).

The MPQ2024A's power stage is implemented as a cascade, starting with a step-up pre-boost regulator, followed by an LDO. The step-up regulator (a DC/DC boost converter) provides the LDO input voltage level, which enables the LDO to regulate the output during cold-crank conditions.

The LDO output is adjustable via the I²C interface, from 1V to 13.6V with 200m/step, or from 1V to 7.3V with 100mV/step.

The regulator output current is limited internally, and the device is protected against short-circuit, overload, and over-temperature conditions.

The LDO peak output current limitation range can be configured to be between 100mA and 500mA via the I²C interface.

If the junction temperature (T_J) is too high, the thermal sensor sends a signal to the control logic that shuts down the device. Once the temperature has sufficiently cooled, the IC restarts.

The maximum power output current is a function of the package's maximum power dissipation for a given temperature. The maximum power dissipation is dependent on the thermal resistance of the case and the circuit board, the temperature difference between the die junction and the ambient air, and the rate of airflow. GND and the exposed pad must be connected to the ground plane for proper dissipation.

Pre-Boost Regulator

The boost converter is intended to function as a pre-boost regulator, and provides a step-up converter function. After the reverse protection circuit, the converter transfers energy from the battery voltage to a higher output voltage (LDO_IN) with high efficiency. The regulator integrates power switching and a sense resistor for over-current (OC) detection.

The pre-boost regulator parameters can be set via I²C interface. The threshold at which it activates can be selected via the dedicated register. The corresponding pre-boost regulator output voltage (V_{OUT_BOOST}) is also set via a register. If the pre-boost regulator is enabled, its switches automatically start to switch when V_{IN} falls below the selected threshold voltage. They stop switching when they cross this threshold (including a hysteresis) again. A bit in the I²C register indicates whether the pre-boost regulator has been activated. The over-current (OC), under-voltage (UV), and over-voltage (OV) functions stop working when V_{IN} exceeds its boost active threshold.

The normal runtime power for the LDO is provided directly from the battery input, not from the pre-boost regulator. The regulator is only activated in case of cranking, or other scenarios in which the battery input dips to a voltage below the boost active voltage threshold.

The pre-boost regulator works in pulse-width modulation (PWM) mode and peak current control mode, with a fixed frequency of 400kHz or 2.2MHz. This frequency can be selected via the I²C interface.

The pre-boost regulator's power switching has a minimum turn-on time of 60ns, which means that power switching remains in the on state for at least 60ns once it turns on. To prevent V_{OUT_BOOST} from overshooting at the 2.2MHz frequency, a frequency foldback block is activated to reduce the frequency when V_{IN} is close to V_{OUT_BOOST}. The frequency folds back to 1MHz when $5/6 < V_{IN} / V_{OUT\_BOOST} < 10/11$, and to 500kHz when $V_{IN} / V_{OUT\_BOOST} > 10/11$.

Fault Indicator and Diagnostics

The device provides full diagnostics for different fault conditions. The MPQ2024A monitors the LDO's load current through an internal sense resistor to protect against OC and short-circuit (SC) conditions. In addition, the device also detects output OV and UV conditions, and it features LDO output pin short-to-battery protection and thermal shutdown.

The /FT pin pulls high during normal operation. Any fault or warning pulls this pin down to indicate a fault status (see Table 1 on page 29).

The /FT pin is the open drain of a MOSFET. It should be connected to a ≤5V voltage source through a resistor (e.g. 100kΩ).

The MPQ2024A also has dedicated register bits that serve as fault flags and indicate the device's status for system diagnostics. See the Register Map on page 35 for more details.

Table 1: Fault Indicator

Fault	Register Fault Flag	/FT Indication	Fault Actions
Thermal	Yes	Yes	If register 0x04, bit[0] = 0b: latch-off mode If register 0x04, bit[0] = 1b: hiccup mode
Short to battery	Yes	Yes	If register 0x04, bit[0] = 0b: latch-off mode If register 0x04, bit[0] = 1b: hiccup mode
LDO over-current (OC)	Yes	Yes	No action. The chip continues operating until thermal shutdown occurs.
LDO over-voltage (OV)	Yes	Yes	No action. The chip continues operating with the OV status.
LDO under-voltage (UV)	Yes	Yes	No action. The chip continues operating with the UV status until thermal shutdown occurs.
LDO open-load (OL)	Yes	Yes	No action. The chip continues operating with the OL status until thermal shutdown occurs.
Boost OC	Yes	Yes	No action. The chip continues operating with the OC status.
Boost OV	Yes	Yes	No action. The chip continues operating in the OV status.
Boost UV	Yes	Yes	No action. The chip continues operating in the UV status.

Fault Handling

After a short-to-battery or thermal shutdown fault occurs, the device operates based on the corresponding fault mode set via register 0x04, bit[0]. There are two operating schemes: hiccup mode and latch-off mode.

In hiccup mode, the chip attempts to restart the converter. After the converter completely shuts down, a fault recovery timer starts. After a 100ms delay time, the converter attempts to soft start (SS) automatically. If the fault condition is not removed, the converter reinitiates the fault protection and repeats the auto-recovery process in hiccup mode. If the fault condition is removed once SS ends and the converter operates normally for a consecutive 80µs, then the fault status resets.

Latch-off mode stops the converter until the power is cycled on the input supply or EN. The part restarts in normal mode after the 15ms blanking time specified in register 0x0F, bits D[7:6].

Short-Circuit (SC) and Over-Current (OC) Conditions

The LDO channel's current limit is configured via the I^2C interface to protect the device during short-circuit (SC) to GND or over-current (OC) conditions. When the LDO output current (I_{OUT}) reaches its internal threshold, I_{OUT} is limited and a dedicated bit in the register is set to indicate the fault. The /FT pin asserts low, but the output is not disabled. The /FT pin and the status of the internal register diagnostic bits should be monitored by the external microcontroller (MCU), and the channel experiencing the SC or OC condition should be disabled by the MCU by setting the dedicated register bits via the I^2C interface. If a severe condition occurs, the MCU can shut down the MPQ2024A by pulling the EN pin low. If this condition persists, thermal shutdown can occur, at which point both outputs are disabled.

Short-to-Battery (STB) Detection

It is possible to short the LDO output pin to the battery due to a system fault. The LDO channel can detect this failure by comparing the corresponding voltage at the OUT and VIN pins before the device's internal switches turn on. An adjustable blanking time asserts each time the device is enabled when both VIN and EN exceed their rising threshold, or the device recovers from thermal shutdown or hiccup mode. Short-to-battery detection occurs during this adjustable blanking time.

If the device detects a short-to-battery fault, both the boost regulator's and LDO's switches latch off or enter hiccup mode (based on register 0x04, bit D[0]), the /FT pin asserts low, and the dedicated bits in the register are set to indicate the fault channel. After the short-to-battery fault is removed, the device can recover to normal operation automatically if hiccup mode is selected. If latch-off mode is selected, cycle the power on VIN or EN to reset VCC and restart the device. If the short-to-battery condition occurs outside of the blanking time, the short-to-battery function does not work.

The blanking time is adjustable from 1ms to 15ms, based on the setting of register 0x0F, bits D[7:6]. 15ms is the default value.

Thermal Shutdown

Thermal shutdown circuitry protects the device from overheating. Typically, the switch turns off immediately when T_J exceeds 170°C. The switch turns on again after the device temperature drops by about 20°C (typical).

Integrated Inductive Clamp

During output shutdown, the cable inductance continues to source the current from the device output. The device integrates an inductive clamp to help dissipate the inductive energy stored in the cable. An internal diode is connected between the OUT and GND pins, with a DC current capability of 300mA for inductive clamp protection. Add an additional diode for higher currents.

Input Under-Voltage Lockout (UVLO)

V_{IN} has an internally fixed UVLO threshold. When the voltage on the VIN pin drops below its falling threshold, UVLO activates. This threshold is 2V when the pre-boost regulator is enabled, and is 3.8V when the regulator is disabled. UVLO ensures that the regulator is not latched to an unknown state when the input supply voltage is low. If V_{IN} has a negative transient that drops below the UVLO threshold and then recovers, the regulator shuts down then starts up with a normal start-up sequence when V_{IN} exceeds the UVLO rising threshold. This threshold is 2.8V when the pre-boost regulator is enabled, and 4.2V when the regulator is disabled.

Enable (EN)

The EN pin can be used to enable and disable the entire device. Pull EN below its falling threshold (2.2V) to shut down the chip. Pull EN above its rising threshold (2.4V) to enable the chip.

There are separate, dedicated register bits to enable the software for the pre-boost regulator and LDO. The physical EN pin has a higher priority than the software enable function.

VCC Regulator

During normal operation, an internal low-dropout (LDO) regulator outputs a nominal 5V VCC supply from VIN. This supplies power to all control blocks and the I^2C block. Add a 1µF to 10µF, low-ESR ceramic capacitor to act as the bypass capacitor from VCC to GND.

The VCC supply cannot maintain a 5V output once V_{IN} drops below 5V. If the pre-boost regulator is enabled, its output takes over the VCC supply from FB.

VCC has an internal UVLO block. If V_{CC} drops below its falling threshold (2.4V), the chip shuts down. Once V_{CC} exceeds its rising threshold (2.6V), the device restarts and resumes normal operation. If V_{CC} falls to 2.4V, the part resets to the value set via the OTP memory.

Frequency Dithering for Low EMI

Frequency dithering reduces EMI, which is especially critical for EMI-sensitive applications. Frequency spread spectrum (FSS) modulation spreads the frequency spectrum of the boost converter, which then spreads the energy of the switching harmonics across a wider band while reducing their amplitudes. This enables the device to meet stringent EMI goals.

The MPQ2024A's FSS function provides a ±10% variation range for the selected switching frequency, with a 9kHz dithering cycle.

FSS modulation is enabled by default; it can be disabled via the I^2C interface.

Soft Start (SS)

To prevent overshoot during start-up, the MPQ2024A has a built-in, 1ms soft-start time (t_{SS}) for the pre-boost regulator's output. When the chip starts, the internal circuitry generates a soft-start voltage (V_{SS}) that ramps up slowly. When V_{SS} falls below the internal reference

voltage (V_{REF}), V_{SS} overrides V_{REF} as the error amplifier reference. When V_{SS} exceeds V_{REF}, V_{REF} acts as the reference.

At this point, SS finishes and the MPQ2024A enters steady state. During SS, OV/UV/PG indication in the I^2C registers are invalid and /FT remains high.

Adjustable LDO Output Voltage (V_{OUT})

The MPQ2024A's LDO output voltage (V_{OUT}) is adjustable from 1V to 13.6V via the I^2C interface. V_{OUT} is also adjustable by tracking the external voltage on the ADJ pin.

External voltage tracking mode is enabled via the I^2C interface. If this function is enabled, V_{OUT} is equal to the voltage at the ADJ pin. The applied voltage range on ADJ is also 3V to 13V. To track higher voltages, a resistor divider can be used to scale down the voltage level.

If external voltage tracking mode enabled, /FT pin indication and LDO output OV, UV, and power good (PG) indication in the I^2C registers are invalid. The /FT pin remains high.

LDO Output Voltage and Current Monitor

The MPQ2024A has a dedicated analog-to-digital converter (ADC) block to monitor V_{OUT} and the LDO load current. The ADC can be enabled via the I^2C. Read register 06 and register 08 to monitor V_{OUT} and the LDO load current.

The MPQ2024A provides open-load functionality. When the open-load function is enabled and the load is below the open load falling threshold, the MPQ2024A considers this an open load state and the /FT pin is pulled down. By default, the open-load function is disabled. This function does not work while disabled. Contact an MPS FAE for more details.

One-Time Programmable (OTP) Memory

The MPQ2024A features 2 pages of OTP memory to permanently store the desired settings.

For long-term reliability, a differential OTP cell is used instead of a single-ended cell. Data is stored on two floating gate avalanche injection metal oxide semiconductors (FAMOS), and output comparators are used for differential reading.

The first page of the multi-page OTP has been configured following custom codes.

Once the device is enabled, the default values on the first page set the control parameters in the registers. If there is data on other pages of the OTP memory, the newest setting is identified by an internal indicator to the write registers. See the Register Map on page 35 for more details.

I²C INTERFACE

I²C Serial Interface Description

The I²C is a two-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. Connecting to the line, a master device generates the SCL signal and device address, and arranges the communication sequence. The MPQ2024A interface is an I²C slave that supports both fast mode (400kHz) and typically high-speed mode (3.4MHz), adding flexibility to the power supply solution. The output voltage, transition slew rate, and additional parameters can be instantaneously controlled via the I²C interface.

Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low (see Figure 7).

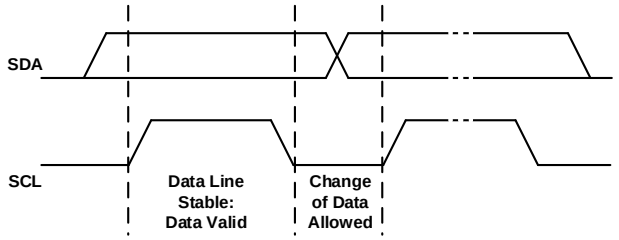


Figure 7: Bit Transfer on the I²C Bus

Start and Stop Commands

Start (S) and stop (P) commands are signaled by the master device, which signifies the beginning and the end of the I²C transfer. A start command is defined as the SDA signal transitioning from high to low while the SCL is high. A stop command is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 8).

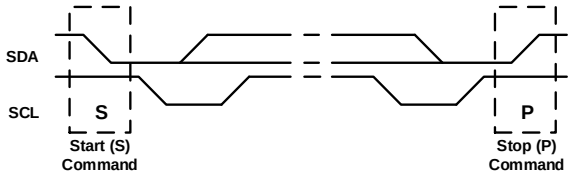


Figure 8: Start and Stop Commands

Start and stop commands are always generated by the master. The bus is considered busy after a start command. The bus is considered free again a minimum of 4.7µs after the stop command. If a repeated start (Sr) command is generated instead of a stop command, the bus remains busy. The start and repeated start commands are functionally identical.

Transfer Data

Every byte put on the SDA line must be 8 bits long. Each byte must be followed by an acknowledge (ACK) bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse, so that it remains stable and low during the high period of the clock pulse.

Figure 9 shows the format for data transfers. After the start command, a slave address is sent. This address is 7 bits long, followed by an 8th data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). A data transfer is terminated by a stop command, which is generated by the master. If the master still wishes to communicate on the bus, it can generate a repeated start command and address another slave device without first generating a stop command.

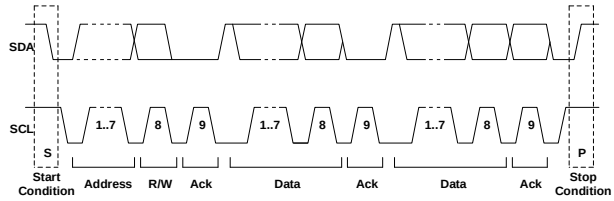


Figure 9: A Complete Data Transfer

Packet Error Checking (PEC)

The packet error checking (PEC) mechanism is employed to improve communication reliability and robustness. When applicable, PEC is implemented by appending a packet error code at the end of each message transfer.

The PEC is a CRC-8 error-checking byte, calculated on all the message bytes (including addresses and read/write bits). The PEC is appended to the message by the device that supplied the last data byte.

Write Sequence

A typical write sequence requires a master's start command, a valid slave address, a register index byte, a corresponding data byte, and ends with a PEC for a single data update.

After receiving each byte, the MPQ2024A acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MPQ2024A. The MPQ2024A performs an update on the falling edge of the LSB byte.

The PEC byte in a write sequence can be calculated with CRC-8. It requires the slave address, register index, and data to make the calculation. CRC-8 can be calculated with Equation (1):

$$CRC\text{-}8 = X^8 + X^2 + X + 1 \quad (1)$$

Figure 10 shows a write sequence.

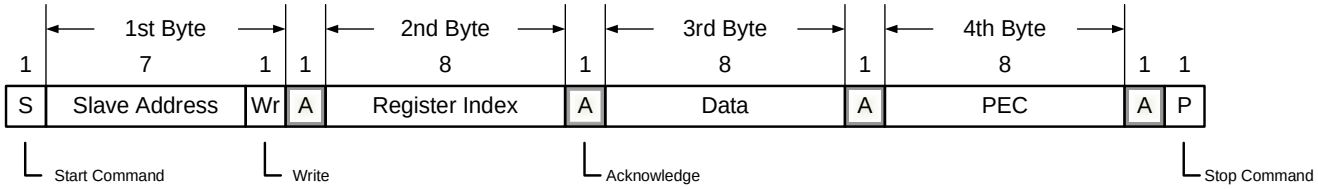


Figure 10: Write Sequence

Read Sequence

A typical read sequence is 5 bytes long. It starts with the master's start condition, then a write valid slave address, followed by a register index byte. Unlike a write sequence, the master sends a start command again. The bus direction then turns around with the re-broadcast of the slave address, with bit[1] indicating a read cycle. The following 4th byte contains the data being returned by the MPQ2024A. That byte value in the data byte reflects the value of the register index being queried before. Finally, the MPQ2024A sends a PEC byte to end the read sequence. Only one register can be read at a time.

The PEC byte in a read sequence can be calculated with CRC-8. It requires the slave address, register index, and data to make the calculation. CRC-8 can be calculated with Equation (1).

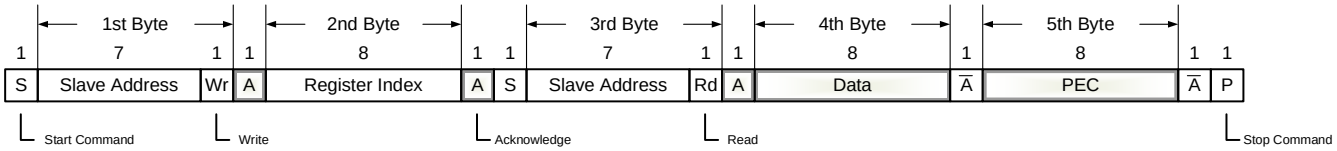


Figure 11: Read Sequence

I²C Update Sequence

The MPQ2024A requires a start command, a valid I²C address, a register address byte, and a data byte for a single data update. After receiving each byte, the MPQ2024A acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MPQ2024A. The MPQ2024A performs an update on the falling edge of the LSB byte.

I²C Chip Address

The ADD pin can be used to configure the I²C address by adjusting the value of the resistor that is connected between the ADD pin and ground. A 10μA current flows from the ADD pin and generates a voltage on the ADD resistor. The MPQ2024A supports seven addresses, for up to seven voltage rails, by detecting the different voltages on the ADD pin. Table 2 on page 34 shows the resistances for different I²C addresses. The resistor's tolerance should not exceed 1% of the recommended resistance.

When the master sends the address as an 8-bit value, the 7-bit address should be followed by a 0 or 1 to indicate a write or read operation.

Table 2: I²C Address

Address	Resistance (kΩ)	Window Low (mV)	Typical ADD Voltage (mV)	Window High (mV)	Min (μA)	Typical ADD Current (μA)	Max (μA)
21h	0 (1%)	0	0	40	9.5	10	10.5
22h	6.98 (1%)	40	70	100			
23h	15 (1%)	100	150	200			
24h	30 (1%)	200	300	400			
25h	54.9 (1%)	400	550	700			
26h	95.3 (1%)	700	950	1200			
27h	>130 (1%) or floating	1200	-	-			

REGISTER MAP

Register Short Name	R/W	Add	Default (9)	D7	D6	D5	D4	D3	D2	D1	D0
Device Status and Diagnostics											
DEV_REV	R	0x00	00h	SILICON_INFORMATION							
DEV_STAT	R	0x01	-	PRE BOOST_ ACTIVE	RESERVED (10)	LDO_ ACTIVE	RESERVED (10)	VOUT_ PG	FT_ ASSERT	I2C_ERR	POR
ERR_FLAG_1	R	0x02	-	RESERVED (10)	RESERVED (10)	VOUT_ OV	VOUT_ UV	VOUT_ BST_OV	VOUT_ BST_UV	RESERVED (10)	LDO_STB
ERR_FLAG_2	R	0x03	-	RESERVED (10)	LDO_OC	PRE BOOST_ OC	OT	RESERVED (10)	LDO_OL	RESERVED (10)	RESERVED (10)
DEV_CTRL	R/W	0x04	A1h	PRE BOOST_ EN	RESERVED (10)	LDO_ EN	SHUT DOWN	ADC-EN	SOFT _RST	BOOST _FREQ_ SEL	FAULT _HANDLE
Monitoring											
RESERVED	R	0x05	-	RESERVED (10)							
MON_VOUT	R	0x06	-	VOUT_MON							
RESERVED	R	0x07	-	RESERVED (10)							
MON_IOUT	R	0x08	-	IOUT_MON							
Power Management											
SET_FAULT_CLEAR	R/W	0x09	68h	FAULT_ CLEAR	RESERVED (10)						
SET_VOUT	R/W	0x0A	68h	RESERVED (10)	VOUT_ STEP	VOUT_SET					
SET_VPREBOOST_1	R/W	0x0B	78h	VPREBOOST_SET							
SET_VPREBOOST_2	R/W	0x0C	9Ch	VPREBOOST_ON_THR				PREBOOST_OV		PREBOOST_UV	
SET_PG_UVOV	R/W	0x0D	00h	RESERVED (10)		VOUT _OV_THR	VOUT _UV_THR	RESERVED (10)		VOUT_PG _H_THR	VOUT_PG _L_THR
SET_LDO_TRC	R/W	0x0E	10h	RESERVED (10)	LDO_ TRC	FSS_DIS	RESERVED (10)				
SET_IOUT_LIM	R/W	0x0F	10h	STB_DETECTION_ WINDOW		OC_MIN	IOUT_OC_THR				

Note:

9) Default values for MPQ2024A-0000 registers. The default value can be redefined if the OTP function is available.
10) This bit is not defined, and is reserved for future use.

REGISTER DESCRIPTION

DEV_REV (0x00)

Access: Read-only

POR/Soft Reset Value: 00000000

The DEV_REV command returns the device revision and information.

Bits	Name	Description
D[7:0]	SILICON_ INFORMATION	Returns the silicon information.

DEV_STAT (0x01)

Access: Read-only

POR/Soft Reset Value: 00000000

The DEV_STAT command returns the device status.

Bits	Name	Description
D[7]	PREBOOST_ ACTIVE	0: The pre-boost converter is not active 1: The pre-boost converter is active
D[6]	RESERVED	Reserved. Always reads as 0.
D[5]	LDO_ACTIVE	0: LDO is not active 1: LDO is active
D[4]	RESERVED	Reserved. Always reads as 0.
D[3]	VOUT_PG	0: V_{OUT} is not within its power good (PG) range 1: V_{OUT} is within its PG range
D[2]	FT_ASSERT	0: The /FT pin is not asserting 1: The /FT pin is asserting (active low)
D[1]	I2C_ERR	0: No I^2C communication error has occurred 1: An I^2C communication error has occurred Note that if an I^2C communication error occurs, the chip can be read, but not written.
D[0]	POR	0: No power-on reset (POR) event has occurred 1: A POR event has occurred and finished

ERR_FLAG_1 (0x02)

Access: Read-only

POR/Soft Reset Value: 00000000

The ERR_FLAG_1 command returns device error flags for over-voltage (OV) and under-voltage (UV) conditions.

Bits	Name	Description
D[7:6]	RESERVED	Reserved. Always reads as 0.
D[5]	VOUT_OV	0: Clears to 0 when there is no over-voltage (OV) condition on OUT 1: An OV condition has been detected on OUT
D[4]	VOUT_UV	0: Clears to 0 when there is no under-voltage (UV) condition on OUT 1: A UV condition has been detected on OUT
D[3]	VOUT_BST_OV	0: Clears to 0 when no OV condition has been detected on FB 1: An OV condition has been detected on FB
D[2]	VOUT_BST_UV	0: Clears to 0 when no UV condition has been detected on FB 1: A UV condition has been detected on FB

D[1]	RESERVED	Reserved. Always reads as 0.
D[0]	LDO_STB	0: Clears to 0 when no short-to-battery condition has been detected on LDO 1: A short-to-battery condition has been detected on LDO

ERR_FLAG_2 (0x03)

Access: Read-only

POR/Soft Reset Value: 00000000

The ERR_FLAG_2 command returns device error flags for over-current (OC) and over-temperature (OT) conditions.

Bits	Name	Description
D[7]	RESERVED	Reserved. Always reads as 0.
D[6]	LDO_OC	0: Clears to 0 when no over-current (OC) condition has been detected on OUT 1: An OC condition has been detected on OUT
D[5]	PREBOOST_OC	0: Clear to 0 when no OC condition has been detected in the pre-boost regulator 1: An OC condition has been detected in the pre-boost regulator
D[4]	OT	0: Clears to 0 when no over-temperature (OT) condition has been detected 1: An OT condition has been detected
D[3]	RESERVED	Reserved. Always reads as 0.
D[2]	LDO_OL	0: Clears to 0 when no open load (OL) condition has been detected on OUT 1: An OL condition has been detected on OUT This bit is only valid when the open-load function is enabled.
D[1:0]	RESERVED	Reserved. Always reads as 0.

DEV_CTRL (0x04)

Access: R/W

POR/Soft Reset Value: 10100001

The DEV_CTRL command controls the device.

Bits	Name	Description
D[7]	PREBOOST_EN	0: The pre-boost converter is disabled 1: The pre-boost converter is enabled
D[6]	RESERVED	Reserved. Always reads as 0.
D[5]	LDO_EN	0: The LDO is disabled 1: The LDO is enabled
D[4]	SHUTDOWN	0: Turn on the device if the EN pin voltage exceeds $V_{EN\_TH\_R}$ 1: The device is forced to shut down
D[3]	ADC-EN	0: The analog-to-digital converter (ADC) is disabled 1: ADC is enabled
D[2]	SOFT_RST	0: No soft reset has been required 1: A soft reset has been requested. The device returns to the state of the OTP code
D[1]	BOOST_FREQ_SEL	0: 400kHz switching frequency (f_{SW}) 1: 2.2MHz f_{SW}
D[0]	FAULT_HANDLE	0: Latch-off mode 1: Hiccup mode with a 100ms blank time

RESERVED (0x05)

Access: Read-only

POR/Soft Reset Value: 00000000

Bits	Name	Description
D[7:0]	RESERVED	Reserved. Always reads as 0.

MON_VOUT (0x06)

Access: Read-only

POR/Soft Reset Value: 00000000

The MON_VOUT command returns the monitored LDO output voltage (V_{OUT}).

Bits	Name	Description
D[7:0]	VOUT_MON	Records the monitored V_{OUT} by the ADC. This value refreshes each time it is read. 1 LSB = 55mV. The value can be calculated with the following equation: VOUT_MON = D[7:0] x 55mV For example, if bits D[7:0] = $(10100100)_2$, this is $(164)_{10}$, and V_{OUT} = 164 x 55mV = 9.02V.

RESERVED (0x07)

Access: Read-only

POR/Soft Reset Value: 00000000

Bits	Name	Description
D[7:0]	RESERVED	Reserved. Always reads as 0.

MON_IOUT (0x08)

Access: Read-only

POR/Soft Reset Value: 00000000

The MON_IOUT command returns the monitored LDO output current (I_{OUT}).

Bits	Name	Description
D[7:0]	IOUT_MON	Records the monitored I_{OUT} by the ADC. This value refreshes each time it is read. 1 LSB = 1.2mA. The value can be calculated with the following equation: IOUT_MON = D[7:0] x 1.2mA For example, if bits D[7:0] = $(11111010)_2$, this is equal to $(250)_{10}$, and I_{OUT} = 250 x 1.2mA = 300mA.

SET_FAULT_CLEAR (0x09)

Access: R/W

POR/Soft Reset Value: 01101000

The SET_FAULT_CLEAR command clears all fault flags.

Bits	Name	Description
D[7]	FAULT_CLEAR	0: No action (default) 1: Clear all fault flags and de-assert the /FT pin. For example, if I2C_ERR occurs, set D[7] = 1, and then the chip can be written again
D[6:0]	RESERVED	Reserved. Always reads as 0.

SET_VOUT (0x0A)

Access: R/W

POR/Soft Reset Value: 01101000

The SET_VOUT command sets the LDO output voltage (V_{OUT}).

Bits	Name	Description
D[7]	RESERVED	Reserved. Always reads as 0.
D[6]	VOUT_STEP	Sets the V_{OUT} step. This bit is set to 1 by default. 0: 100mV 1: 200mV
D[5:0]	VOUT_SET	Sets V_{OUT}, calculated with the following equation: V_{OUT} = 1V + VOUT_SET x VOUT_STEP If the default is D[5:0] = $(101000)_2$, which is $(40)_{10}$, then the default V_{OUT} = 1V + 40 x 200mV = 9V

SET_VPREBOOST_1 (0x0B)

Access: R/W

POR/Soft Reset Value: 01111000

The SET_VPREBOOST_1 command sets the pre-boost regulator output voltage (V_{OUT_BOOST}).

Bits	Name	Description
D[7:0]	VPREBOOST_SET	Sets V_{OUT_BOOST}. The default value is 12V. 00h~40h: Reserved 41h~9Fh: D[7:0] x 100mV (100mV/step). 6.5V to 15.9V A0h~FFh: Reserved

SET_VPREBOOST_2 (0x0C)

Access: R/W

POR/Soft Reset Value: 10011100

The SET_VPREBOOST_2 command sets the pre-boost regulator's on voltage threshold for over-voltage (OV) and under-voltage (UV) conditions.

Bits	Name	Description
D[7:4]	VPREBOOST_ ON_THR	Sets the pre-boost regulator's turn on threshold, The default value is 11V. 00h~0Dh: D[7:4] x 500mV + 6.5V (500mV/step) 0Eh: 14V 0Fh: 15V
D[3:2]	PREBOOST_OV_R	00: 110% of V_{REF} 01: 115% of V_{REF} 10: 120% of V_{REF} 11: 130% of V_{REF}
D[1:0]	PREBOOST_UV_F	00: 70% of V_{REF} 01: 75% of V_{REF} 10: 80% of V_{REF} 11: 85% of V_{REF}

SET_PG_UVOV (0x0D)

Access: R/W

POR/Soft Reset Value: 00000000

The SET_PG_UVOV command sets the power good (PG) and LDO under-voltage (UV) and over-voltage (OV) settings.

Bits	Name	Description
D[7:6]	RESERVED	Reserved. Always reads as 0.
D[5]	VOUT_OV_THR	0: The V_{OUT} over-voltage (OV) threshold is 115% of the set V_{OUT} 1: The V_{OUT} OV threshold is 120% of the set V_{OUT}
D[4]	VOUT_UV_THR	0: The V_{OUT} under-voltage (UV) threshold is 75% of the set V_{OUT} 1: The V_{OUT} UV threshold is 80% of the set V_{OUT}
D[3:2]	RESERVED	Reserved. Always reads as 0.
D[1]	VOUT_PG_H_THR	0: The upper boundary of the V_{OUT} power good (PG) threshold is 105% of the set voltage 1: The upper boundary of the V_{OUT} PG threshold is 110% of the set voltage
D[0]	VOUT_PG_L_THR	0: The lower boundary of the V_{OUT} PG threshold is 90% of the set voltage 1: The lower boundary of the V_{OUT} PG threshold is 95% of the set voltage

SET_LDO_TRC (0x0E)

Access: R/W

POR/Soft Reset Value: 00010000

The SET_LDO_TRC command sets the LDO tracking mode and sets boost FSS.

Bits	Name	Description
D[7]	RESERVED	Reserved. Always reads as 0.
D[6]	LDO-TRC	0: Disable LDO tracking mode 1: Enable LDO tracking mode
D[5]	FSS_DIS	0: Enable FSS modulation 1: Disable FSS modulation
D[4:0]	RESERVED	Reserved. Always reads as 0.

SET_IOUT_LIM (0x0F)

Access: R/W

POR/Soft Reset Value: 00010000

The SET_IOUT_LIM command sets the LDO current limit threshold

Bits	Name	Description
D[7:6]	STB_DETECTION_ WINDOW	00: 15ms 01: 7ms 10: 3ms 11: 1ms
D[5]	OC_MIN	Sets the minimum over-current (OC) threshold for LDO. The default value is 300mA. 0: 300mA 1: 100mA
D[4:0]	IOUT_OC_THR	Sets the output OC threshold. 1 LSB = 6.25mA. This value can be calculated with the following equation: I_{LIMIT} = D[4:0] x 6.25mA + OC_MIN OC_MIN is set by register 0x0F, bit[5]. The default D[4:0] = $(10000)_2$, which is equal to $(16)_{10}$, and I_{LIMIT} = 16 x 6.25 + 300 = 400mA.

APPLICATION INFORMATION

Figure 12 shows the MPQ2024A's typical application circuit.

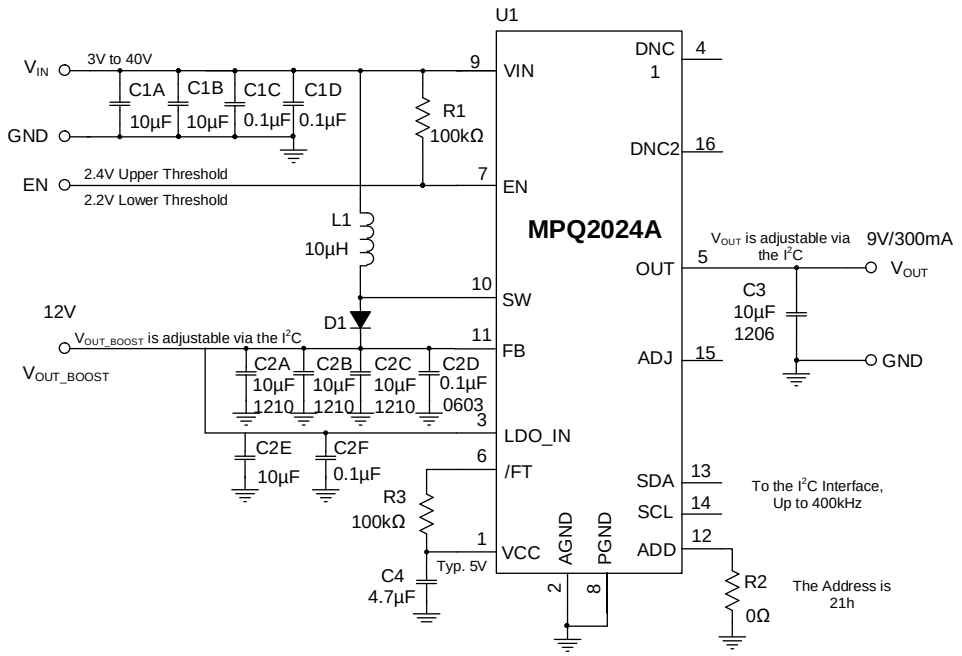


Figure 12: Typical Application Circuit (Boost + LDO, V_{OUT_BOOST} = 12V, V_{OUT} = 9V, f_{SW} = 400kHz)

Table 3 shows the design guide index. For more details, see Figure 12 above.

Table 3: Design Guide Index

Pin #	Name	Components	Design Guide Index
1	VCC	C4	Internal VCC (VCC, Pin 1)
2	AGND	-	GND connection (PGND, Pin 8; AGND, Pin 2)
3	LDO_IN	C2E, C2F	Selecting the Input Capacitors for the LDO (LDO_IN, Pin 3)
4	DNC1	-	Do Not Connect (DNC1, Pin 4)
5	OUT	C3	Selecting the Output Capacitors for the LDO (OUT, Pin 5)
6	/FT	R3	Fault Indicator (/FT, Pin 6)
7	EN	R1	Enable (EN, Pin 7)
8	GND	-	GND Connection (PGND 8; AGND 2)
9	VIN	C1A, C1B, C1C, C1D	Selecting the Input Capacitors for the Pre-Boost Regulator (VIN, Pin 9)
10	SW	L1, D1	Selecting the Inductor for the Pre-Boost Regulator (SW, Pin 10) Selecting the Schottky Diode for the Pre-Boost Regulator (SW, Pin 10)
11	FB	C2A, C2B, C2C, C2D	Selecting the Boost Output Capacitors (FB, Pin 11)
12	ADD	R2	Selecting the I²C Address Resistor (ADD, Pin 12)
13	SDA	-	I²C Interface (SDA, Pin 13; SCL, Pin 14)
14	SCL	-	I²C Interface (SDA, Pin 13; SCL, Pin 14)
5	ADJ	-	Reference Voltage Input for the LDO (ADJ, Pin 15)
16	DNC2	-	Do Not Connect (DNC2, Pin 16)

Internal VCC (VCC, Pin 1)

The VCC capacitor (C4) should be between 1µF and 10µF. Generally, a 4.7µF ceramic capacitor is recommended.

All of the control blocks and the I²C block are powered by the internal regulator. This regulator uses V_{IN} as its input and operates across the full V_{IN} range.

In latch-off mode, V_{CC} should drop below its falling threshold before start-up to prevent a failed start-up. Do not use I²C communication when V_{CC} is below its UVLO threshold.

It is not recommended that V_{CC} be used to supply power to external circuits.

Selecting the Input Capacitor for the LDO (LDO_IN, Pin 3)

For efficient operation, place a 1µF to 10µF ceramic capacitor with dielectrics (X5R or X7R) between LDO_IN and ground. Larger-value capacitors in this range improve line transient response.

Do Not Connect (DNC1, Pin 4; DNC2, Pin 16)

Do not connect. Reserved for factory functions. It is recommended to leave DNC1 floating. It is recommended to leave DNC2 floating or connect it to ground.

Selecting the Output Capacitor for the LDO (OUT, Pin 5)

For stable operation, use a 4.7µF to 22µF, ceramic capacitor with X5R or X7R dielectrics. Larger-value capacitors in this range improve line transient response and reduce noise. Output capacitors of other dielectric types may be used, but they are not recommended, as their capacitance can deviate greatly from their rated value across different temperatures.

The LDO output may appear as a negative voltage under short-circuit conditions; this can be solved by adding a Schottky diode between the OUT and GND pins. The Schottky diode is recommended to be 40V/1A.

Setting the Boost and LDO Output Voltages

The MPQ2024A does not require an external resistor to set the output voltages. OTP register 0x0B sets V_{OUT_BOOST}, while OTP register 0x0A sets V_{OUT} (see the Register Map on page 35).

V_{OUT_BOOST} is configured via register 0x0B, bits D[7:0], and the voltage can be calculated with (bits D[7:0] x 100mV). This voltage can be between 6.5V and 15.9V.

For example, if 0x0B is set to 78h, then V_{OUT_BOOST} = 0.1V x 120 = 12V.

V_{OUT} is configured via register 0x0A. It can be set between 1V and 13.6V with 200mV per step, or between 1V and 7.3V with 100mV per step. V_{OUT} can be calculated with (bits D[5:0] x step) + 1V.

For example, if register 0x0A, bits D[7:0] are set to 68h, and the step is 200mV, then V_{OUT} = 1V + (40 x 0.2V) = 9V.

When V_{LDO_IN} is almost equal to V_{OUT}, the LDO enters dropout mode, and the LDO's current limit drops by 15%. The difference between V_{LDO_IN} and V_{OUT} must stay above 1.5V when designing the circuit.

Fault Indicator (/FT, Pin 6)

The R_{FT} resistance (R2) is recommended to be about 100kΩ.

The /FT pin is connected to the open drain of an internal MOSFET. It should be connected to a ≤5V voltage through an external pull-up resistor for fault indication.

Float or ground /FT if it is not used.

At low input voltages, /FT may be falsely triggered after start-up. This is because the /FT blanking time may not be long enough during start-up, which can trigger a V_{OUT} UV condition.

Enable (EN, Pin 7)

The EN pin can be used to enable and disable the entire device. Pull EN below the falling threshold (2.2V) to shut down the chip. Drive EN above its rising threshold (2.4V) to enable the chip.

There are separate, dedicated register bits to enable the software for the pre-boost regulator and LDO. The physical EN pin has a higher priority than the software enable function.

Since EN has a 3.3MΩ pull-down resistor, float EN to shut down the chip. EN can be connected to a high-voltage bus (e.g. the VIN pin) through a pull-up resistor. In this scenario, it is recommended to use a 100kΩ pull-up resistor.

The MPQ2024A has an internal, fixed UVLO threshold. In the normal input range, the rising threshold is 2.8V and the falling threshold is 2V when the pre-boost regulator is enabled. When the pre-boost regulator is disabled, the rising threshold is 4.2V and the falling threshold is 3.8V. For applications that require a higher UVLO threshold, place an external resistor between the VIN and EN pins to raise the equivalent UVLO threshold (see Figure 13).

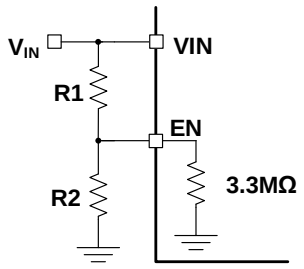


Figure 13: Adjustable UVLO through EN Divider

The UVLO rising and falling thresholds can be calculated with Equation (2) and Equation (3), respectively:

$$V_{IN\_UVLO\_RISING}=(1+\frac{R1}{R2||3.3M\Omega})\times V_{EN\_TH\_R} \quad (2)$$

$$V_{IN\_UVLO\_FALLING}=(1+\frac{R1}{R2||3.3M\Omega})\times V_{EN\_TH\_F} \quad (3)$$

Where $V_{EN\_TH\_R}$ = 2.4V, and $V_{EN\_TH\_F}$ = 2.2V.

To quickly turn EN on and off, the EN off time should be longer than 500µs.

Selecting Input Capacitor for the Pre-Boost Regulator (VIN, Pin 9)

The input requires a capacitor to supply the AC ripple current to the inductor, while limiting noise at the input source. Use a low-ESR capacitor with a value >4.7µF to minimize the IC noise. Ceramic capacitors are recommended, but tantalum or low-ESR electrolytic capacitors can also suffice. However, since the capacitor absorbs the input switching current, it requires an adequate ripple current rating. Use a capacitor with an RMS current rating that exceeds the inductor ripple current.

To ensure stable operation, place the input capacitor as close to the IC as possible. As an alternative, place a small, high-quality ceramic 0.1µF capacitor close to the IC, and place the larger capacitor further away. If using the latter technique, use either tantalum or electrolytic capacitors for the larger-value capacitor. Place all ceramic capacitors close to the MPQ2024A.

Selecting the Inductor for the Pre-Boost Regulator (SW, Pin 10)

The inductor forces V_{OUT} to exceed V_{IN}. A larger inductance results in less ripple current and reduces the peak inductor current, which reduces the stress on the internal N-channel MOSFET. However, a larger-value inductor is physically larger, has a higher series resistance, and lower saturation current.

A good rule of thumb is to allow the peak-to-peak ripple current to equal 30% to 50% of the maximum input current. To prevent regulator losses due to the current limit, ensure that the peak inductor current is less than 75% of the current limit during duty cycle operation. Also ensure that the inductor does not saturate under the worst-case load transient response and start-up conditions. Calculate the required inductance (L) with Equation (4):

$$L=\frac{V_{IN}\times(V_{OUT}-V_{IN})}{V_{OUT}\times f_{SW}\times\Delta I} \quad (4)$$

Where ΔI is the peak-to-peak inductor ripple current, estimated with Equation (5):

$$\Delta I = (30\% \text{ to } 50\%) \times I_{LOAD(MAX)} \quad (5)$$

Where I_{LOAD}(max) is the maximum load current.

Calculate $I_{IN(MAX)}$ with Equation (6):

$$I_{IN(MAX)}=\frac{V_{OUT}\times I_{LOAD(MAX)}}{V_{IN}\times\eta} \quad (6)$$

Selecting the Schottky Diode for the Pre-Boost Regulator (SW, Pin 10)

The output rectifier diode supplies current to the inductor when the internal MOSFET is off. Use a Schottky diode to reduce losses due to the diode's forward voltage and recovery time. The diode should be rated for a reverse voltage equal to or greater than the expected V_{OUT_BOOST}. The average current rating must exceed the maximum expected load current, and the peak current rating must exceed the peak inductor current. Float the SW pin if it is not used.

Selecting Output Capacitor for the Pre-Boost Regulator (FB, Pin 11)

The output capacitor maintains the DC output voltage. For the best results, use low-ESR capacitors to minimize the output voltage ripple. The output capacitor's characteristics also affect the regulatory control system's stability. For the best results, use ceramic, tantalum, or low-ESR electrolytic capacitors. For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, which means that the output voltage ripple is mostly independent of the ESR. Estimate the output voltage ripple (V_{RIPPLE}) with Equation (7):

$$V_{RIPPLE} \cong I_{LOAD} \times \frac{1-\frac{V_{IN}}{V_{OUT}}}{C_{OUT} \times f_{SW}} \quad (7)$$

Where V_{IN} and V_{OUT} are the DC input and output voltages, respectively, I_{LOAD} is the pre-boost regulator's load current, f_{SW} is the switching frequency, and C_{OUT} is the value of the pre-boost regulator's output capacitor.

For tantalum or low-ESR electrolytic capacitors, the ESR dominates the impedance at the switching frequency. In this scenario, V_{RIPPLE} can be calculated with Equation (8):

$$V_{RIPPLE} \cong I_{LOAD} \times \frac{1-\frac{V_{IN}}{V_{OUT}}}{C_{OUT} \times f_{SW}} + \frac{I_{LOAD} \times R_{ESR} \times V_{OUT}}{V_{IN}} \quad (8)$$

Where R_{ESR} is the equivalent series resistance (ESR) of the output capacitor(s).

Choose an output capacitor that meets the design's output ripple and load transient response requirements. A ceramic capacitor exceeding 22µF is recommended for most applications. Float the FB pin if it is not used.

Selecting the I²C Address Resistor (ADD, Pin 12)

The MPQ2024A supports seven addresses for up to seven voltage rails by detecting the voltage on the ADD pin. Table 2 on page 34 shows the resistances for different I²C addresses. The resistor tolerance should not exceed 1% of the recommended resistance.

I²C Interface (SDA, Pin 13; SCL, Pin 14)

The MPQ2024A interface is an I²C slave that supports fast mode (400kHz), adding flexibility to the power supply solution. See the I²C Interface section on page 32 for details.

If the I²C interface is not used, it is recommended to connect the SDA and SCL pins to the VCC pin through a resistor (e.g. 100kΩ).

Setting the Reference Voltage Input for the LDO (ADJ, Pin 15)

External voltage tracking mode can be enabled via the I²C interface. If enabled, V_{OUT} is equal to the voltage at the ADJ pin. For stable operation, use a 10nF to 100nF ceramic capacitor with X5R or X7R dielectrics.

If the ADJ pin is not used, leave it floating or connect it to GND.

GND Connection (AGND, Pin 2; GND, Pin 8)

See the PCB Layout Guidelines section on page 46 for more details.

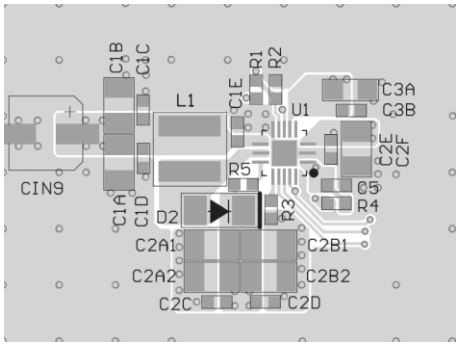
PCB Layout Guidelines (11)

Efficient PCB layout is critical for stable operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 14 and the guidelines below:

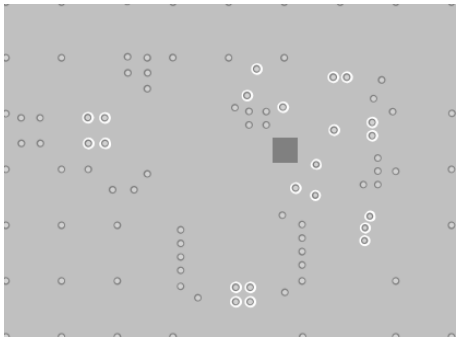
1. Place the symmetric input capacitor as close to the VIN and GND pins as possible.
2. Place L1 and D2 as close to the FB pin as possible.
3. Place the symmetric boost output capacitor as close to the Schottky diode as possible.
4. Use a large ground plane to connect directly to PGND. If the bottom layer is a ground plane, add vias near PGND.
5. Ensure that the high-current paths (e.g. PGND and SW/LDO_IN) have short, direct, and wide traces.
6. Place the ceramic input capacitor, especially the small package size (0603) input/output bypass capacitor, as close as possible to the VIN, OUT, FB, and PGND pins to minimize high-frequency noise.
7. Keep the connection between the input capacitor and VIN as short and wide as possible.
8. Keep the connection between the LDO input capacitor and LDO_IN pin as short and wide as possible.
9. Place the VCC capacitor as close to the VCC and AGND pins as possible.
10. Route SW away from sensitive analog areas.
11. Use multiple visa to connect the power planes to the internal layers.

Notes:

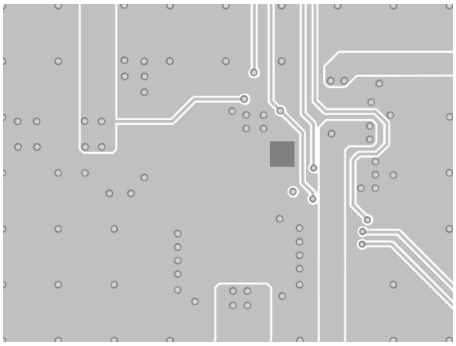
11) The recommended PCB layout is based on the typical application circuit (see Figure 17 on page 48).



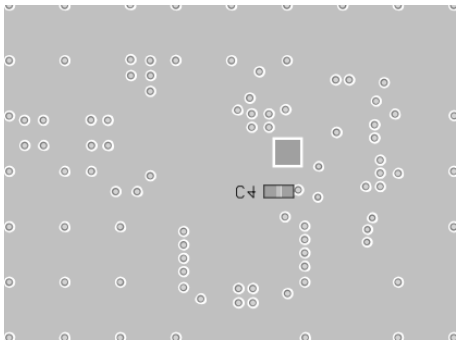
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 14: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

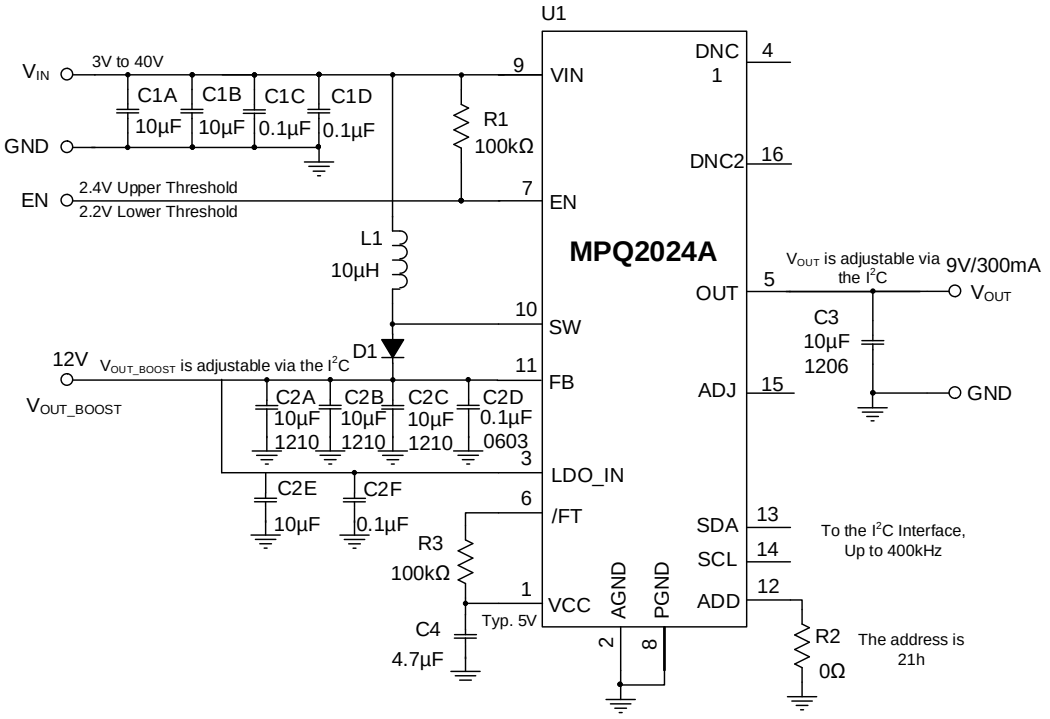


Figure 15: Typical Application Circuit (Boost + LDO, V_{OUT_BOOST} = 12V, V_{OUT} = 9V, f_{SW} = 400kHz)

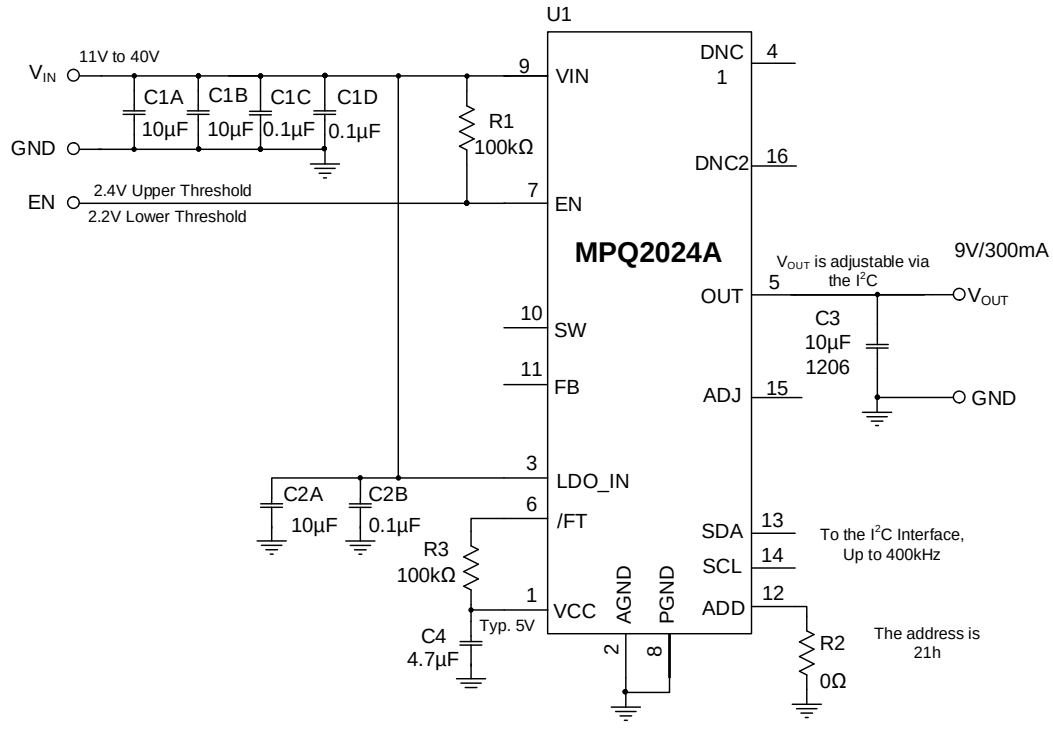


Figure 16: Typical Application Circuit (Single LDO, V_{OUT} = 9V)

TYPICAL APPLICATION CIRCUITS *(continued)*

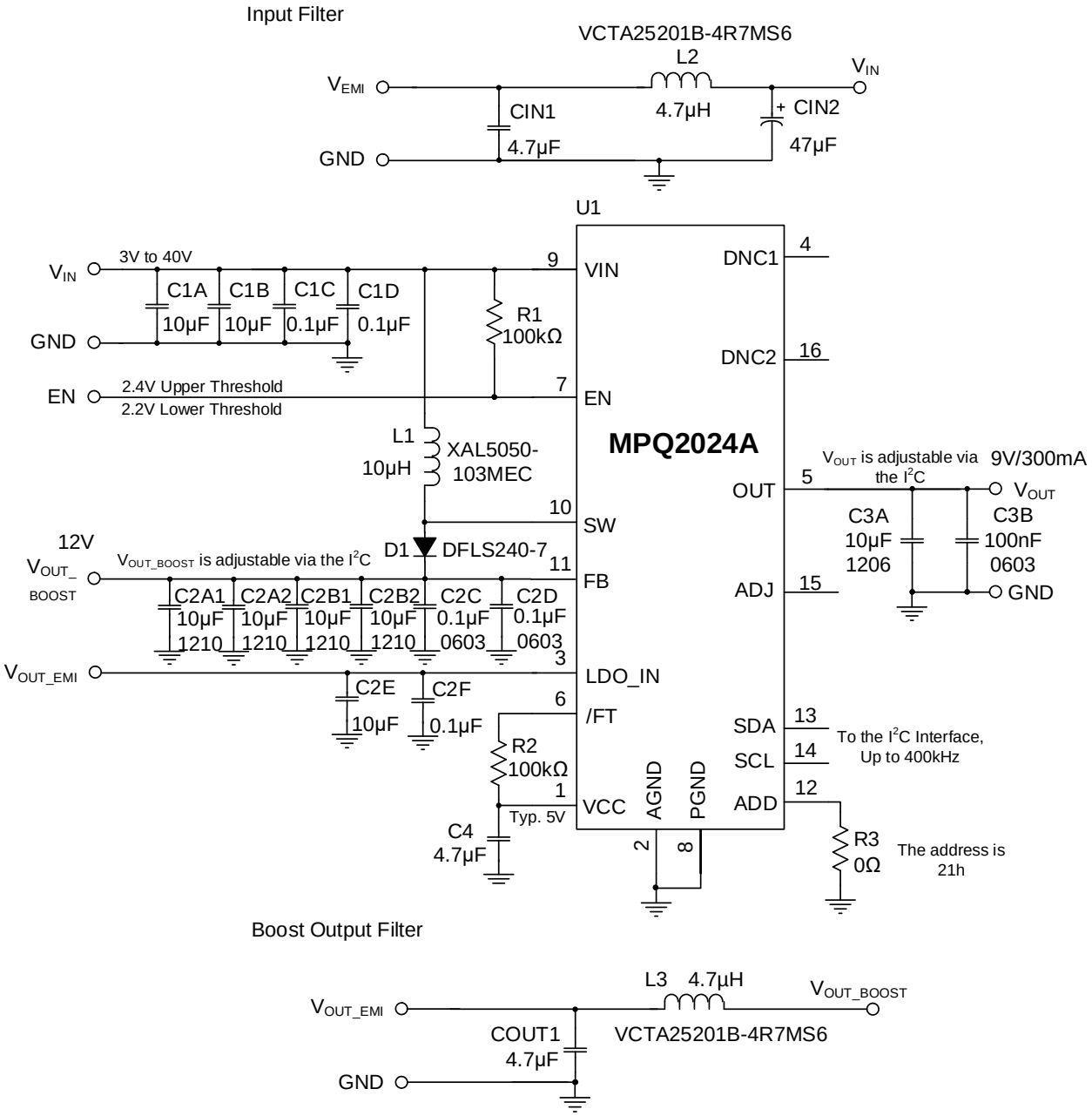
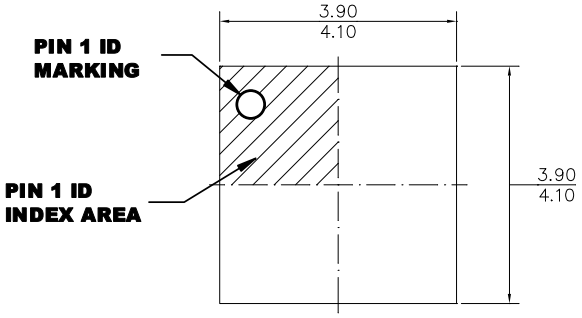


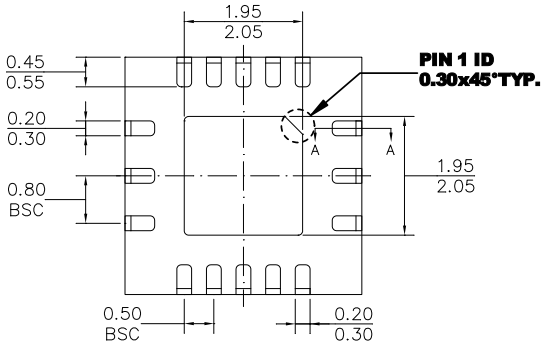
Figure 17: Typical Application Circuit (Boost + LDO, V_{OUT_BOOST} = 12V, V_{OUT} = 9V, f_{SW} = 400kHz, with EMI Filters)

PACKAGE INFORMATION

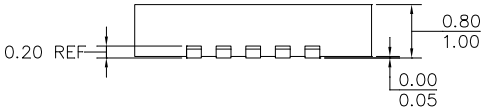
QFN-16 (4mmx4mm)
Wettable Flank



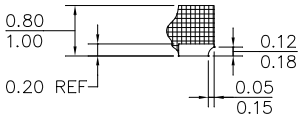
TOP VIEW



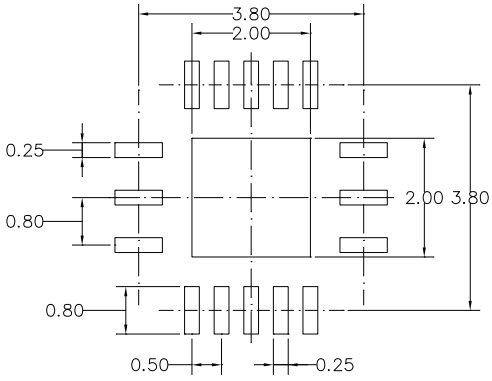
BOTTOM VIEW



SIDE VIEW



SECTION A-A

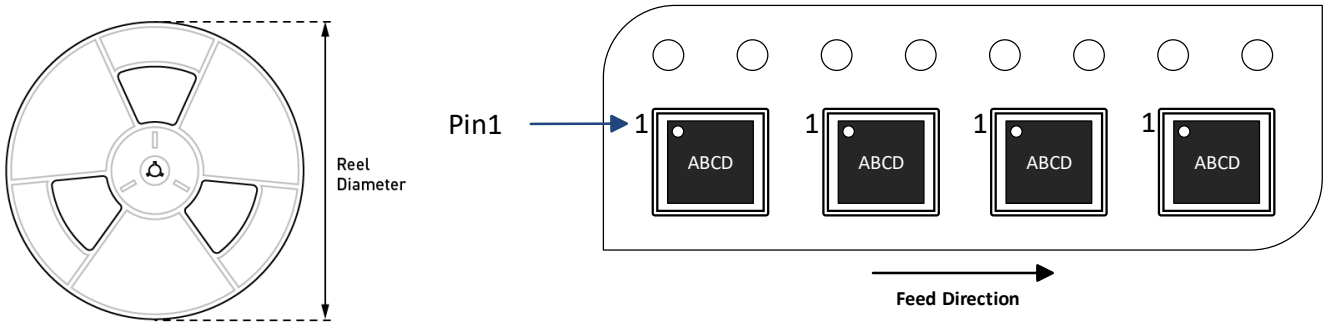


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) DRAWING REFERENCE TO JEDEC MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity /Reel	Quantity /Tube	Quantity /Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ2024AGRE-xxxx-AEC1-Z	QFN-16 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/23/2023	Initial Release	-