MPQ2019A

40V, 300mA, Low Quiescent Current, Linear Regulator with Adjustable Output, AEC-Q100 Qualified

DESCRIPTION

The MPQ2019A is a low-power linear regulator that supplies power to systems with high-voltage batteries. The device has a wide 3V to 40V input voltage (V_{IN}) range, low dropout voltage, and low quiescent supply current. The low quiescent current and low dropout voltage allow for operation at extremely low power levels. This makes the MPQ2019A well-suited for low-power microcontrollers (MCUs) and battery-powered equipment.

The MPQ2019A provides an adjustable output that can be set between 1.25V and 36V.

The MPQ2019A includes thermal shutdown and current limiting fault protection. The output current (I_{OUT}) is limited internally, and the device is protected against short circuit, overload, and over-temperature (OT) conditions.

The MPQ2019A is available in an SOIC-8EP package.

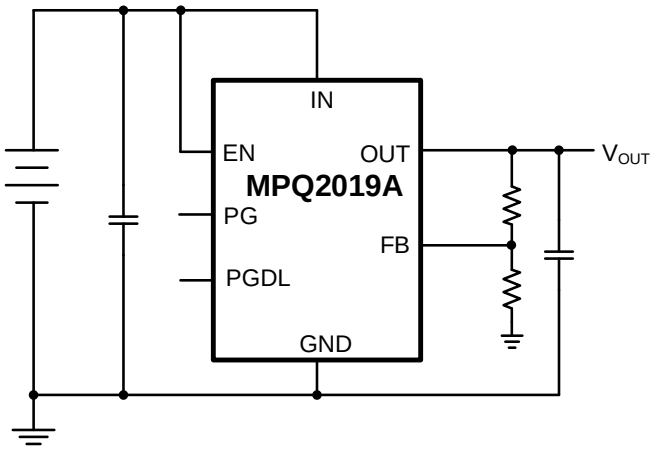
FEATURES

- 3V to 40V Input Voltage (V_{IN}) Range
- 10µA Quiescent Supply Current
- Stable with Lower-Value (>0.47µF) Ceramic Output Capacitors
- 300mA Specified Current
- Adjustable Output (1.25V to 36V)
- Output ±2% Accuracy at Full Temperature
- Specified Current Limit (I_{LIMIT})
- Power Good (I_Q)
- Configurable PG Delay
- Thermal Shutdown and Short-Circuit Protection (SCP)
- -40°C to +150°C Specified Junction Temperature (T_J) Range
- Available in an SOIC-8EP Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Industrial/Automotive Applications
- Portable/Battery-Powered Equipment
- Ultra-Low Power Microcontrollers (MCUs)
- Cellular Handsets
- Medical Imaging

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ2019AGN-AEC1	SOIC8-EP	*See Below*	2a

* For Tape & Reel, add suffix -Z (e.g. MPQ2019AGN-AEC1-Z).

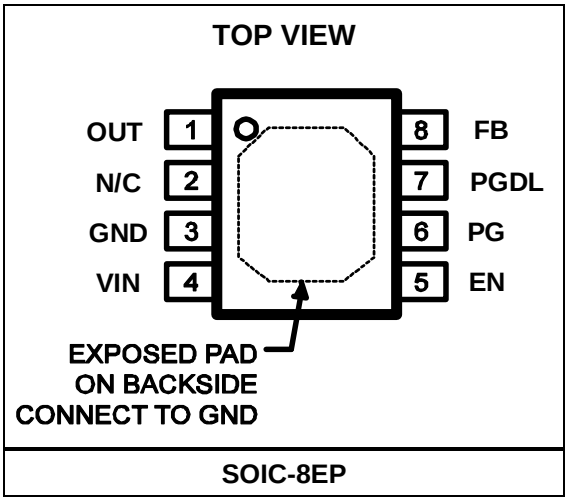
** Moisture Sensitivity Level Rating

TOP MARKING

MP2019A
LLLLLLLL
MPSYWW

MP2019A: Part number
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

PACKAGE REFERENCE



SOIC-8EP

PIN FUNCTIONS

Pin #	Name	Description
1	OUT	**Regulated output voltage.** For stability, place a low-value ceramic capacitor (≥0.47µF) on the output.
2	N/C	**Not connected.**
3	GND	**Ground.** Connect the exposed pad and the GND pin to the same ground plane.
4	IN	**Input voltage.** Connect a 3V to 40V supply to the IN pin.
5	EN	**Regulator on/off control input.** Pull the EN pin to logic high to turn the regulator on; pull EN to logic low to turn it off. Connect EN to IN for automatic start-up.
6	PG	**Power good.** Float the PG pin if not used.
7	PGDL	**Configurable power good delay time.** Float the PGDL pin if not used.
8	FB	**Feedback input for the adjustable output.** The FB pin is regulated to 1.25V nominally. FB is used to set the output voltage (V_{OUT}).

ABSOLUTE MAXIMUM RATINGS (1)

IN, EN .....-0.3V to +42V
OUT .....-0.3V to +40V
PG .....-0.3V to +15V
PGDL, FB .....-0.3V to +6V
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C
Continuous power dissipation (T_A = 25°C) (2)
SOIC-8EP 2.5W

ESD Ratings (3)

Human body model (HBM).....4kV
Machine model (MM).....200V

Recommended Operating Conditions (4)

Input voltage (V_{IN}) .....3V to 40V
Output voltage (V_{OUT}) .....1.25V to 36V
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance (5) θ_{JA} θ_{JC}

SOIC-8EP	50	10... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Devices are ESD sensitive; handle with precaution.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on a JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 13.5V, T_A = -40°C to +125°C, T_A ≤ T_J ≤ 150°C, typical values are at T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input voltage	V_{IN}		3		40	V
Output voltage	V_{OUT}		1.25		36	V
Ground (GND) current	I_{GND}	0 < I_{LOAD} < 1mA		10	15	µA
		1mA < I_{LOAD} < 30mA		15	21	µA
		30mA < I_{LOAD} < 300mA		65	95	µA
Shutdown supply current	I_{SD}	V_{EN} = 0V			1	µA
Load current limit	I_{LIMIT}	V_{IN} = 7V, V_{OUT} = 0V, T_A = 25°C	600	1000	1350	mA
Feedback (FB) voltage	V_{FB}	FB = OUT, I_{LOAD} = 5mA	1.225	1.25	1.275	V
Dropout voltage (6)	$V_{DROPOUT}$	V_{OUT} = 5V, I_{LOAD} = 150mA		200	400	mV
		T_A = +25°C, V_{OUT}=5V, I_{LOAD} = 300mA		420	550	mV
FB input current	I_{FB}	V_{FB} = 1.3V			50	nA
Line regulation		V_{IN} = 3V to 40V, I_{LOAD} = 5mA, V_{OUT} = V_{FB}	-10	1	+10	mV
Load regulation		I_{LOAD} = 5mA to 300mA, V_{OUT} = 5V, T_A = 25°C		1	15	mV
V_{OUT} PSRR (7)		100Hz, C_{OUT} = 10µF, I_{LOAD} = 10mA		57		dB
		1kHz, C_{OUT} = 10µF, I_{LOAD} = 10mA		45		
		100kHz, C_{OUT} = 10µF, I_{LOAD} = 10mA		51		
Start-up response time		R_{LOAD} = 500Ω, V_{OUT} = 5V, C_{OUT} = 22µF, V_{OUT} from 10% to 90%		0.9	1.5	ms
Enable (EN) voltage (V_{EN}) threshold	V_{EN_LOW}				0.3	V
	V_{EN_HIGH}		1.8			V
EN input current		EN = 0V or 15V		0.1	0.5	µA
Power good (PG) rising threshold			89	93	97	% of V_{FB}
PG rising threshold hysteresis				5		% of V_{FB}
PG low voltage		Sink 1mA Current		0.1	0.4	V
PG leakage current		V_{PG} = 5V			1	µA
PGDL charging current		V_{PGDL} = 1V	3	5.5	9	µA
PGDL rising threshold	V_{PGDL_RISING}		1.4	1.7	2	V
PGDL falling threshold	$V_{PGDL\_FALLING}$		0.2	0.4	0.7	V
PG delay time		C_{PGDL} = 47nF	5	10	15	ms
PG reaction time		C_{PGDL} = 47nF		0.5	2	µs
Thermal shutdown (7)	T_{SD}			165		°C
Thermal shutdown hysteresis (7)	ΔT_{SD}			30		°C

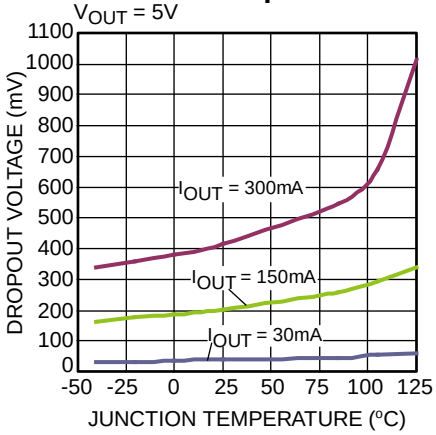
Notes:

6) The dropout voltage ($V_{DROPOUT}$) is measured when the output voltage (V_{OUT}) has dropped 100mV below the nominal value obtained at V_{IN} = 13.5V.

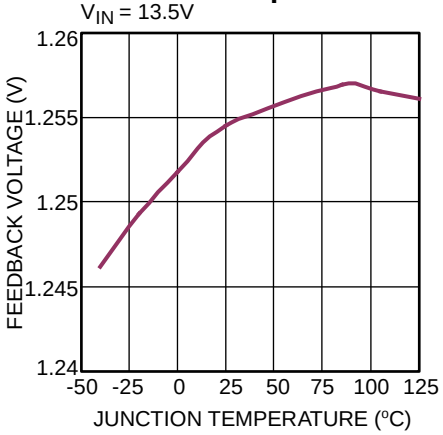
7) Derived from bench characterization. Not tested in production.

TYPICAL PERFORMANCE CHARACTERISTICS

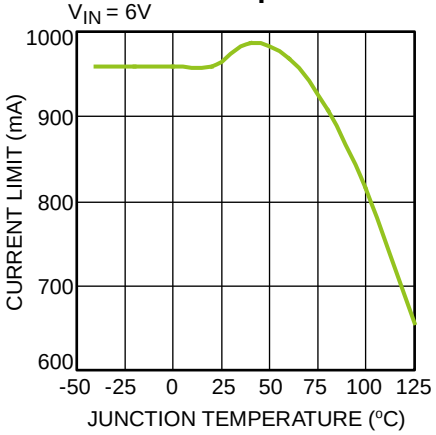
Dropout Voltage vs. Junction Temperature



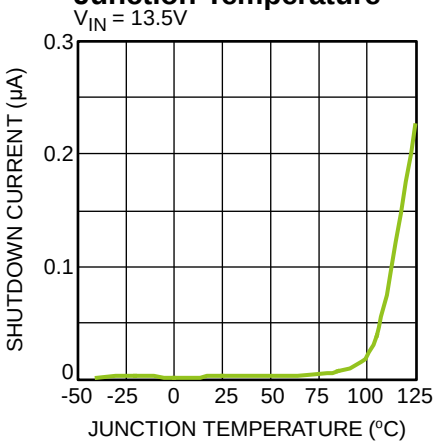
Feedback Voltage vs. Junction Temperature



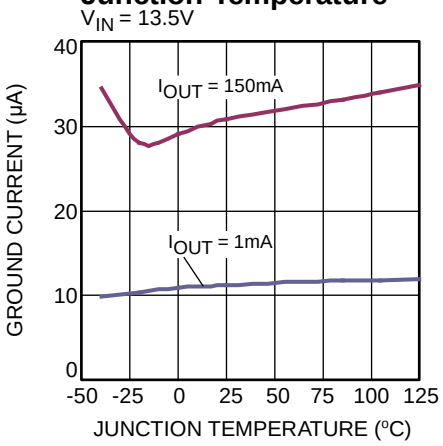
Current Limit vs. Junction Temperature



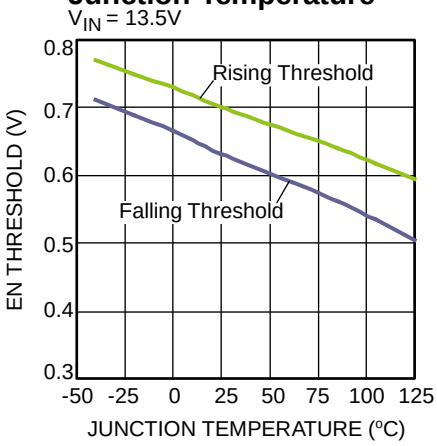
Shutdown Current vs. Junction Temperature



GND Current vs. Junction Temperature



EN Threshold vs. Junction Temperature

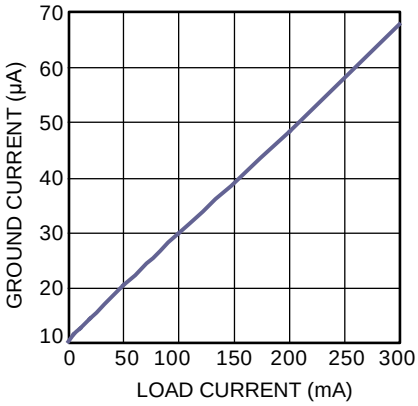


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

C_{IN} = 1µF, C_{OUT} = 22µF, V_{OUT} = 5V, T_A = 25°C, unless otherwise noted.

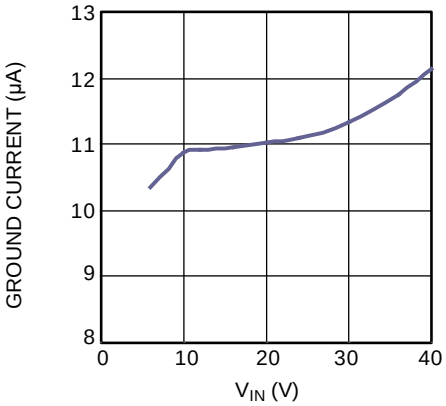
Ground Current vs. Load Current

V_{IN} = 6V



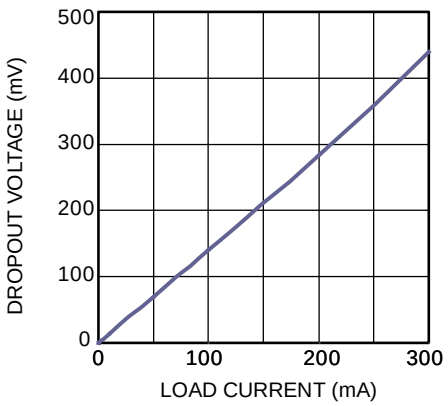
Ground Current vs. V_{IN}

I_{OUT} = 0mA

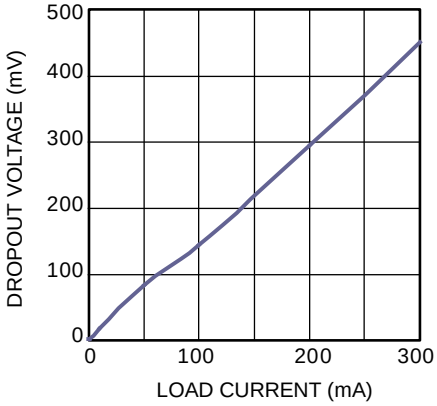


Dropout Voltage vs. Load Current

V_{OUT} = 3.3V

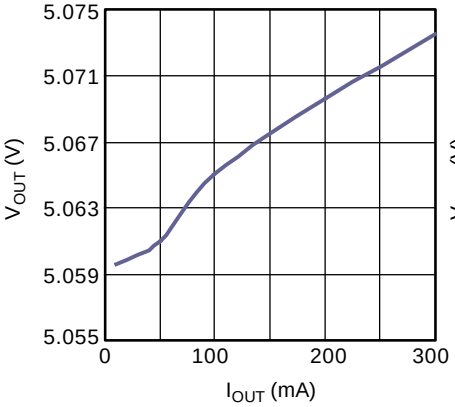


Dropout Voltage vs. Load Current

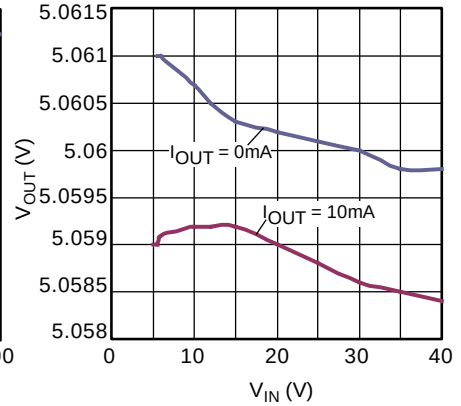


V_{OUT} vs. I_{OUT}

V_{IN} = 6V

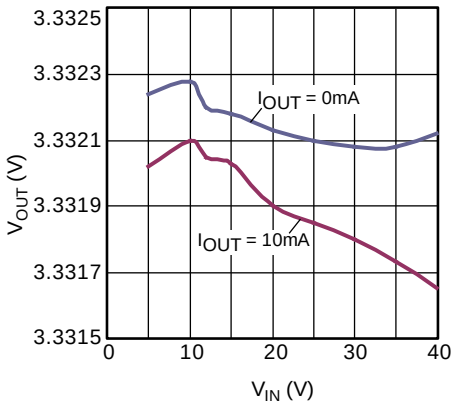


V_{OUT} vs. V_{IN}



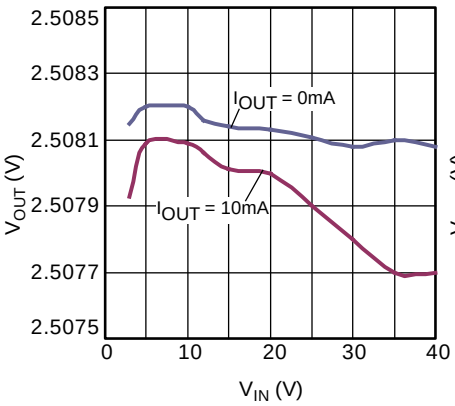
V_{OUT} vs. V_{IN}

V_{OUT} = 3.3V



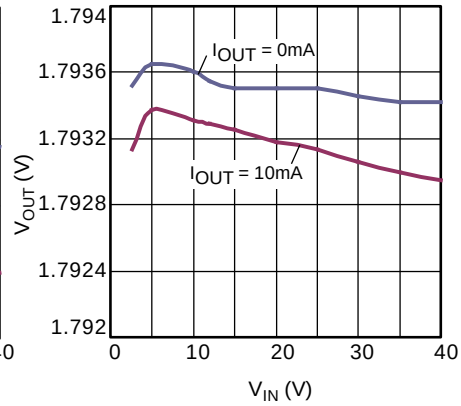
V_{OUT} vs. V_{IN}

V_{OUT} = 2.5V



V_{OUT} vs. V_{IN}

V_{OUT} = 1.8V

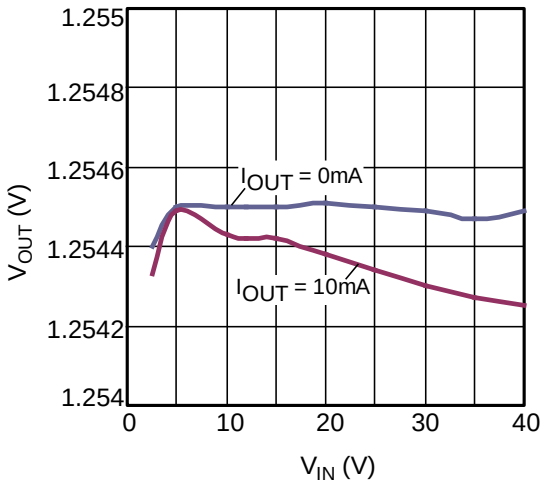


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

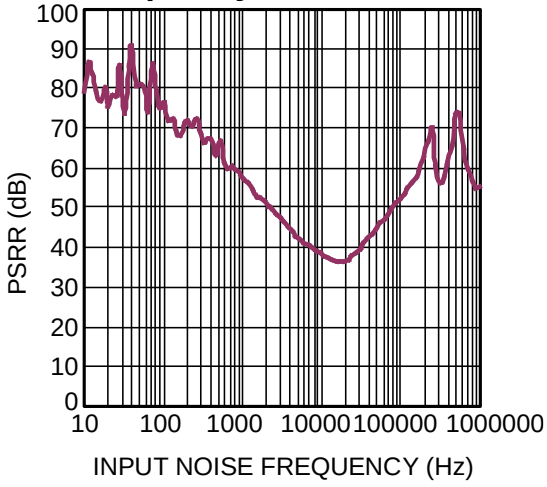
C_{IN} = 1µF, C_{OUT} = 22µF, V_{OUT} = 5V, T_A = 25°C, unless otherwise noted.

V_{OUT} vs. V_{IN}

V_{OUT} = 1.25V



PSRR vs. Input Noise Frequency

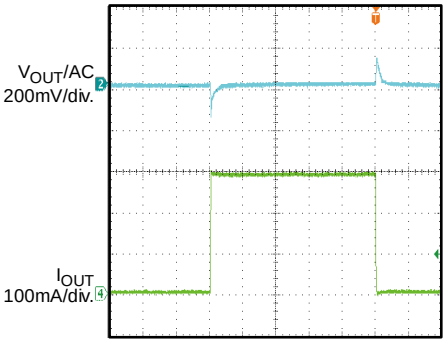


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

C_{IN} = 1µF, C_{OUT} = 22µF, V_{OUT} = 5V, T_A = 25°C, unless otherwise noted.

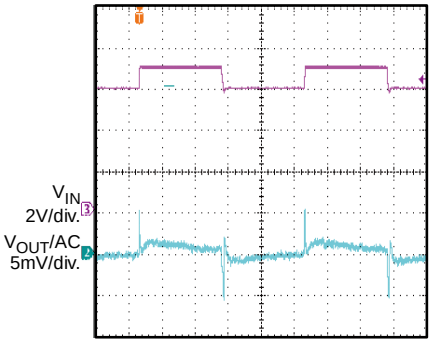
Load Transient

V_{IN} = 12V, I_{OUT} = 300mA



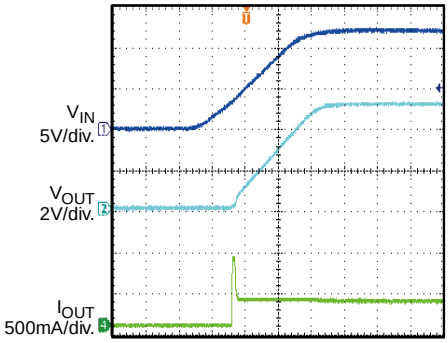
Line Transient

V_{IN} = 6V to 7V, I_{OUT} = 300mA



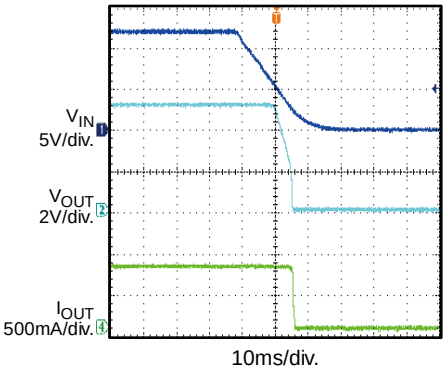
Start-Up through V_{IN}

V_{IN} = 12V, I_{OUT} = 300mA



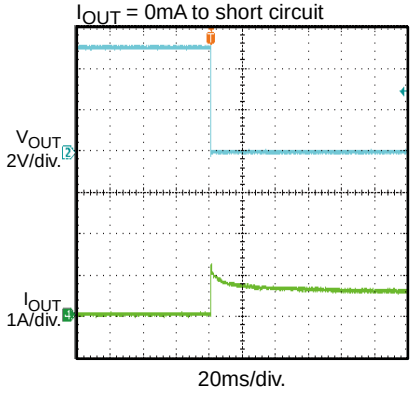
Shutdown through V_{IN}

V_{IN} = 12V, I_{OUT} = 300mA



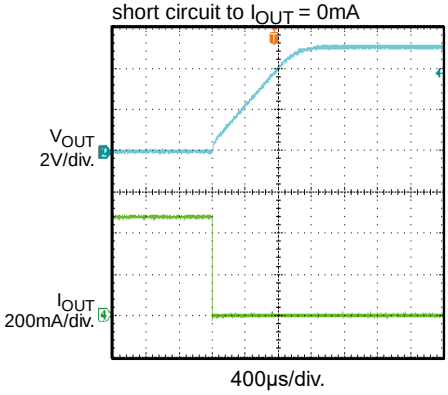
SCP Entry

V_{IN} = 12V,
I_{OUT} = 0mA to short circuit



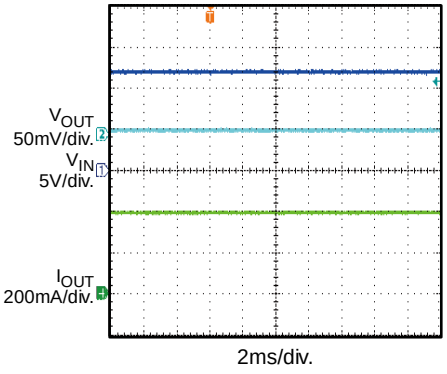
SCP Recovery

V_{IN} = 12V,
short circuit to I_{OUT} = 0mA



SCP Steady State

V_{IN} = 12V



FUNCTIONAL BLOCK DIAGRAM

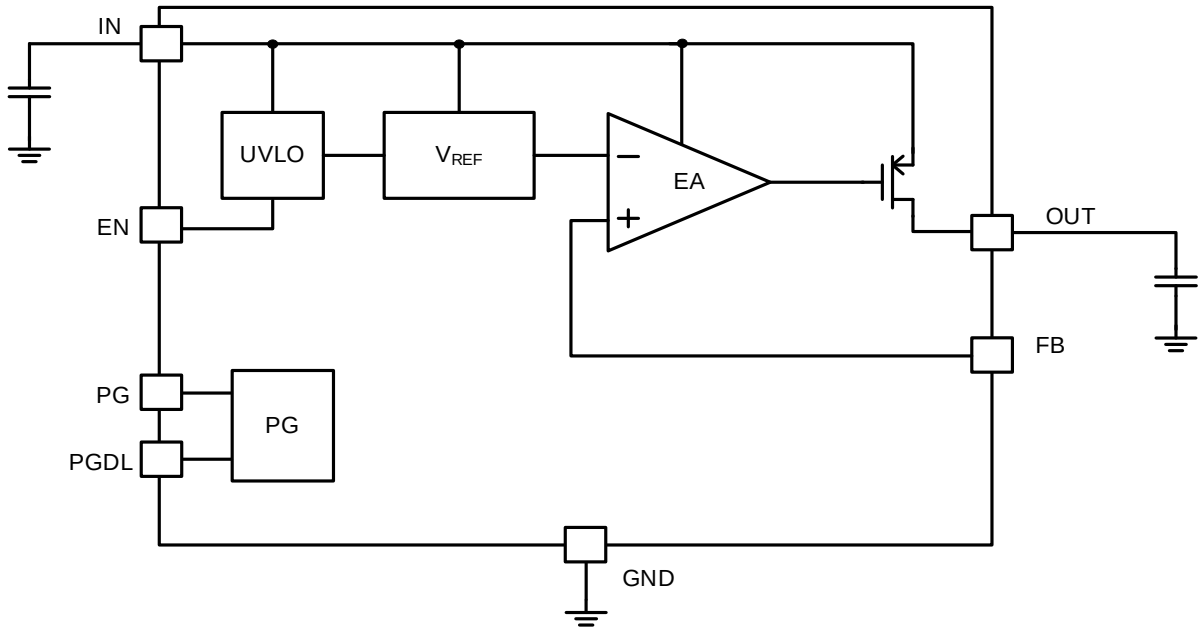


Figure 1: Functional Block Diagram

OPERATION

The MPQ2019A is a linear regulator that supplies power to systems with high-voltage batteries. The device includes a wide 3V to 40V input voltage (V_{IN}) range, low dropout voltage, and a low quiescent supply current (see Figure 1 on page 9).

The MPQ2019A provides an adjustable output that can be set between 1.25V and 36V with a simple resistor divider. With external feedback (FB), the user can set the output voltage (V_{OUT}) with an external resistor divider. The typical FB pin voltage is 1.25V.

The MPQ2019A enters shutdown mode when EN is low. In shutdown mode, the pass transistor, control circuitry, reference, and all biases turn off. This reduces the supply current to <1μA. Connect EN to IN for automatic start-up.

The output current (I_{OUT}) is limited internally, and the device is protected against short-circuit, overload, and over-temperature (OT) conditions (see Figure 2 on page 11).

The peak I_{OUT} is limited to about 1000mA; however, the recommended continuous I_{OUT} is 300mA.

When the junction temperature (T_J) exceeds its limit, the thermal sensor sends a signal to the control logic that shuts down the MPQ2019A. The device restarts once the temperature has sufficiently cooled.

The maximum I_{OUT} is a function of the package's maximum power dissipation for a given temperature.

The maximum power dissipation is dependent on the thermal resistance of the case and the circuit board, the temperature difference between the die junction and the ambient air, and the rate of air flow. GND and the exposed pad should be connected to the ground plane to ensure proper dissipation.

The power good (PG) pin is the open drain of an internal MOSFET. Connect PG to an external voltage source (<15V) using a resistor (e.g. 100kΩ). After the FB voltage (V_{FB}) reaches 93% of the nominal value, the MOSFET turns off and the PG pin is pulled high by V_{OUT} or the external voltage source. When V_{FB} drops to 88% of the nominal value, PG is pulled down to GND.

There is a delay time before PG asserts high. The delay time can be configured by the PGDL capacitor (C_{PGDL}). C_{PGDL} can be calculated with Equation (1):

$$C_{PGDL}(nF) = \frac{t_{PGDL}(ms) \times I_{PGDL}(\mu A)}{V_{PGDL\_RISING}(V)} \quad (1)$$

Where t_{PGDL} is the desired delay time before PG asserts high, I_{PGDL} is the PGDL charging current, and V_{PGDL_RISING} is 1.7V.

Figure 2 on page 11 shows the PG timing.

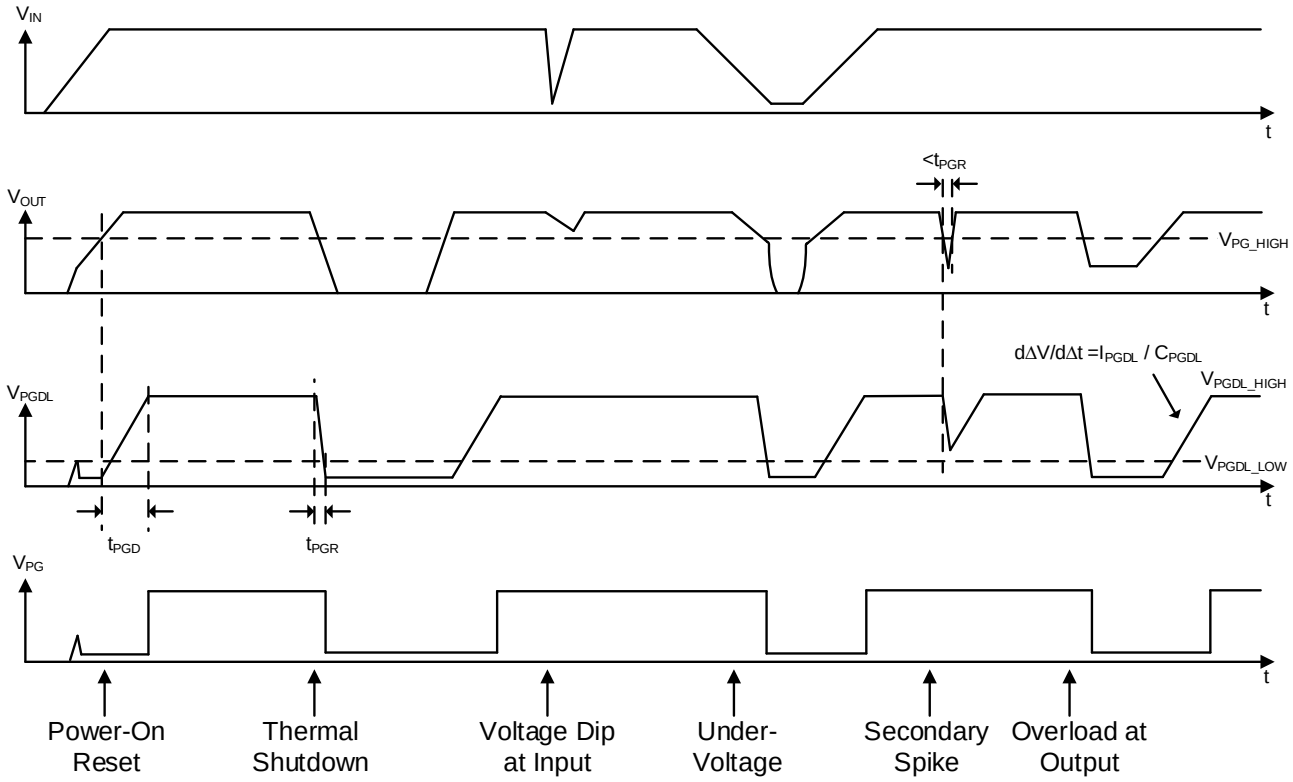


Figure 2: Power Good Timing

APPLICATION INFORMATION

Setting the Output Voltage

Set V_{OUT} using the FB resistor divider (see Figure 3).

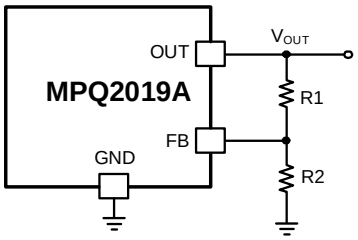


Figure 3. Feedback Resistor Divider to Set V_{OUT}

Choose R2 to be 1MΩ to maintain a 1.215μA minimum load. R1 can be calculated with Equation (2):

$$R1 = R2 \times \left(\frac{V_{OUT}}{1.25V} - 1 \right) \quad (2)$$

Enable (EN) Control

EN is a digital control pin that turns the regulator on and off. When EN is pulled below 0.3V, the chip shuts down. When EN is pulled above 1.8V, the chip starts up. If this function is not used, EN can be connected directly to V_{IN}.

Selecting the Input Capacitor

For efficient operation, place a 1μF to 10μF ceramic capacitor (C1) with X5R or X7R dielectrics between the IN and GND pins. Larger capacitances in this range improve line transient response.

Selecting the Output Capacitor

For stable operation, use a 1μF to 22μF ceramic capacitor (C2) with X5R or X7R dielectrics. Larger capacitances in this range improve load transient response and reduce noise. Output capacitors with other dielectrics may be used, but are not recommended, as their capacitance can deviate greatly from their rated OT value.

To improve load transient response, add a small, 2.2nF, ceramic feed-forward capacitor with X5R, X7R, or Y5V dielectrics in parallel with R1. The feed-forward capacitor is not required for stable operation.

Output Noise

The MPQ2019A exhibits noise on the output during normal operation. This noise is negligible for most applications. However, in applications that include analog-to-digital converters (ADCs) of more than 12 bits, consider the ADC's power supply rejection specifications. The feed-forward capacitor (C2) across R1 can significantly reduce output noise.

External Reverse Voltage Protection

In some situations (e.g. a backup battery is connected as the MPQ2019A's load), V_{OUT} may be held at a higher voltage while the input is pulled to ground, pulled to an intermediate voltage, or is floating. In this scenario, V_{OUT} exceeds V_{IN}.

Since the MPQ2019A's P-channel MOSFET pass element has a body diode, a current conducts from the output to input, and it is not limited internally. The MPQ2019A may be damaged by this unlimited reverse current. To prevent damage, it is recommended to place an external diode at the input (see Figure 4).

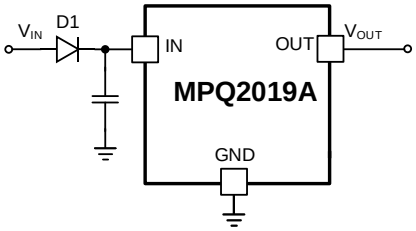


Figure 4: External Reverse Voltage Protection

Design Example

Figure 5 shows a design example following the application guidelines for V_{OUT} = 3.3V with a feed-forward capacitor.

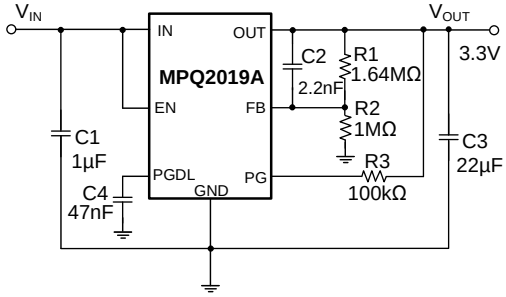


Figure 5: Design Example

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation, and to achieve good regulation, ripple rejection, transient response, and thermal performance. It is recommended to duplicate the EVB layout for optimal performance. For the best results, refer to Figure 6 and Figure 7, and follow the guidelines below:

1. Place the ceramic input bypass capacitors close to the IN pin.
2. Place the ceramic output bypass capacitors close to the OUT pin.
3. Ensure that all feedback connections are short and direct.
4. Place the feedback resistors and compensation components as close to the chip as possible.
5. Connect IN, OUT, and GND to a large copper area to cool the chip, and to improve thermal performance and long-term reliability. This is particularly important for GND.

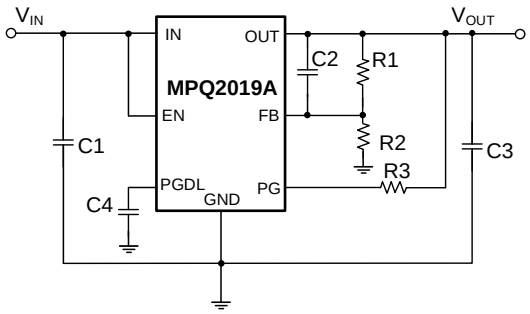
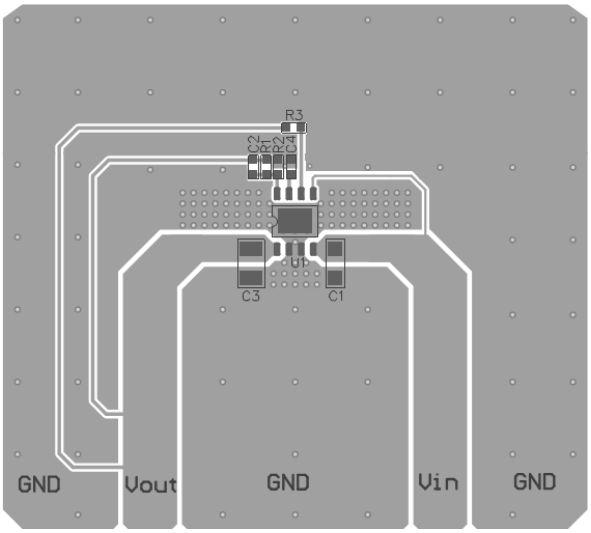
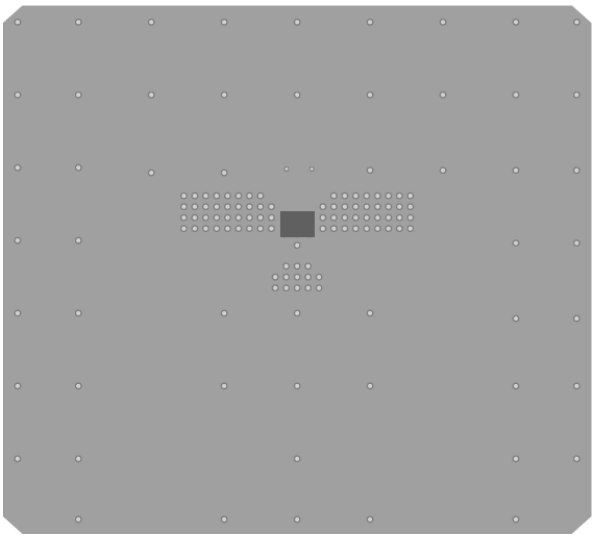


Figure 6: Typical Application Circuit



Top Layer



Bottom Layer

Figure 7: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

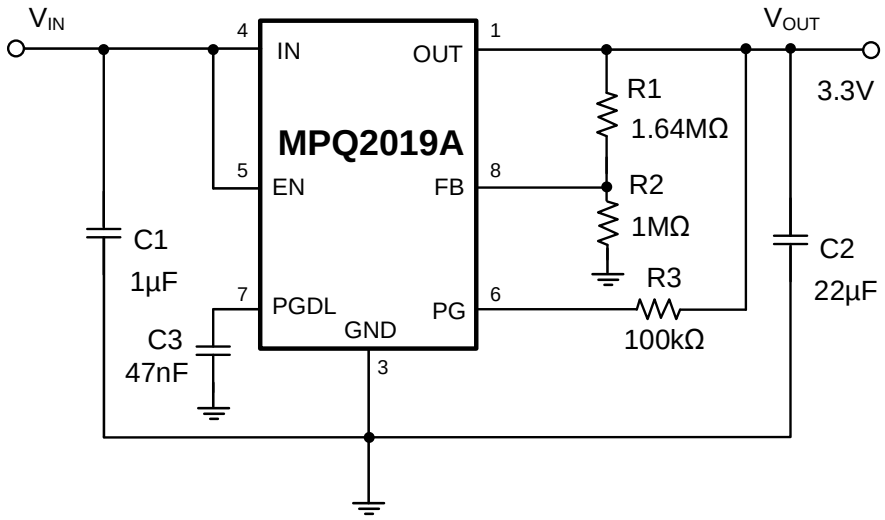


Figure 8: Typical Application Circuit (3.3V Output)

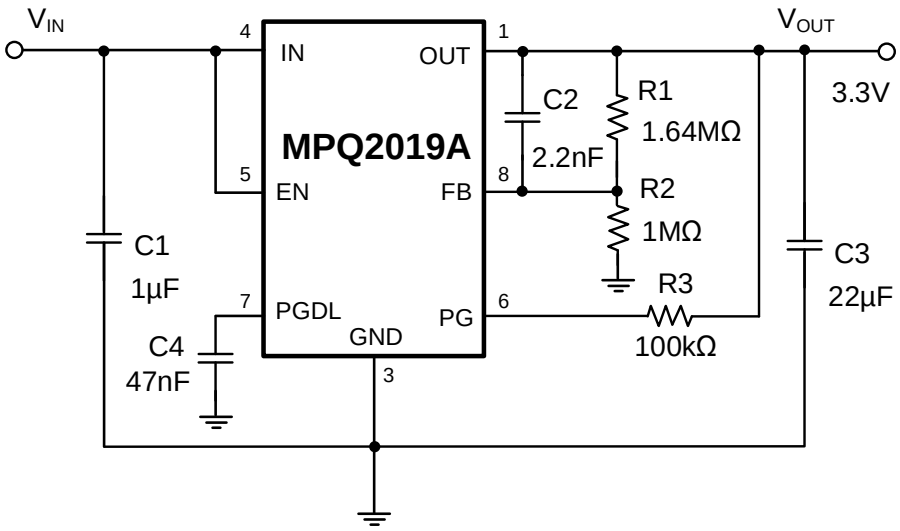
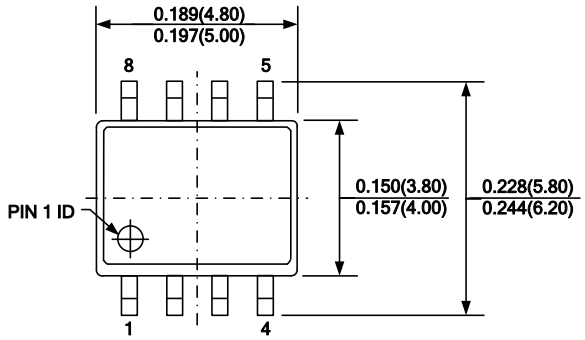


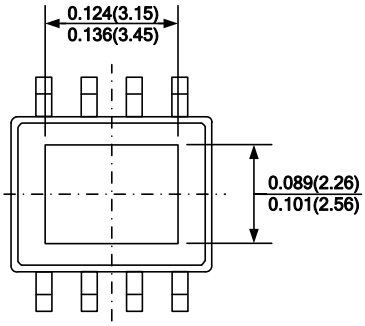
Figure 9: Typical Application Circuit (3.3V Output with Feed-Forward Capacitor)

PACKAGE INFORMATION

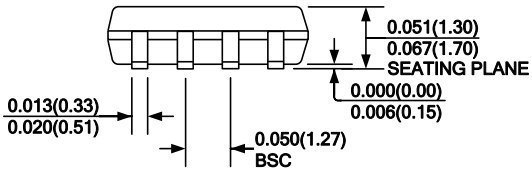
SOIC-8EP



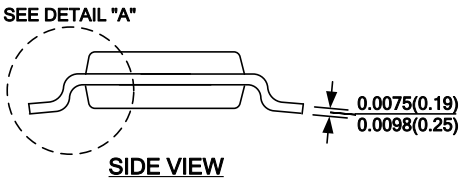
TOP VIEW



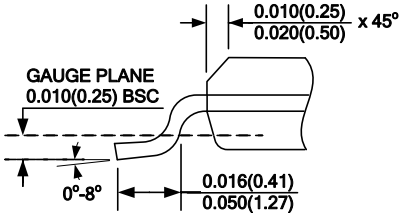
BOTTOM VIEW



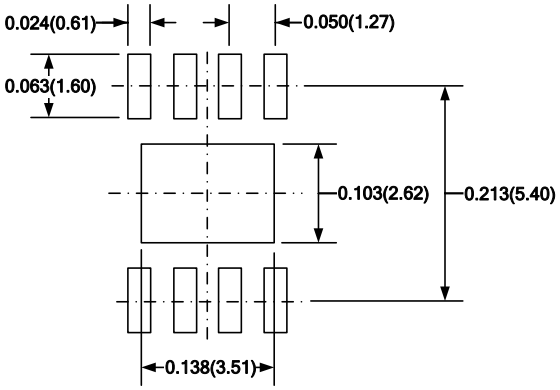
FRONT VIEW



SIDE VIEW



DETAIL "A"

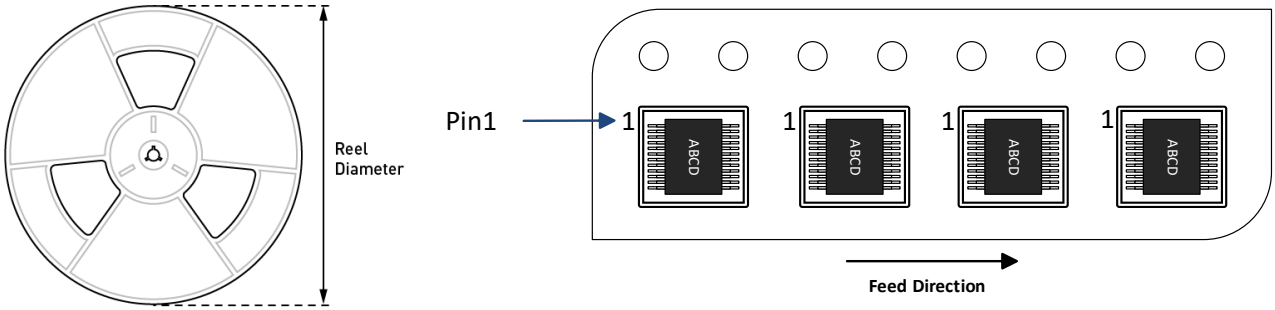


RECOMMENDED LAND PATTERN

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ2019AGN-AEC1-Z	SOIC8-EP	2500	100	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/19/2023	Initial Release	-