



The Future of Analog IC Technology®

# MPQ20056

Low-Noise, High-PSRR, 250mA  
Linear Regulator  
AEC-Q100 Qualified

## DESCRIPTION

The MPQ20056 is a low-dropout linear regulator that supplies up to 250mA current with a 100mV dropout voltage and can operate from 2.5V to 5.5V input. The output voltage is preset at 1.8V, 2.5V, 3.3V or adjustable for the two different packages. An external resistor divider can adjust the output voltage from 0.8V to 5V.

An internal PMOS pass element allows for a low 150µA ground current, making the MPQ20056 suitable for battery-powered devices. Other features include low-power shutdown, short-circuit protection, and thermal protection. The MPQ20056 is available in a 2mm×2mm 8-pin QFN and a 5-pin TSOT23-5 packages.

## FEATURES

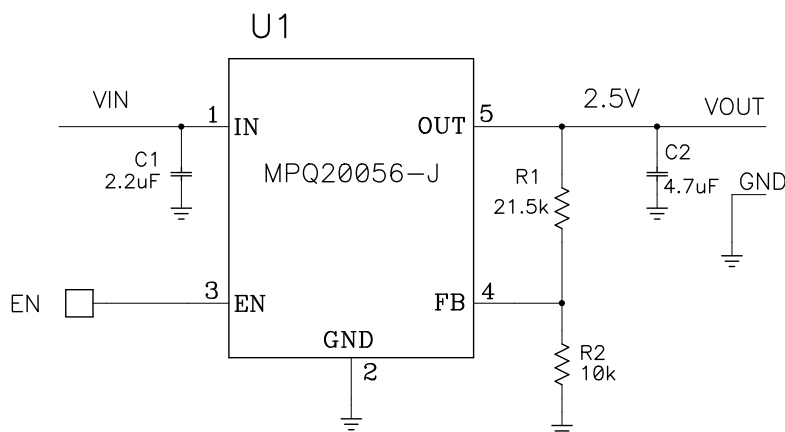
- Guaranteed Industrial/Automotive Temp. Range Limits
- Up to 250mA Output Current
- Low 100mV Dropout at 250mA
- Low 150µA Ground Current
- Low Noise: 13µV<sub>RMS</sub> typical (10Hz to 100kHz)
- 63dB PSRR @1kHz
- Stable with Ceramic Capacitor
- Excellent Load/Line Transient Response
- Current Limiting and Thermal Protection
- Fixed output voltage 1.8V, 2.5V, and 3.3V.
- Adjustable Output Voltage from 0.8V to 5V Using an External Resistor Divider
- Available in AEC-Q100 Qualified Grade

## APPLICATIONS

- Notebook Computers
- Cordless Phones
- Cellular Phones
- Wireless Communication Equipment
- Hand-Held Instruments

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## TYPICAL APPLICATION

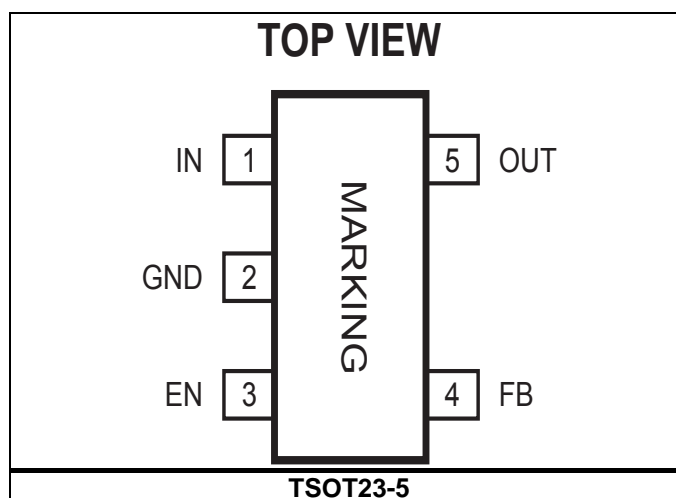
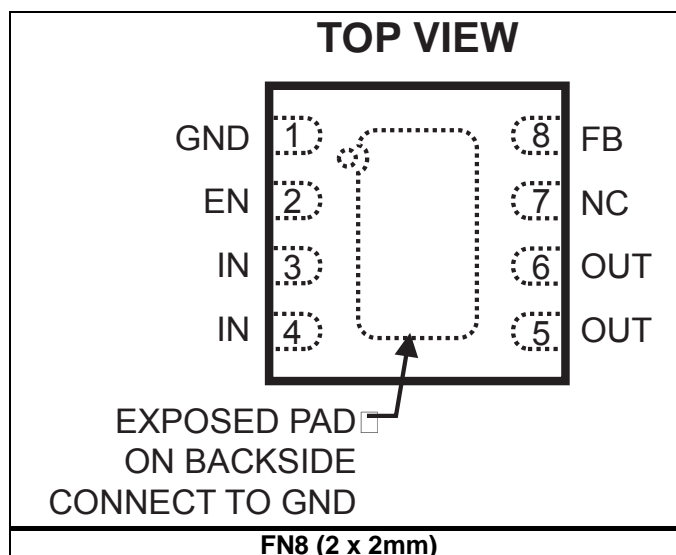


### ORDERING INFORMATION

Part Number*	Package	Top Marking
MPQ20056GG-18	QFN8(2x2mm)	BK
MPQ20056GG-18-AEC1	QFN8(2x2mm)	BK
MPQ20056GJ-25	TSOT23-5	ALA
MPQ20056GJ-25-AEC1	TSOT23-5	ALA
MPQ20056GJ-33	TSOT23-5	AFT
MPQ20056GJ-33-AEC1	TSOT23-5	AFT
MPQ20056GG-33	QFN8(2x2mm)	BV
MPQ20056GG-33-AEC1	QFN8(2x2mm)	BV
MPQ20056GJ	TSOT23-5	AWZ
MPQ20056GJ-AEC1	TSOT23-5	AWZ

\* For Tape & Reel, add suffix -Z (e.g. MPQ20056GG-18-Z)

### PACKAGE REFERENCE



**ABSOLUTE MAXIMUM RATINGS (1)**

VIN, EN, FB to GND .....	-0.3V to +6V
OUT to GND.....	-0.5V to (VIN + 0.5V)
Continuous Power Dissipation .....	(TA=25°C) (2)
QFN8 (2x2mm) .....	1.6W
TSOT23-5 .....	0.57W
Junction Temperature.....	150°C
Storage Temperature Range .....	-65°C to 150°C
Lead Temperature (Soldering, 10sec).....	260°C

**ESD SUSCEPTIBILITY(3)**

HBM (Human Body Mode).....	2kV
MM (Machine Mode) .....	200V

**Recommended Operating Conditions (4)**

Supply Input Voltage.....	2.5V to 5.5V
Enable Input Voltage .....	0V to 5.5V
Operating Junction Temp. (TJ).	-40°C to +125°C

<b>Thermal Resistance (5)</b>	<b><math>\theta_{JA}</math></b>	<b><math>\theta_{JC}</math></b>	
QFN8 (2x2mm).....	80	16...	°C/W
TSOT23-5 .....	220	110..	°C/W

**Notes:**

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature TJ (MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature TA. The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D (MAX) = (T_J (MAX) - T_A) / \theta_{JA}$ . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the device will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) Devices are ESD sensitive. Handling precaution recommended.
- 4) The device is not guaranteed to function outside of its operating conditions.
- 5) Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

$V_{IN}=V_{OUT}+0.5V$  or  $V_{IN}=2.5V$ ,  $EN=V_{IN}$ ,  $V_{OUT}=1.8V$  or  $3.3V$ .  $T_J=-40^{\circ}C$  to  $+125^{\circ}C$ , Typical values are at  $T_J=25^{\circ}C$ , unless otherwise specified.

Parameter	Condition	Min	Typ	Max	Units	
Input Voltage		2.5		5.5	V	
Input Under-Voltage Lockout	$V_{IN}$ rising, $V_{OUT}=1.8V$	1.95		2.3	V	
Hysteresis of UVLO			160		mV	
FB Voltage	$V_{OUT}=0.8V$ , $I_{OUT}=1mA$ , $T_J=25^{\circ}C$	0.784	0.8	0.816	V	
	$V_{OUT}=0.8V$ , $I_{OUT}=1mA$ , $-40^{\circ}C \leq T_J \leq +125^{\circ}C$	0.776		0.824	V	
Output Voltage Accuracy	$I_{OUT}=1mA$ , $T_J=25^{\circ}C$	-2		2	%	
	$I_{OUT}=1mA$ , $-40^{\circ}C \leq T_J \leq 125^{\circ}C$	-3		3	%	
Maximum Output Current	Continuous	250			mA	
Short-Circuit Current Limit	$V_{OUT}=0$ , $V_{IN} \geq 2.5V$	350	550	850	mA	
In-Regulation Current Limit	$V_{OUT}$ within 4% of normal output voltage $V_{IN}=5.5V$	300	550	800	mA	
Ground Current	$I_{OUT}=0.1mA$		150	250	$\mu A$	
	$I_{OUT}=250mA$		220	330	$\mu A$	
Dropout Voltage <sup>(6)</sup>	$I_{OUT}=250mA$ , $V_{OUT}=3.3V$ , $T_J=25^{\circ}C$ $-40^{\circ}C \leq T_J \leq 125^{\circ}C$		100	150	mV	
			100	200		
Line Regulation <sup>(7)</sup>	$V_{IN}$ from $V_{OUT}+0.5V$ or $2.5V$ to $5.5V$ , $I_{OUT}=100mA$ ,	-0.15		0.15	%/V	
Load Regulation@Vtyp <sup>(8)</sup>	$I_{OUT}$ from 100mA to 250mA	$V_{OUT}=1.8V, 3.3V$	-0.3	0.3	%	
		$V_{OUT}=2.5V$	-0.4	0.4		
Output-Voltage Noise <sup>(9)</sup>	$I_{OUT}=100mA$ , f ranges from 10Hz to 100kHz	$V_{OUT}=1.8V$		20	$\mu V_{RMS}$	
		$V_{OUT}=3.3V$		35		
PSRR <sup>(9)</sup>	$V_{OUT} = 1.8V, 2.5V, 3.3V$ $I_{OUT} = 250mA$	$f=100Hz$		65	dB	
		$f=1kHz$		63		
		$f=10kHz$		63		
		$f=1MHz$		33		
Shutdown Supply Current	$V_{IN}=+5.5V$	$T_J=25^{\circ}C$		0.1	0.3	$\mu A$
		$-40^{\circ}C \leq T_J \leq 125^{\circ}C$		10	30	
EN Pin Current , Enabled	$V_{IN}=V_{EN}=+5.5V$		0.1	0.3	$\mu A$	
Startup Time	$C_{OUT}=4.7\mu F$ , $V_{OUT}=10\%$ to $90\%V_{OUT(NOM)}$	$V_{OUT}=1.8V$	100		300	$\mu s$
		$V_{OUT}=3.3V, 2.5V$	100		450	
EN PIN Threshold	EN Logic High		1.5		V	
	EN Logic Low			0.4		
Thermal Shutdown <sup>(9)</sup>			150		$^{\circ}C$	
Thermal Shutdown Hysteresis <sup>(9)</sup>			20		$^{\circ}C$	

**Notes:**

6) Dropout Voltage is defined as the input to output differential when the output voltage drops 100mV below its nominal value.

$$7) \text{ Line Regulation} = \frac{V_{OUT[V_{IN(MAX)}]} - V_{OUT[V_{IN(MIN)}]}}{[V_{IN(MAX)} - V_{IN(MIN)}] \times V_{OUT(NOM)}} \times (\% / V)$$

$$8) \text{ Load Regulation} = \frac{V_{OUT[I_{OUT(MAX)}]} - V_{OUT[I_{OUT(MIN)}]}}{V_{OUT(NOM)}} \times (\%)$$

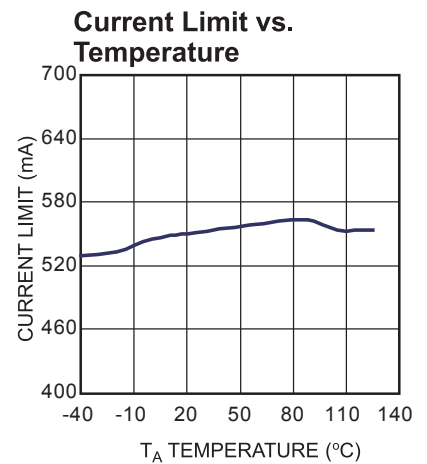
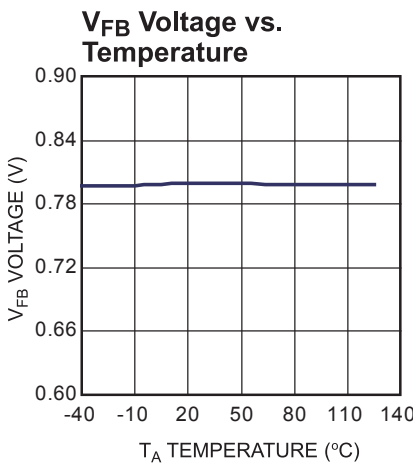
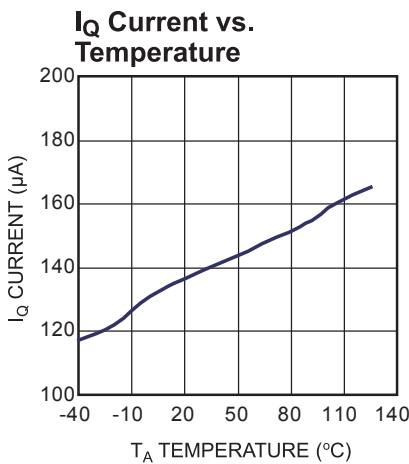
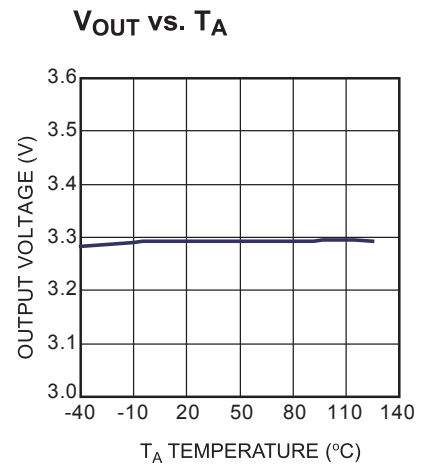
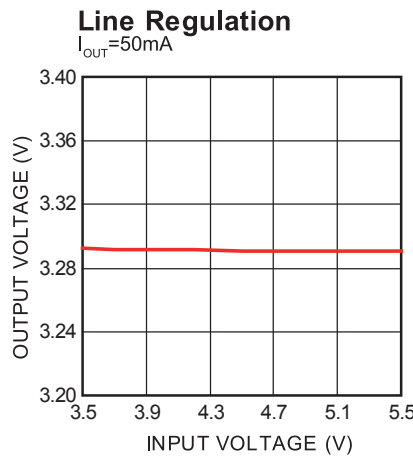
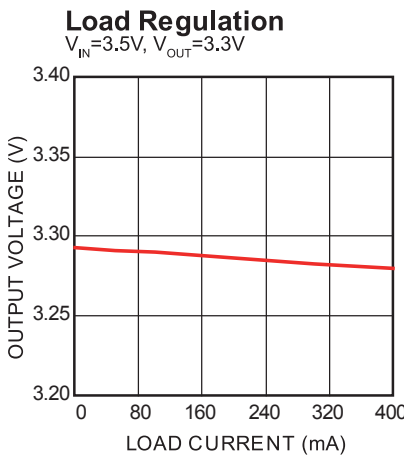
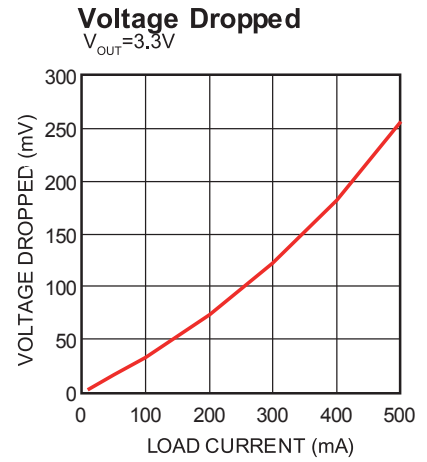
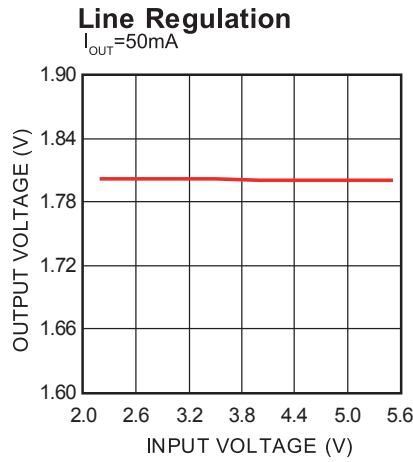
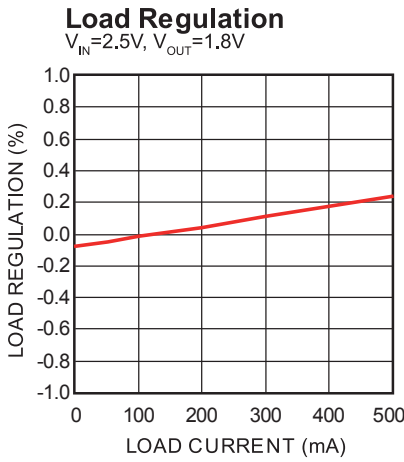
9) Design guarantee, no test in production

## PIN FUNCTIONS

Pin # QFN8 (2x2mm)	Pin # TSOT23-5	Name	Pin Function
1, Exposed Pad	2	GND	Ground. Connect exposed pad to GND plane for optimal thermal performance.
2	3	EN	Regulator Enable Control Input. Drive EN above 1.5V to turn on the MPQ20056. Drive EN below 0.4V to turn it off. Do not float the EN pin.
3, 4	1	VIN	Regulator Input. Supply voltage ranges from 2.5V to 5.5V. Bypass with a 2.2 $\mu$ F capacitor. These pins must be externally connected for proper operation even if they are internally connected.
5, 6	5	VOUT	Regulator Output. Bypass with a standard 4.7 $\mu$ F ceramic capacitor to GND. Connect all the pins together externally.
7		NC	No Connection. Leave this NC pin open.
8	4	FB	Feedback Input. Connect FB to the center point of the external resistor divider. The feedback threshold voltage is 0.8V.

## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN}=2.5V/3.7V$ ,  $V_{OUT}=1.8V/3.3V$ ,  $T_A=25^\circ C$ , unless otherwise noted.

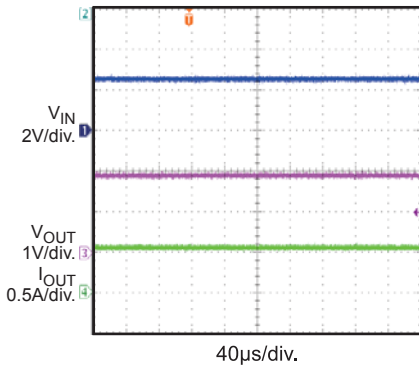


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

$V_{IN}=2.5V$ ,  $V_{OUT}=1.8V$ ,  $T_A=25^{\circ}C$ , unless otherwise noted.

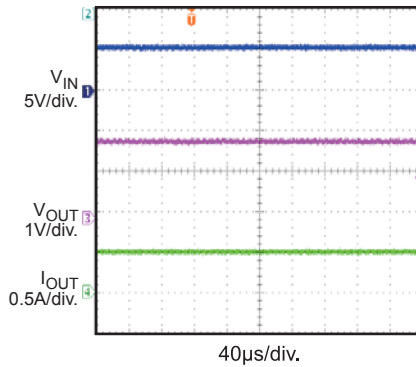
**Steady State**

$I_{OUT} = 0.5A$



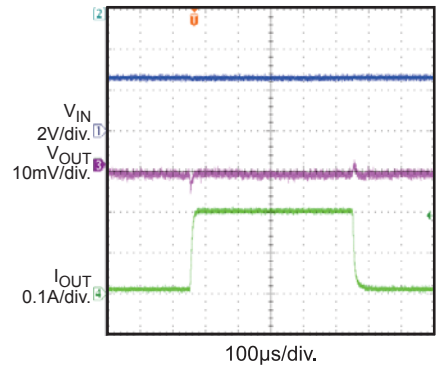
**Steady State**

$V_{IN} = 5.5V$ ,  $I_{OUT} = 0.5A$



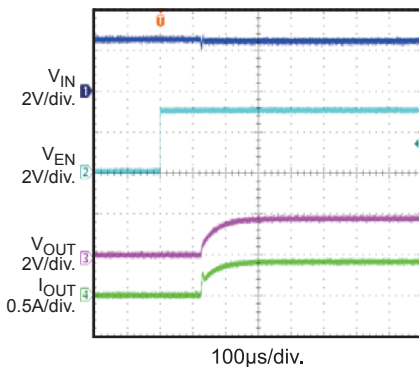
**Load Transient**

$I_{OUT} = 10mA-0.2A$



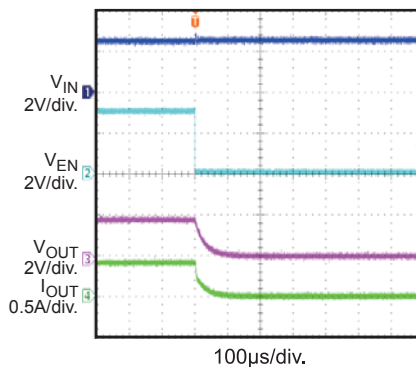
**Enable On**

$I_{OUT} = 0.4A$



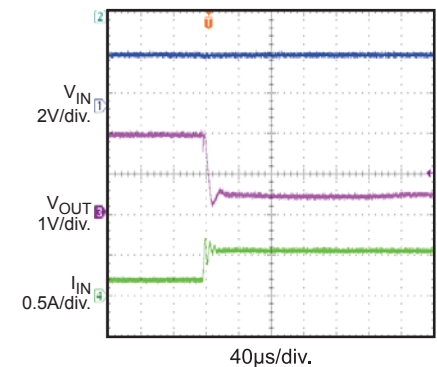
**Enable Off**

$I_{OUT} = 0.4A$



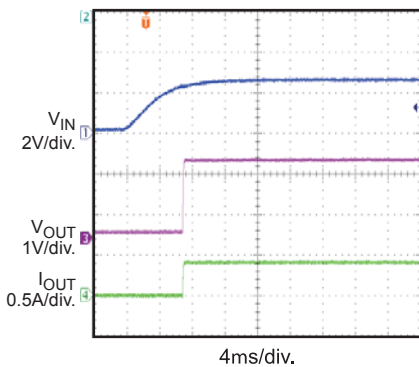
**Short Output**

$I_{OUT} = 0.2A$



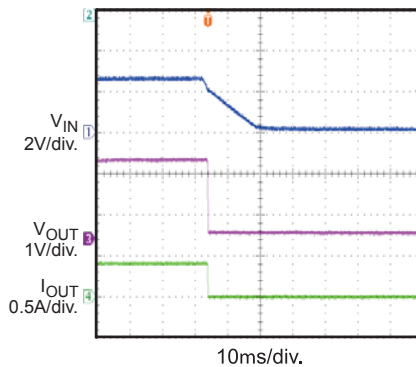
**Power Ramp Up**

$I_{OUT} = 0.4A$



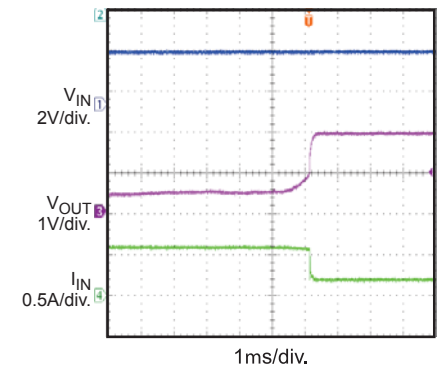
**Power Ramp Down**

$I_{OUT} = 0.4A$



**Short Output Recovery**

$I_{OUT} = 0.2A$

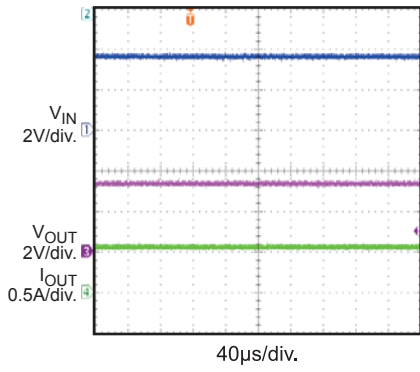


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

$V_{IN}=3.7V$ ,  $V_{OUT}=3.3V$ ,  $T_A=25^{\circ}C$ , unless otherwise noted.

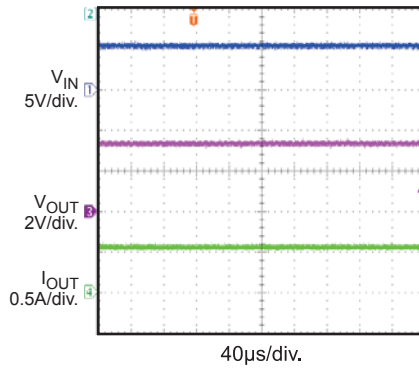
**Steady State**

$I_{OUT} = 0.5A$



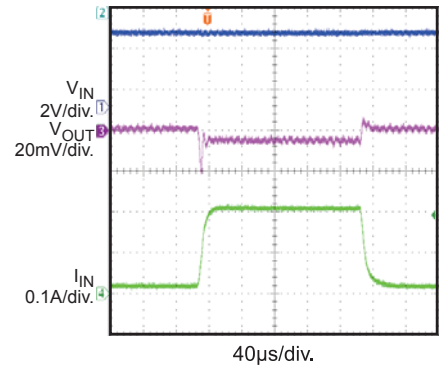
**Steady State**

$I_{OUT} = 0.5A$



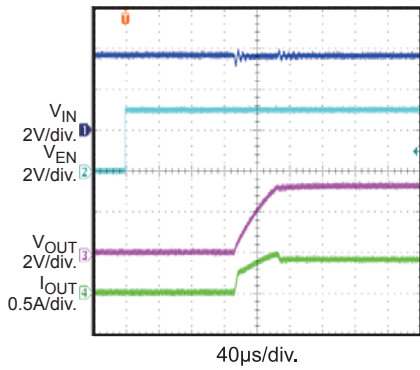
**Load Transient**

$I_{OUT} = 50mA-0.2A$



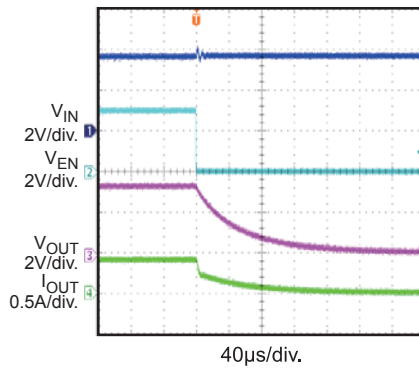
**Enable On**

$I_{OUT} = 0.4A$

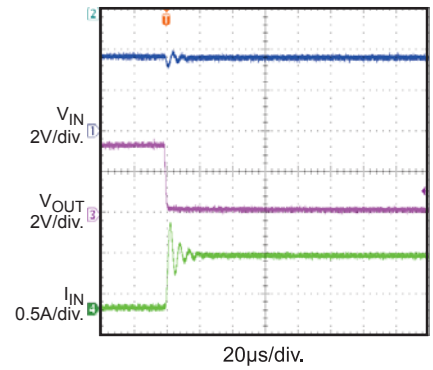


**Enable Off**

$I_{OUT} = 0.4A$

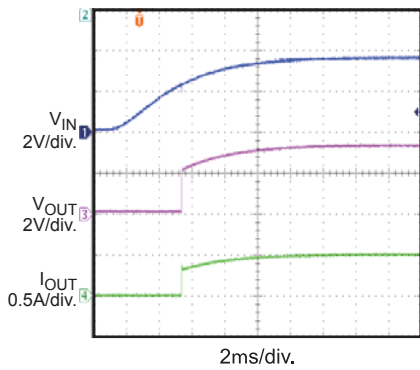


**Short Output**



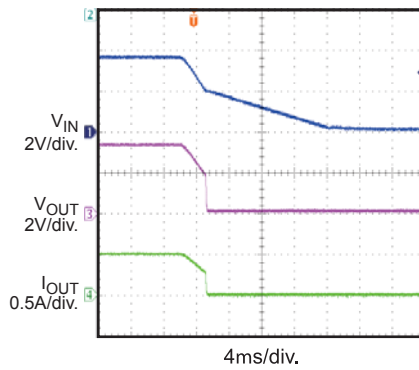
**Power Ramp Up**

$I_{OUT} = 0.5A$

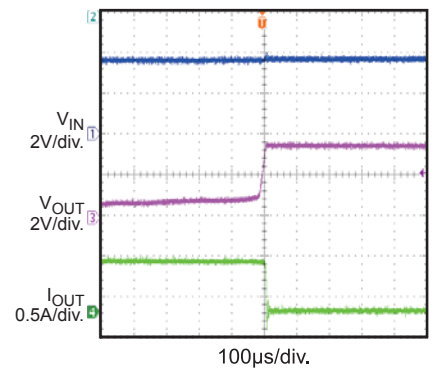


**Power Ramp Down**

$I_{OUT} = 0.5A$



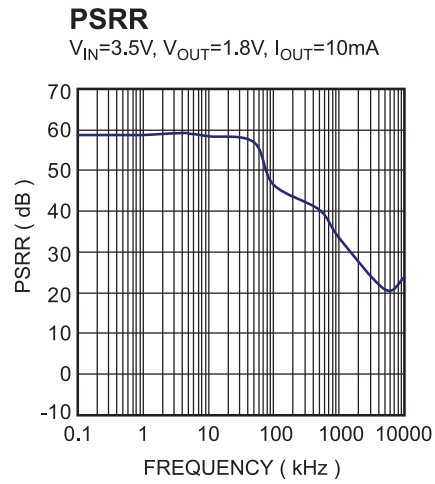
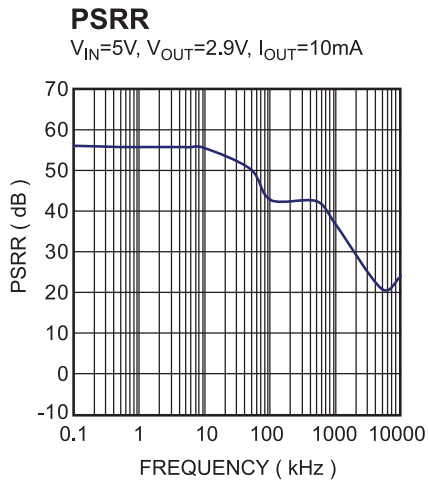
**Short Output Recovery**





### TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

T<sub>A</sub>=25°C, unless otherwise noted.



## FUNCTIONAL BLOCK DIAGRAM

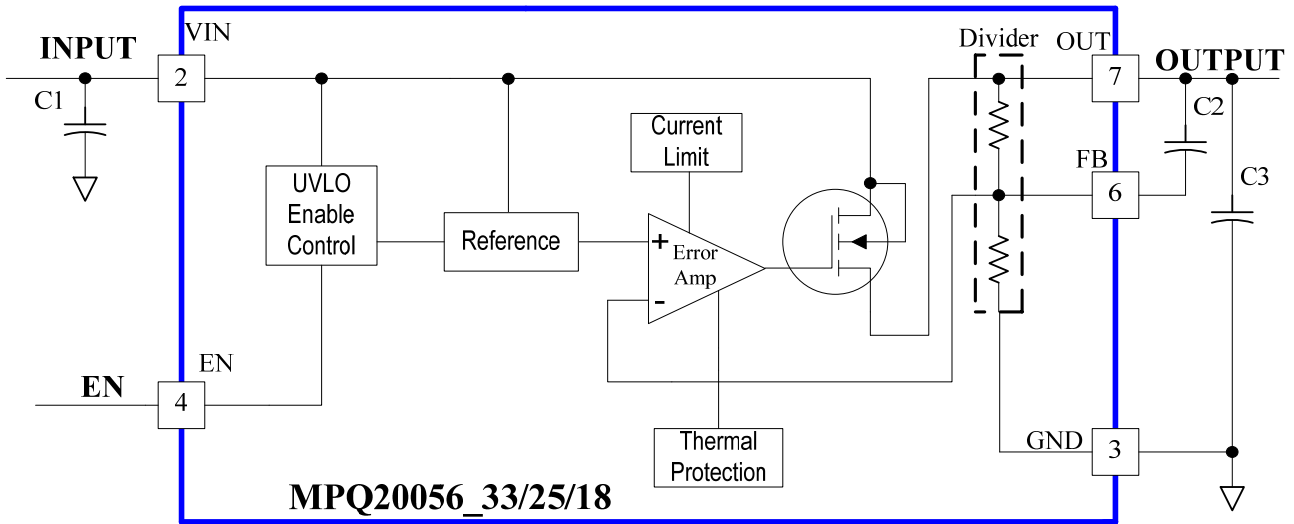


Figure 1: Fixed Output Functional Diagram

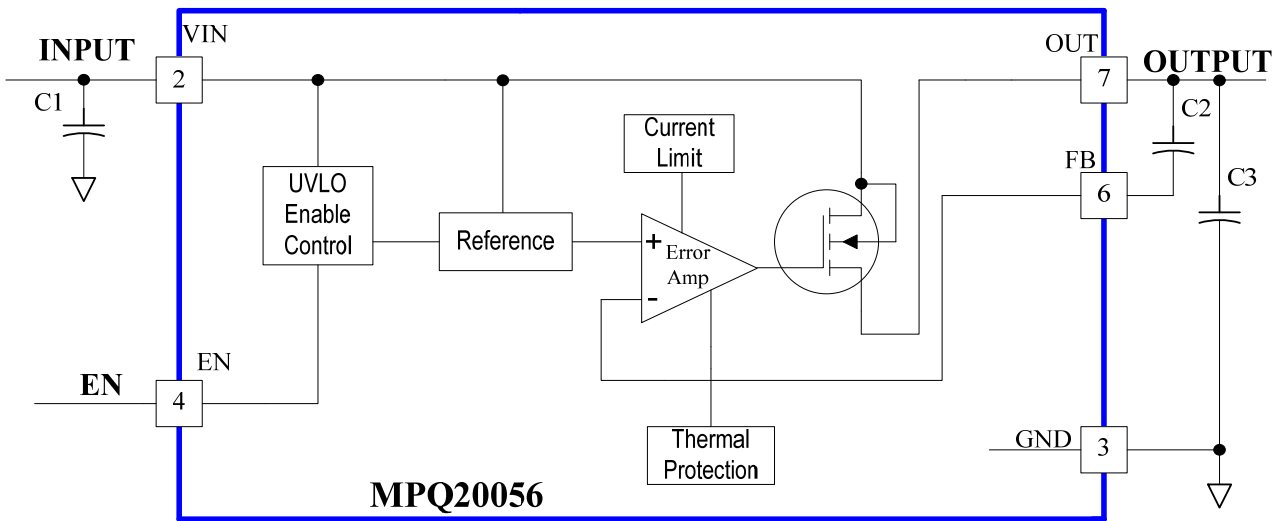


Figure 2: Adjustable Output Functional Block Diagram

## OPERATION

The MPQ20056 is a low-dropout linear regulator that can supply up to 250mA current, which makes it suitable for very low voltage, low quiescent, low noise, and high PSRR applications, such as wireless LAN transceivers, notebook computers, smartphones, and other low-power electronics.

The MPQ20056 uses an internal PMOS as the pass element and includes both thermal shutdown and an internal current-limiting circuit.

### Dropout Voltage

Dropout voltage is the minimum input to output differential voltage required for the regulator to maintain an output voltage within 100mV of its nominal value. Because the PMOS pass element behaves as a low-value resistor.

### Shutdown

The MPQ20056 can be switched ON or OFF by a logic input at the EN pin: Logic high turns the regulator on and logic low turns it off. Tie the EN pin to VIN if the application does not require the shutdown feature. Do not float the EN pin.

### Current Limit

The MPQ20056 includes a current limit structure that monitors and controls the PMOS gate voltage to limit the guaranteed maximum output current to 0.4A.

### Thermal Protection

Thermal protection turns off the PMOS when the junction temperature exceeds 150°C, allowing the IC to cool. When the IC's junction temperature drops by 20°C, the PMOS will turn on again. Thermal protection limits total power dissipation in the MPQ20056. For reliable operation, limit the junction temperature to a maximum of 125°C.

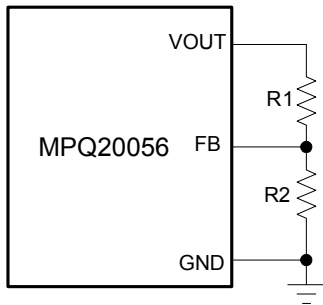
### Load-Transient Considerations

The output response of the load-transient consists of a transient response and DC shift—the MPQ20056's excellent load regulation effectively limits the DC shift. The output voltage transient depends on the output capacitor's value and ESR. Increasing the capacitance and decreasing the ESR will improve the transient response.

## APPLICATION INFORMATION

### Setting the Output Voltage

The output voltage of the MPQ20056 is preset to 1.8V, 2.5V or 3.3V by internal resistor divider. The output voltage also can be adjusted by using an external resistor divider (R1 and R2 in Figure 3).



**Figure 3: Setting the Output Voltage**

However, the sum of R1 and R2 should not exceed 10kΩ to minimize their impact on the internal resistor divider. For an accurate output-voltage setting, use 1kΩ (±1%) for R2, and determine R1 with:

$$R1 = R2 \times \left( \frac{V_{OUT} - V_{FB}}{V_{FB}} \right)$$

For example, for a 1.1V output voltage, R2 is 1kΩ, and R1 is 374Ω. You can select a standard 374Ω (±1%) resistor for R1.

### Power Dissipation

The power dissipation for any package depends on the thermal resistance of the case and circuit board, the temperature differential between the junction and ambient air, and the rate of air flow. The power dissipation across the device can be represented by the equation:

$$P = (V_{IN} - V_{OUT}) \times I_{OUT}$$

The allowable power dissipation can be calculated using the following equation:

$$P_{(MAX)} = (T_{Junction} - T_{Ambient}) / \theta_{JA}$$

Where (T<sub>Junction</sub> - T<sub>Ambient</sub>) is the temperature differential between the junction and the surrounding environment, θ<sub>JA</sub> is the thermal resistance from the junction to the ambient environment. Connecting the exposed GND pad to a large ground pad or plane helps to channel away heat.

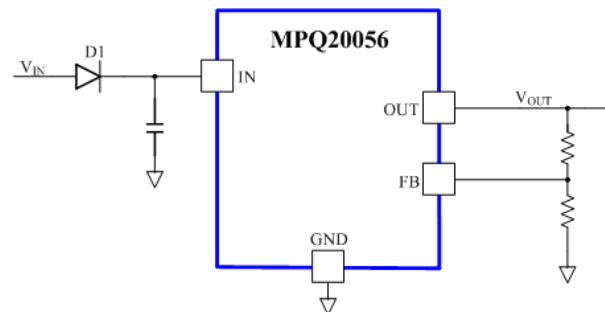
### Output Capacitor Selection

The MPQ20056 is specifically designed to work

with a standard ceramic output capacitor to save space and improve performance. Use a 4.7μF ceramic capacitor for most applications. Larger output capacitors will improve load transient response and reduce noise at the cost of increased size.

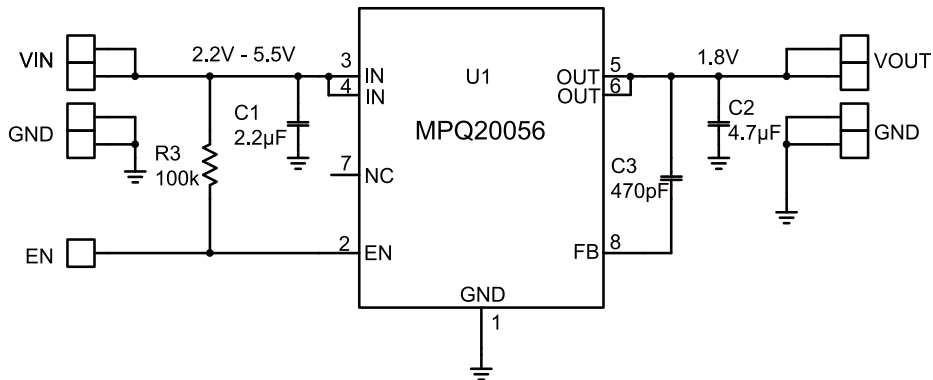
### External Reverse Voltage Protection

In some situations, e.g. a backup battery is connected as MPQ20056 load, the output voltage may be held up while the input is either pulled to ground to some intermediated voltage or is floating. Thus, the output voltage is higher than input voltage. Since MPQ20056 internal PMOS pass element has a body diode, a current will conduct from the output to input and is not internally limited. It's possible that the IC will be damaged by this unlimited reverse current. To avoid this, it's recommended to place an external diode at input like below.

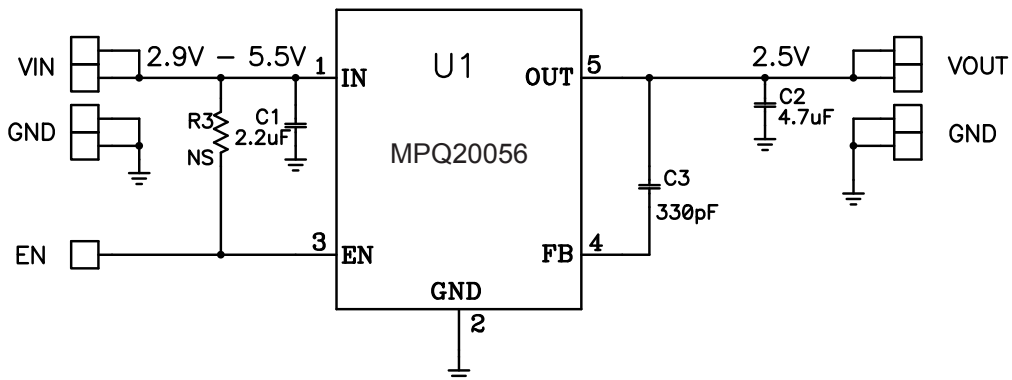


**Adding A Input Diode**

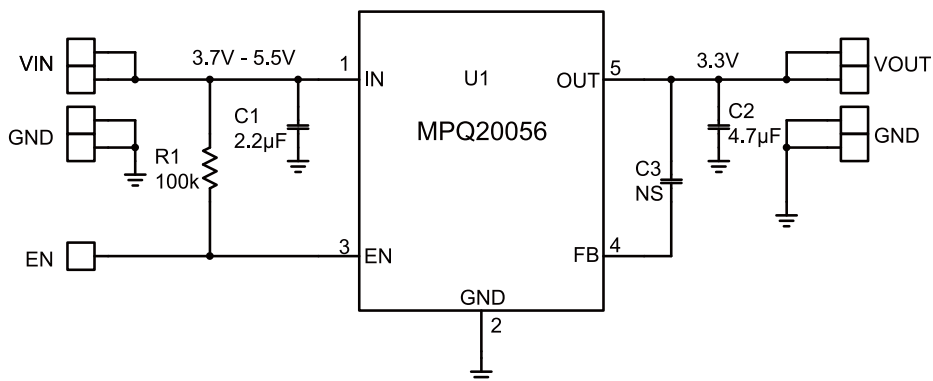
## TYPICAL APPLICATION CIRCUITS



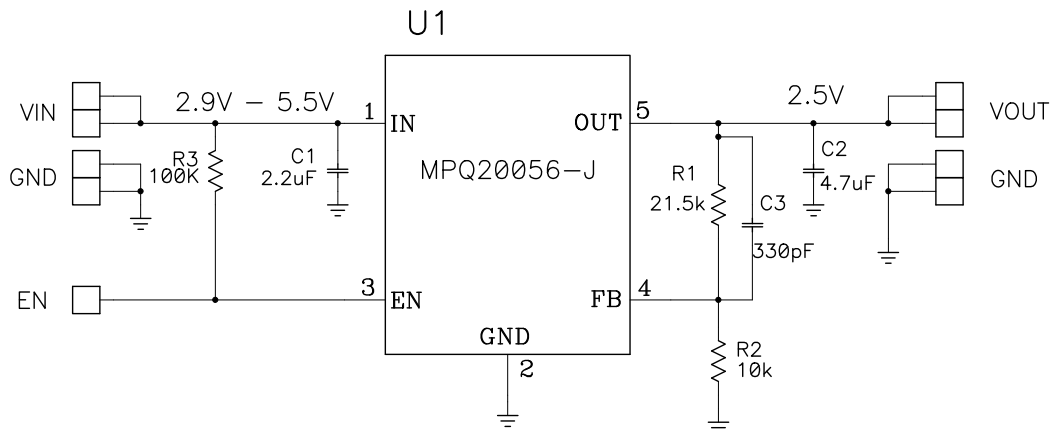
**Figure 4: 1.8V Fixed Output Application (QFN-8L)**



**Figure 5: 2.5V Fixed Output Application (TSOT23-5L)**



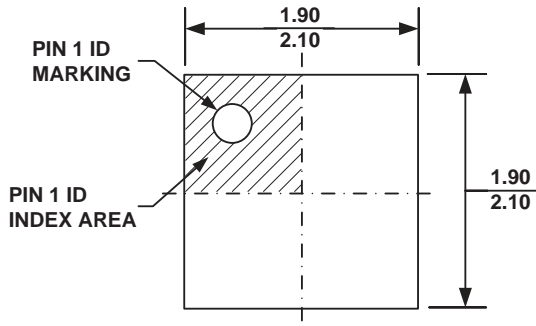
**Figure 6: 3.3V Fixed Output Application (TSOT23-5L)**



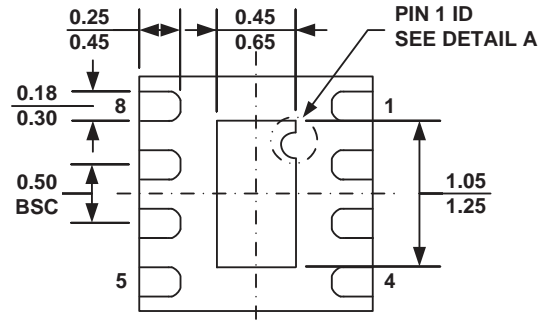
**Figure 7: Adjustable Output Application (TSOT23-5L)**

## PACKAGE INFORMATION

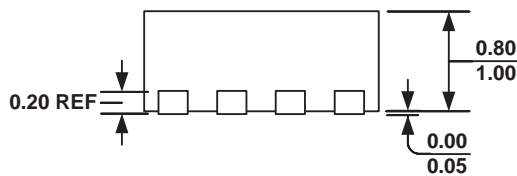
### QFN8 (2×2mm)



**TOP VIEW**

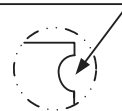


**BOTTOM VIEW**



**SIDE VIEW**

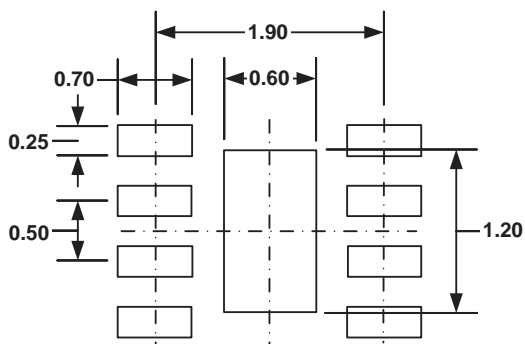
**PIN 1 ID OPTION A**  
R0.20 TYP.



**PIN 1 ID OPTION B**  
R0.20 TYP.



**DETAIL A**



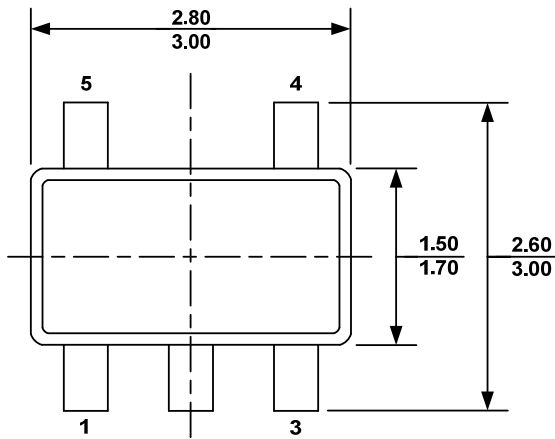
**RECOMMENDED LAND PATTERN**

#### NOTE:

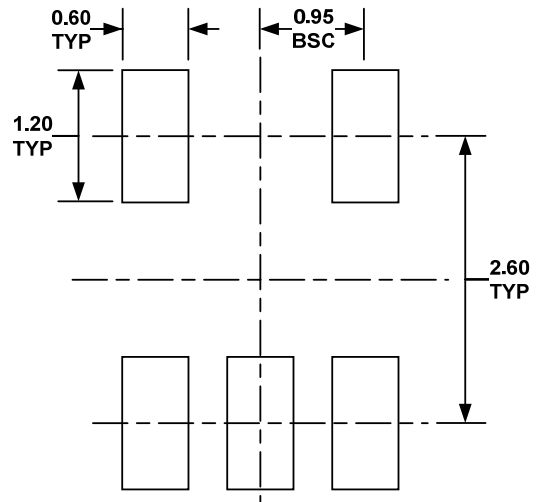
- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
- 4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VCCD-3.
- 5) DRAWING IS NOT TO SCALE.

**PACKAGE INFORMATION**

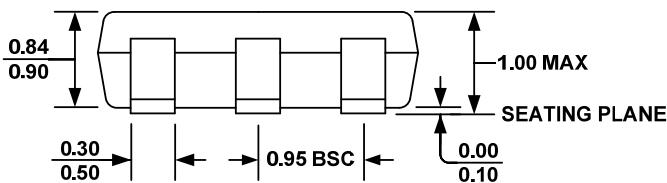
**TSOT23-5**



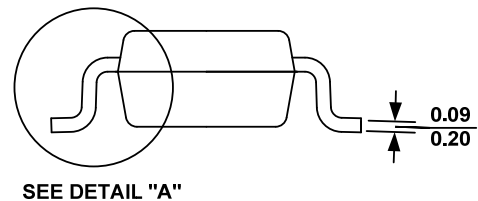
**TOP VIEW**



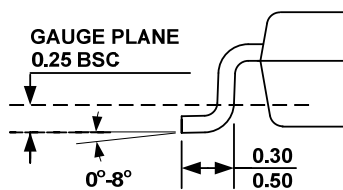
**RECOMMENDED LAND PATTERN**



**FRONT VIEW**



**SIDE VIEW**



**DETAIL "A"**

**NOTE:**

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
- 5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AA.
- 6) DRAWING IS NOT TO SCALE.

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