MPQ1925

100V, 4A, High-Frequency, Half-Bridge Gate Driver

DESCRIPTION

The MPQ1925 is a high-frequency, N-channel MOSFET, half-bridge gate driver. The device's low-side MOSFET (LS-FET) and high-side MOSFET (HS-FET) driver channels are independently controlled, and are matched with less than 5ns in time delay. In the case of an insufficient supply, the device's HS-FET and LS-FET under-voltage lockout (UVLO) protection forces the outputs low. The MPQ1925 also features an integrated bootstrap (BST) diode to reduce the external component count.

The MPQ1925 is available in a QFN-8 (4mmx4mm) package.

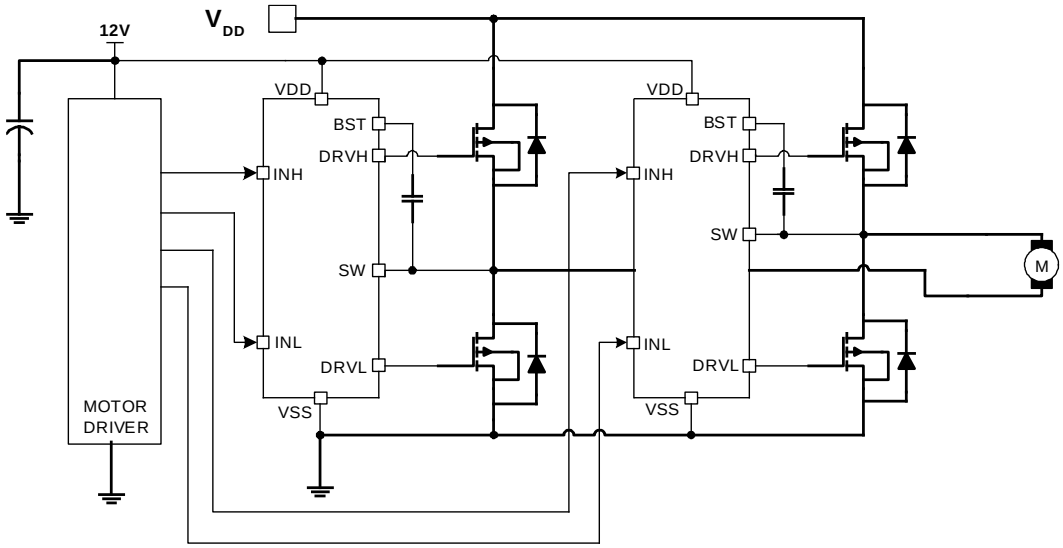
FEATURES

- Drives an N-Channel MOSFET Half-Bridge
- 115V Bootstrap Voltage (V_{BST}) Range
- On-Chip Bootstrap (BST) Diode
- Typical 20ns Propagation Delay
- <5ns Gate Driver Matching Time
- Drives a 2.2nF Load with a 15ns Rise Time and 10ns Fall Time at 12V V_{DD}
- Transistor-to-Transistor Logic (TTL)-Compatible Input
- <150µA Quiescent Current (I_Q)
- High-Side MOSFET (HS-FET) and Low-Side MOSFET (LS-FET) Under-Voltage Lockout (UVLO) Protection
- Available in a QFN-8 (4mmx4mm) Package

APPLICATIONS

- Motor Drivers
- Telecommunication Half-Bridge Power Supplies
- Avionics DC/DC Converters
- Two-Switch Forward Converters
- Active-Clamp Forward Converters

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ1925HR	QFN-8 (4mmx4mm)	*See Below*	1

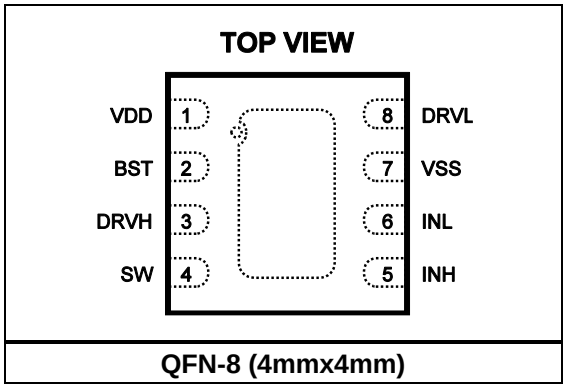
* For Tape & Reel, add suffix -Z (e.g. MPQ1925HR-Z).
For RoHS-compliant packaging, add suffix -LF (e.g. MPQ1925HR-LF-Z).

TOP MARKING

MPSYWW
MP1925
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP1925: Part number
LLLLLL: Lot number

PACKAGE REFERENCE



QFN-8 (4mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1	VDD	**Supply input.** The VDD pin supplies power to the internal circuitry. Place a decoupling capacitor to ground, close to VDD, to ensure a stable and clean supply.
2	BST	**Bootstrap.** The BST pin is the positive power supply for the internal, high-side MOSFET (HS-FET) floating driver. Connect a bypass capacitor between the BST and SW pins.
3	DRVH	**Floating driver output.**
4	SW	**Switching node.**
5	INH	**Floating driver control signal input.**
6	INL	**Low-side (LS) driver control signal input.**
7	VSS, exposed pad	**Chip ground.** Connect the VSS pin to the exposed pad for proper thermal operation.
8	DRVL	**LS driver output.**

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{DD}) .....-0.3V to +18V
SW voltage (V_{SW}) .....-5V to +105V
SW voltage (V_{SW}) ..... -25V (<100ns) to +105V
BST voltage (V_{BST}) .....-0.3V to +115V
BST voltage (V_{BST}) ..... -15V (<100ns) to +115V
BST to SW .....-0.3V to +18V
DRVH to SW (2) .....-0.3V to +18.3V
DRVH to SW (2)……-5V (<100ns) to +18.3V
DRVH to VSS.....-0.3V to (BST - VSS) + 0.3V
DRVH to VSS .....
……..-15V (<100ns) to (BST - VSS) +0.3V
DRVL to VSS (2) .....-0.3V to +18.3V
DRVL to VSS (2) ..... -5V (<100ns) to +18.3V
INH/INL to VSS.....-0.3V to (VDD + 0.3V)
INH/INL to VSS.....
…..…….-5V (<100ns) to (VDD + 0.3V)
All other pins ..... -0.3V to (V_{DD} + 0.3V)
Continuous power dissipation (T_A = 25°C) (3)
QFN-8 (4mmx4mm)..... 2.66W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±1.5kV
Charged device model (CDM).....±750V

Recommended Operating Conditions (4)

Supply voltage (V_{DD}) .....8V to 15V
SW voltage (V_{SW}) .....-1V to +100V
SW slew rate..... <50V/ns
Operating junction temp (T_J = T_A) .....
……..-40°C to +150°C

Thermal Resistance (5) θ_{JA} θ_{JC}

QFN-8 (4mmx4mm).....47 ..... 7.... °C/W

Notes:

1) Exceeding these ratings may damage the device. The repetitive pulse rating is guaranteed for a period of ≤100ns with a 1000kHz maximum repetition rate when V_{DD} is ≤15V.
2) DRVH and DRVL are outputs pins that cannot be connected to the external supply voltage.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{DD} = V_{BST} - V_{SW} = 12V, V_{SS} = V_{SW} = 0V, no load at DRVH and DRVL, T_J = -40°C to +150°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
VDD quiescent current (I_Q)	I_{DDQ}	INL = INH = 0		110	150	µA
VDD operating current	I_{DDO}	f_{SW} = 500kHz		7	12	mA
Floating driver I_Q	I_{BSTQ}	INL = INH = 0		60	90	µA
Floating driver operating current	I_{BSTO}	f_{SW} = 500kHz		6.5	11	mA
Leakage current	I_{LK}	BST = SW = 100V		0.05	10	µA
Inputs						
INL/INH high				2	2.4	V
INL/INH low			1	1.5		V
INL/INH internal pull-down resistance	R_{IN}		100	170	240	kΩ
Under-Voltage Lockout (UVLO) Protection						
V_{DD} UVLO rising threshold	V_{DDR}		6	7	7.7	V
V_{DD} UVLO hysteresis	V_{DDH}			0.4	0.7	V
V_{BST} - V_{SW} UVLO rising threshold	V_{BSTR}		5.8	6.8	7.5	V
V_{BST} - V_{SW} UVLO hysteresis	V_{BSTH}			0.4	0.7	V
Bootstrap (BST) Diode						
BST diode forward voltage	V_{F1}	At 100µA	0.2	0.5	0.9	V
BST diode forward voltage	V_{F2}	At 100mA	0.7	0.95	1.3	V
BST diode dynamic resistance	R_D	At 100mA		2.5	6	Ω
Low-Side (LS) Gate Driver						
Low output voltage	V_{OLL}	I_{OUT} = 100mA		0.1	0.2	V
High output voltage to rail	V_{OHL}	I_{OUT} = -100mA		0.2	0.35	V
Source current (6)	I_{OHL}	V_{DRVL} = 0V, V_{DD} = 12V		3		A
		V_{DRVL} = 0V, V_{DD} = 16V		4.7		A
Sink current (6)	I_{OLL}	V_{DRVL} = V_{DD} = 12V		4.5		A
		V_{DRVL} = V_{DD} = 16V		6		A
Floating Gate Driver						
Low output voltage	V_{OLH}	I_{OUT} = 100mA		0.1	0.2	V
High output voltage to rail	V_{OHH}	I_{OUT} = -100mA		0.2	0.35	V
Source current (6)	I_{OHH}	V_{DRVH} = 0V, V_{DD} = 12V		2.6		A
		V_{DRVH} = 0V, V_{DD} = 16V		4		A
Sink current (6)	I_{OLH}	V_{DRVH} = V_{DD} = 12V		4.5		A
		V_{DRVH} = V_{DD} = 16V		5.9		A
Switching Specifications of the LS Gate Driver						
INL falling to DRVL falling shutdown propagation delay	t_{DLFF}			20	50	ns
INL rising to DRVL rising start-up propagation delay	t_{DLRR}			20	50	ns
DRVL rise time		C_L = 2.2nF		15		ns
DRVL fall time		C_L = 2.2nF		10		ns

ELECTRICAL CHARACTERISTICS *(continued)*

V_{DD} = V_{BST} - V_{SW} = 12V, V_{SS} = V_{SW} = 0V, no load at DRVH and DRVL, T_J = -40°C to +150°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Switching Specifications of the Floating Gate Driver						
INH falling to DRVH falling shutdown propagation delay	t_{DHFF}			20	50	ns
INH rising to DRVH rising start-up propagation delay,	t_{DHRR}			20	50	ns
DRVH rise time		C_L = 2.2nF		15		ns
DRVH fall time		C_L = 2.2nF		10		ns
Switching Specifications for Matching						
Floating driver shutdown to LS driver start-up (6)	t_{MON}			1	5	ns
LS driver shutdown to floating driver start-up (6)	t_{MOFF}			1	5	ns
Minimum input pulse width to change the output (6)	t_{PW}				50	ns
BST diode start-up or shutdown time (6)	t_{BS}			10		ns

Note:

6) Guaranteed by design.

TIMING DIAGRAM

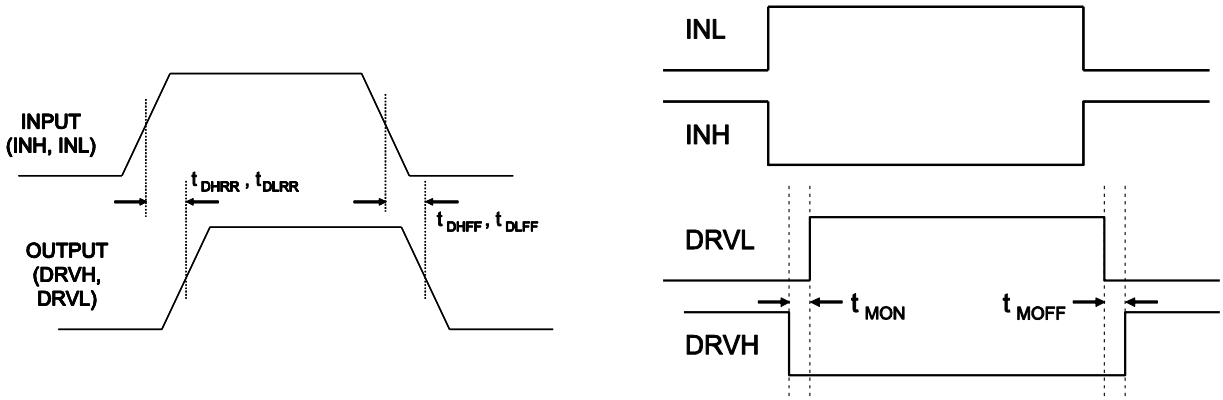
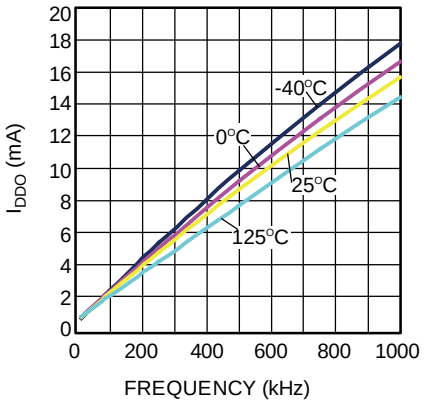


Figure 1: Timing Diagram

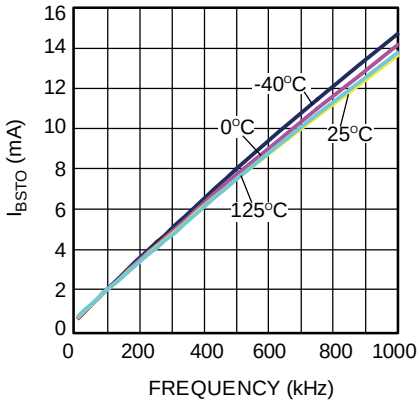
TYPICAL CHARACTERISTICS

V_{DD} = 12V, V_{SS} = V_{SW} = 0V, T_A = 25°C, unless otherwise noted.

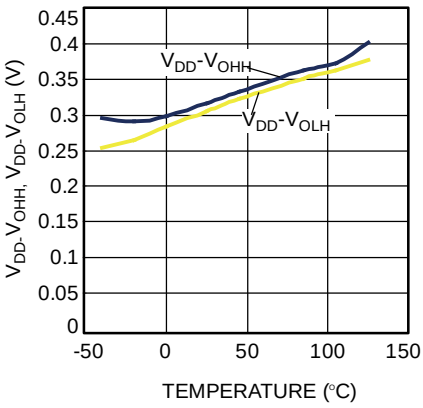
VDD Operating Current vs. Frequency



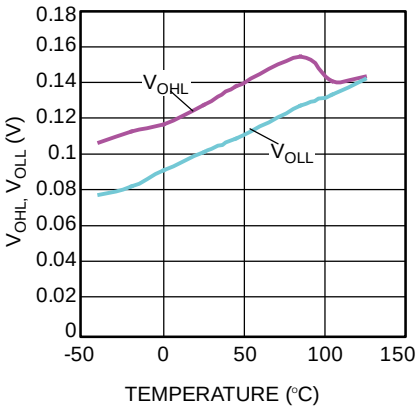
Floating Driver Operating Current vs. Frequency



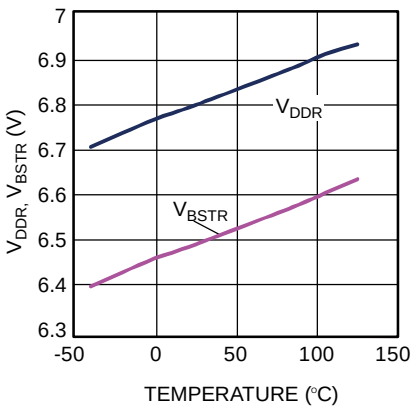
High Output Voltage vs. Temperature



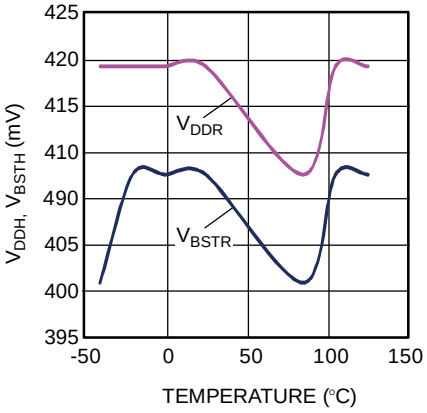
Low Output Voltage vs. Temperature



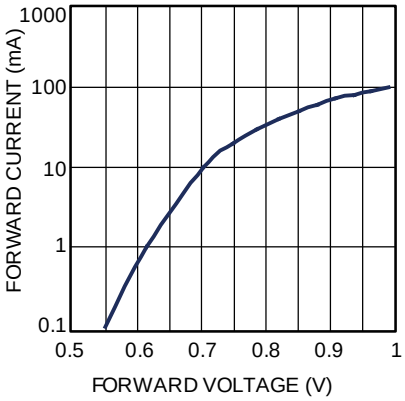
Under-Voltage Lockout Threshold vs. Temperature



Under-Voltage Lockout Hysteresis vs. Temperature

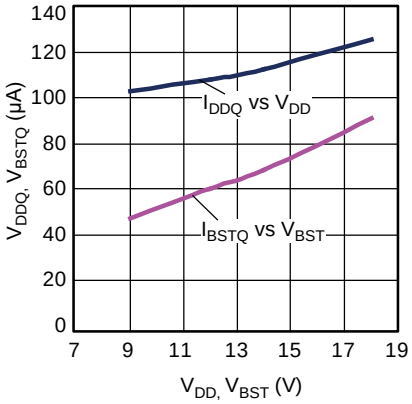


Bootstrap Diode I-V Characteristics

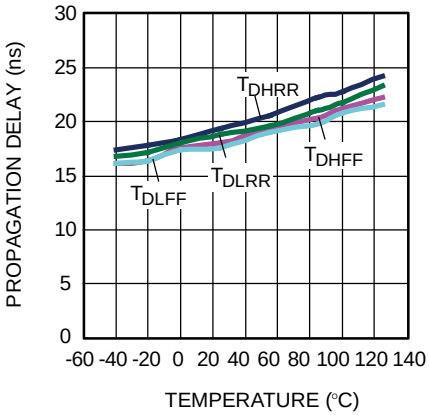


Quiescent Current vs. Voltage

INH = INL = 0V



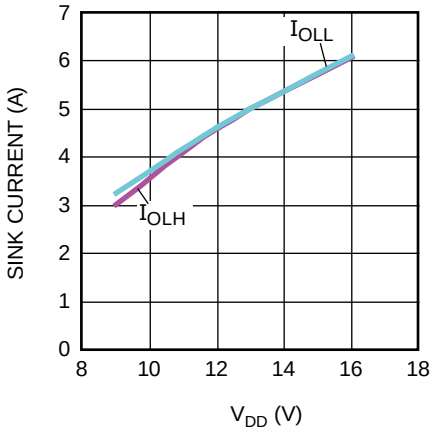
Propagation Delay vs. Temperature



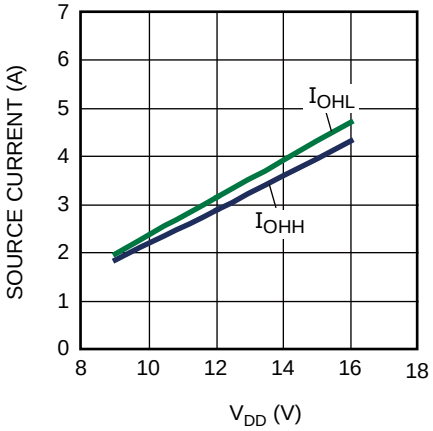
TYPICAL CHARACTERISTICS *(continued)*

V_{DD} = 12V, V_{SS} = V_{SW} = 0V, T_A = 25°C, unless otherwise noted.

Sink Current vs. V_{DD}

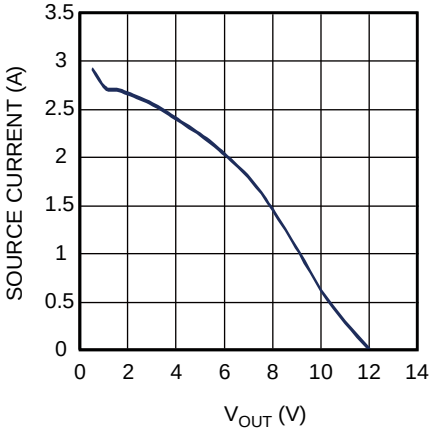


Source Current vs. V_{DD}



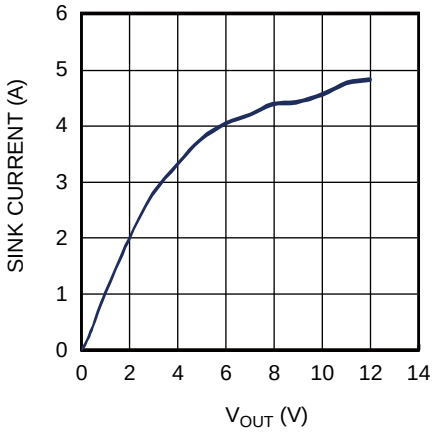
Source Current vs. Output Voltage

V_{DD}=12V



Sink Current vs. Output Voltage

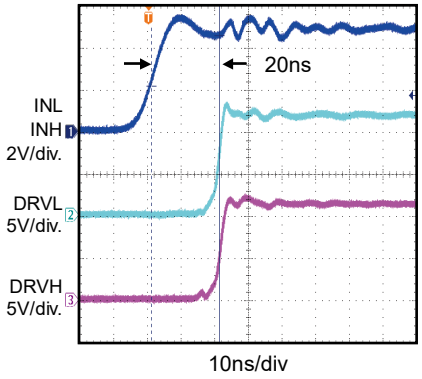
V_{DD}=12V



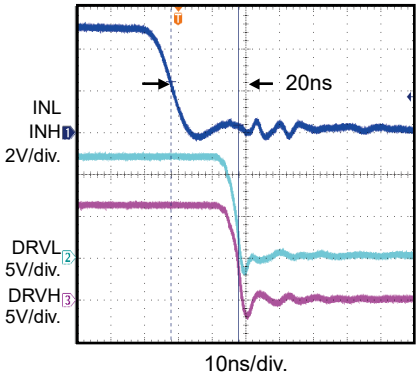
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 12V, V_{SS} = V_{SW} = 0V, T_A = 25°C, unless otherwise noted.

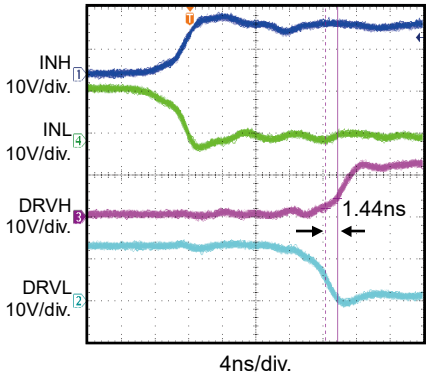
Turn-On Propagation Delay



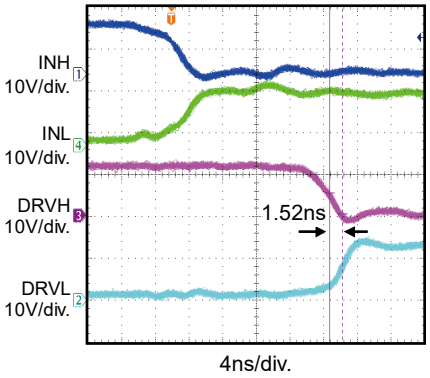
Turn-Off Propagation Delay



Driver Matching Time

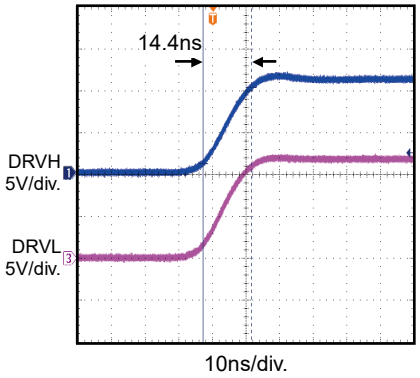


Driver Matching Time



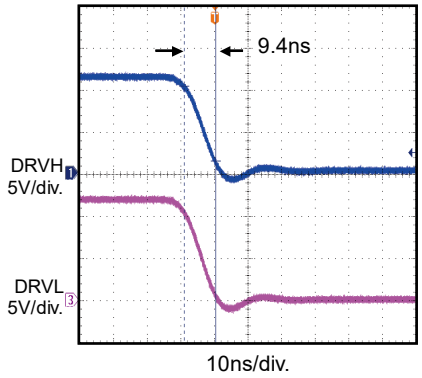
Driver Rising Time

2.2nF load



Driver Falling Time

2.2nF load



FUNCTIONAL BLOCK DIAGRAM

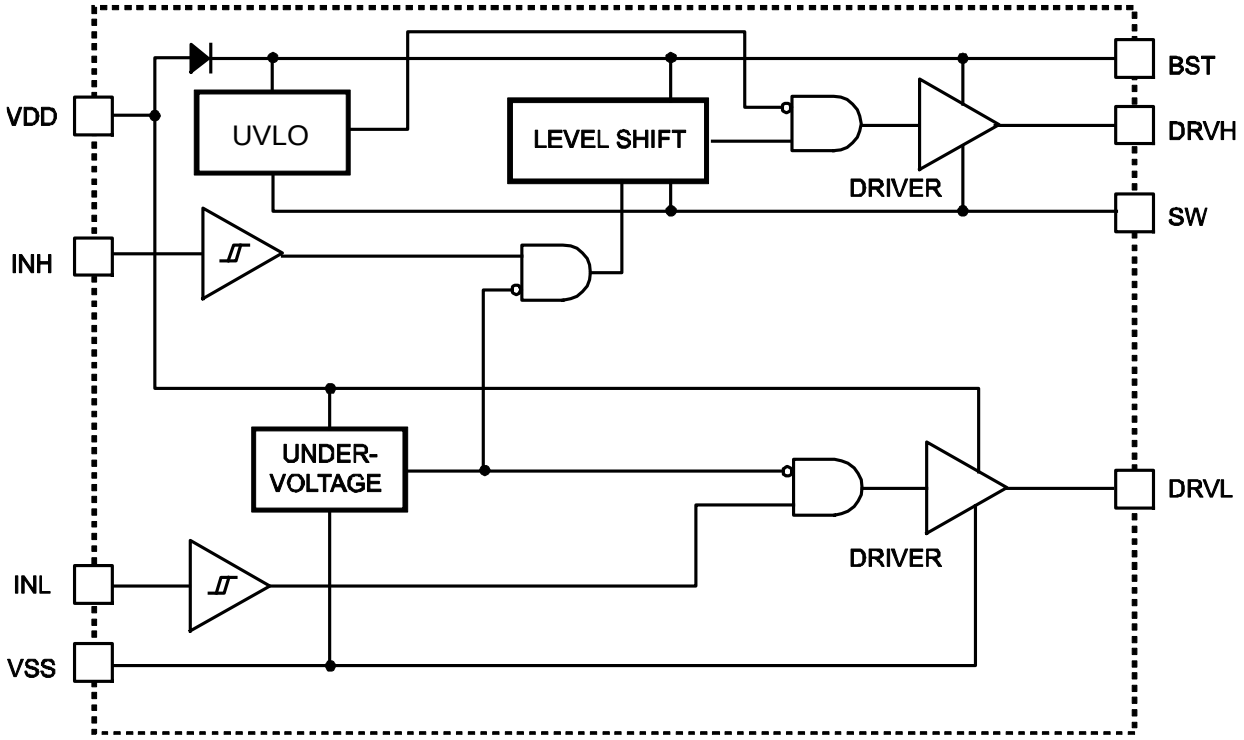


Figure 2: Functional Block Diagram

REFERENCE DESIGN CIRCUITS

Half-Bridge Converter

In a half-bridge converter topology, the high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET) are driven alternately with a dead time (DT) inserted between their respective on periods. INT and INL are driven with alternating signals via the pulse-width modulation (PWM) controller. The input voltage (V_{IN}) can rise up to 100V when in a half-bridge topology (see Figure 5 in the Typical Application Circuits section on page 13).

Two-Switch Forward Converter

In a two-switch forward converter topology, the HS-FET and LS-FET start up and shutdown simultaneously. During current-mode control, the INH and INL input signals sense the output voltage (V_{OUT}) and output current (I_{OUT}) via a PWM controller.

The Schottky diodes clamp the power transformer's reverse swing, and must be rated for V_{IN}, which can rise up to 100V (see Figure 6 in the Typical Application Circuits section on page 13).

Active-Clamp Forward Converter

In an active-clamp forward converter topology, the HS-FET and LS-FET are driven alternately. The HS-FET and reset capacitor (C_{RESET}) reset the power transformer without loss.

Active-clamp forward converter topologies are optimal for duty cycles exceeding 50%. The MPQ1925 may not be able to operate at 100V in an active-clamp forward topology (see Figure 7 in the Typical Application Circuits section on page 13).

APPLICATION INFORMATION

The INH and INL input signals can be controlled independently. If both INH and INL control the HS-FET and LS-FET of the same bridge, set a sufficient DT between the low INH and INL signals (and vice versa) to avoid shoot-through. DT is the time interval between low INH and low INL. Figure 3 shows the shoot-through timing diagram.

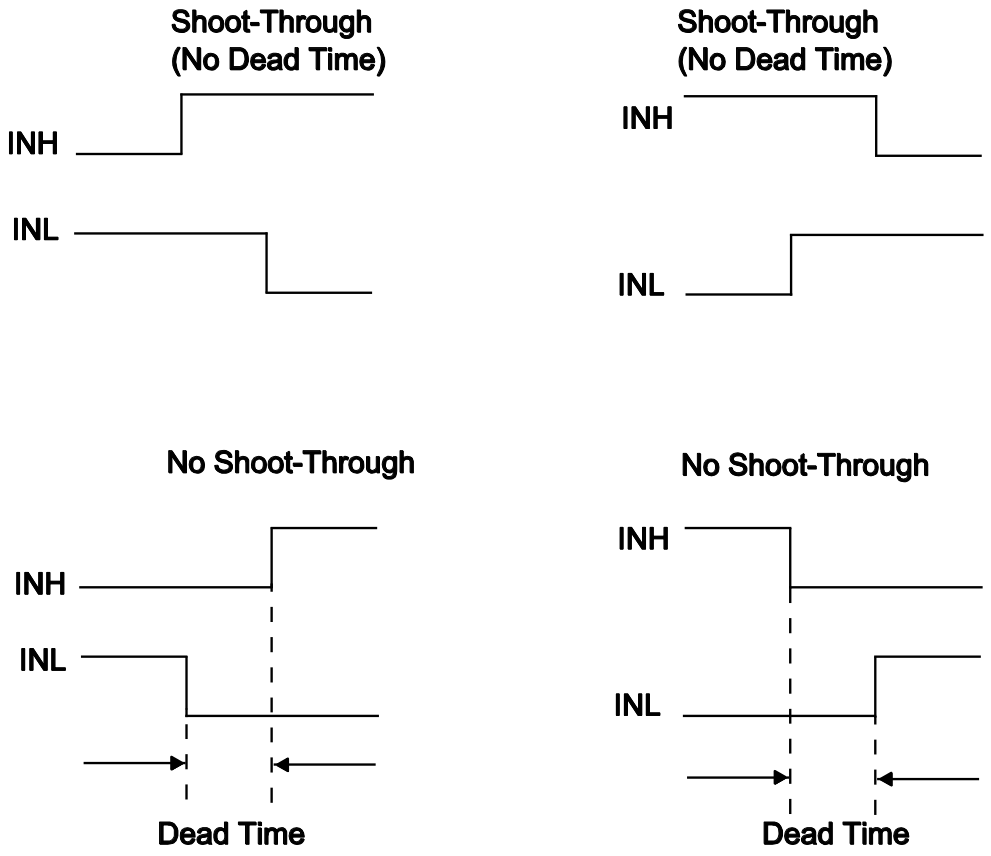


Figure 3: Shoot-Through Timing Diagram

PCB Layout Guidelines

Proper PCB layout is critical for the optimal performance of the HS-FET and LS-FET gate drivers. The MPQ1925 is designed to accommodate negative undershoot; however, excessive undershoot can lead to unpredictable operation or damage to the IC. For the best results, refer to Figure 4 and follow the guidelines below:

1. Make the connection between the HS-FET source and the LS-FET drain as direct as possible to avoid a negative undershoot on the phase node due to parasitic inductance.
2. Use surface-mount N-channel MOSFETs that allow for a very short connection between the HS-FETs and LS-FETs.
3. Place the bootstrap capacitor (C3) and supply bypass capacitor (C2) as close as possible to the IC.
4. Use multiple vias to connect the ground side of these capacitors, which are connected to a solid ground plane, to both the GND pin and exposed pad.
5. Keep the high-current ground path between the input supply, input bulk capacitor (C6), and the MOSFETs away from the IC.

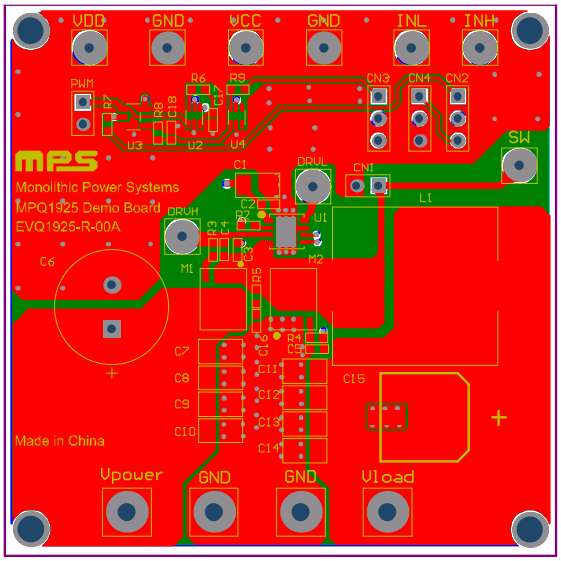


Figure 4: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

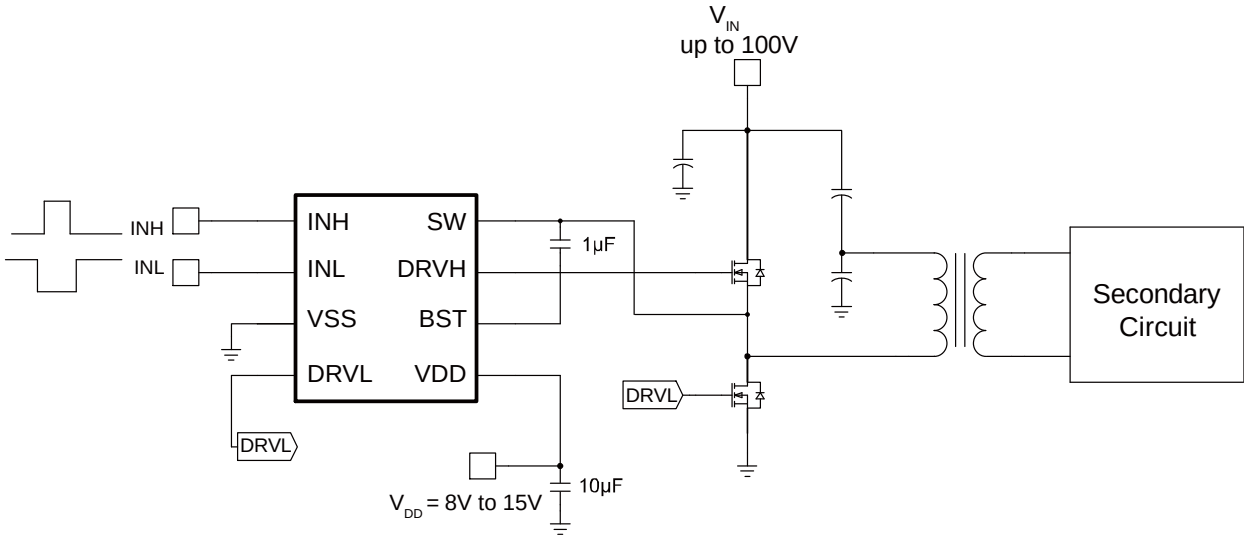


Figure 5: Typical Application Circuit (Half-Bridge Converter Topology)

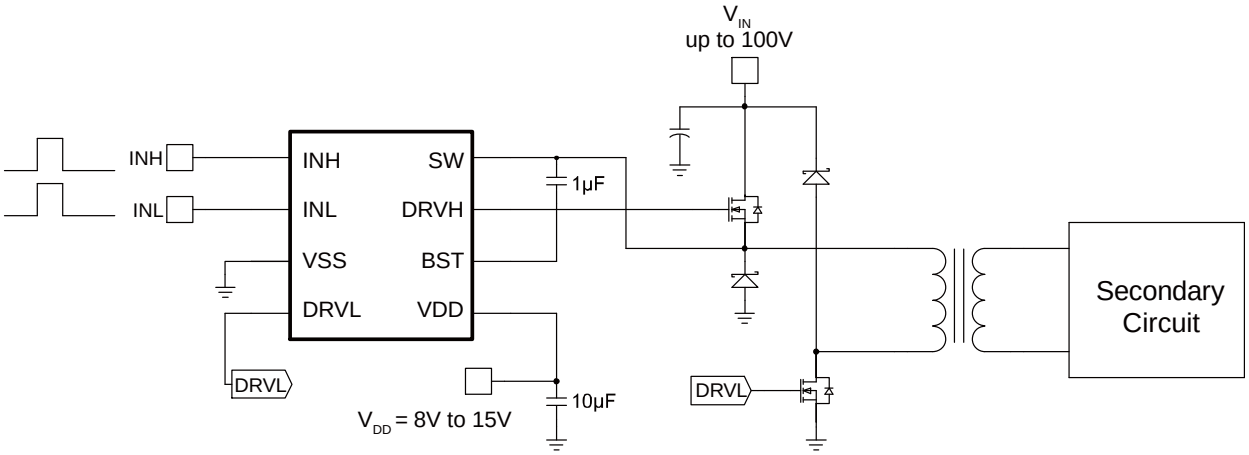


Figure 6: Typical Application Circuit (Two-Switch Forward Converter Topology)

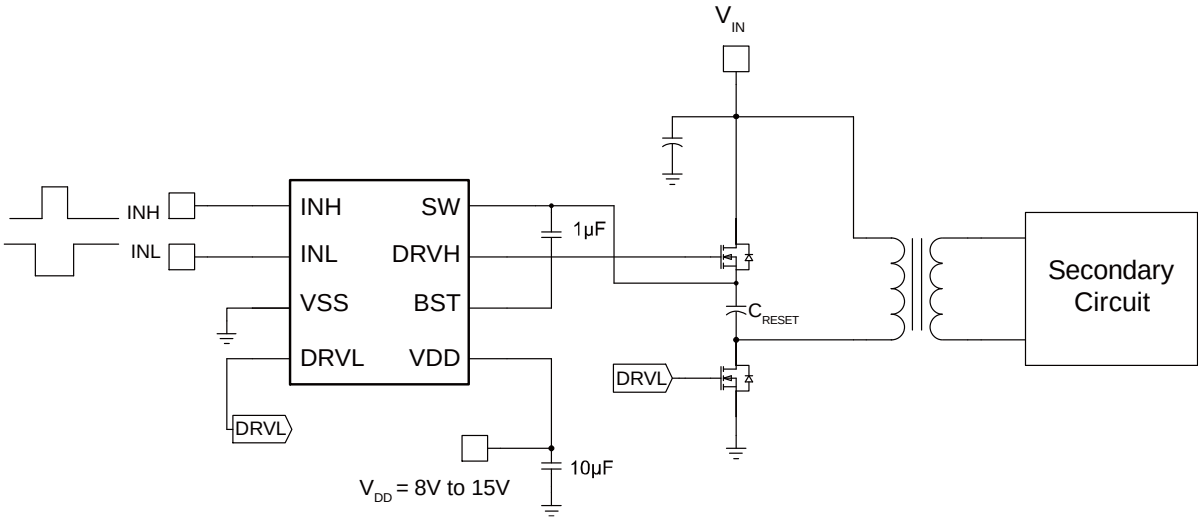
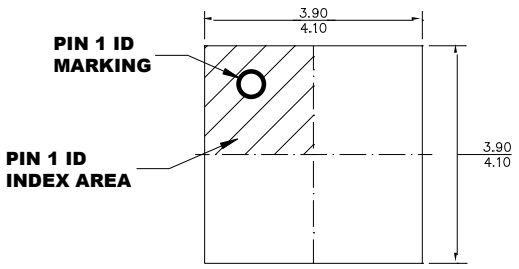


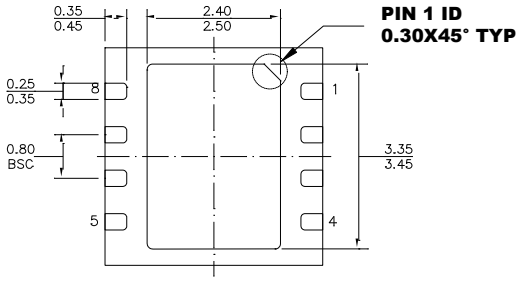
Figure 7: Typical Application Circuit (Active-Clamp Forward Converter Topology)

PACKAGE INFORMATION

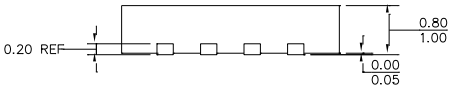
QFN-8 (4mmx4mm)



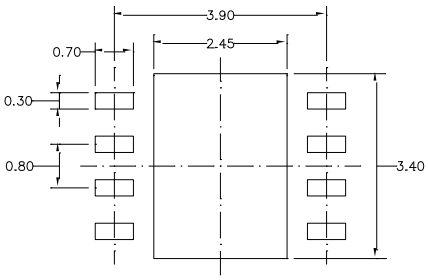
TOP VIEW



BOTTOM VIEW



SIDE VIEW

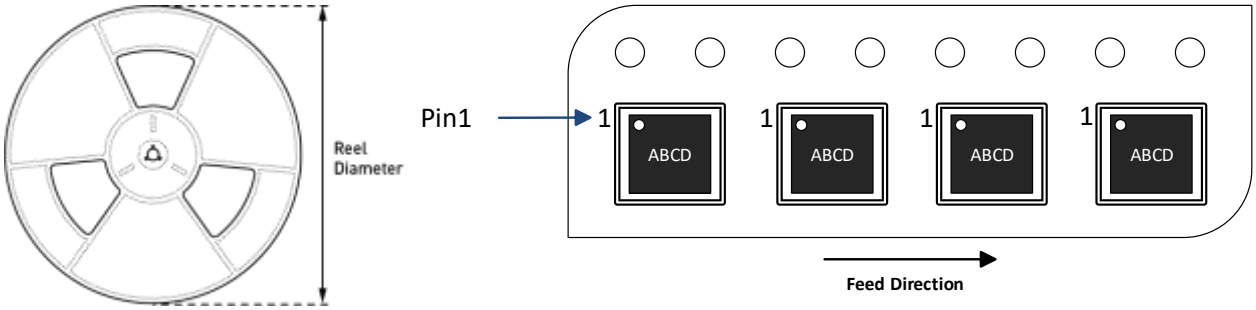


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ1925HR-Z	QFN-8 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/8/2022	Initial Release	-