MPM3816C

2.7V to 5.5V, 1A, Ultra-Small and Ultra-Low Noise Power Module

DESCRIPTION

The MPM3816C is a synchronous, step-down, power module with an integrated inductor. The MPM3816C achieves up to 1A of continuous output current (I_{OUT}) from a 2.7V to 5.5V input voltage (V_{IN}) range, with excellent load and line regulation. The output voltage (V_{OUT}) can be regulated as low as 0.4V.

Only feedback (FB) resistors, input capacitors, and output capacitors are required to complete the design.

The constant-on-time (COT) control scheme provides fast transient response and eases loop stabilization. Fault protections include cycle-by-cycle current limiting and thermal shutdown.

The MPM3816C requires a minimal number of readily available, standard external components, and is available in an ultra-small ECLGA-10 (2mmx2.2mmx1.2mm) package.

FEATURES

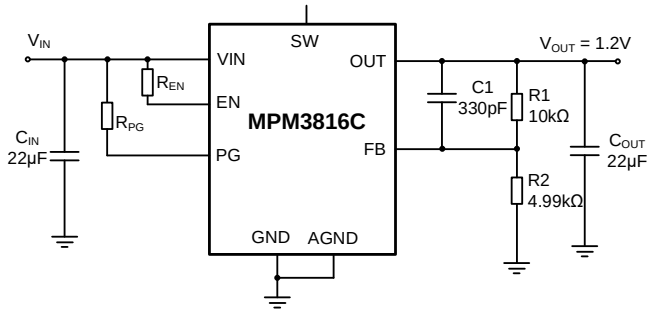
- Wide 2.7V to 5.5V Operating Input Voltage (V_{IN}) Range
- Adjustable Output Voltage (V_{OUT}) from 0.4V
- Up to 1A of Continuous I_{OUT}
- Forced Continuous Conduction Mode (FCCM)
- 2.4MHz Switching Frequency (f_{SW})
- Enable (EN) and Power Good (PG) for Power Sequencing
- Output Discharge
- Cycle-by-Cycle Over-Current Protection (OCP)
- Short-Circuit Protection (SCP) with Hiccup Mode
- Available in an ECLGA-10 (2mmx2.2mmx1.2mm) Package

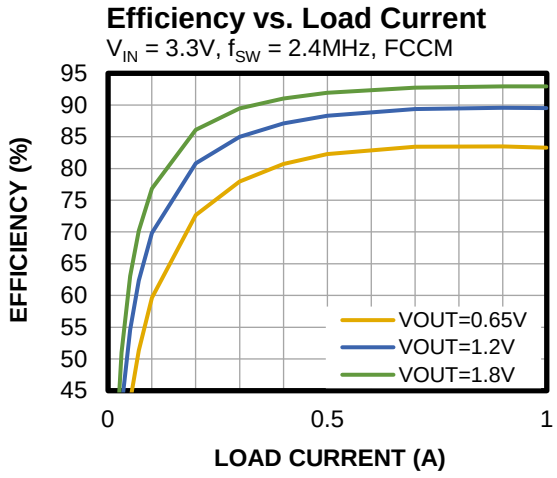
APPLICATIONS

- FPGA, ASIC, and DSP Power
- Optical Modules
- LDO Replacements
- Power for Portable Products
- SSD and HDD Storage
- Space-Limited Applications

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. “MPS”, the MPS logo, and “Simple, Easy Solutions” are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

TYPICAL APPLICATION





MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPM3816CGPE	ECLGA-10 (2mmx2.2mmx1.2mm)	*See Below*	3

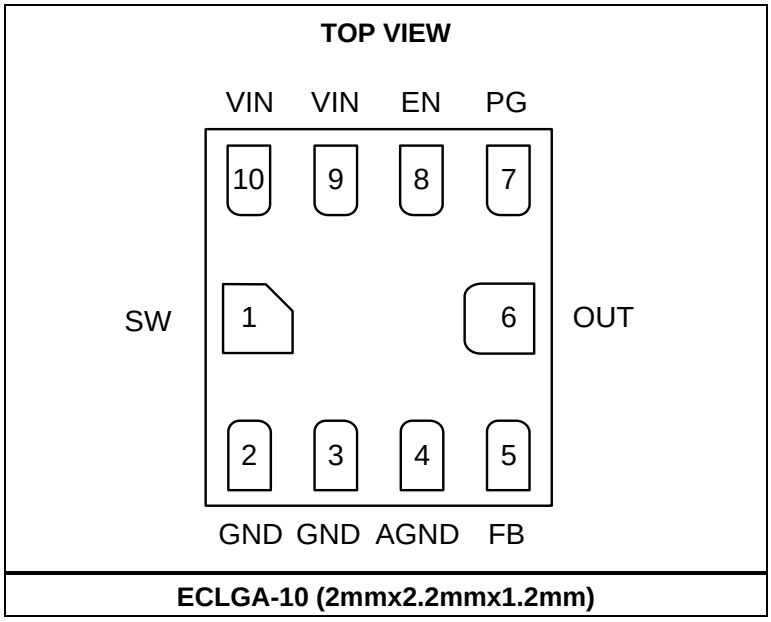
* For Tape & Reel, add suffix -Z (e.g. MPM3816CGPE-Z).

TOP MARKING

$\overline{\text{MXY}}$
LLL

MX: Product code
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



ECLGA-10 (2mmx2.2mmx1.2mm)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin#	Name	Description
1	SW	**Output switching node.** The SW pin is a test pin. It can be left floating.
2, 3	GND	**Power ground.** The GND pin is the reference ground of the regulated output voltage (V_{OUT}). It requires extra care during PCB layout. Connect the GND pins together with large copper and vias to enhance heat dissipation.
4	AGND	**Analog ground for the internal control circuit.** Connect the AGND pin to GND during PCB layout.
5	FB	**Feedback.** An external resistor divider connected from the output to AGND, and tapped to FB, sets V_{OUT}.
6	OUT	**Power output.**
7	PG	**Power good indicator.** The output of the PG pin is an open drain.
8	EN	**On/off control.**
9, 10	VIN	**Power input.**

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 6.2V
V_{SW}.....
.....-0.3V (-5V for <10ns) to 6.5V (8V for <10ns)
All other pins .....-0.3V to +6.2V
Continuous power dissipation (T_A = 25°C) (2)
ECLGA-10 (2mmx2.2mm) 4W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Operation V_{IN} range .....2.7V to 5.5V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (4) (5) (6) (7)

ECLGA-10 (2mmx2.2mmx1.2mm)
θ_{JA} ..... 30.84°C/W
θ_{JC_TOP} ..... 18.75°C/W
θ_{JB} ..... 26.53°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) θ_{JA} is the junction-to-ambient thermal resistance, θ_{JC_TOP} is the junction-to-case top thermal characterization parameter, θ_{JB} is the junction-to-board thermal characterization parameter.
5) The thermal parameter is based on testing on MPS evaluation board (EVM3816C-PE-01A) under no airflow cooling conditions in a standard enclosure. The board is 5.1cmx5.1cm, 4 layers, and the top and bottom layer copper thickness is 2oz.
6) The gjunction-to-case top thermal characterization parameter, θ_{JC_TOP} , estimates the junction temperature in the real system, based on $T_J = \theta_{JC_TOP} \times P_{LOSS} + T_{CASE_TOP}$, where P_{LOSS} is the entire loss of module at real application, and T_{CASE_TOP} is the case top temperature.
7) The junction-to-board thermal characterization parameter, θ_{JB}, is estimated the junction temperature in the real system, based on $T_J = \theta_{JB} \times P_{LOSS} + T_{BOARD}$, where P_{LOSS} is the entire loss of module at real application, and T_{BOARD} is the board temperature.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6V, T_J = -40°C to +125ºC [8], typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input voltage (V_{IN}) range	V_{IN}		2.7		5.5	V
Under-voltage lockout (UVLO) rising threshold	$V_{IN_UVLO_RISING}$			2.55	2.7	V
UVLO threshold hysteresis	$V_{IN_UVLO_HYS}$			200		mV
Shutdown supply current	I_{SD}	V_{EN} = 0V, T_J = 25°C		0.2	0.5	µA
Quiescent supply current	I_Q	V_{EN} = 2V, V_{FB} = 0.405V		450	520	µA
Feedback (FB) voltage	V_{FB}	T_J = 25°C	396	400	404	mV
		T_J = -40°C to +125°C	394	400	406	
FB current	I_{FB}	V_{FB} = 0.405V		10	50	nA
Switching frequency	f_{SW}	V_{IN} = 5V, V_{OUT} = 1.2V, operating in FCCM	2000	2400	2700	kHz
Minimum on time [9]	t_{MIN_ON}			40		ns
P-channel MOSFET peak current limit	I_{PEAK}		2	3		A
N-channel MOSFET valley current limit	I_{VALLEY}		1	2		A
Soft-start (SS) time	t_{SS}	Time from 5% to 95% of nominal V_{OUT}		2		ms
Power good (PG) under-voltage (UV) rising threshold	$V_{PGUVVTH_HI}$	FB rising edge		95		%
PG UV falling threshold	$V_{PGUVVTH_LO}$	FB falling edge		90		%
PG over-voltage (OV) rising threshold	$V_{PGOVVTH_HI}$	With reference to V_{FB}		110		%
PG OV falling threshold	$V_{PGOVVTH_LO}$	With reference to V_{FB}		105		%
PG rising delay	t_{PGTD_HI}	PG rising edge		60		µs
PG falling delay	t_{PGTD_LO}	PG falling edge		50		µs
PG sink current capability	V_{PG}	Sink 1mA			0.4	V
PG leakage current/logic high	I_{PG_LEAK}	5V logic high		2.6		µA
Enable (EN) turn-on delay	t_{ENTD_ON}	EN on to SW active		450		µs
EN turn-off delay	t_{ENTD_OFF}	EN off to stop switching		3.5		µs
EN input logic low voltage	V_{EN_LO}				0.4	V
EN input logic high voltage	V_{EN_HI}		1.2			V
EN pull-down resistor	R_{EN}			1.7		MΩ
Output discharge resistor	R_{DIS}	V_{EN} = 0V, V_{OUT} = 1.2V		50		Ω
EN input current	I_{EN}	V_{EN} = 2V		0.1		µA
		V_{EN} = 0V		0		µA

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_J = -40°C to +125ºC [8], typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Negative current limit	I_{NOCP}	Current flow from SW to GND		3		A
Thermal shutdown [9]	T_{SD}			150		°C
Thermal hysteresis [9]	T_{SD_HYS}			20		°C

Notes:

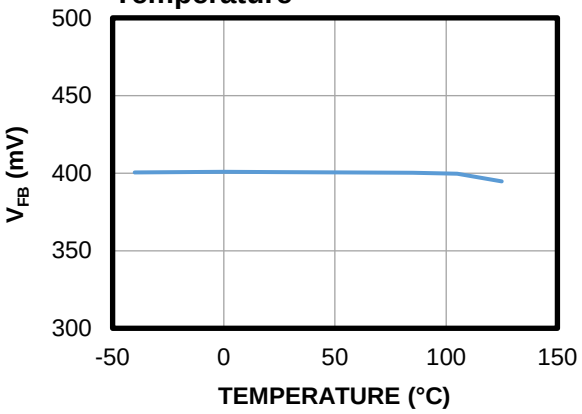
8) Not tested in production. Derived by over-temperature correlation.
9) Derived by sample characterization. Not tested in production.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

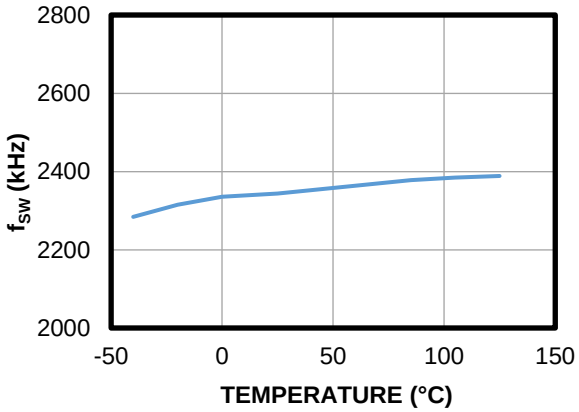
TYPICAL CHARACTERISTICS

V_{IN} = 3.3V, V_{OUT} = 1.2V, C_{OUT} = 2 x 22µF, T_A = 25°C, unless otherwise noted.

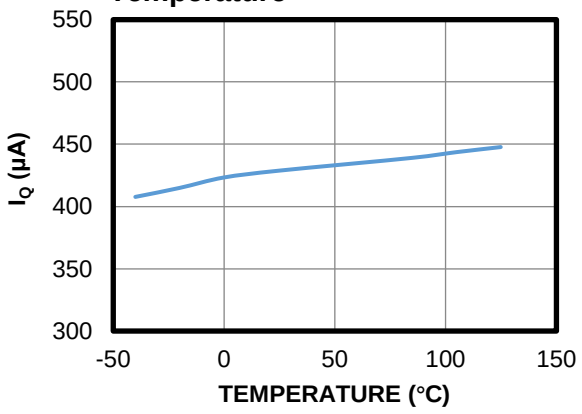
Feedback Voltage vs. Temperature



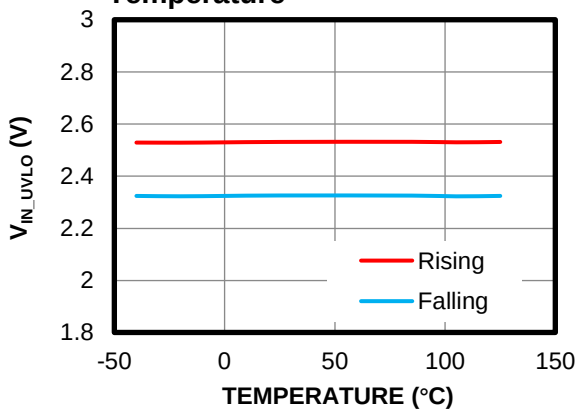
Switching Frequency vs. Temperature



Quiescent Current vs. Temperature



V_{IN} UVLO Threshold vs. Temperature



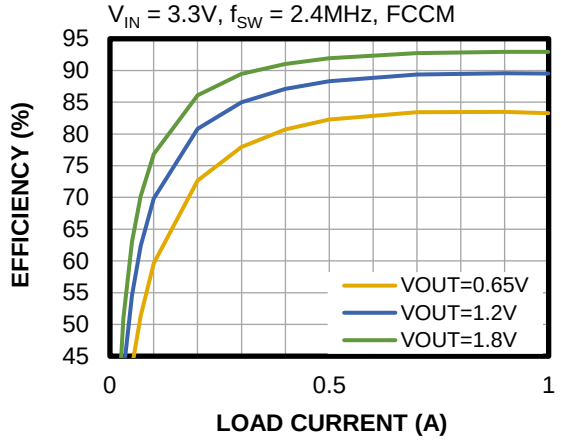
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3V, V_{OUT} = 1.2V, C_{OUT} = 2 x 22µF, T_A = 25°C, unless otherwise noted.

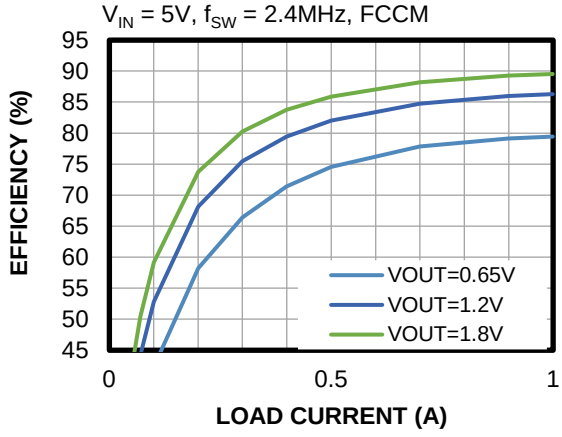
Efficiency vs. Load Current

V_{IN} = 3.3V, f_{SW} = 2.4MHz, FCCM



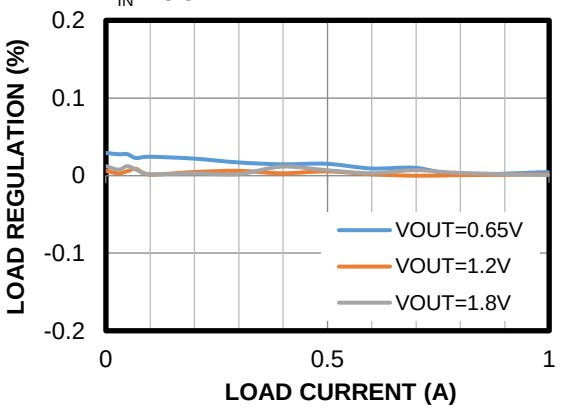
Efficiency vs. Load Current

V_{IN} = 5V, f_{SW} = 2.4MHz, FCCM



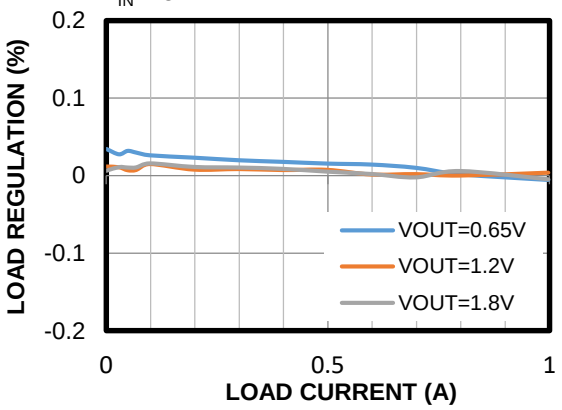
Load Regulation

V_{IN} = 3.3V



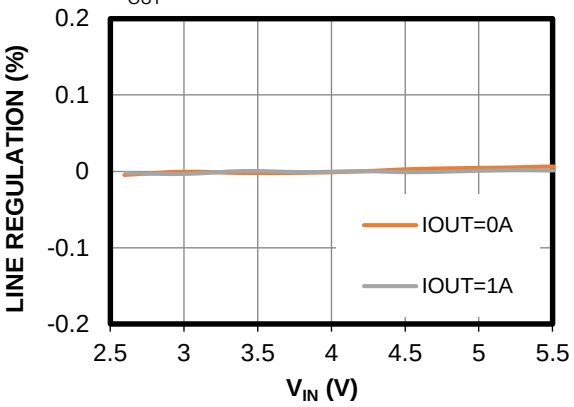
Load Regulation

V_{IN} = 5V



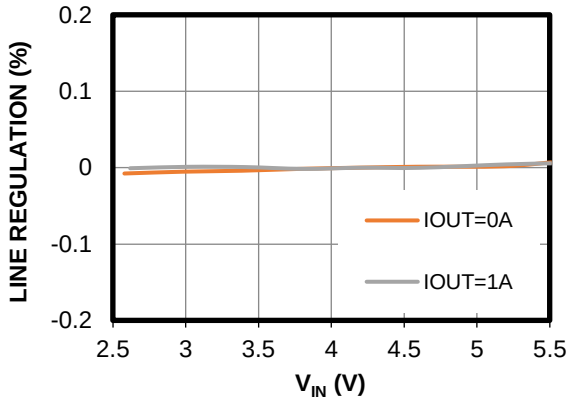
Line Regulation

V_{OUT} = 0.65V



Line Regulation

V_{OUT} = 1.2V



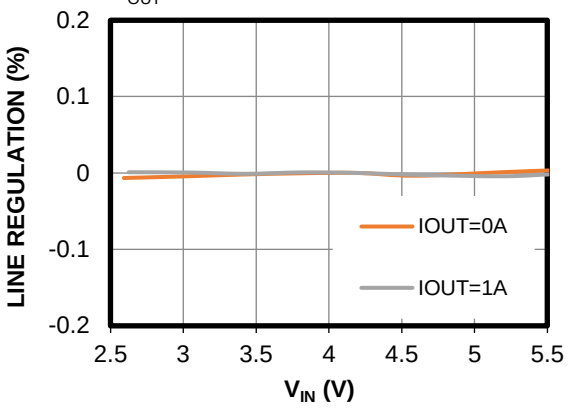
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 1.2V, C_{OUT} = 2 x 22µF, T_A = 25°C, unless otherwise noted.

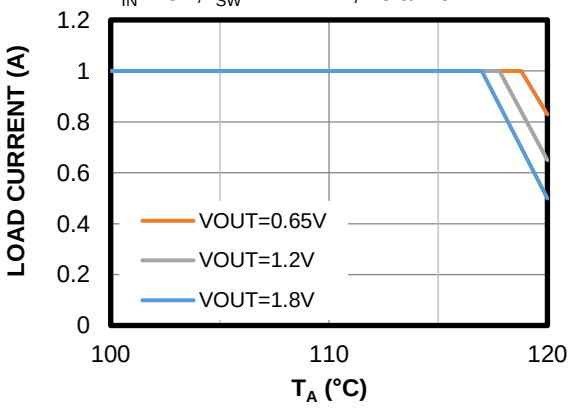
Line Regulation

V_{OUT} = 1.8V



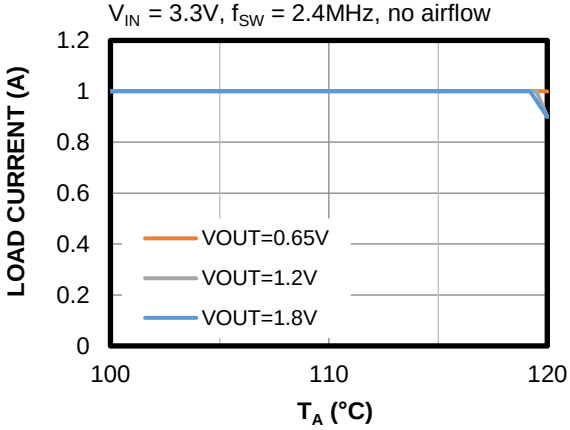
Thermal Derating

V_{IN} = 5V, f_{SW} = 2.4MHz, no airflow



Thermal Derating

V_{IN} = 3.3V, f_{SW} = 2.4MHz, no airflow



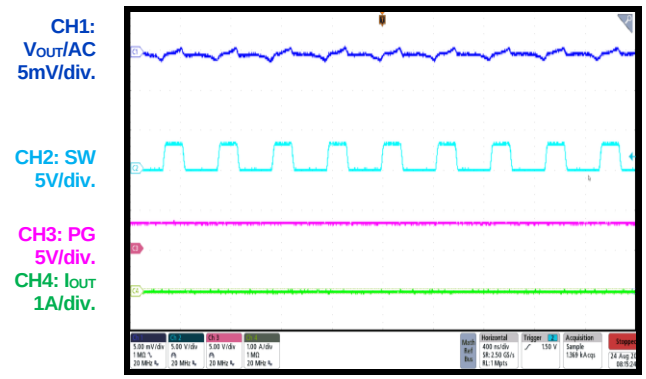
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 1.2V, C_{OUT} = 2 x 22µF, T_A = 25°C, unless otherwise noted.

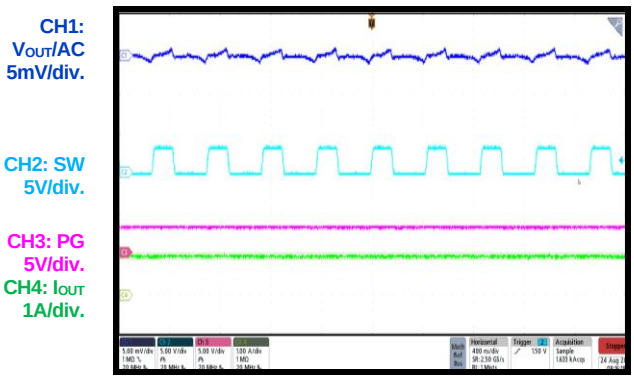
Steady State

V_{IN} = 3.3V, V_{OUT} = 1.2V, I_{OUT} = 0A



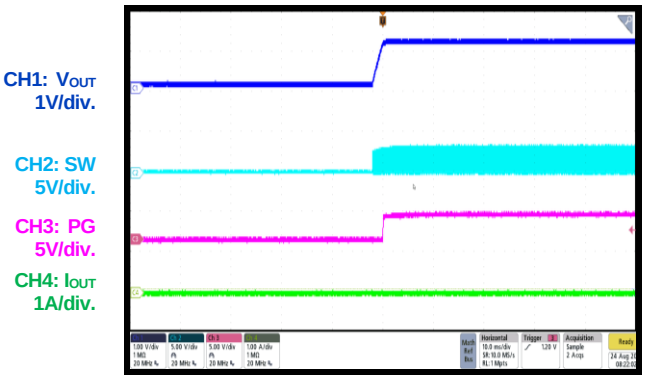
Steady State

V_{IN} = 3.3V, V_{OUT} = 1.2V, I_{OUT} = 1A



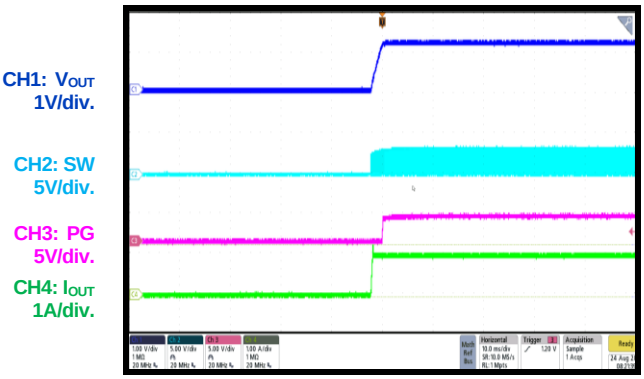
Start-Up through VIN

V_{IN} = 3.3V, V_{OUT} = 1.2V, I_{OUT} = 0A



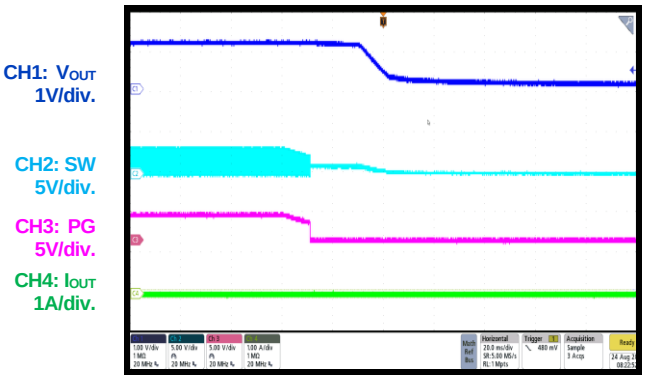
Start-Up through VIN

V_{IN} = 3.3V, V_{OUT} = 1.2V, I_{OUT} = 1A



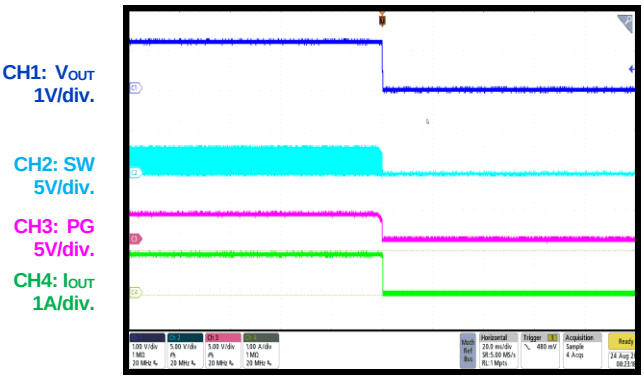
Shutdown through VIN

V_{IN} = 3.3V, V_{OUT} = 1.2V, I_{OUT} = 0A



Shutdown through VIN

V_{IN} = 3.3V, V_{OUT} = 1.2V, I_{OUT} = 1A



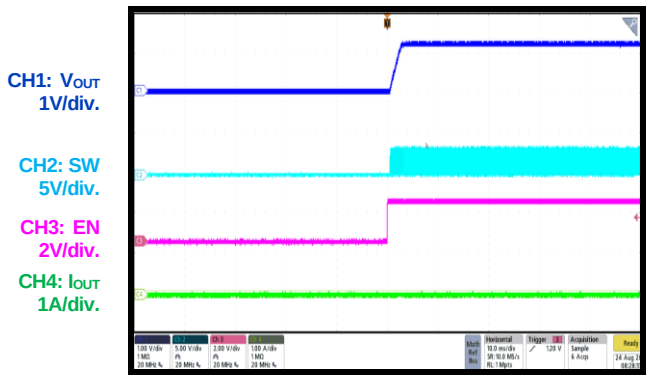
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 1.2V, C_{OUT} = 2 x 22µF, T_A = 25°C, unless otherwise noted.

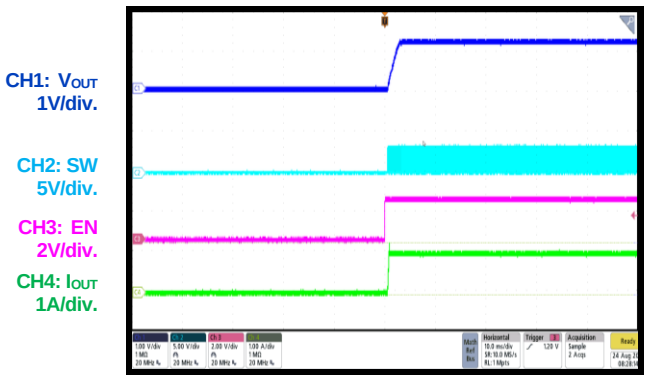
Start-Up through EN

V_{IN} = 3.3V, V_{OUT} = 1.2V, I_{OUT} = 0A



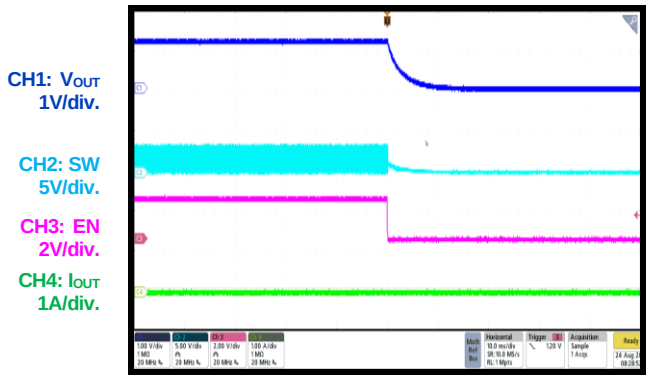
Start-Up through EN

V_{IN} = 3.3V, V_{OUT} = 1.2V, I_{OUT} = 1A



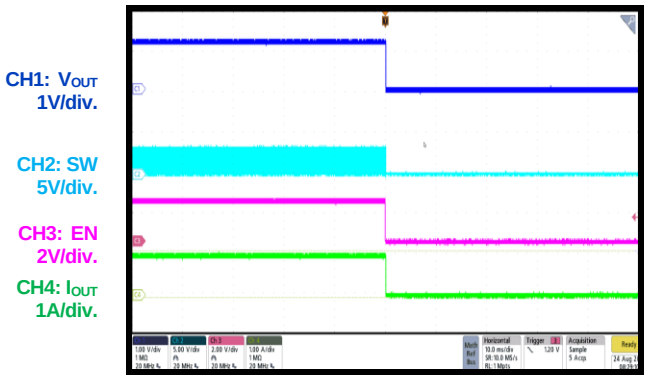
Shutdown through EN

V_{IN} = 3.3V, V_{OUT} = 1.2V, I_{OUT} = 0A



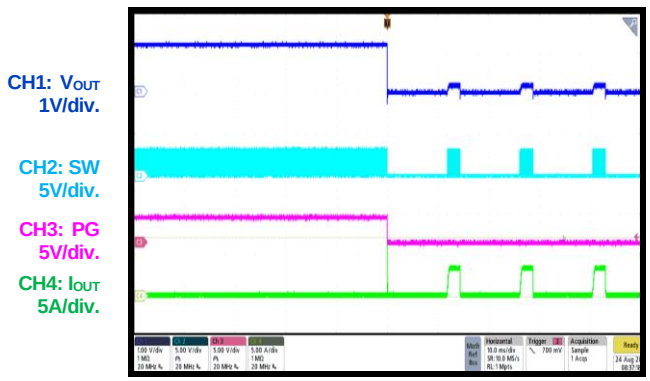
Shutdown through EN

V_{IN} = 3.3V, V_{OUT} = 1.2V, I_{OUT} = 1A



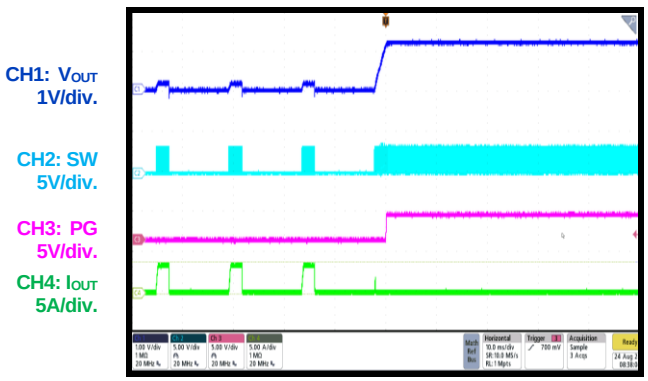
SCP Entry

V_{IN} = 3.3V, V_{OUT} = 1.2V, I_{OUT} = 0A



SCP Recovery

V_{IN} = 3.3V, V_{OUT} = 1.2V, I_{OUT} = 0A



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

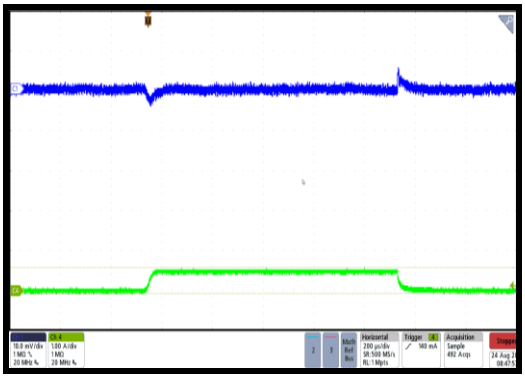
V_{IN} = 3.3V, V_{OUT} = 1.2V, C_{OUT} = 2 x 22µF, T_A = 25°C, unless otherwise noted.

Load Transient

V_{IN} = 3.3V, V_{OUT} = 1.2V, I_{OUT} = 0A to 0.5A, 0.8A/µs, e-load

CH1: V_{OUT}/AC 10mV/div.

CH4: I_{OUT} 1A/div.

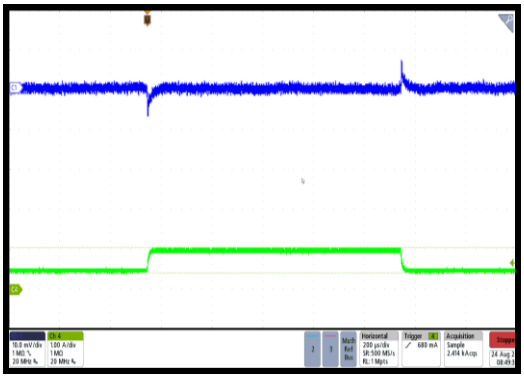


Load Transient

V_{IN} = 3.3V, V_{OUT} = 1.2V, I_{OUT} = 0.5A to 1A, 0.8A/µs, e-load

CH1: V_{OUT}/AC 10mV/div.

CH4: I_{OUT} 1A/div.



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

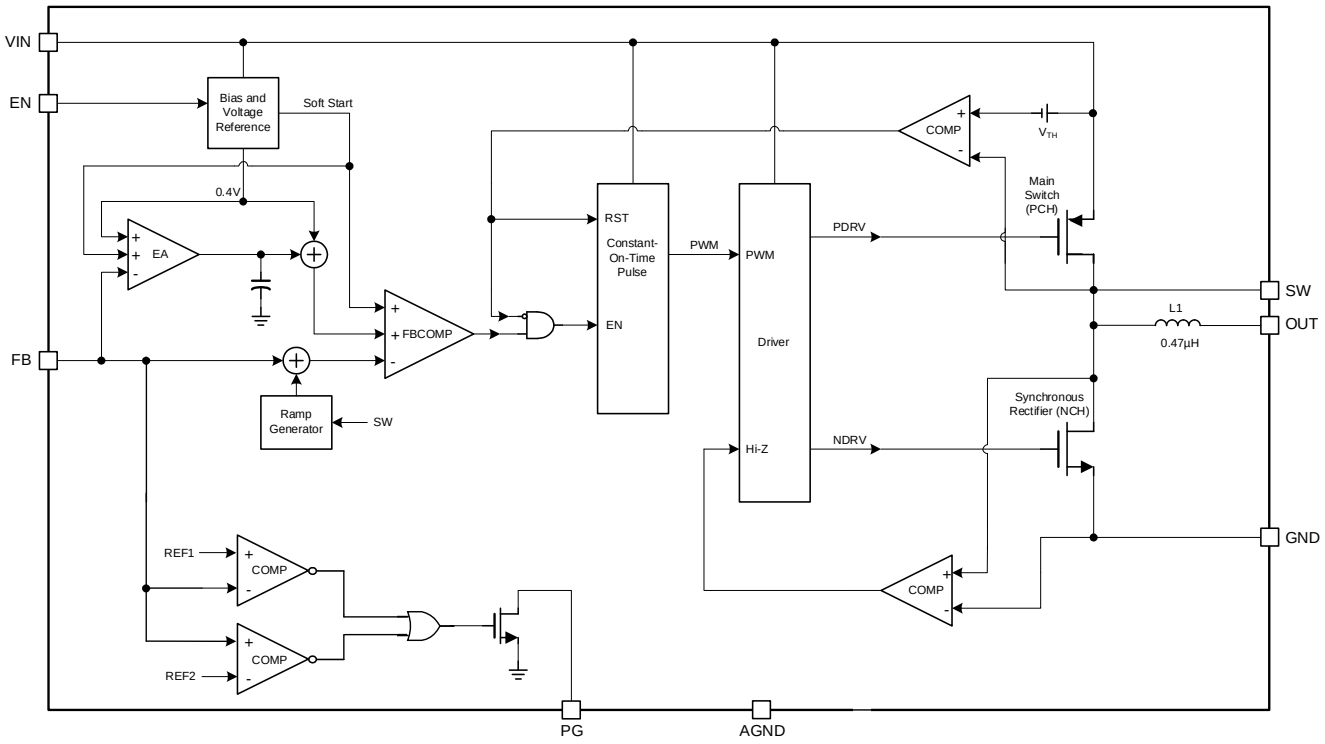


Figure 1: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

OPERATION

The MPM3816C uses constant-on-time (COT) control with input voltage (V_{IN}) feed-forward to stabilize the switching frequency (f_{SW}) across the entire V_{IN} range. It achieves up to 1A of continuous output current (I_{OUT}) from a 2.7V to 5.5V V_{IN}, with excellent load and line regulation. The output voltage (V_{OUT}) can be regulated to as low as 0.4V.

Constant-On-Time (COT) Control

Compared to fixed-frequency pulse-width modulation (PWM) control, COT control offers a simpler control loop and faster transient response. By using V_{IN} feed-forward, the MPM3816C maintains a nearly constant f_{SW} across the V_{IN} and V_{OUT} ranges. The switching pulse on time (t_{ON}) can be estimated with Equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 0.417\mu s \quad (1)$$

To prevent inductor current (I_L) runaway during the load transient, the MPM3816C has a fixed minimum off time and valley current protection.

Enable (EN)

When V_{IN} exceeds the under-voltage lockout (UVLO) threshold, the MPM3816C can be enabled by pulling EN above 1.2V. Leave EN floating or pull EN down to GND to disable the MPM3816C. There is an internal 1.7MΩ resistor connected from the EN pin to GND.

When the device is disabled, the part goes into output discharge mode automatically. The internal discharge MOSFET provides a resistive discharge path for the output capacitor (C_{OUT}).

Internal Soft Start (SS)

The MPM3816C has an internal soft start (SS) that ramps up V_{OUT} at a controlled slew rate to avoid overshoot during start-up. The soft-start time (t_{SS_ON}) is typically about 2ms.

Current Limit

The MPM3816C typically has a typical 3A high-side MOSFET (HS-FET) current limit. When the high-side switch reaches its current limit and V_{OUT} drops to 50% of its set value, the MPM3816C enters hiccup mode to periodically restart the part. This prevents I_L from continuing to rise and possibly damaging components.

Short-Circuit Protection (SCP) and Recovery

If the MPM3816C's output is shorted to GND and reaches the current limit, the part enters short-circuit protection (SCP). It then tries to recover with hiccup mode. The MPM3816C disables the power stage, discharges the SS capacitor (C_{SS}), and attempts to SS again automatically. If the short-circuit condition remains after SS ends, the MPM3816C repeats this cycle until the short circuit is removed and the V_{OUT} rises back to the regulation level.

Power Good (PG) Indicator

The MPM3816C has an open-drain output and requires an external pull-up resistor (100kΩ to 500kΩ) for the power good (PG) indicator. When the feedback (FB) voltage (V_{FB}) exceeds 90% of the regulation voltage, V_{PG} is pulled up to V_{OUT} or V_{IN} by the external resistor. If V_{FB} exceeds the PG under-voltage (UV) falling threshold or PG OV rising threshold, the internal MOSFET pulls PG to GND.

If VIN and EN are not available, PG is clamped low, even though PG is tied to an external DC source through a pull-up resistor. Figure 2 shows the relationship between the PG voltage and the pull-up current.

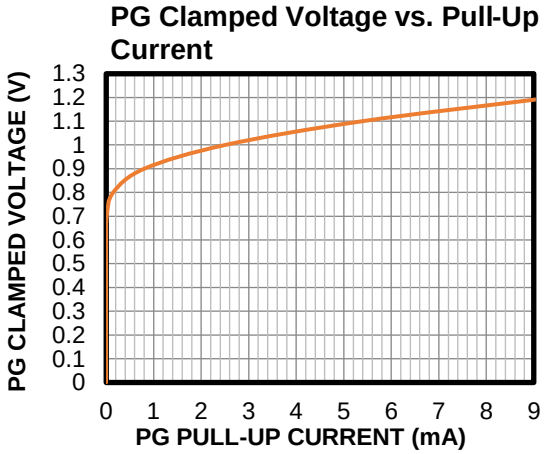


Figure 2: PG Clamped Voltage

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage (V_{OUT}) (see Figure 3). Select the feedback (FB) resistor (R1, also called R_{FB}) that reduces the V_{OUT} leakage current (typically between 5kΩ and 10kΩ). There is no strict requirement on R1; it is recommended for R1 to be about 10kΩ. R2 can then be calculated with Equation (2):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.4} - 1} \quad (2)$$

Figure 3 shows the FB circuit.

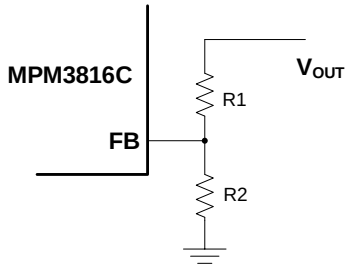


Figure 3: Feedback Network

Table 1 shows the recommended resistances for common output voltages.

Table 1: Resistances for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
0.65	10	16
0.95	9.31	6.8
1.2	10	4.99
1.8	9.31	2.7

Maximum Output Voltage

The maximum V_{OUT} (V_{OUT_MAX}) is determined by maximum on time (t_{ON_MAX}) and minimum off time (t_{OFF_MIN}). V_{OUT_MAX} can be calculated with Equation (3):

$$V_{OUT_MAX} = \frac{V_{IN} \times t_{ON_MAX}}{t_{ON_MAX} + t_{OFF_MIN}} \quad (3)$$

When t_{OFF_MIN} is triggered, the MPM3816C decreases the switching frequency (f_{SW}) to regulate V_{OUT} until t_{ON_MAX} is triggered. t_{OFF_MIN} is about 80ns. t_{ON_MAX} can be estimated with Equation (4):

$$t_{ON_MAX} = \frac{7.2\mu s}{V_{IN}} \quad (4)$$

For example, if V_{IN} = 5V, the calculated t_{ON_MAX} is 1.44µs, so V_{OUT_MAX} is about 4.7V with no load, which may have a slight shift as the load current increases due to the voltage drop across the power MOSFET, inductor resistance, and PCB resistance.

Selecting the Input Capacitor

The step-down converter has a discontinuous input current (I_{IN}) and requires a capacitor to supply the AC current to the converter while maintaining the DC V_{IN}. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

The input capacitor (C1, also called C_{IN}) requires an adequate ripple current rating, because it absorbs the input switching current. Estimate the RMS current in C1 (I_{C1}) with Equation (5):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

The worst-case scenario occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (6):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

C1 can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic 0.1µF capacitor as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at the input. The V_{IN} ripple (ΔV_{IN}) caused by the capacitance can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

Selecting the Output Capacitor

The output capacitor (C2, also called C_{OUT}) stabilizes the DC V_{OUT}. Ceramic capacitors are recommended. Low-ESR capacitors are preferred to limit the V_{OUT} ripple (ΔV_{OUT}). Estimate ΔV_{OUT} with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (8)$$

Where L is the inductance (0.47µH), and R_{ESR} is the equivalent series resistance (ESR) of C2.

When using ceramic capacitors, the capacitance dominates the impedance at f_{SW} and causes most of ΔV_{OUT}. For simplification, ΔV_{OUT} can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated with Equation (10):

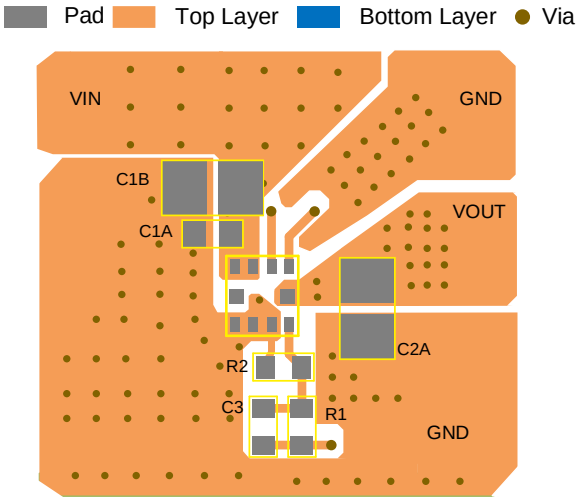
$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (10)$$

The characteristics of C2 also affect the stability of the regulation system.

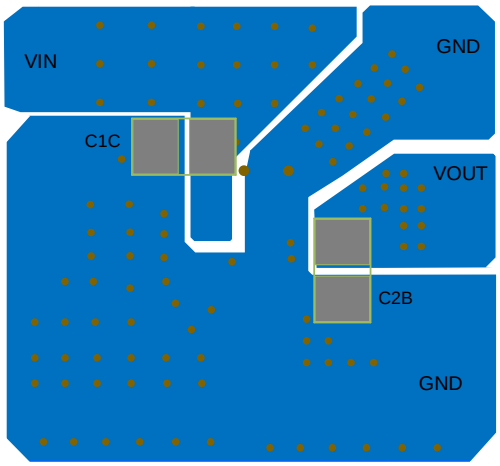
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best performance, refer to Figure 4 and follow the guidelines below.

1. Place the MLCC input capacitors as close to the VIN and GND pins as possible.
2. Place all signal traces far away from SW.
3. Maximize the VIN and GND copper plane to minimize parasitic impedance.
4. Ensure that the high-current paths (GND, VIN, and VOUT) have short, direct, and wide traces.
5. Place as many GND vias as possible close to the GND pin to minimize both the parasitic impedance and thermal resistance.
6. Place the external feedback network next to the FB pin.
7. Keep the feedback network away from the switching node.



Top Layer



Bottom Layer

Figure 4: Recommended PCB Layout

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUIT

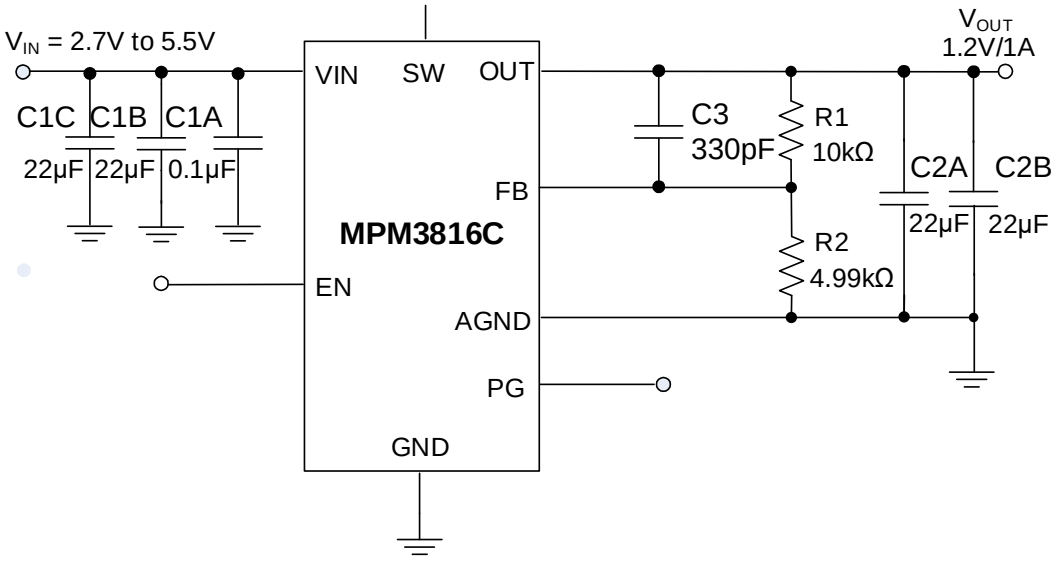


Figure 5: Typical Application Circuit (10)

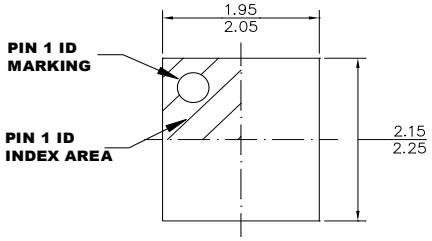
Note:

10) V_{IN} < 3.3V may require more input capacitance.

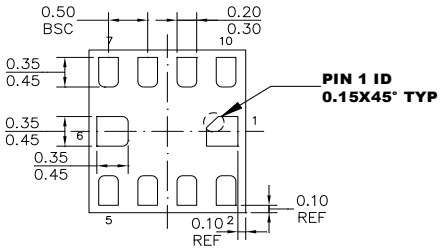
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

PACKAGE INFORMATION

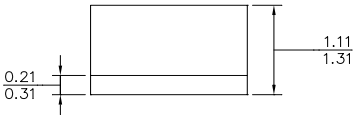
ECLGA-10 (2mmx2.2mmx1.2mm)



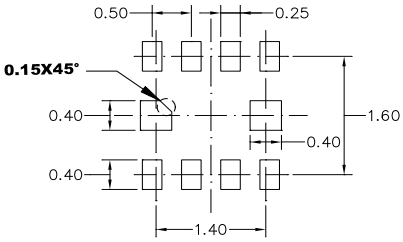
TOP VIEW



BOTTOM VIEW



SIDE VIEW



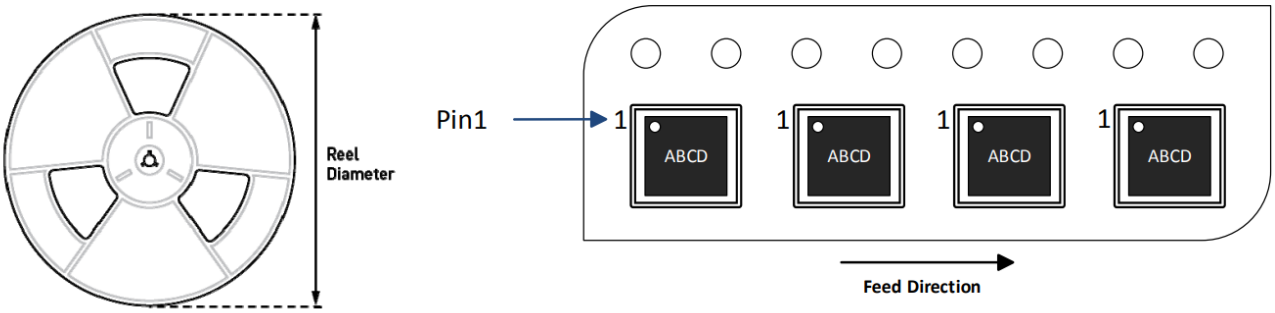
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-303.
4) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM3816CGPE -Z	ECLGA-10 (2mmx2.2mmx1.2mm)	2500	N/A	N/A	13in	12mm	8mm

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	8/22/2025	Initial Release	-

Notice: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.