



MPM3809

2.3V to 5.5V Input, 0.6A, PSM Power Module with Ultra-Small Package

DESCRIPTION

The MPM3809 is a monolithic, step-down switch-mode converter with built-in, internal power MOSFETs and an inductor. The MPM3809 achieves 0.6A of continuous output current (I_{OUT}) from a 2.3V to 5.5V input voltage (V_{IN}) range, with excellent load and line regulation.

The MPM3809 is ideal for a wide range of applications, including high-performance digital signal processors (DSPs), wireless power, portable and mobile devices, and other low-power systems. The output voltage (V_{OUT}) can be regulated to as low as 0.6V. Only input capacitors, output capacitors, and feedback (FB) resistors are needed to complete the design.

The constant-on-time (COT) control scheme provides fast transient response, high light-load efficiency, and facilitates loop stabilization.

Full protection features include cycle-by-cycle current limiting and thermal shutdown.

The MPM3809 requires a minimal number of readily available, standard external components and is available in an ultra-small ECLGA-6 (1.5mmx2mmx1mm) package.

FEATURES

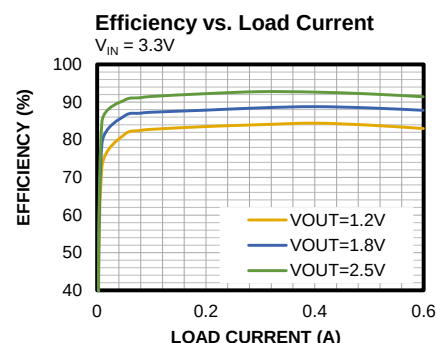
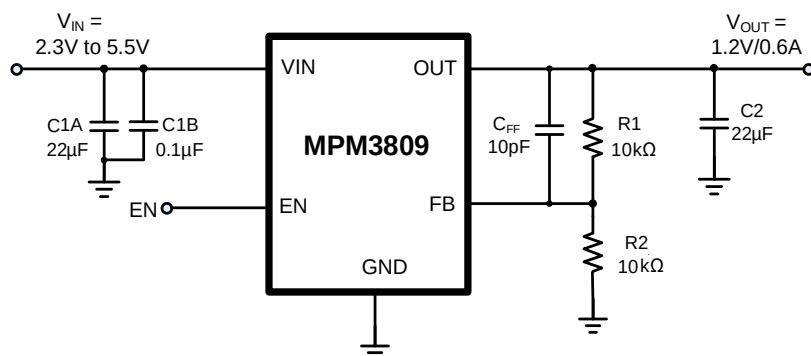
- Wide 2.3V to 5.5V Operating Input Voltage (V_{IN}) Range
- Output Voltage (V_{OUT}) as Low as 0.6V
- 100% Duty Cycle in Dropout
- 0.6A Output Current (I_{OUT})
- 2.4MHz Switching Frequency (f_{SW})
- EN for Power Sequencing
- Cycle-by-Cycle Over-Current Protection (OCP)
- 0.5ms Internal Soft-Start (SS) Time (t_{SS-ON})
- Output Discharge
- Short-Circuit Protection (SCP) with Hiccup Mode
- Thermal Shutdown
- Stable with Low-ESR, Ceramic Output Capacitors
- Available in an ECLGA-6 (1.5mmx2mmx1mm) Package

APPLICATIONS

- Optical Modules
- Industrial Products
- Internet of Things (IoT) Devices
- Space-Constrained Applications
- Low-Voltage I/O Supplies
- Low-Dropout Regulator (LDO) Replacements

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TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPM3809GPH	ECLGA-6 (1.5mmx2mmx1mm)	See Below	3

* For Tape & Reel, add suffix -Z (e.g. MPM3809GPH-Z).

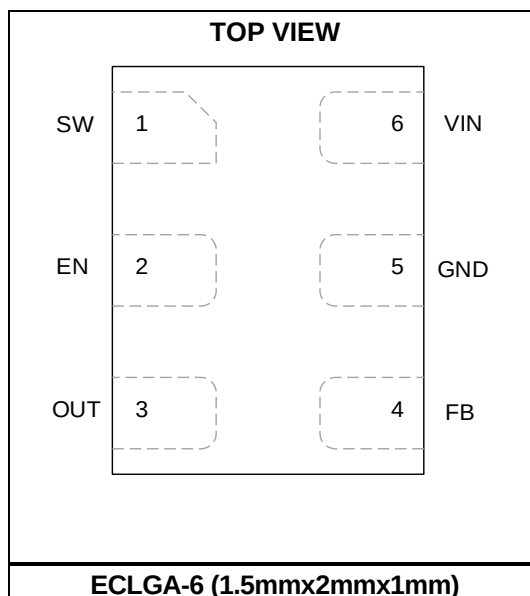
TOP MARKING

QK
LL

QK: Product code of MPM3809GPH

LL: Lot number

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	SW	Output switching node. The SW pin is a test pin. It can be left floating.
2	EN	On/off control.
3	OUT	Output voltage (V_{OUT}) power rail and input sense pin for V_{OUT}. Connect the load to the OUT pin. An output capacitor is required at OUT to reduce the output voltage ripple.
4	FB	Feedback. An external resistor divider from the output to GND, and tapped to FB, sets the output voltage.
5	GND	Power ground.
6	VIN	Supply voltage. The MPM3809 operates from a 2.3V to 5.5V unregulated input voltage (V _{IN}) range. A decoupling capacitor is required to prevent large voltage spikes from appearing at the input.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Supply voltage (V_{IN}) 6V
V_{SW} -0.3V (-5V for <10ns)
to +6V (+8V for <10ns or +10V for <3ns)
All other pins -0.3V to +6V
Junction temperature (T_J) 150°C
Lead temperature 260°C
Continuous power dissipation (T_A = 25°C) ^{(2) (4)}
..... 2.85W
Storage temperature -65°C to +150°C

Recommended Operating Conditions ⁽³⁾

Supply voltage (V_{IN}) 2.3V to 5.5V
Operating junction temp (T_J) ... -40°C to +125°C

Thermal Resistance ^{(4) (5) (6) (7)}

ECLGA-6 (1.5mmx2mmx1mm)

θ_{JA} 43.87°C/W
θ_{JC_TOP} 24.98°C/W

Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- θ_{JA} is the junction-to-ambient thermal resistance, θ_{JC_TOP} is the junction-to-case top thermal characterization parameter, and θ_{JB} is the junction-to-board thermal characterization parameter.
- The thermal parameter is based on tests on an MPS evaluation board (EVM3809 -PH-01A) under no airflow cooling conditions in a standard enclosure. The board size is 5.1cmx5.1cm, 4 layers, of which top and bottom layer's copper thickness is 2oz.
- The junction-to-case top thermal characterization parameter, θ_{JC_TOP}, estimates the junction temperature in the real system, based on equation T_J = θ_{JC_TOP} × P_{LOSS} + T_{CASE_TOP}, where P_{LOSS} is the entire loss of module in a real application, and T_{CASE_TOP} is the case top temperature.
- Junction-to-board thermal characterization parameter, θ_{JB}, estimation the junction temperature in the real system, based on equation T_J = θ_{JB} × P_{LOSS} + T_{BOARD}, where P_{LOSS} is the entire loss of module at real application, T_{BOARD} is the board temperature.

ELECTRICAL CHARACTERISTICS

$V_{IN} = 3.6V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$ ⁽⁸⁾, typical value is tested at $T_J = 25^{\circ}C$. The over-temperature limit is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Feedback voltage ⁽⁸⁾	V_{FB}	$2.3V \leq V_{IN} \leq 5.5V$, $T_J = -40^{\circ}C$ to $+85^{\circ}C$	0.594	0.600	0.606	V
		$2.3V \leq V_{IN} \leq 5.5V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$	0.591	0.600	0.609	
Feedback current	I_{FB}	$V_{FB} = 0.63V$		50	100	nA
Dropout resistance	R_{DR}	100% on duty cycle		250		m Ω
Switch leakage		$V_{EN} = 0V$		0	1	μA
P-channel MOSFET peak current limit			1.4	1.9		A
N-channel MOSFET valley current limit				1.2		A
Switching frequency ⁽⁹⁾	f_{SW}	$V_{OUT} = 1.2V$, $I_{OUT} = 500mA$		2400		kHz
Minimum off time ⁽⁹⁾	$t_{MIN-OFF}$			60		ns
Minimum on time ⁽⁹⁾	t_{MIN-ON}			60		ns
Soft-start time	t_{SS-ON}	V_{OUT} rises from 10% to 90%		0.5		ms
Under-voltage lockout (UVLO) rising threshold				2	2.25	V
UVLO threshold hysteresis				150		mV
EN input logic low voltage					0.4	V
EN input logic high voltage			1.2			V
EN input current		$V_{EN} = 2V$		1.2		μA
		$V_{EN} = 0V$		0		μA
Supply current (shutdown)		$V_{EN} = 0V$		0	1	μA
Supply current (quiescent)		$V_{IN} = 3.6V$, $V_{EN} = 2V$, $V_{FB} = 0.63V$		330	450	μA
Thermal shutdown ⁽⁹⁾				160		$^{\circ}C$
Thermal hysteresis ⁽⁹⁾				30		$^{\circ}C$
Output discharge resistor	R_{DIS}	$V_{EN} = 0V$, $V_{OUT} = 1.2V$		1		k Ω

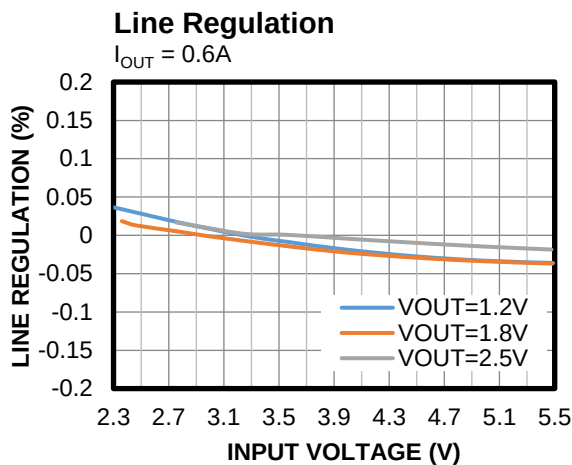
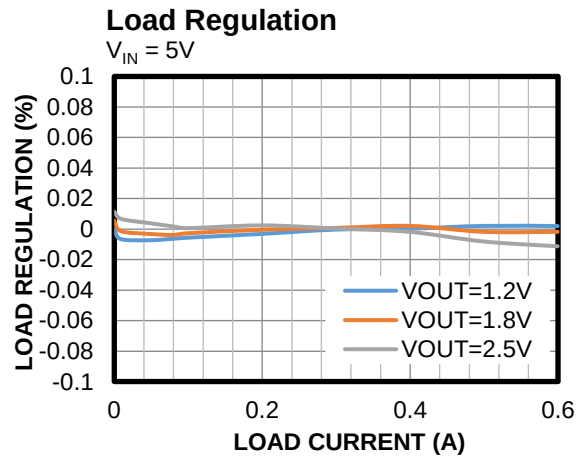
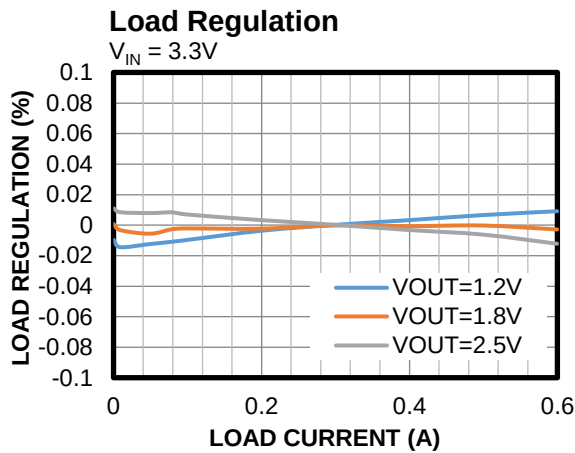
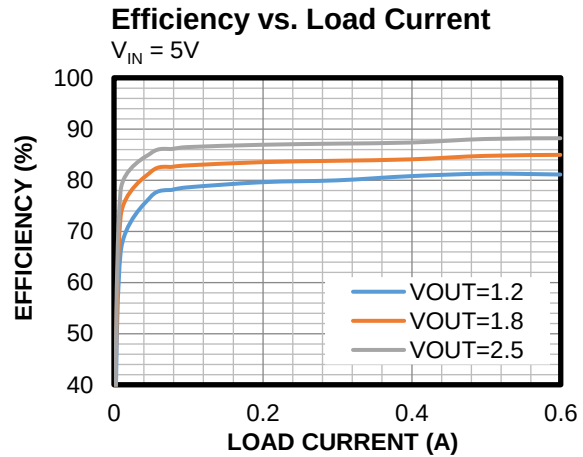
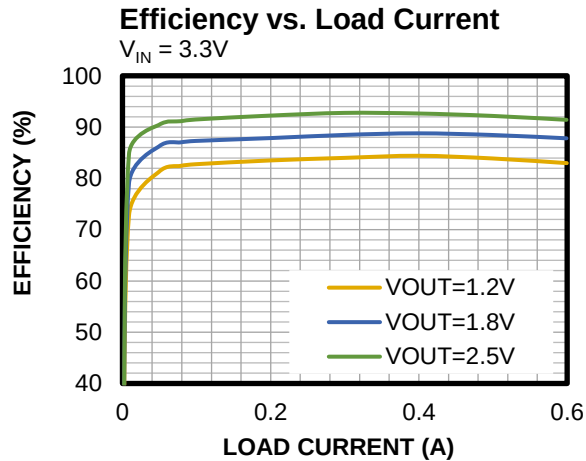
Notes:

8) Not tested in production. Guaranteed by over-temperature correlation.

9) Guaranteed by engineering sample characterization.

TYPICAL CHARACTERISTICS

Performance curves are test on the evaluation board. $V_{IN} = 3.3V$, $V_{OUT} = 1.2V$, $C_{IN} = 22\mu F$, $C_{OUT} = 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

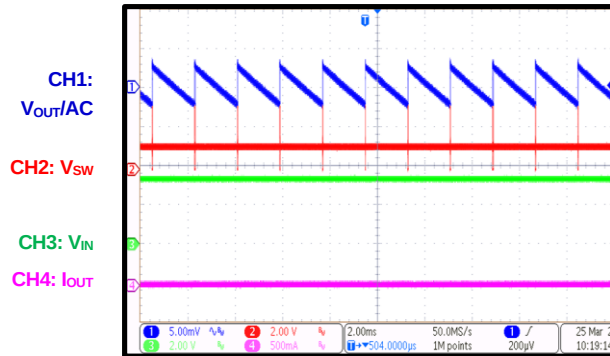


TYPICAL CHARACTERISTICS (continued)

Performance curves are test on the evaluation board. $V_{IN} = 3.3V$, $V_{OUT} = 1.2V$, $C_{IN} = 22\mu F$, $C_{OUT} = 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

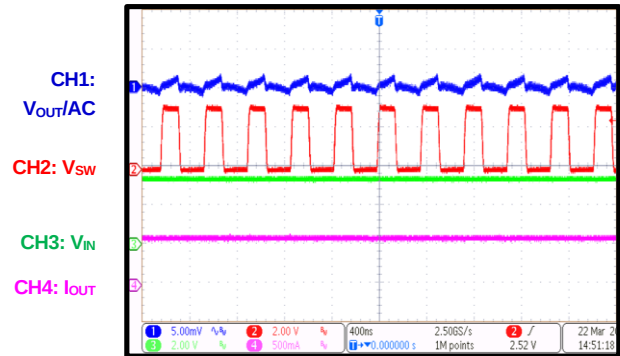
Steady State

$V_{IN} = 3.3V$, $V_{OUT} = 1.2V$, $I_{OUT} = 0A$



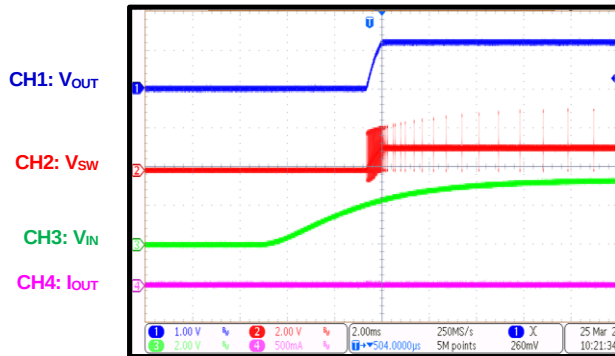
Steady State

$V_{IN} = 3.3V$, $V_{OUT} = 1.2V$, $I_{OUT} = 0.6A$



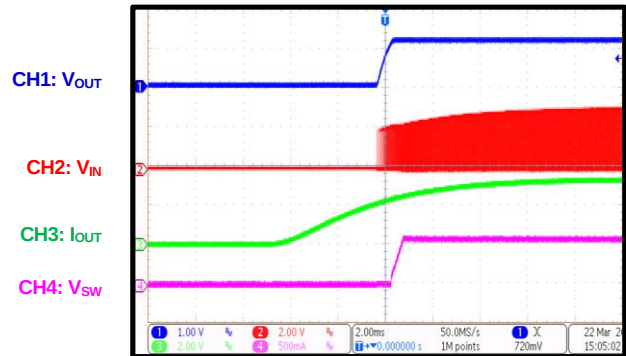
Start-Up through VIN

$V_{IN} = 3.3V$, $V_{OUT} = 1.2V$, $I_{OUT} = 0A$



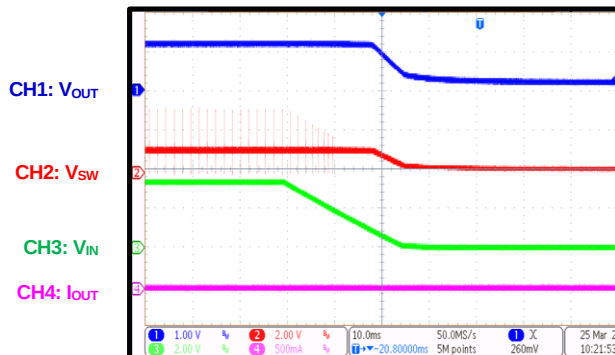
Start-Up through VIN

$V_{IN} = 3.3V$, $V_{OUT} = 1.2V$, $I_{OUT} = 0.6A$



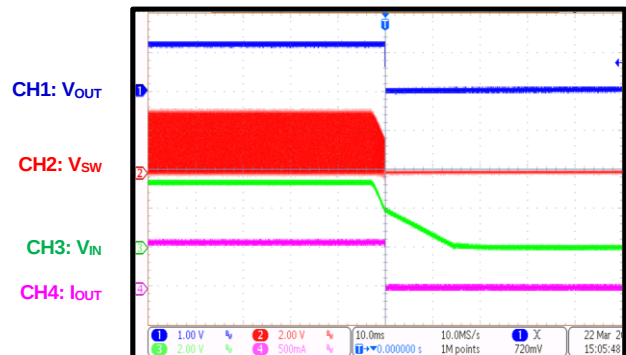
Shutdown through VIN

$V_{IN} = 3.3V$, $V_{OUT} = 1.2V$, $I_{OUT} = 0A$



Shutdown through VIN

$V_{IN} = 3.3V$, $V_{OUT} = 1.2V$, $I_{OUT} = 0.6A$

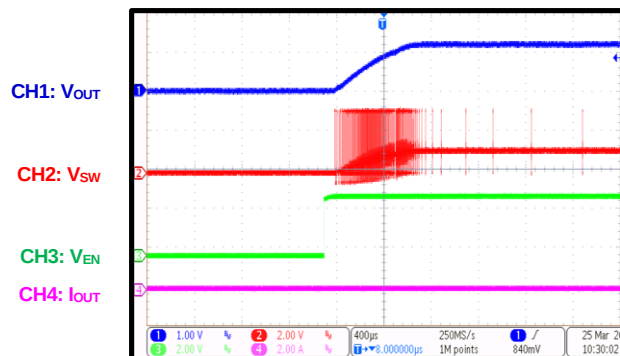


TYPICAL CHARACTERISTICS (continued)

Performance curves are test on the evaluation board. $V_{IN} = 3.3V$, $V_{OUT} = 1.2V$, $C_{IN} = 22\mu F$, $C_{OUT} = 22\mu F$, $T_A = 25^{\circ}C$, unless otherwise noted.

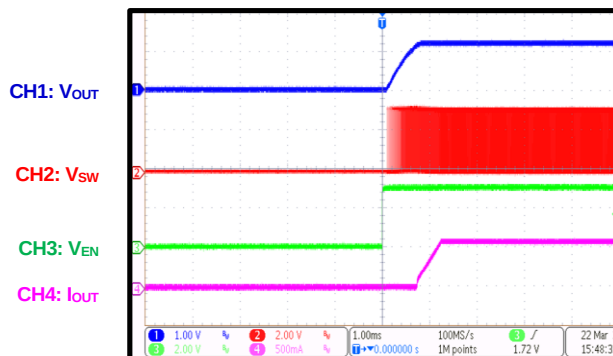
Start-Up through EN

$V_{IN} = 3.3V$, $V_{OUT} = 1.2V$, $I_{OUT} = 0A$



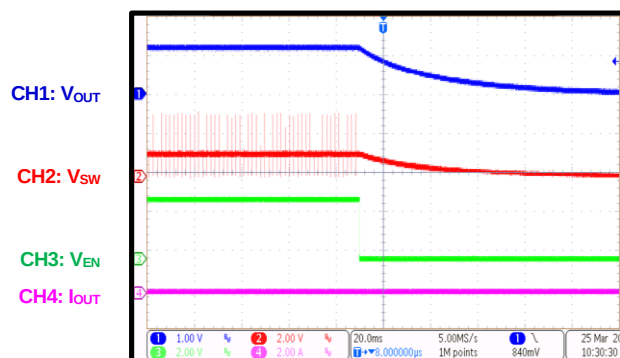
Start-Up through EN

$V_{IN} = 3.3V$, $V_{OUT} = 1.2V$, $I_{OUT} = 0.6A$



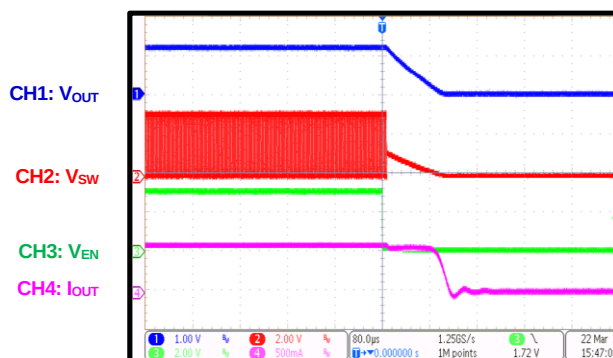
Shutdown through EN

$V_{IN} = 3.3V$, $V_{OUT} = 1.2V$, $I_{OUT} = 0A$



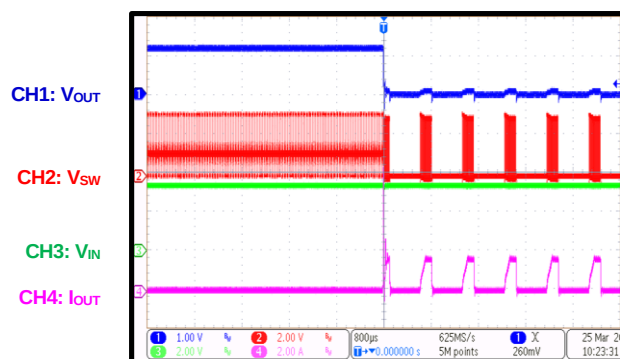
Shutdown through EN

$V_{IN} = 3.3V$, $V_{OUT} = 1.2V$, $I_{OUT} = 0.6A$



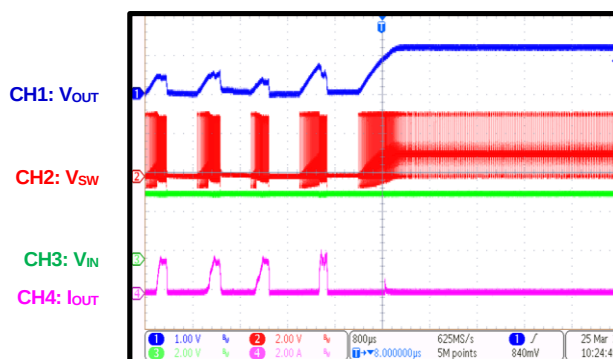
SCP Entry

$V_{IN} = 3.3V$, $V_{OUT} = 1.2V$, $I_{OUT} = 0A$



SCP Recovery

$V_{IN} = 3.3V$, $V_{OUT} = 1.2V$, $I_{OUT} = 0A$

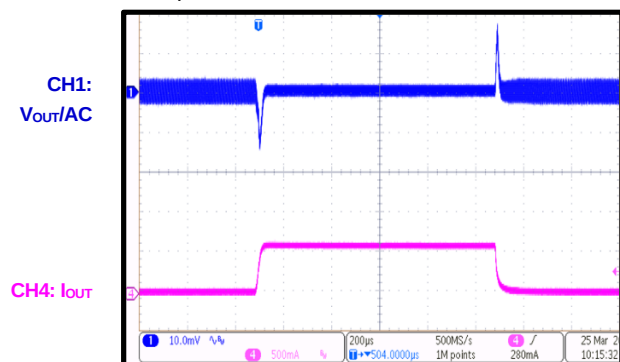


TYPICAL CHARACTERISTICS *(continued)*

Performance curves are test on the evaluation board. $V_{IN} = 3.3V$, $V_{OUT} = 1.2V$, $C_{IN} = 22\mu F$, $C_{OUT} = 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

Load Transient Response

$V_{IN} = 3.3V$, $V_{OUT} = 1.2V$, $I_{OUT} = 0A$ to $0.6A$,
 $0.8A/\mu s$ E-load



FUNCTIONAL BLOCK DIAGRAM

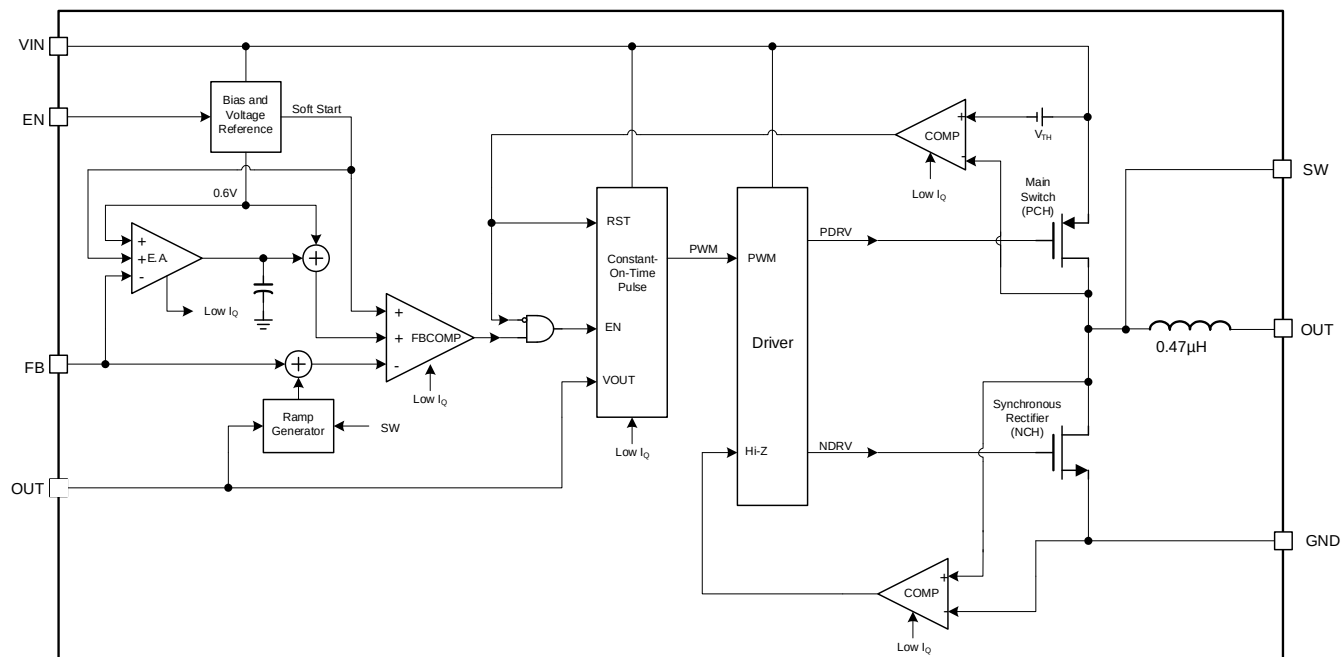


Figure 1: Functional Block Diagram

OPERATION

The MPM3809 uses constant-on-time (COT) control with input voltage (V_{IN}) feed-forward to stabilize the switching frequency (f_{SW}) across the entire V_{IN} range. The MPM3809 achieves 0.6A of continuous output current (I_{OUT}) from a 2.3V to 5.5V V_{IN} range, with excellent load and line regulation. The output voltage (V_{OUT}) can be regulated to as low as 0.6V.

Constant-On-Time (COT) Control

Compared to fixed-frequency pulse-width modulation (PWM) control, COT control offers a simpler control loop and faster transient response. By using V_{IN} feed-forward, the MPM3809 maintains a nearly constant f_{SW} across the V_{IN} and V_{OUT} ranges. The switching on-time pulse (t_{ON}) can be calculated with Equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 0.416\mu s \quad (1)$$

To prevent inductor current (I_L) runaway during the load transient, the MPM3809 has a fixed minimum off time of 60ns. This minimum off time limit does not affect steady state operation.

Power-Save Mode (PSM) at Light Loads

The MPM3809 uses advanced asynchronous modulation (AAM) mode and power-save mode (PSM) with a zero-current detection (ZCD) circuit for light-load operation (see Figure 2). The AAM mode current (I_{AAM}) is set internally. Under light-load operation, the SW on-time pulse is determined by the on-time generator and AAM mode comparator. The MPM3809 works in PSM to achieve excellent efficiency at light loads.

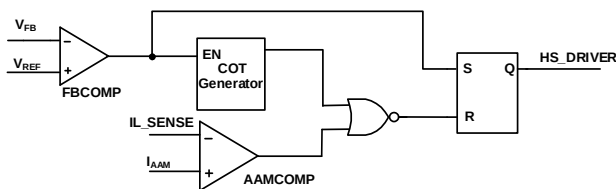


Figure 2: Simplified AAM Mode Control Logic

The MPM3809 uses ZCD to determine when I_L begins reversing.

When I_L reaches the ZCD threshold, the low-side MOSFET (LS-FET) turns off. AAM mode and the ZCD circuit work together to make the MPM3809 work in discontinuous conduction mode (DCM) continuously at light loads, even if V_{OUT} is almost equal to V_{IN} .

Enable (EN)

When V_{IN} exceeds the under-voltage lockout (UVLO) threshold (typically 2V), the MPM3809 can be enabled by pulling EN above 1.2V. Leave EN floating or pull EN down to ground to disable the MPM3809. There is an internal 1.7MΩ resistor connected from the EN pin to ground. When the device is disabled, the part goes into output discharge mode automatically. The internal discharge MOSFET provides a resistive discharge path for the output capacitor.

Soft Start (SS)

The MPM3809 has a built-in soft start (SS) that ramps up V_{OUT} at a controlled slew rate to avoid overshooting at start-up. The soft-start time (t_{SS-ON}) is about 0.5ms, typically.

Current Limit

The MPM3809 has a 1.9A high-side MOSFET (HS-FET) current limit, typically. When the HS-FET reaches its current limit, the MPM3809 remains in hiccup mode until the current drops. This prevents I_L from continuing to rise and damaging components.

Short-Circuit Protection (SCP) and Recovery

The MPM3809 enters short-circuit protection (SCP) mode when it reaches the current limit, and it attempts to recover with hiccup mode. The MPM3809 disables the output power stage, discharges the soft-start capacitor, and attempts to soft start again automatically. If the short-circuit condition remains after soft start ends, the MPM3809 repeats this cycle until the short circuit is removed and the output rises back to the regulation level.

APPLICATION INFORMATION

Setting the Output Voltage (V_{OUT})

The external resistor divider sets the output voltage (see Figure 5 on page 13). Select the feedback resistor (R1) to reduce the V_{OUT} leakage current; typically. There is no strict requirement for the feedback resistor. Selecting R1 to be 10k Ω is sufficient for most applications. R2 can be calculated with Equation (2):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6} - 1} \quad (2)$$

Figure 3 shows the feedback circuit.

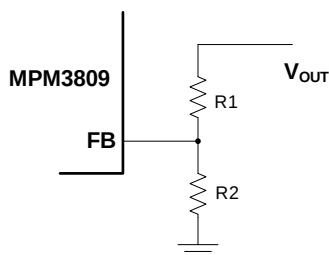


Figure 3: Feedback Network

Table 1 shows the recommended resistor values for common output voltages.

Table 1: Resistor Values for Common Output Voltages

V_{OUT} (V)	R1 (k Ω)	R2 (k Ω)
1.0	10 (1%)	15 (1%)
1.2	10 (1%)	10 (1%)
1.8	10 (1%)	5 (1%)
2.5	11.3 (1%)	3.6 (1%)
3.3	10 (1%)	2.2 (1%)

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. Generally, a 22 μ F input capacitor is sufficient for most applications.

The input capacitor requires an adequate ripple current rating since it absorbs the input switching current. Estimate the input capacitor's RMS current with Equation (3):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (3)$$

The worst-case condition occurs at $V_{IN} = 2 \times V_{OUT}$, calculated with Equation (4):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (4)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality, 0.1 μ F, ceramic capacitor as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

Selecting the Output Capacitor

The output capacitor (C2) stabilizes the DC output voltage. Low-ESR ceramic capacitors are recommended to limit the output voltage ripple. Estimate the output voltage ripple with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (6)$$

Where L_1 is the inductance, and R_{ESR} is the output capacitor's equivalent series resistance (ESR). The MPM3809 has an internal, co-packaged, 0.47 μ H power inductor.

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be calculated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (8)$$

The output capacitor's characteristics also affect the system's regulation stability. Typically, a 22μF output capacitor is sufficient for most applications. Add additional output capacitance to achieve a low output voltage ripple.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best performance, refer to Figure 4 and follow the guidelines below:

1. Place the input MLCC capacitors as close to the VIN and PGND pins as possible.
2. Route all signal traces far away from SW.
3. Maximize the VIN and PGND copper plane to minimize parasitic impedance.
4. Ensure that the high-current paths (PGND, VIN, and VOUT) have short, direct, and wide traces.

5. Place as many PGND vias as possible close to PGND to minimize the parasitic impedance and thermal resistance.
6. Place the external feedback network next to FB.
7. Route the feedback network away from the switching node.

■ Pad ■ Top Layer ■ Bottom Layer ● Via

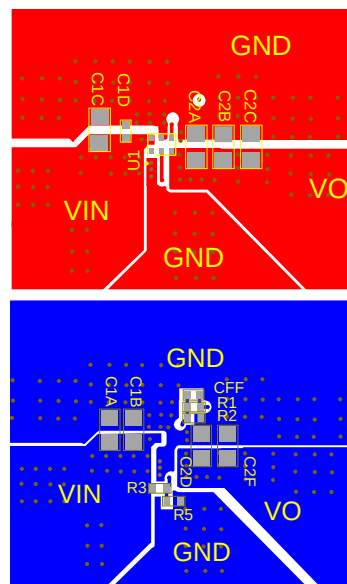


Figure 4: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

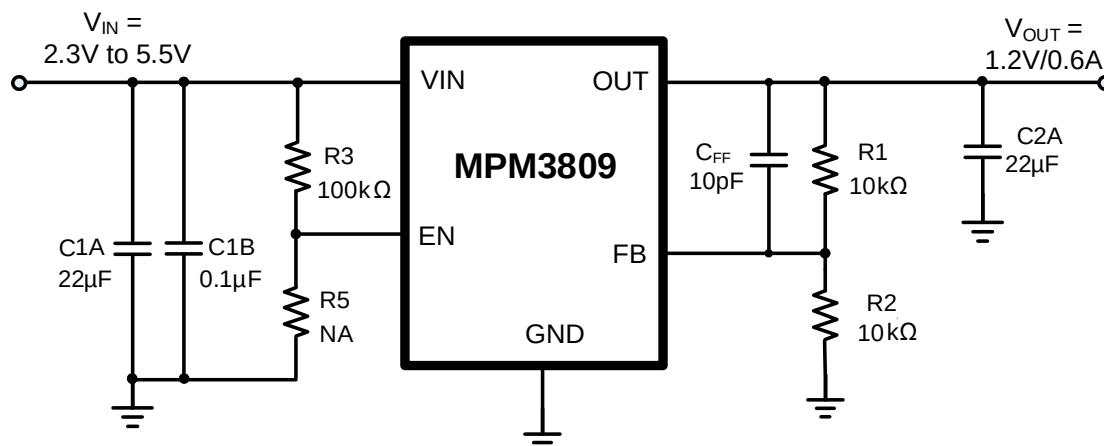
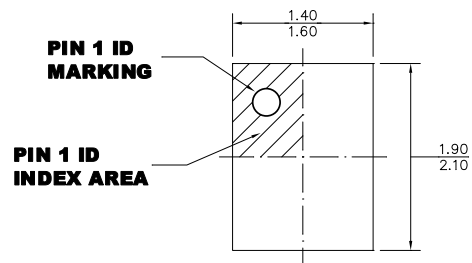


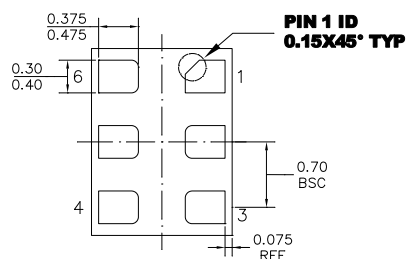
Figure 5: Typical Application Circuit

PACKAGE INFORMATION

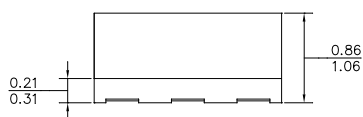
ECLGA-6 (1.5mmx2mmx1mm)



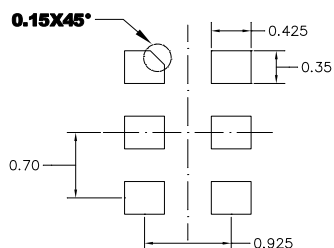
TOP VIEW



BOTTOM VIEW



SIDE VIEW

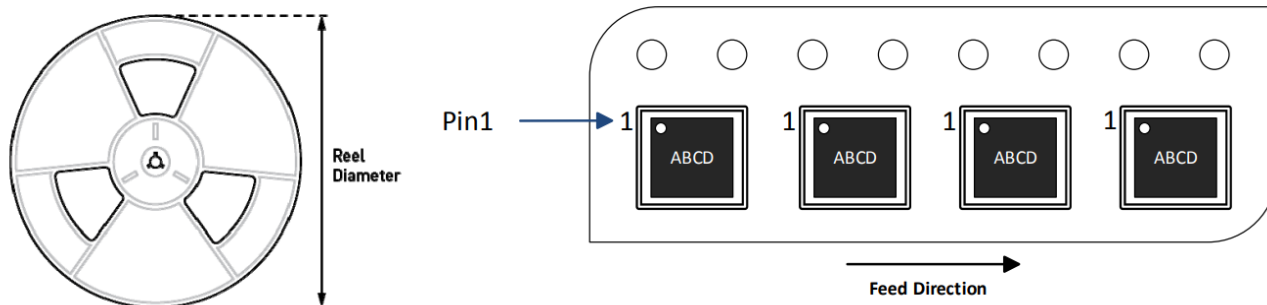


RECOMMENDED LAND PATTERN

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
- 3) JEDEC REFERENCE IS MO-303.
- 4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM3809GPH-Z	ECLGA-6 (1.5mmx2mmx1mm)	5000	N/A	N/A	13in	8mm	4mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	2/10/2025	Initial Release	-

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