MPM3806C

5.5V, 1A, 2.4MHz, Synchronous Step-Down Module, AEC-Q100 Qualified

DESCRIPTION

The MPM3806C is an easy-to-use, fully integrated, synchronous step-down power module with built-in MOSFET switches and an inductor. The device can achieve up to 1A of continuous output current (I_{OUT}) with excellent load and line regulation.

The constant-on-time (COT) control scheme provides fast transient response and eases loop stabilization. Fault protections include cycle-by-cycle current limiting and thermal shutdown.

An open-drain power good (PG) signal indicates whether the output exceeds 90% of its nominal voltage.

The MPM3806C is well-suited for a wide range of applications including high-performance digital signal processors (DSPs), advanced driver assistance system (ADAS) sensors, portable and mobile devices, and other space-constrained, low-power systems.

The MPM3806C requires a minimal number of readily available, standard external components. It is available in a small QFN-15 (3mmx4mmx1.6mm) package.

FEATURES

- Designed for Automotive Applications:
  - Wide 2.5V to 5.5V Operating Input Voltage (V_{IN}) Range
  - Up to 1A Output Current (I_{OUT})
  - 1% Feedback (FB) Accuracy
  - -40°C to +150°C Operating T_J Range
  - Available in AEC-Q100 Grade 1
- High Performance for Improved Thermals:
  - 75mΩ and 45mΩ Integrated Internal Power MOSFETs
- Optimized for EMC and EMI:
  - FCCM across the Full Load Range
  - 2.4MHz Switching Frequency (f_{SW})
  - MeshConnect™ Flip-Chip Package
- Optimized for Board Size and BOM:
  - Integrated Internal Power MOSFETs
  - Integrated Compensation Network
  - Available in a QFN-15 (3mmx4mmx1.6mm) Package
  - Fixed Output Options (1): 0.8V, 1V, 1.1V, 1.2V, 1.25V, 1.5V, 1.8V, 2.5V, 2.8V, 3.3V
- Additional Features:
  - Enable (EN) for Power Sequencing
  - Power Good (PG)
  - 100% Duty Cycle
  - External Soft Start (SS) Control
  - Output Discharge
  - Output Over-Voltage Protection (OVP)
  - Short-Circuit Protection (SCP) with Hiccup Mode
  - Available in a Wettable Flank Package

APPLICATIONS

- Camera Modules
- ADAS Sensors
- Automotive Infotainment
- Automotive V2X

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. “MPS”, the MPS logo, and “Simple, Easy Solutions” are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

Note:

1) See the Ordering Information section on page 3 for the exact availability of each fixed output version. Additional output voltages may be available. Contact MPS for details.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

TYPICAL APPLICATION

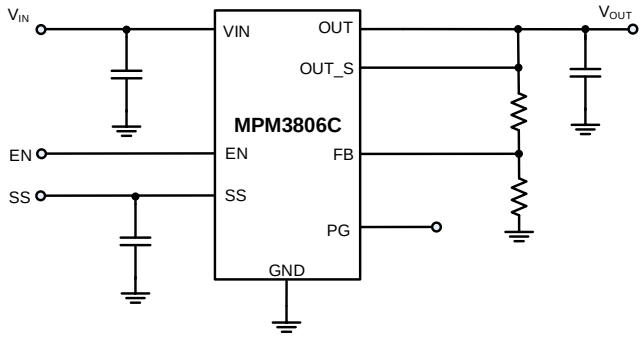
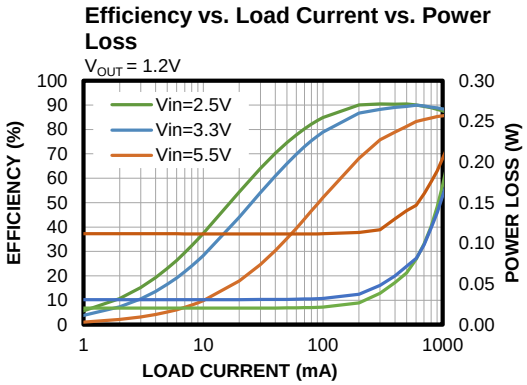


Figure 1: Typical Application (Adjustable Output)



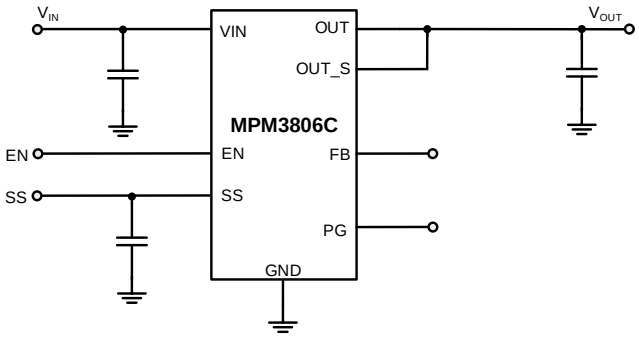


Figure 2: Typical Application (Fixed Output)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number* (2)	Output Voltage	Package	Top Marking	MSL Rating**
MPM3806CGLE-AEC1***	Adjustable	QFN-15 (3mmx4mmx1.6mm)	*See Below*	1
MPM3806CGLE-12-AEC1***	Fixed 1.2V	QFN-15 (3mmx4mmx1.6mm)	*See Below*	1
MPM3806CGLE-18-AEC1***	Fixed 1.8V	QFN-15 (3mmx4mmx1.6mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPM3806CGLE-AEC1-Z).

**Moisture Sensitivity Level Rating

***Wettable flank

Note:

2) Additional output voltages may be available. Contact MPS for details.

TOP MARKING (MPM3806CGLE-AEC1)

MPYW
3806
CLLL
ME

MP: MPS prefix
Y: Year code
W: Week code
3806: First four digits of the part number
C: FCCM
LLL: Lot number
M: Module
E: Wettable flank frame

TOP MARKING (MPM3806CGLE-12-AEC1)

MPYW
3806
CLLL
ME12

MP: MPS prefix
Y: Year code
W: Week code
3806: First four digits of the part number
C: FCCM
LLL: Lot number
M: Module
E: Wettable flank frame
12: 1.2V fixed output version of MPM3806C

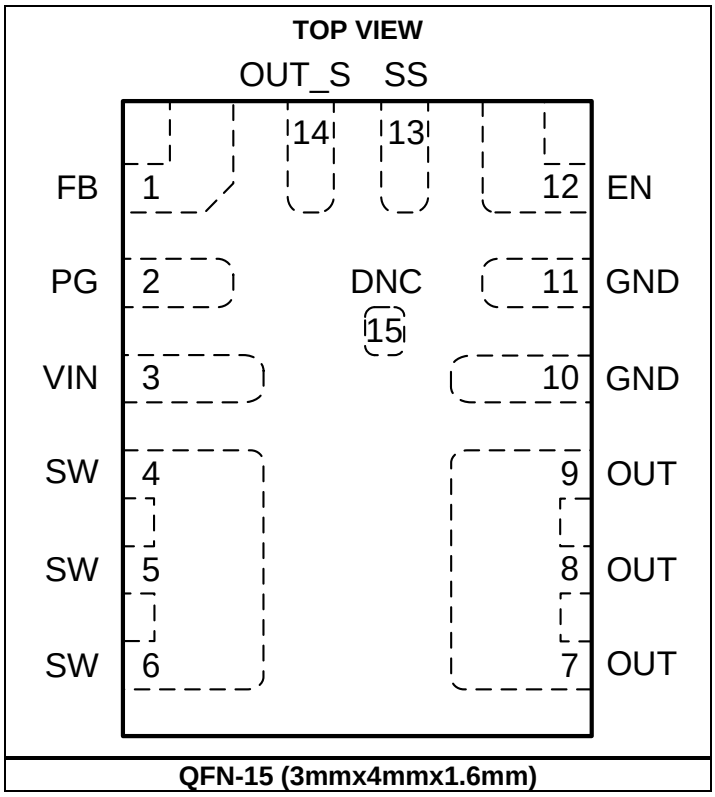
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

TOP MARKING (MPM3806CGLE-18-AEC1)

MPYW
3806
CLLL
ME18

MP: MPS prefix
Y: Year code
W: Week code
3806: First four digits of the part number
C: FCCM
LLL: Lot number
M: Module
E: Wettable flank frame
18: 1.8V fixed output version of MPM3806C

PACKAGE REFERENCE



QFN-15 (3mmx4mmx1.6mm)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Description
1	FB	**Feedback pin.** For the adjustable output version, the output voltage (V_{OUT}) is set by an external resistor divider from the output to GND, tapped to the FB pin. To set the regulation voltage, V_{FB} is compared to the internal V_{REF} (about 0.6V). For the fixed output version, float this pin.
2	PG	**Power good indicator.** The output of the PG pin is an open drain. Connect PG to a voltage source using an external resistor. PG is pulled high when V_{FB} exceeds 90% of V_{REF}; PG is pulled low to GND if V_{FB} drops below 85% of V_{REF}. Float this pin if it is not used.
3	VIN	**Input supply.** The MPM3806C operates from a 2.5V to 5.5V input. Connect a decoupling capacitor to the VIN pin to prevent large voltage spikes from appearing at the input.
4, 5, 6	SW	**Switch output.** The SW pin is the drain of the internal, high-side P-channel MOSFET. SW is internally connected to the power inductor.
7, 8, 9	OUT	**Power output.** Connect the load to the OUT pin. Use an output capacitor to reduce the voltage ripple.
10, 11	GND	**IC ground.** Connect the GND pin to the negative terminals of the input and output capacitors with a large copper area. In addition, use several vias to connect to the GND plane.
12	EN	**Enable.** Pull the EN pin below the falling threshold (0.65V) to shut down the chip. Pull EN above the rising threshold (0.9V) to enable the chip. There is an internal 2MΩ resistor connected from EN to ground.
13	SS	**Soft start.** Connect a capacitor from the SS pin to GND to set the soft-start time and avoid an inrush current at start-up. The minimum recommended soft-start capacitance (C_{SS}) is 1nF.
14	OUT_S	**Output sense.** OUT_S is the sense pin for V_{OUT} and the discharge path to a 150Ω resistor load.
15	DNC	**Do not connect.** The DNC pad is internally connected to the SW pin. Do not route or place vias under this area.

ABSOLUTE MAXIMUM RATINGS (3)

All pins……..-0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (4)(8)
QFN-15 (3mmx4mmx1.6mm)…….. 2.4W
Operating junction temperature .....150°C
Lead temperature…….....260°C
Storage temperature…….. -65°C to +150°C

Electrostatic Discharge (ESD) Rating

Human body model (HBM) ..... Class 2 (5)
Charged device model (CDM) ..... Class 2b (6)

Recommended Operating Conditions

Input voltage (V_{IN})…… ……..…...2.5V to 5.5V
Output voltage (V_{OUT})…….0.6V to V_{IN} - 0.5V
Load current range……0A to 1A
Operating junction temp (T_J)…..-40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-15 (3mmx4mmx1.6mm)
JESD51-7…..……..……...65……..14.... °C/W (7)
EVM3806C-LE-00A.....53.....10... °C/W (8)

Notes:

3) Exceeding these ratings may damage the device.
4) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX) = (T_J (MAX) - T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
5) Per AEC-Q100-002
6) Per AEC-Q100-011
7) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. The value of θ_{JC} shows the thermal resistance from junction-to-case bottom.
8) Measured on MPS MPM3806C standard EVB, 6.3cmx6.3cm, 4-layer, 2oz cooper PCB. The value of θ_{JC} shows the thermal resistance from junction-to-case top.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply						
Under-voltage lockout (UVLO) rising threshold	V_{UVLO_RISING}			2.3	2.45	V
V_{IN} UVLO falling threshold	$V_{UVLO\_FALLING}$			2.1		V
V_{IN} UVLO hysteresis	V_{UVLO_HYS}			0.2		V
V_{IN} quiescent current	I_Q	V_{EN} = 2V, V_{FB} = 0.63V, V_{IN} = 3.6V, T_J = 25°C		460	650	µA
V_{IN} shutdown current	I_{SHDN}	V_{EN} = 0V, T_J = 25°C		0.01	1	µA
		V_{EN} = 0V, T_J = -40°C to +125°C (9)			3	
		V_{EN} = 0V, T_J = -40°C to +150°C			20	
V_{IN} over-voltage protection (OVP) rising threshold	V_{INOVP_RISING}	After V_{OUT} OVP is enabled		6.15		V
V_{IN} OVP falling threshold	$V_{INOVP\_FALLING}$			5.95		V
V_{IN} OVP hysteresis	V_{INOVP_HYS}			0.2		V
Frequency, Switches and Inductor						
Switching frequency	f_{SW}		2000	2400	2640	kHz
Minimum on time (9)	t_{ON_MIN}	V_{IN} = 5V		50		ns
Minimum off time (9)	t_{OFF_MIN}	V_{IN} = 5V		80		ns
Maximum duty cycle	D_{MAX}			100		%
Switch leakage current	I_{SW_LKG}	V_{EN} = 0V, V_{IN} = 6V, V_{SW} = 0V or 6V, T_J = 25°C		0.0	1	µA
		V_{EN} = 0V, V_{IN} = 6V, V_{SW} = 0V or 6V, T_J = -40°C to +125°C (9)			30	
High-side (HS) switch on resistance	R_{ON_HS}	V_{IN} = 5V		75	110	mΩ
Low-side (LS) switch on resistance	R_{ON_LS}	V_{IN} = 5V		45	70	mΩ
Integrated inductor value (9)	L		376	470	564	nH
Integrated inductor DC resistance	R_L			25	65	mΩ
Integrated inductor saturation current (9)	I_{L_SAT}		4.8	5.4		A
Output and Regulation						
FB voltage (adjustable output version)	V_{FB}	T_J = 25°C	0.594	0.6	0.606	V
		T_J = -40°C to +150°C	0.591	0.6	0.609	V
Output regulation voltage (fixed output version)	V_{OUT_REG}	1.2V fixed output	1.176	1.2	1.224	V
		1.8V fixed output	1.764	1.8	1.836	V
FB input current	I_{FB}	Adjustable output version		50	100	nA
		1.2V fixed output		3	8	µA
		1.8V fixed output		5	10	
V_{OUT} discharge resistance	R_{DIS}	V_{EN} = 0V, V_{OUT} = 1.2V		150		Ω

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
EN						
EN rising threshold	V_{EN_RISING}			0.9	1.2	V
EN falling threshold	$V_{EN\_FALLING}$		0.4	0.65		V
EN threshold hysteresis	V_{EN_HYS}			0.25		V
EN turn-on delay		EN high to SW active		100		µs
EN turn-off delay		EN low to stop switching		30		µs
EN pull-down resistor				2		MΩ
EN input current	I_{EN}	V_{EN} = 2V		1.2		µA
		V_{EN} = 0V		0		µA
Soft Start						
Soft-start current	I_{SS}		1.5	3	4.5	µA
PG						
PG rising threshold	PG_{VTH_RISING}	FB rising edge	87%	90%	93%	V_{FB}
PG falling threshold	$PG_{VTH\_FALLING}$	FB falling edge	82%	85%	88%	V_{FB}
PG logic high voltage	V_{PG_HIGH}	V_{IN} = 5V, V_{FB} = 0.6V	4.9			V
PG sink current capability	V_{PG_LOW}	Sink 1mA			0.4	V
PG rising deglitch	t_{PGOOD_R}			80		µs
PG falling deglitch	t_{PGOOD_F}			80		µs
PG leakage current (high)		5V logic high			100	nA
PG self-bias		V_{IN} = 0V, V_{EN} = 0V, PG is pulled up between 3V and 5.5V via a 100kΩ resistor			0.7	V
Protections						
HS peak current limit	I_{LIMIT_HS}		1.6	2.5	3.4	A
LS valley current limit	I_{LIMIT_LS}		0.4	1	1.6	A
LS reverse current limit	$I_{LIMIT\_REVERSE}$	Current flows from SW to GND		1.2		A
Thermal shutdown (9)	T_{SD}			170		°C
Thermal shutdown hysteresis (9)	T_{SD_HYS}			20		°C
Output OVP threshold	V_{OVP}		110%	115%	120%	V_{FB}
Output OVP hysteresis	V_{OVP_HYS}			10%		V_{FB}
OVP delay				2		µs

Note:

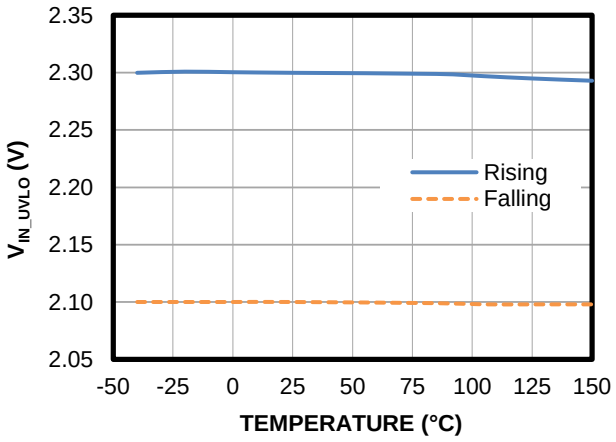
9) Not tested in production. Guaranteed by design and characterization.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

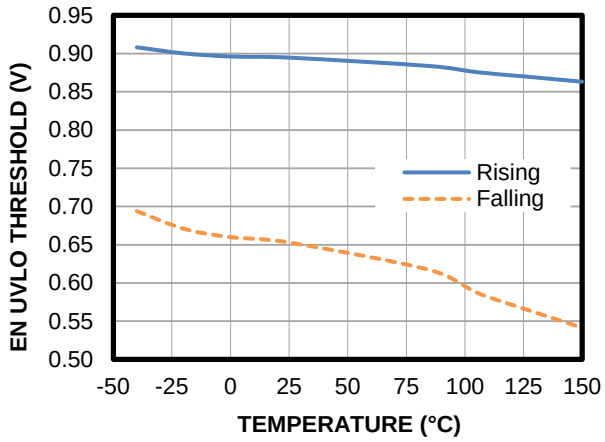
TYPICAL CHARACTERISTICS

V_{IN} = 3.6V, T_J = -40°C to +150°C, unless otherwise noted.

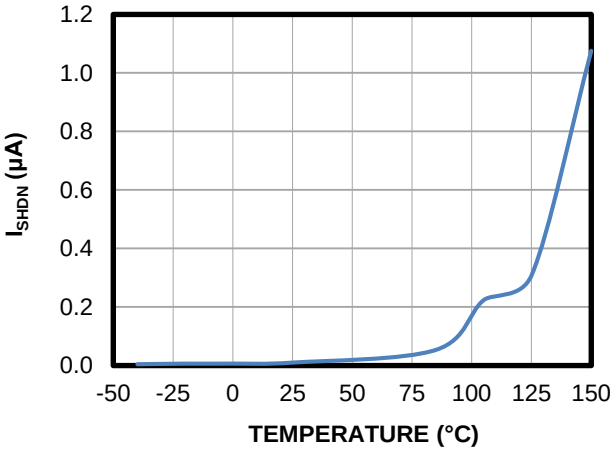
V_{IN} UVLO Threshold vs. Temperature



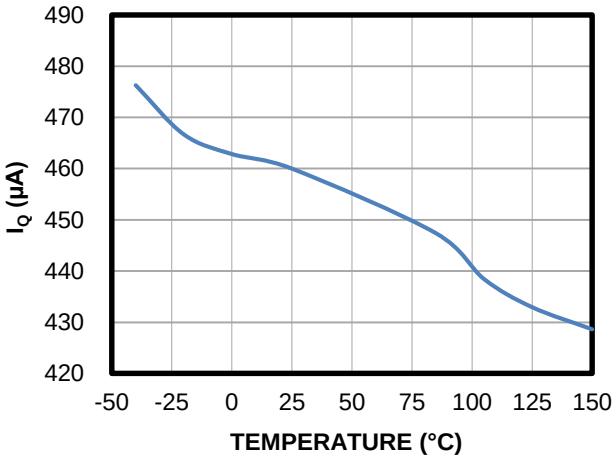
EN UVLO Threshold vs. Temperature



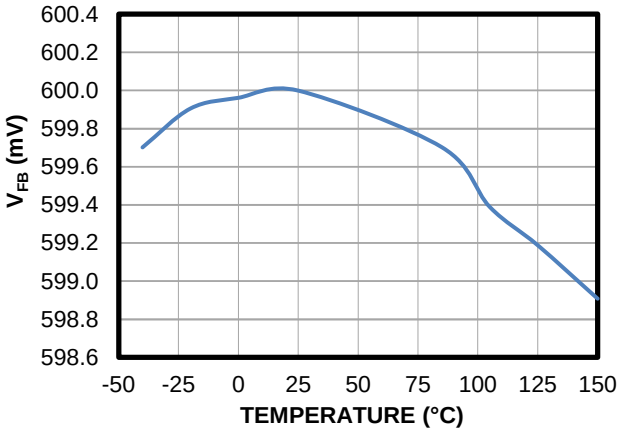
Shutdown Current vs. Temperature



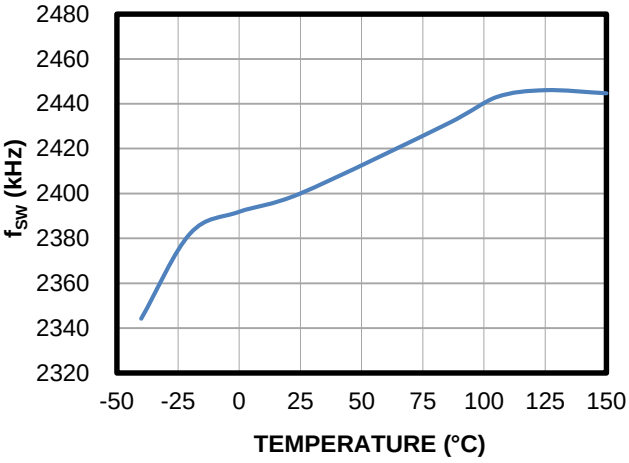
Quiescent Current vs. Temperature



Feedback Voltage vs. Temperature



Switching Frequency vs. Temperature

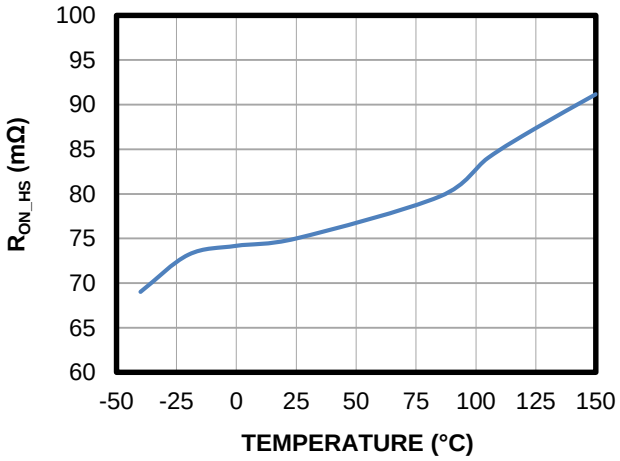


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

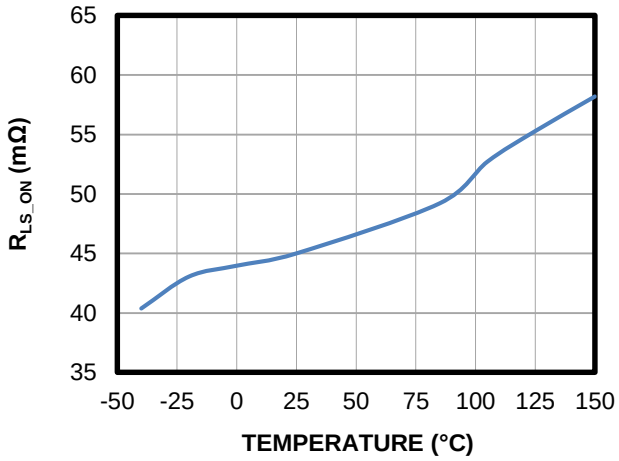
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_J = -40°C to +150°C, unless otherwise noted.

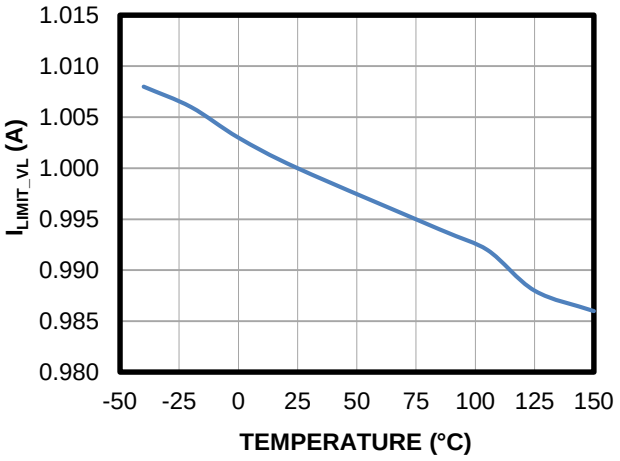
R_{ON_HS} vs. Temperature



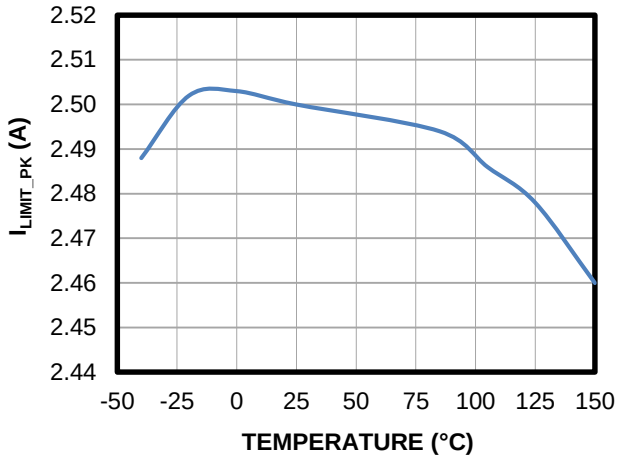
R_{ON_LS} vs. Temperature



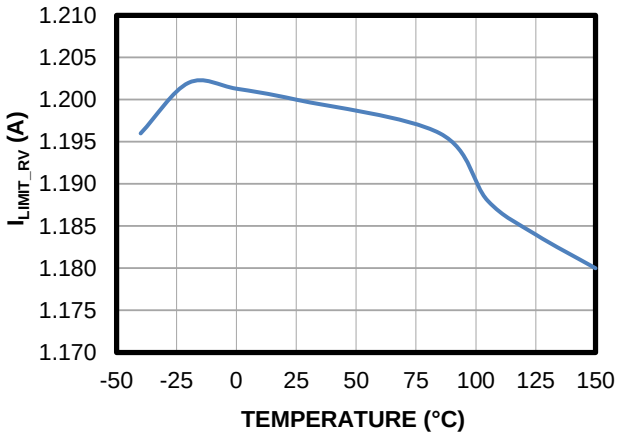
Valley Current Limit vs. Temperature



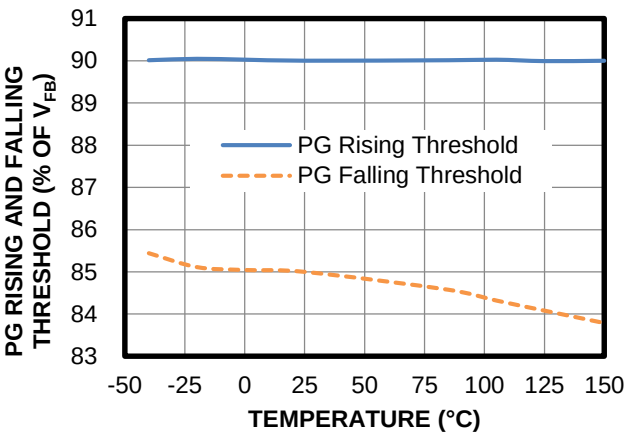
Peak Current Limit vs. Temperature



LS-FET Reverse Current Limit vs. Temperature



PG Threshold vs. Temperature

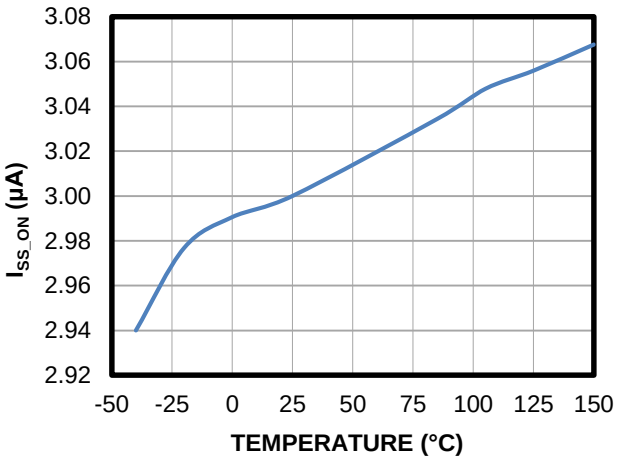


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_J = -40°C to +150°C, unless otherwise noted.

Soft-Start Current vs. Temperature



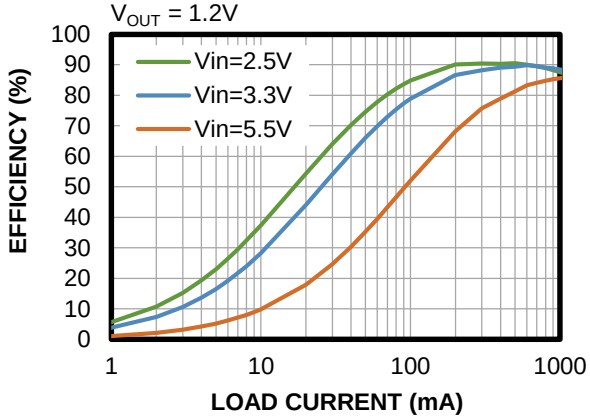
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3V, V_{OUT} = 1.2V, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

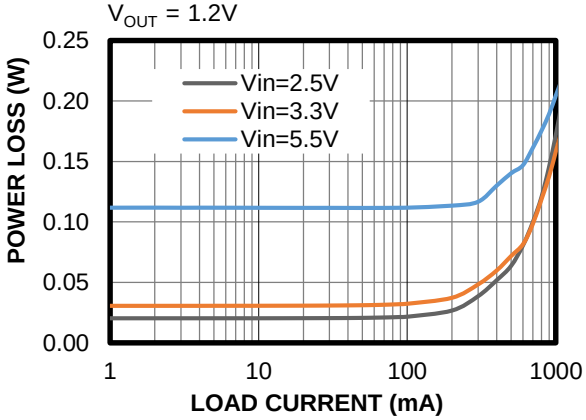
Efficiency vs. Load Current

V_{OUT} = 1.2V



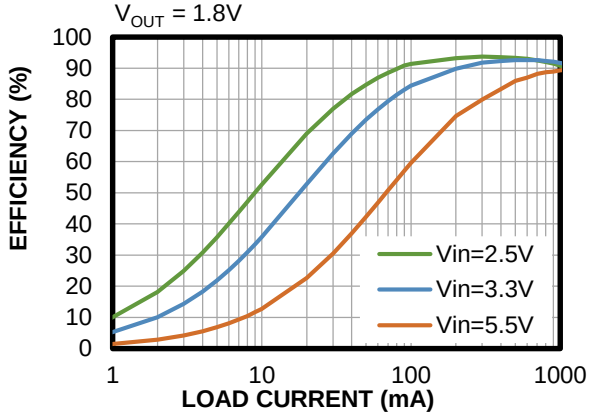
Power Loss vs. Load Current

V_{OUT} = 1.2V



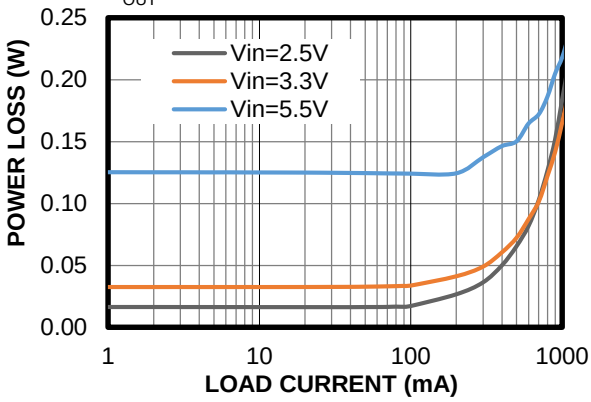
Efficiency vs. Load Current

V_{OUT} = 1.8V



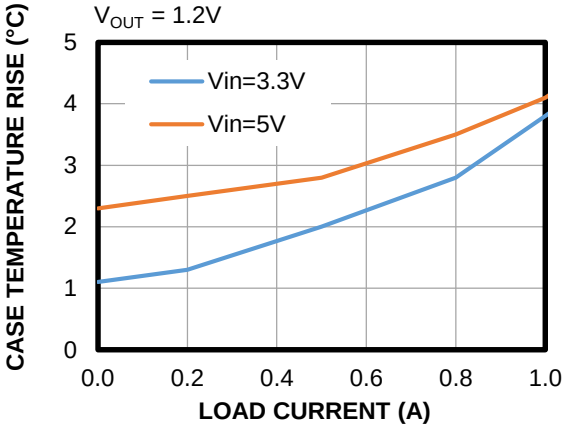
Power Loss vs. Load Current

V_{OUT} = 1.8V



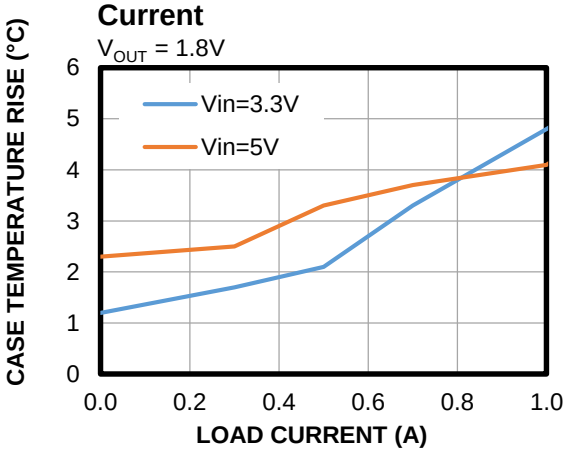
Case Temperature Rise vs. Load Current

V_{OUT} = 1.2V



Case Temperature Rise vs. Load Current

V_{OUT} = 1.8V

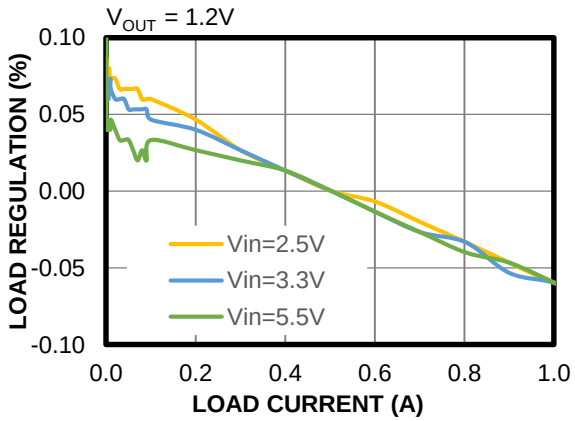


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

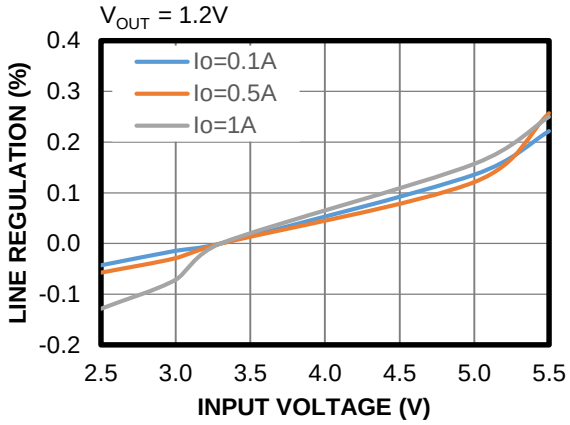
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 1.2V, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

Load Regulation vs. Load Current



Line Regulation vs. Input Voltage

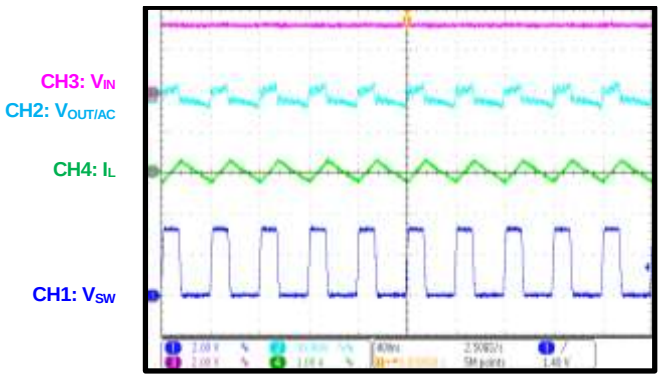


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

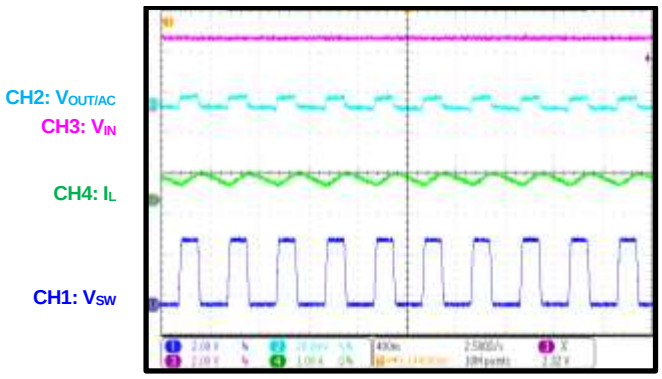
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 1.2V, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

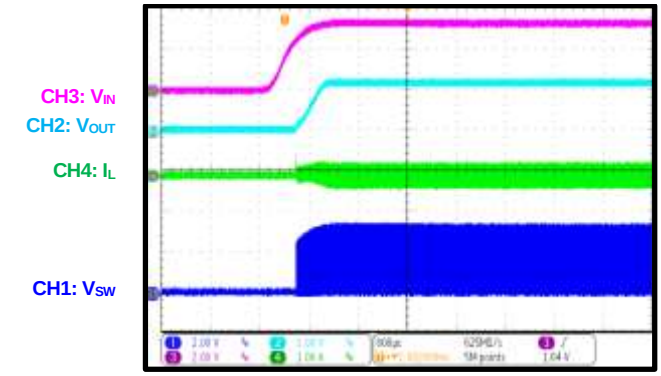
Steady State
I_{OUT} = 0A



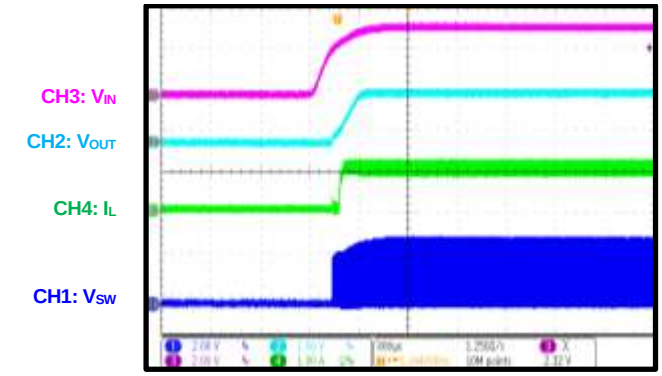
Steady State
I_{OUT} = 1A



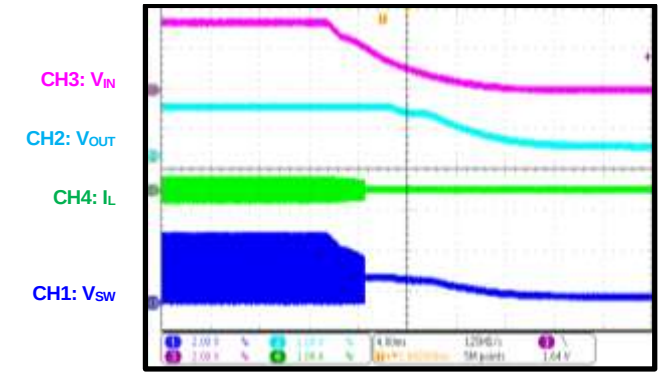
Start-Up through VIN
I_{OUT} = 0A



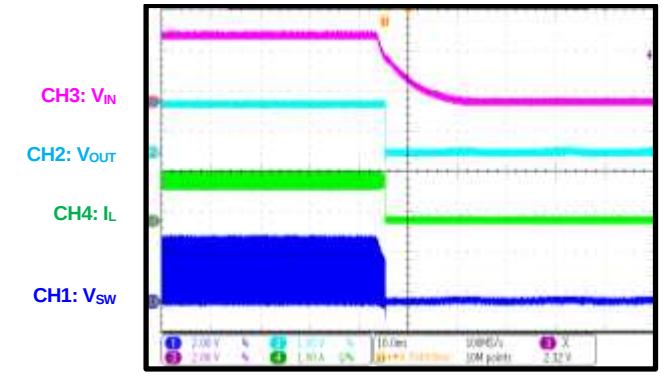
Start-Up through VIN
I_{OUT} = 1A



Shutdown through VIN
I_{OUT} = 0A



Shutdown through VIN
I_{OUT} = 1A



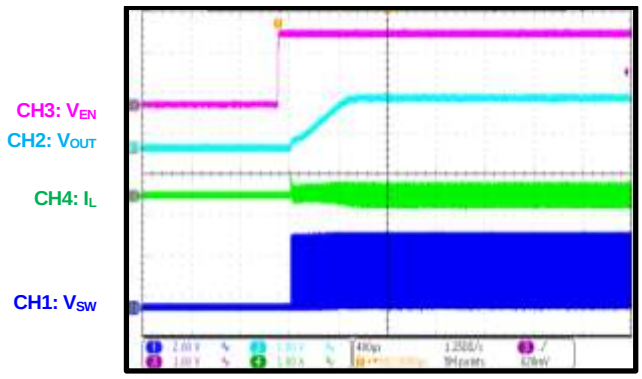
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 1.2V, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

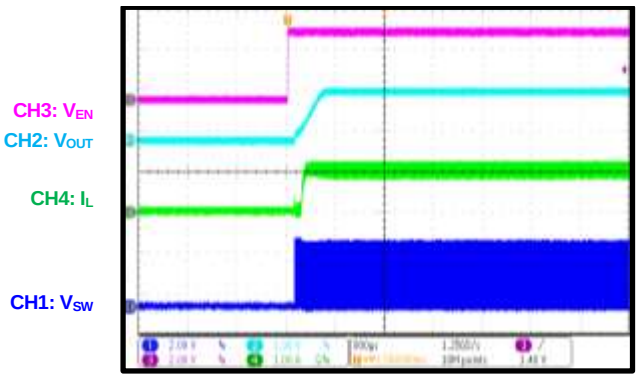
Start-Up through EN

I_{OUT} = 0A



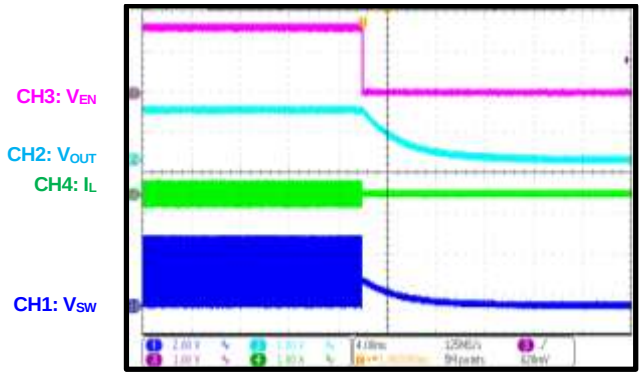
Start-Up through EN

I_{OUT} = 1A



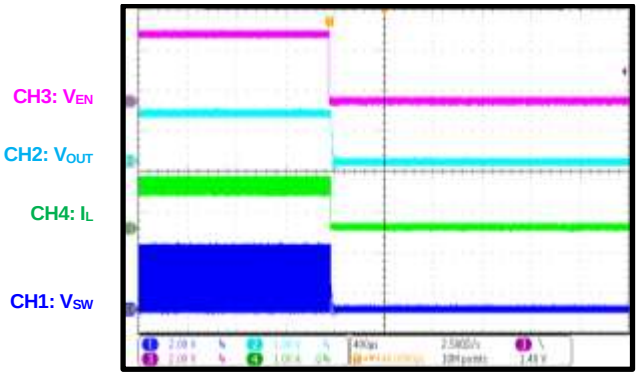
Shutdown through EN

I_{OUT} = 0A



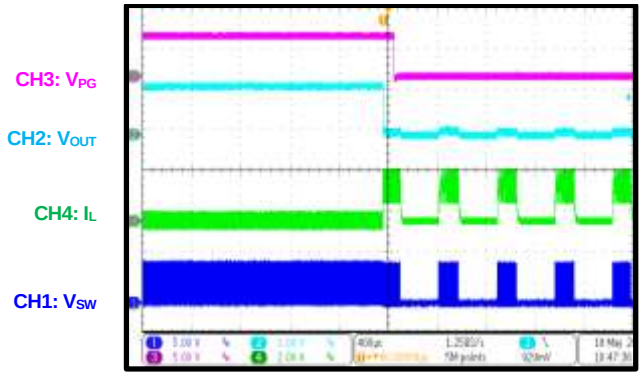
Shutdown through EN

I_{OUT} = 1A



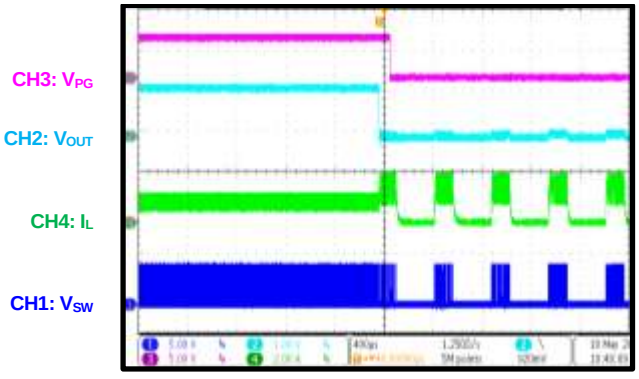
SCP Entry

I_{OUT} = 0A



SCP Entry

I_{OUT} = 1A

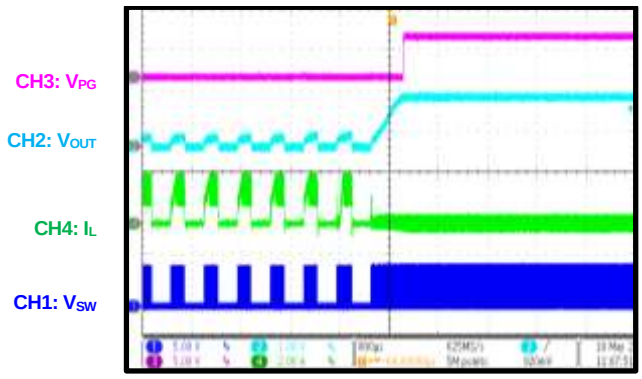


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

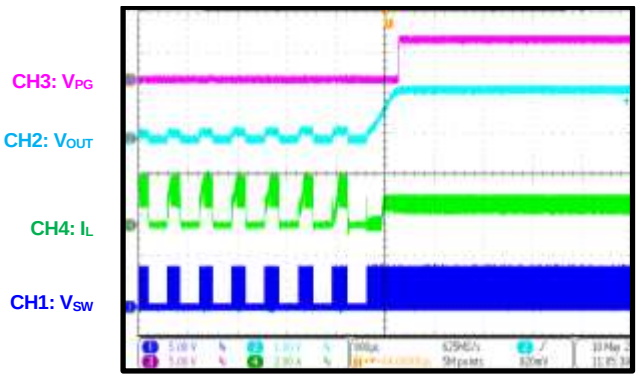
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 1.2V, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

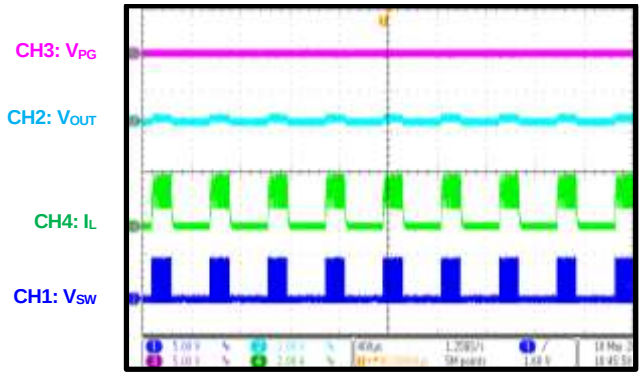
SCP Recovery
I_{OUT} = 0A



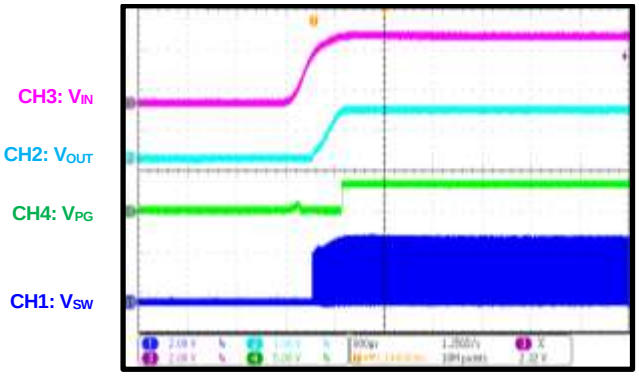
SCP Recovery
I_{OUT} = 1A



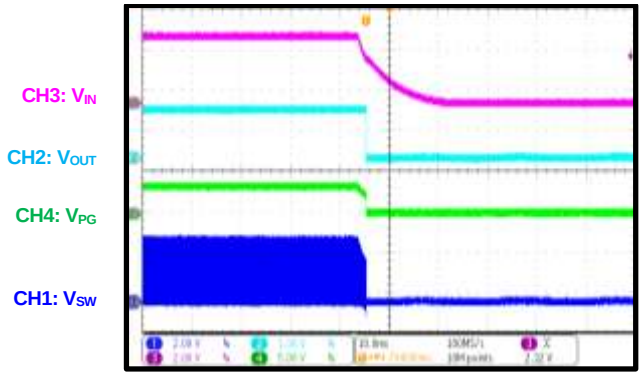
SCP
I_{OUT} = 0A



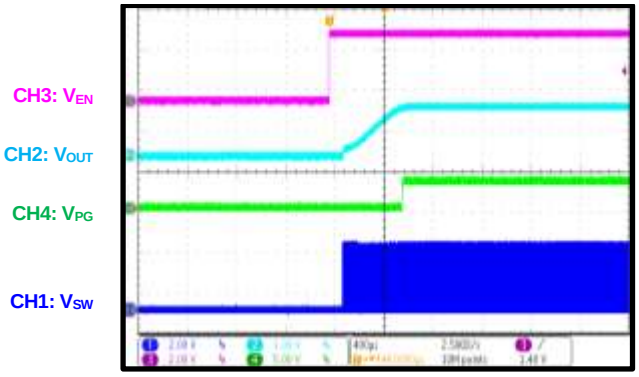
PG Start-Up through VIN
I_{OUT} = 1A



PG Shutdown through VIN
I_{OUT} = 1A



PG Start-Up through EN
I_{OUT} = 1A



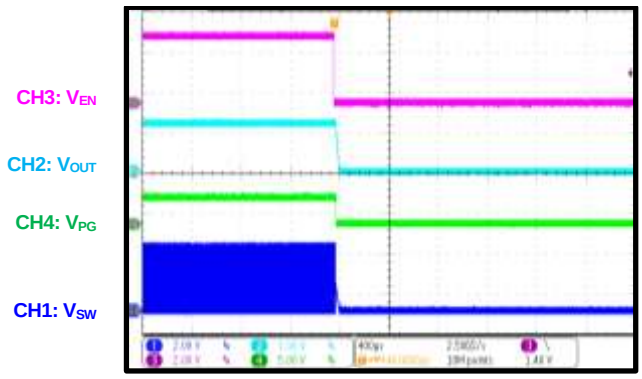
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 1.2V, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

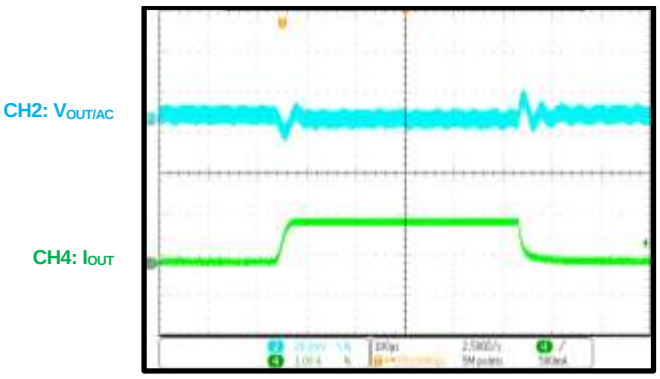
PG Shutdown through EN

I_{OUT} = 1A



Load Transient Response

I_{OUT} = 0A to 1A, 1A/µs



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

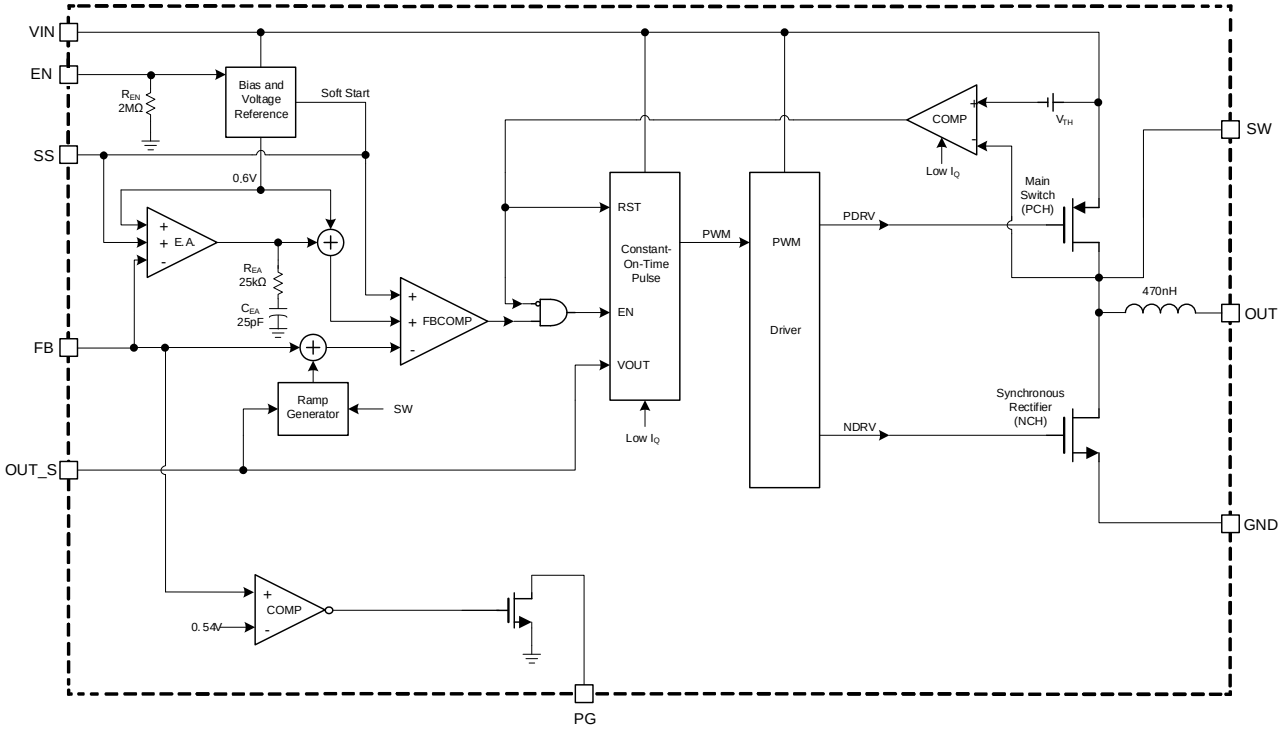


Figure 3: Functional Block Diagram (Adjustable Output Version)

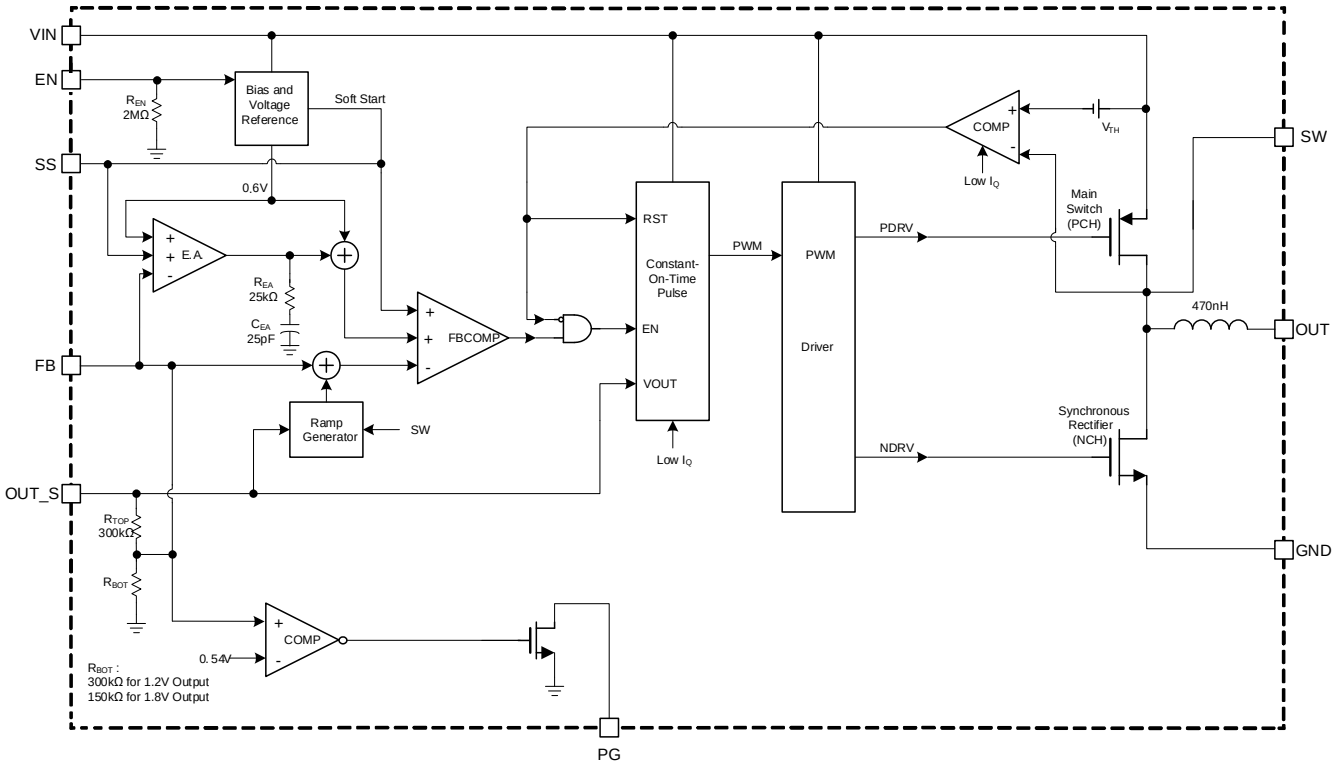


Figure 4: Functional Block Diagram (Fixed Output Version)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

OPERATION

The MPM3806C employs input voltage (V_{IN}) feed-forward and constant-on-time (COT) control to stabilize the switching frequency (f_{SW}) across the entire V_{IN} range. The device can achieve 1A of output current (I_{OUT}) across a 2.5V to 5.5V V_{IN} range, with excellent load and line regulation. The output voltage (V_{OUT}) can be regulated to as low as 0.6V. A 100% maximum duty cycle can be reached in low-dropout mode.

Constant-On-Time (COT) Control and Forced Continuous Conduction Mode (FCCM)

COT control provides a simpler control loop and faster transient response. The MPM3806C's switching cycles have a fixed minimum off time (t_{OFF_MIN}) to prevent inductor current (I_L) runaway during load transients. If the low-side MOSFET (LS-FET) turns on, it remains on for at least t_{OFF_MIN} (typically 80ns). The high-side MOSFET (HS-FET) turns on once the feedback (FB) voltage (V_{FB}) drops below the reference voltage (V_{REF}). This indicates an insufficient V_{OUT}.

Input voltage feed-forward allows the device to maintain a nearly constant f_{SW} across the input range and load range. The f_{SW} on time (t_{ON}) can be calculated with Equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 400ns \quad (1)$$

To improve frequency stability and reduce the output voltage ripple, the MPM3806C operates in forced continuous conduction mode (FCCM) (see Figure 5). FCCM has a constant f_{SW}.

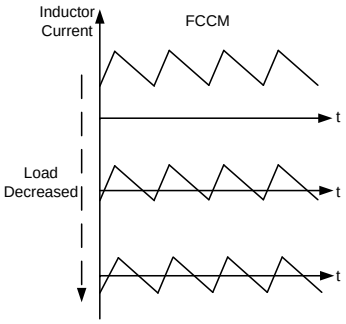


Figure 5: FCCM

Enable (EN) Control

The enable (EN) pin is a digital control pin that turns the MPM3806C on and off. Pull EN above 0.9V to turn the converter on; pull EN below 0.65V or float EN to turn it off. Pulling EN to GND also disables the device. There is an internal 2MΩ resistor connected between EN and GND.

Output Discharge

If the MPM3806C shuts down, the device initiates output discharge mode. The internal discharge MOSFET provides a resistive discharge path for the output capacitor (C2) between the OUT_S pin and GND. To block the output discharge path, add an external capacitor between V_{OUT} and the OUT_S pin (see the Output Discharge Blocking section on page 21).

Soft Start (SS)

The MPM3806C features external soft start. To avoid overshoot during start-up, the SS pin ramps up V_{OUT} at a controlled slew rate. The SS pin's charge current is typically 3μA. The soft-start time (t_{SS}) is determined by the external soft-start capacitor (C_{SS}). t_{SS} can be calculated with Equation (2):

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times 0.6V}{I_{SS}(\mu A)} \quad (2)$$

Where I_{SS} is the internal soft-start charge current (3μA). It is recommended that C_{SS} be at least 1nF.

The MPM3806C has a pre-biased start-up function. Once EN is pulled above 0.9V, the converter starts up, regardless of any pre-biased voltage on the output. Pre-biased start-up works even while the output discharge path is blocked.

Peak Current Limit and Valley Current Limit

Both the HS-FET and LS-FET feature current-limit protection. If I_L reaches the HS-FET's peak current limit (I_{LIMIT_PEAK}, typically 2.5A), the HS-FET turns off and the LS-FET turns on to discharge the energy. The HS-FET does not turn again until I_L drops below the valley current limit (I_{LIMIT_VALLEY}, typically 1A). This prevents current runaway during overload and short-circuit events. I_{LIMIT_VALLEY} is blocked unless the HS-FET turns off due to I_{LIMIT_PEAK} being triggered.

Short-Circuit Protection (SCP) and SCP Recovery

When a short-circuit condition occurs, the MPM3806C reaches its current limit immediately.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

Meanwhile, V_{OUT} drops until V_{FB} falls below 50% of V_{REF}. The MPM3806C considers this an output dead short and triggers short-circuit protection (SCP) with hiccup mode to periodically restart the part. In hiccup mode, the output power stage is disabled and the SS voltage (V_{SS}) is discharged. Once V_{SS} is discharged completely, the device initiates a new soft start. This process repeats until the fault condition is removed.

Over-Voltage Protection (OVP)

The MPM3806C monitors V_{FB} to detect over-voltage (OV) conditions. If V_{FB} exceeds 115% of V_{REF}, then the converter enters its dynamic regulation period. During this period, the LS-FET remains on until the LS-FET current reaches -1.2A. This process discharges V_{OUT} to keep V_{OUT} within its normal range. If the OV condition still remains after this process, there is a 1.5µs delay, and then the LS-FET turns on again.

Once V_{FB} falls below 105% of V_{REF}, the converter exits the regulation period. If the dynamic regulation period cannot prevent V_{OUT} from increasing, and a 6.1V V_{IN} is detected, then OVP is triggered, and the device stops switching until V_{IN} drops below 6V. Once V_{IN} drops below 6V, the MPM3806C resumes normal operation.

Power Good (PG) Indicator

The MPM3806C has a power good (PG) output to indicate whether the converter is operating normally after start-up. PG is the open drain of an internal MOSFET. It is recommended that this MOSFET's maximum on resistance ($R_{DS(ON)}$) be below 400Ω. PG can be connected to V_{IN} or an external voltage source via an external resistor (10kΩ to 100kΩ). Once V_{IN} is applied, the MOSFET turns on, and PG is pulled to GND before soft start is ready.

After V_{FB} reaches 90% of V_{REF}, PG is pulled high by the external voltage source. If V_{FB} drops to 85% of V_{REF}, then the PG voltage (V_{PG}) is pulled to GND to indicate an output failure.

If VIN and EN are not available, and PG is pulled up via an external power supply, then the PG pin self-biases and asserts. If a 100kΩ pull-up resistor is being used, then V_{PG} should be below 0.7V.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the MPM3806C's adjustable V_{OUT}. V_{OUT} can be set from 0.6V to (V_{IN} - 0.5V). Select a feedback (FB) resistor (R4, typically between 10kΩ and 100kΩ) to reduce the V_{OUT} leakage current. Then R5 can be calculated with Equation (3):

$$R5 = \frac{R4}{\frac{V_{OUT}}{0.6} - 1} \quad (3)$$

Figure 6 shows the FB network.

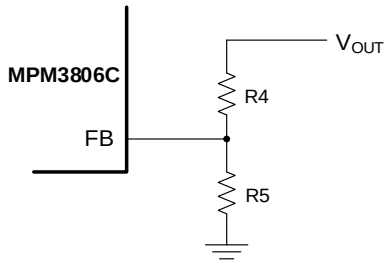


Figure 6: Feedback Network

Table 1 shows the recommended resistor values for common output voltages.

Table 1: Resistor Values for Common Output Voltages

V_{OUT} (V)	R4 (kΩ)	R5 (kΩ)
1	30.9 (1%)	47 (1%)
1.2	100 (1%)	100 (1%)
1.8	36 (1%)	18 (1%)
2.5	51 (1%)	16 (1%)
3.3	68 (1%)	15 (1%)

For the fixed output version of the MPM3806C, an external resistor divider is not required. In this scenario, the FB pin can be floated.

Frequency Scaling at Low Input Voltages

Under heavy-load conditions, the HS-FET voltage decreases as t_{ON} increases and the duty cycle is extended. If t_{OFF_MIN} is reached at a low V_{IN} and under heavy-load conditions, then f_{SW} scales down. To maintain a constant f_{SW} during heavy-load operation, a larger V_{OUT} is required for a larger V_{IN}. For a 1.8V V_{OUT} at a 1A load, V_{IN} should be above 2.9V to keep f_{SW} above 2MHz. If the frequency begins to scale down, V_{IN} can be estimated with Equation (4):

$$V_{IN} = \frac{V_{OUT} + R_{ON\_HS} \times I_{OUT}}{1 - \frac{t_{OFF\_MIN}}{400 \times 10^{-9}}} \quad (4)$$

Where the maximum t_{OFF_MIN} is 125ns. (10)

Note:

10) Guaranteed by design and bench characterization. Not tested in production.

Selecting the Input Capacitor

The step-down converter has a discontinuous input current (I_{IN}), and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, it is recommended to use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are strongly recommended due to their low ESR and small temperature coefficients. For most applications, a 10µF capacitor is sufficient. Higher output voltages may require a 22µF capacitor to increase system stability.

The input capacitor (C1) requires an adequate ripple current rating to absorb the switching I_{IN}.

C1's RMS current rating (I_{C1}) can be estimated with Equation (5):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

The worst-case scenario occurs at $V_{IN} = 2 \times V_{OUT}$, which can be calculated with Equation (6):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

C1 can be an electrolytic, tantalum, or ceramic capacitor. When using electrolytic or tantalum capacitors, place a small, high-quality, 0.1µF ceramic capacitor as close to the IC as possible. When using ceramic capacitors, ensure that the capacitor has enough capacitance to prevent an excessive voltage ripple at the input. The input voltage ripple (ΔV_{IN}) can be estimated with Equation (7):

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

Selecting the Output Capacitor

The output capacitor (C2) stabilizes the DC V_{OUT}. It is recommended to use ceramic capacitors for C2. Low-ESR capacitors are recommended because they effectively limit the output voltage ripple (ΔV_{OUT}). ΔV_{OUT} can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (8)$$

Where L_1 is the inductance, and R_{ESR} is C2's equivalent series resistance (ESR).

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of ΔV_{OUT}.

For simplification, ΔV_{OUT} can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

Ceramic capacitors with X7R or X5R dielectrics are highly recommended due to their low ESR and small temperature coefficients.

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, ΔV_{OUT} can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (10)$$

C2's characteristics can also affect the stability of the regulation system.

Output Discharge Blocking

If the device is disabled, an internal resistive discharge path between the OUT_S pin and GND is enabled to discharge C2. The discharge path can be blocked by adding an external capacitor between V_{OUT} and the OUT_S pin (see Figure 7).

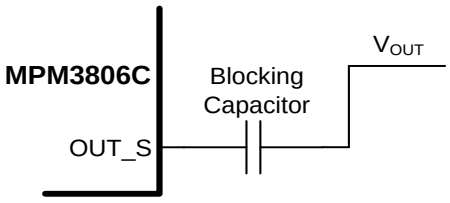


Figure 7: Circuit with V_{OUT} Discharge Blocking

This is only supported by the adjustable output version. For fixed output versions, the OUT_S pin must be connected to V_{OUT} to regulate the output voltage.

To avoid influencing the loop and load transient, select a ≥10nF blocking capacitor. It is recommended to use a 10nF to 100nF blocking capacitor. A larger-value blocking capacitor does not have an impact on loop performance, but a larger-value capacitor is physically larger and is typically unnecessary for the best results.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

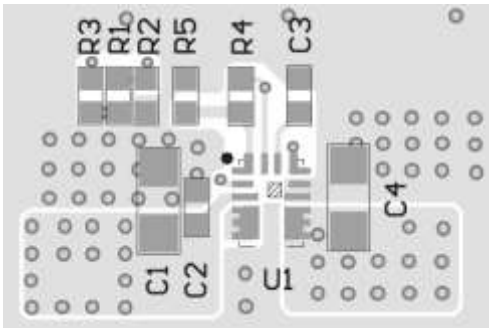
PCB Layout Guidelines (11)

Using a power module with an integrated inductor simplifies the PCB layout design, but some considerations should be taken to ensure proper operation. A 4-layer layout is recommended to improve EMC and thermal performance (although the device can operate sufficiently with a 2-layer PCB). For the best results, refer to Figure 8 and follow the guidelines below:

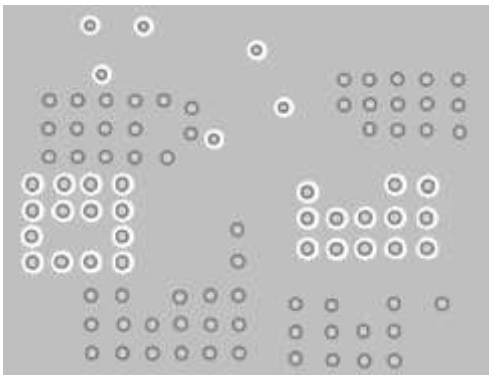
1. Place the high-current paths (e.g. GND and VIN) very close to the device with short, direct, and wide traces.
2. Use large copper areas to minimize conduction loss and thermal stress.
3. Place the ceramic input capacitors as close to the VIN pin as possible.
4. Place several vias close to the GND terminal of the capacitor, and close to the GND pin on the IC, to minimize high-frequency noise.
5. Place the feedback resistors as close as possible to the FB pin to ensure that the trace that connects to the FB pin is as short as possible.
6. Use multiple vias to connect the power planes to the internal layer.

Note:

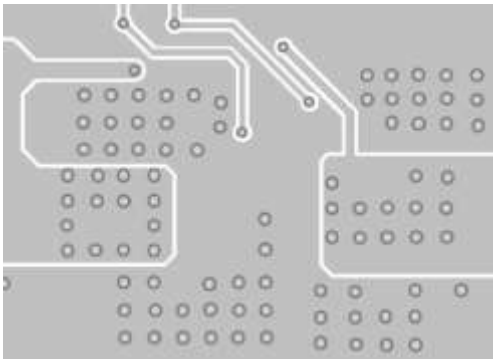
11) The recommended PCB layout is based on Figure 9 on page 23.



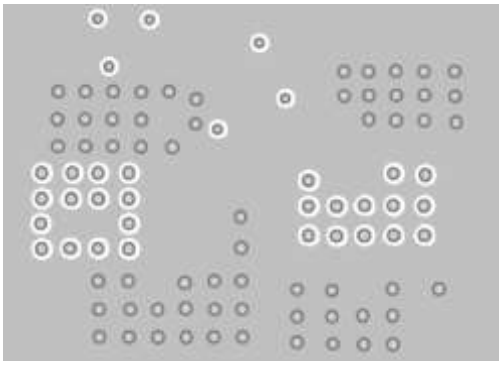
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer and Bottom Silk

Figure 8: Recommended PCB Layout

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS

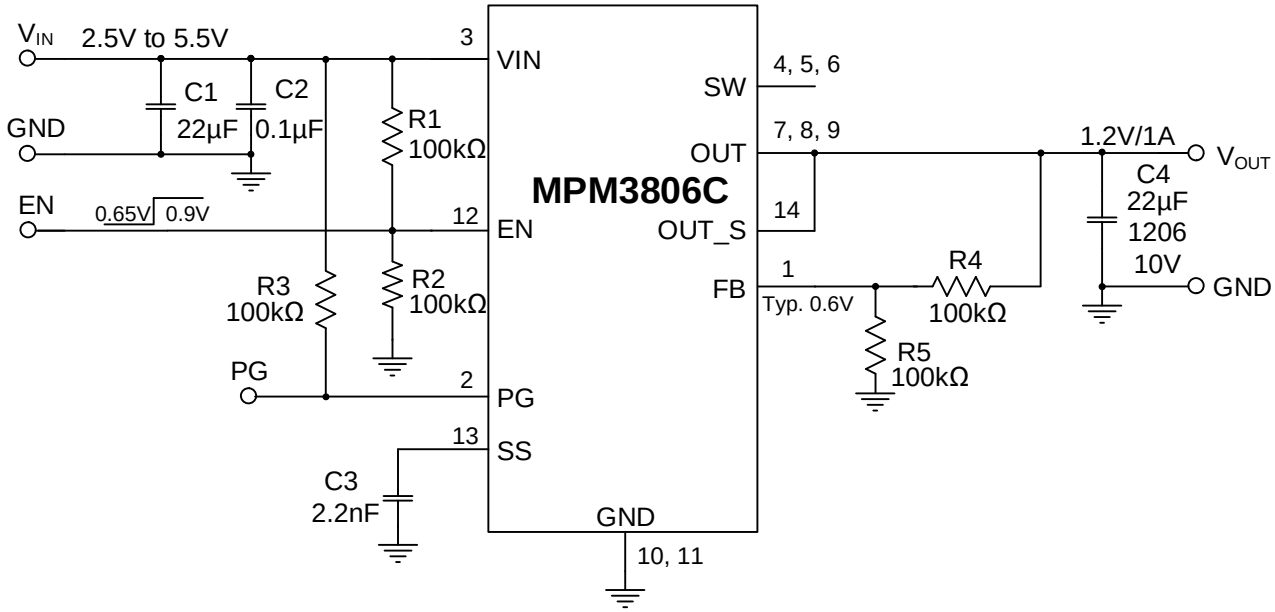


Figure 9: Typical Application Circuit (Adjust Output Version, V_{OUT} = 1.2V)

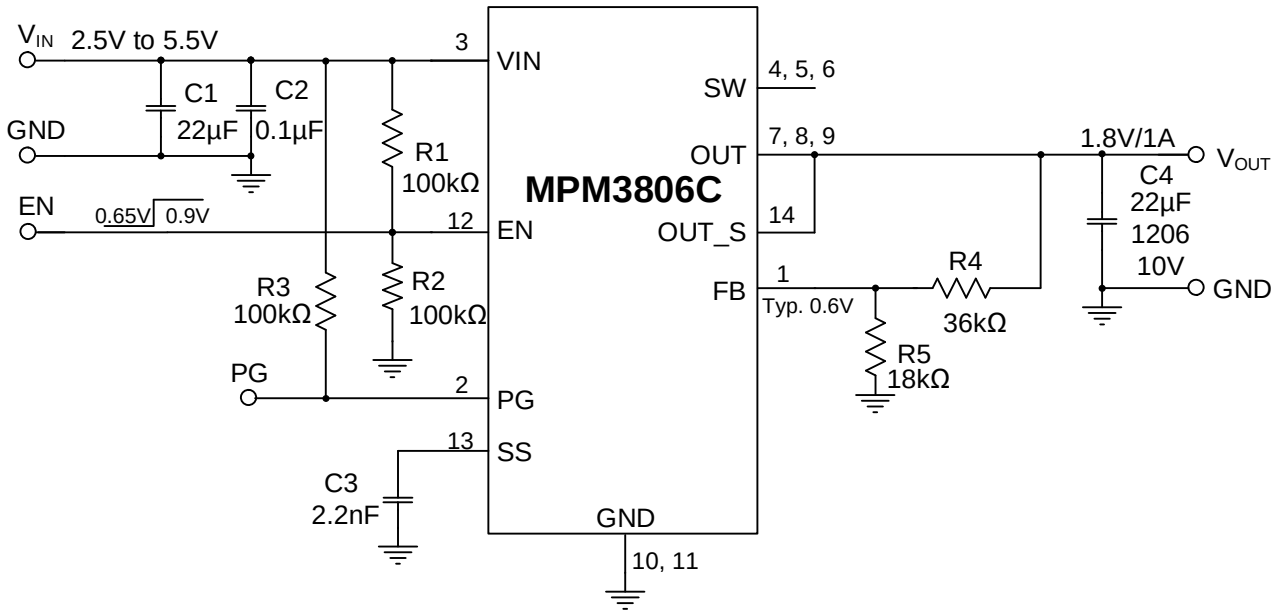


Figure 10: Typical Application Circuit (Adjustable Output Version, V_{OUT} = 1.8V)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS *(continued)*

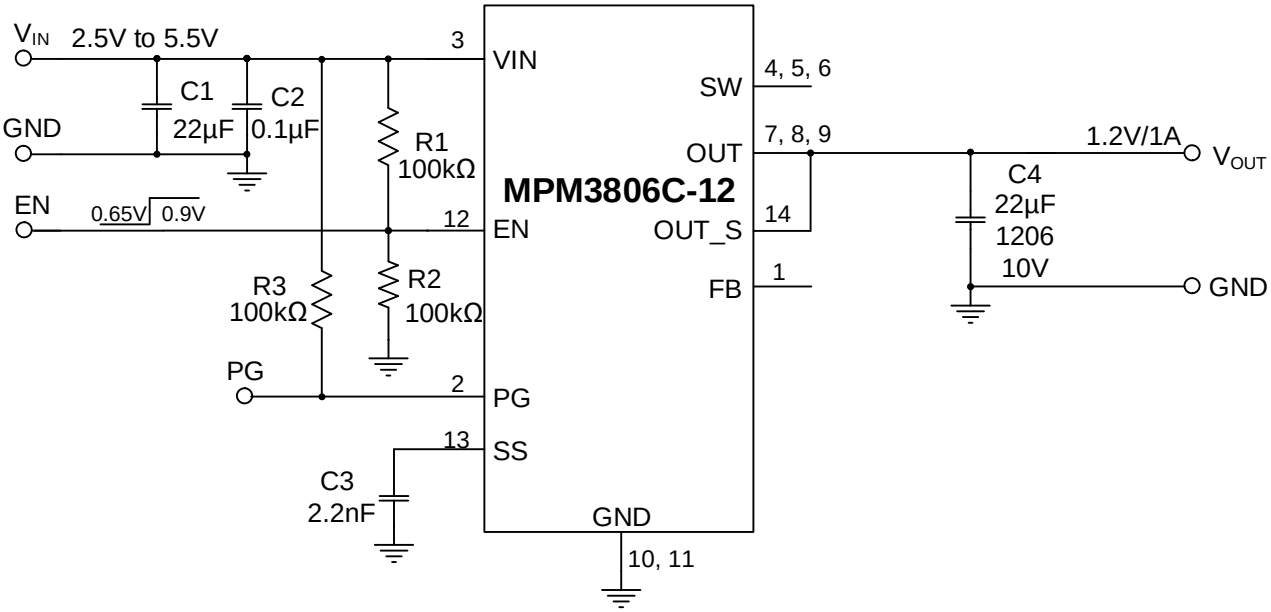


Figure 11: Typical Application Circuit (Fixed Output Version, V_{OUT} = 1.2V)

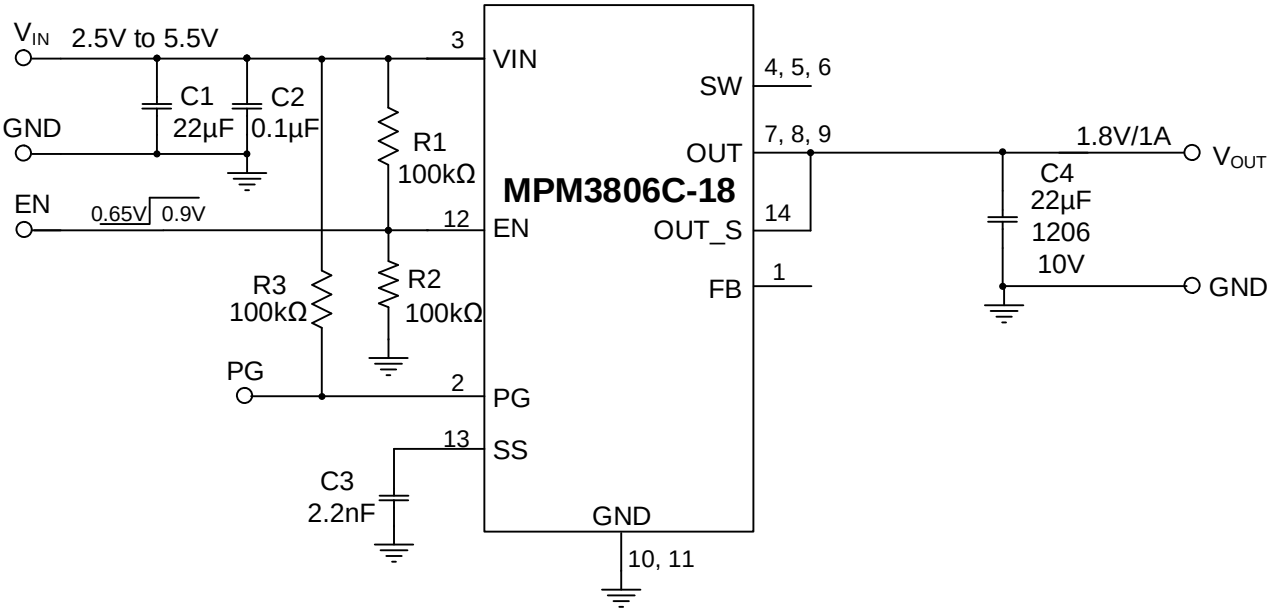


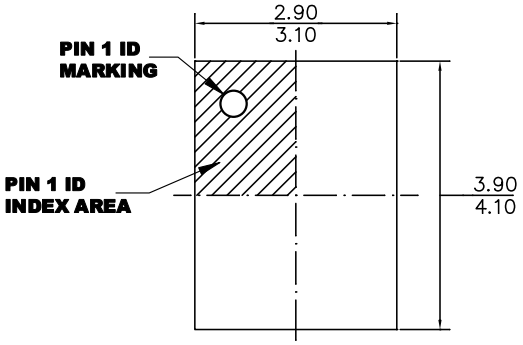
Figure 12: Typical Application Circuit (Fixed Output Version, V_{OUT} = 1.8V)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

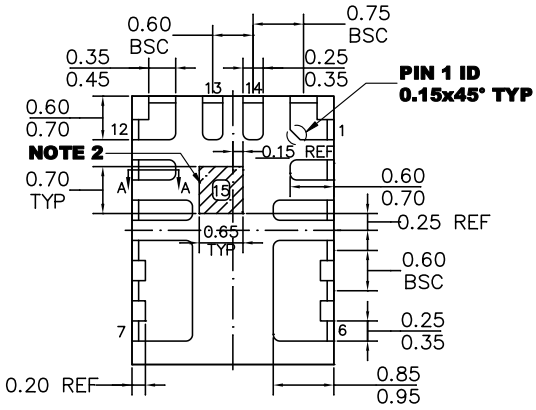
PACKAGE INFORMATION

QFN-15 (3mmx4mmx1.6mm)

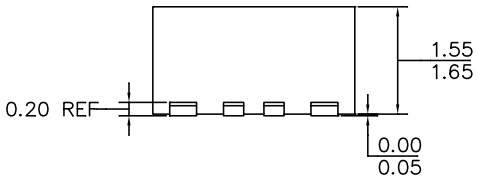
Wettable Flank



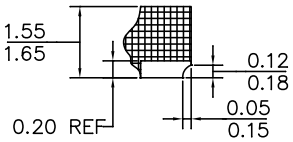
TOP VIEW



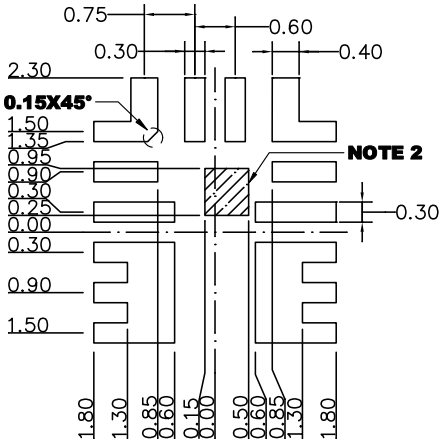
BOTTOM VIEW



SIDE VIEW



SECTION A-A



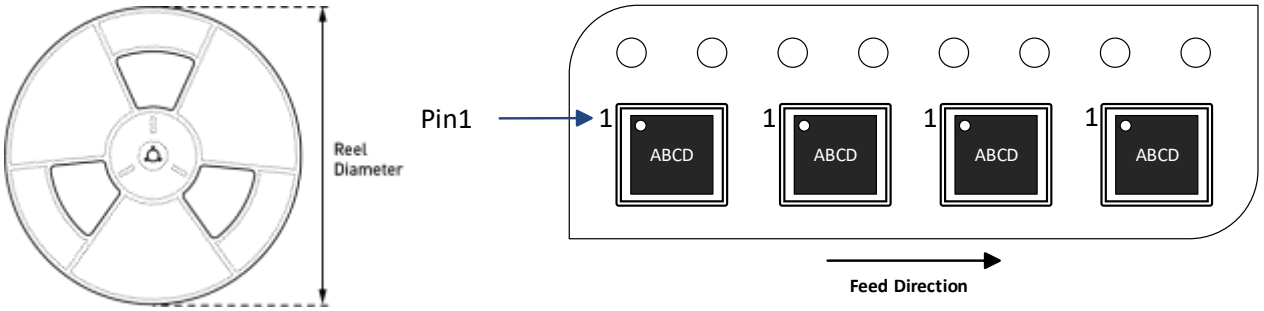
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) SHADED AREA IS THE KEEP-OUT ZONE. NO PCB METAL TRACE OR VIA CAN BE CONNECTED TO THIS AREA ELECTRICALLY OR MECHANICALLY.
3) THE LEAD SIDE IS WETTABLE.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM3806CGLE-AEC1-Z	QFN-15 (3mmx4mmx1.6mm)	2500	N/A	N/A	13in	12mm	8mm
MPM3806CGLE-12-AEC1-Z							
MPM3806CGLE-18-AEC1-Z							

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	10/28/2022	Initial Release	-

Notice: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.