



MPM3695-20

3V to 16V Input Power Module

Continuous 25A

DESCRIPTION

The MPM3695-20 is a scalable, fully integrated power module with a digital interface. The MPM3695-20 offers a complete power solution that achieves up to 25A of continuous output current with excellent load and line regulation over a wide input voltage range. It operates with high efficiency over a wide load range and can be paralleled to deliver a higher load current.

The MPM3695-20 adopts MPS's proprietary, multi-phase constant-on-time (MCOT) control, which provides ultra-fast transient response and simple loop compensation. The digital interface provides module configurations and monitoring of key parameters.

The MPM3695-20 features full protection features, including over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and over-temperature protection (OTP). It requires a minimal number of readily available external components and is available in the ECLGA-29 (5mmx6mmx4.4mm) package.

FEATURES

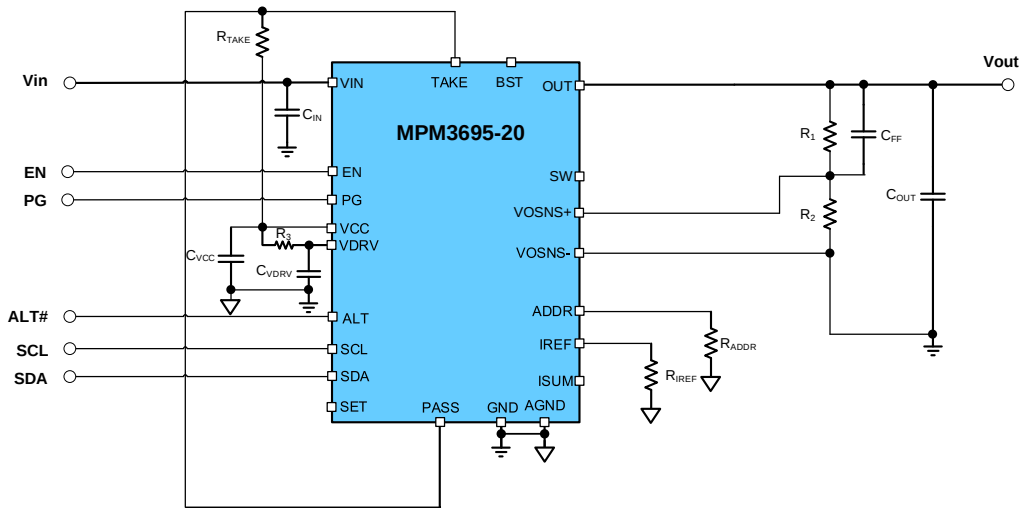
- Wide Input Voltage Range from 3V
 - 3V-16V Input Voltage with External V_{CC}
 - 4V-16V Input Voltage with Internal V_{CC}
- 0.5V to 5.5V Output Voltage Range
- 25A Continuous Output Current
- Auto Interleaving for Multi-Phase Operation
- Auto Compensation with Adaptive MCOT for Ultra-Fast Transient Response
- $\pm 1\%$ Reference Voltage Accuracy(-40°C to $+125^{\circ}\text{C}$)
- True Remote Sense of Output Voltage
- Pre-bias output
- Telemetry Read-Back Including V_{IN} , V_{OUT} , I_{OUT} , Temperature, and Faults
- Built-In MTP to store custom configuration
- Programmable via Digital Interface
 - Current Limit
 - Selection of Pulse-Skip Mode or Continuous Conduction Mode (CCM)
 - Soft-Start Time
 - Selection of switching Frequency from 400kHz,600kHz,800kHz,1000kHz
 - Fault Limits
 - Ramp compensation
- Available in ECLGA-29 (5mmx6mmx4.4mm) Package

APPLICATIONS

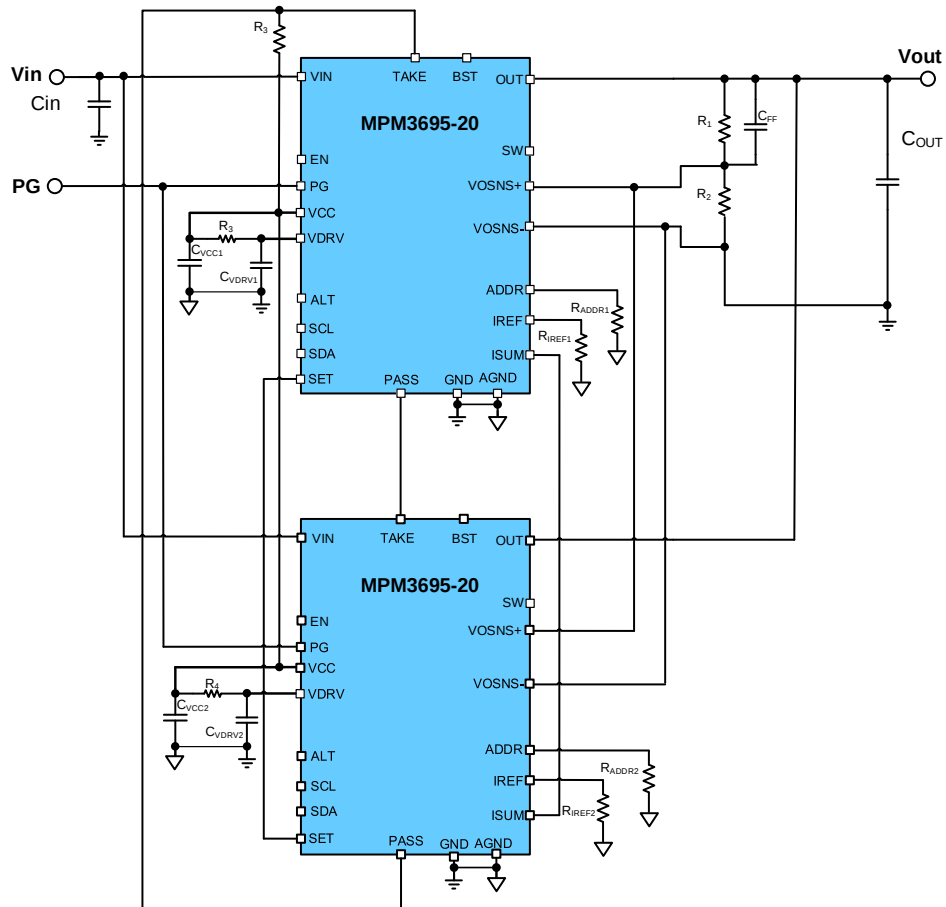
- Telecom and Networking Systems
- Industrial Equipment
- Servers and Computing
- FPGAs/ASIC AI and Data Mining

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TYPICAL APPLICATION



Single Phase Operation



Dual Phase Operation

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPM3695GPJ-20-xxxx**	ECLGA-29 (5mmx6mm4.4mm)	See Below	3
MPM3695GPJ-20-0022	ECLGA-29 (5mmx6mm4.4mm)	See Below	3
MPM3695GPJ-20-3333	ECLGA-29 (5mmx6mm4.4mm)	See Below	3

* For tray, add suffix -T (e.g. MPM3695GPJ-20-xxxx-T)

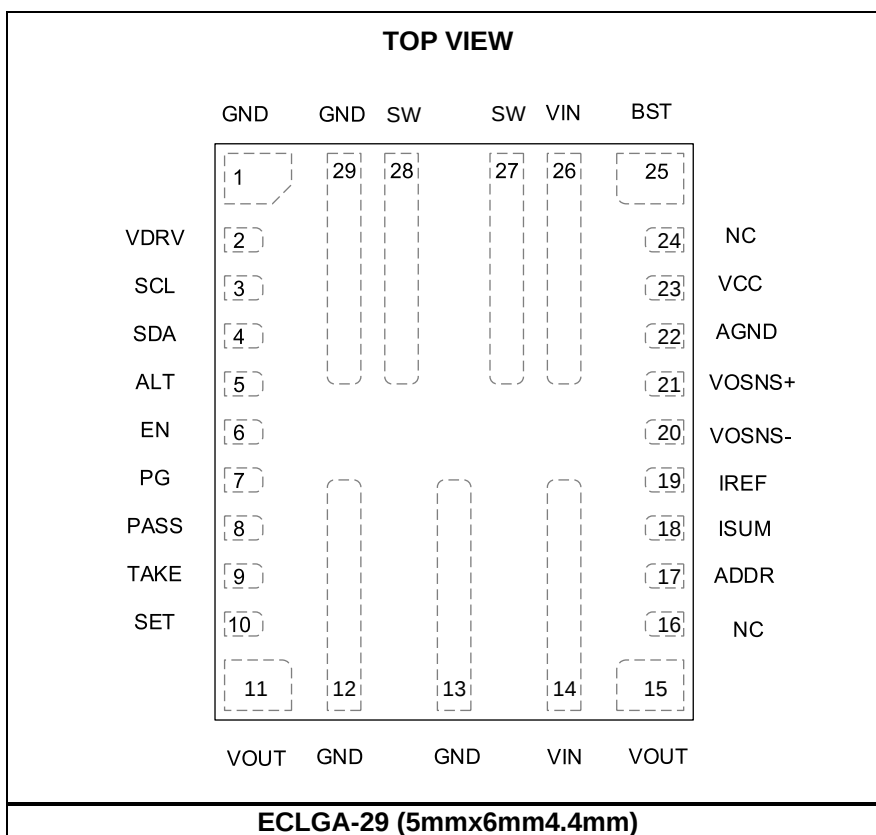
** “xxxx” is the configuration code identifier for the register settings stored in the MTP memory. Each “x” can be a hexadecimal value between 0 and F. Check the detailed configuration of 0022 and 3333 on page 53,54. Please contact MPS to create a unique configuration identifier for customized design.

TOP MARKING

MPSYYWW
MP3695
LLLLLLL
20M

MPS: MPS prefix
YY: Year code
WW: Week code
MP3695: Part number
LLLLLLL: Lot number
20: Suffix of part number
M: Module

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1,12,13,29	GND	Power ground. This pin is the reference point of the regulated output voltage. Connect with PCB copper planes as wide as possible.
2	VDRV	Decoupling pin for 3.3V driver power supply.
3	SCL	PMBus serial clock. Connect this pin to VCC pin with a 10kΩ resistor if this pin is used. Keep connecting to VCC or short to GND if it is not used, do not float it.
4	SDA	PMBus serial data. Connect this pin to VCC pin with a 10kΩ resistor if this pin is used. Keep connecting to VCC or short to GND if it is not used, do not float it.
5	ALT	PMBus alert. Open drain output, active low. A pull-up resistor must be connected to a 3.3V rail.
6	EN	Enable control. EN is a digital input that turns the regulator on or off. Drive EN high to turn the regulator on, drive it low to turn it off. Do not float this pin.
7	PG	Multi-purpose power good output. This pin can be configured as an output pin for single-phase operation or an input and output pin for multi-phase configuration. A pull-up resistor connected to a DC voltage is required to indicate high if the output voltage is higher than 90% of the nominal voltage. Refer to the application section for detailed configuration.
8	PASS	Passes RUN signal to the next phase. Refer to the applications section for connection details.
9	TAKE	Receives RUN signal from the previous phase. Refer to the typical applications section for connection details.
10	SET	PWM signal. The set signal turns on the HSFET when a RUN signal appears. For multi-phase operation, tie the SET pins of all the phases together.
11,15	VOUT	Module output voltage node. Connect with wide PCB copper plane.
17	ADDR	PMBus address setting pin. Connect a resistor between this pin to AGND to set the address of this device. Check Table 3 for reference.
18	ISUM	Reference current output. For single-phase operation, keep this pin floating; for multi-phase operation, connect ISUM pins of all phases together.
19	IREF	Current reference output. This pin is used to select I2C address. Connect a 60.4kohm or 180kohm resistor to AGND.
20	VOSNS-	Output voltage sense negative return. Connect directly to the GND sense point of the load for remote sense. Connect this pin to GND sense point of the output capacitor near the module if remote sense is not used. For parallel operation, connect the VOSNS- pins of the master and slave phases together.
21	VOSNS+	Output voltage sense positive return. Connect this pin to the positive sense point of the load to provide feedback voltage to the system for remote sense. Connect it to positive sense point of the output capacitor near the module if remote sense is not used. For parallel operation, connect the VOSNS+ pins of the master and slave phases together.
22	AGND	Analog ground. Reference point of the control circuit.
23	VCC	Output of the internal 3.3V LDO. The driver and control circuits are powered by this voltage. Must be connected to Pin 2 with a 2.2Ω resistor.
16, 24	NC	No Internal Connection. Keep them floating.
25	BST	Bootstrap. Keep this pin floating.
14, 26	VIN	Supply voltage. This pin provides power to the module. Decoupling capacitors are required to be connected between V _{IN} and GND. Connect V _{IN} with a wide copper plane.
27, 28	SW	Switch node. Keep them floating.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Supply voltage (V_{IN})	18V
$V_{SW(DC)}$	-0.3V to $V_{IN} + 0.3V$
$V_{SW(25ns)}$ ⁽²⁾	-5V to 25V
V_{OUT}	5.5V
V_{BST}	$V_{SW} + 4V$
V_{CC}	4.5V
$V_{CC(1s)}$ ⁽³⁾	6V
All other pins	-0.3V to 4.3V
All other pins ^(1s) ⁽³⁾	6V
Continuous power dissipation ($T_A = +25^\circ C$) ⁽⁴⁾	5W
Junction temperature	170°C
Lead temperature	260°C
Storage temperature	-65°C to +170°C

Recommended Operating Conditions ⁽⁵⁾

Supply voltage (V_{IN})	4V to 16V
Supply voltage (V_{IN}) ⁽⁶⁾	3V to 16V
Output voltage (V_{OUT})	0.5V to 5.5V
All other pins	-0.3V to 3.6V
External V_{CC} bias	3V to 3.6V
Operating junction temp. (T_J)	-40°C to +125°C

Thermal Resistance ⁽⁷⁾ θ_{JA} θ_{JB}

ECLGA-29 (5x6x4.4mm)	14.1	4.8	°C/W
JESD51-7 (5x6x4.4mm)	30	4.6	°C/W

Notes:

- Exceeding these ratings may damage the device.
- Measured by using differential oscilloscope probe.
- Voltage rating during MTP programming.
- The maximum allowable power dissipation is a function of the maximum junction temperature $T_J(MAX)$, the junction-to-ambient thermal resistance θ_{JA} , and the ambient temperature T_A . The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX) = (T_J(MAX) - T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- An external 3.3V V_{CC} bias is required when supply voltage is less than 4V. Writing to MTP memory is not supported with an external 3.3V V_{CC} bias.
- The value of θ_{JB} and θ_{JA} given in this table are only valid for comparison with other packages and cannot be used for design purposes. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

$V_{IN} = 12V$, $T_J = -40^{\circ}C$ to $125^{\circ}C$ ⁽⁸⁾, typical value is tested at $T_J = 25^{\circ}C$, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
V _{IN} Supply Current						
Supply current (shutdown)	I _{IN}	V _{EN} = 0V		2.5	4	mA
Input Voltage						
Input voltage range	V _{IN}	No external VCC	4		16	V
		With External VCC	3		16	V
Output Voltage						
Output voltage range ⁽⁸⁾	V _{OUT_RANGE}		0.5		5.5	V
Load regulation ⁽⁸⁾	V _{OUT_DC_Load}	I _{OUT} from 0A to 25A		±0.5		%V _{OUT}
Line regulation ⁽⁸⁾	V _{OUT_DC_Line}	V _{IN} from 4V to 16V, I _{OUT} = 20A		±0.5		%V _{OUT}
Current Limit						
Typical valley current limit programmable value	I _{LIM}	D7h= 11h		25.5		A
Min valley current limit programmable value ⁽⁸⁾		D7h=01h		1.5		A
Max current limit programmable value ⁽⁸⁾		D7h=15h		31.5		A
Low-side negative current limit in OVP	I _{LIM_NEG_OVP}			-13		A
EN						
EN ON threshold	EN _{ON}		2.2			V
EN OFF threshold	EN _{OFF}				1.2	V
Frequency and Timer						
Typical programmable Switching frequency	f _{SW}	D2h[2:1] =2b'01		600		kHz
Min programmable Switching frequency		D2h[2:1] =2b'00		400		kHz
Max programmable Switching frequency		D2h[2:1] =2b'11		1000		kHz
Minimum on time ⁽⁸⁾	T _{ON_MIN}	F _S = 1000kHz, V _{OUT} = 0.6V		50		ns
Minimum off time ⁽⁸⁾	T _{OFF_MIN}	V _{FB} = 580mV		220		ns
Output Over-Voltage and Under-Voltage Protection						
Default programmable OVP threshold	V _{OVP}	D4h[1:0] = 2b'00	111%	115%	119%	V _{REF}
Default programmable UVP threshold	V _{UVP}	D9h[3:2] = 2b'10	75%	79%	83%	V _{REF}
Max programmable OVP threshold	V _{OVP_max}	D4h[1:0] = 2b'11	126%	130%	134%	V _{REF}
Min programmable OVP threshold	V _{OVP_min}	D4h[1:0] = 2b'00	111%	115%	119%	V _{REF}
Max programmable UVP threshold	V _{UVP_max}	D9h[3:2] = 2b'11	80%	84%	88%	V _{REF}
Min programmable UVP threshold	V _{UVP_min}	D9h[3:2] = 2b'00	65%	69%	73%	V _{REF}

ELECTRICAL CHARACTERISTICS (continued)

$V_{IN} = 12V$, $T_J = -40^{\circ}C$ to $125^{\circ}C$ ⁽⁸⁾, typical value is tested at $T_J = 25^{\circ}C$, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
OSM threshold rising	V_{OSM_RISE}			104%		V_{REF}
OSM threshold falling	V_{OSM_FALL}			102%		V_{REF}
ADC⁽⁸⁾						
Internal ADC range			0		1.28	V
Vin sensing range			0		25.6	V
Vin sensing resolution				25		mV
Vosns sensing range (using external voltage divider)		D1h[1:0] = 2'b00	0.45		0.672	V
Vosns sensing resolution (using external voltage divider)		D1h[1:0] = 2'b00		1.25		mV
I _{sen} sensing range						
I _{sen} sensing resolution						
ADC resolution				10		bits
DNL				1		LSB
Sample rate				3		kHz
DAC (Reference Voltage)						
V _{ref} DAC Range			450	600	672	mV
V _{ref} DAC accuracy	V_{FB}		594	600	606	mV
V _{ref} DAC Resolution ⁽⁸⁾		Per LSB		2		mV
Feedback voltage with margin high ⁽⁸⁾	$V_{FB_MG_HIGH}$			672		mV
Feedback voltage with margin low ⁽⁸⁾	$V_{FB_MG_LOW}$			450		mV
Soft Start and Turn On/Off Delay						
Typical Soft-start time programmable value	t_{SS}	61h[2:0] = 3b'001		2		ms
Min Soft-start time programmable value		61h[2:0] = 3b'000		0		ms
Max Soft-start time programmable value		61h[2:0] = 3b'100		16		ms
Typical Turn-on delay programmable value ⁽⁸⁾	t_{ON_DELAY}	60h[7:0] = 0x00h		0		ms
Min Turn-on delay programmable value ⁽⁸⁾		60h[7:0] = 0x00h		0		ms
Max Turn-on delay programmable value ⁽⁸⁾		60h[7:0] = 0xFFh		1020		ms
Error Amplifier						
Feedback Current (V _{OSNS} + pin)	I_{FB}	$V_{FB} = V_{REF}$ (V_{FB} is the difference of V _{OSNS} + and V _{OSNS} -)		50	100	nA
Soft Shutdown						

ELECTRICAL CHARACTERISTICS *(continued)*

$V_{IN} = 12V$, $T_J = -40^{\circ}C$ to $125^{\circ}C$ ⁽⁸⁾, typical value is tested at $T_J = 25^{\circ}C$, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Soft shutdown discharge FET	R_{ON_DISCH}			60		Ω
Under-Voltage Lockout (UVLO)						
VCC under-voltage lockout threshold	V_{CCVth}		2.6	2.75	2.9	V
VCC under-voltage lockout threshold hysteresis	V_{CCHYS}			250		mV
Min input programmable turn-on voltage	$V_{IN_ON_MIN}$	$V_{CC} = 3.3V$		2.9	3	V
Max input programmable turn-on voltage	$V_{IN_ON_MAX}$		16	16.5	17	V
Min input programmable turn-off voltage	$V_{IN_OFF_MIN}$	$V_{CC} = 3.3V$		2.75		V
Max input programmable turn-off voltage	$V_{IN_OFF_MAX}$			15.75		V

ELECTRICAL CHARACTERISTICS (continued)

$V_{IN} = 12V$, $T_J = -40^{\circ}C$ to $125^{\circ}C$ ⁽⁸⁾, typical value is tested at $T_J = 25^{\circ}C$, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Power Good						
Power good high threshold	PG _{Vth_Hi}	FB from low to high, D9h[1:0] = 2b'01		94%		V _{REF}
Power good low threshold	PG _{Vth_Lo}	FB from high to low, D9h[3:2] = 2b'10		79%		V _{REF}
Power good low to high delay	PG _{Td}	D1h[5:2] = 4b'0000		2.0		ms
Power good sink current capability	I _{PG}	V _{PG} = 0.3V			10	mA
Power good leakage current	I _{PG_LEAK}	V _{PG} = 3V		1.5		μA
Power good low-level output voltage	V _{OL_100}	V _{IN} = 0V, pull PGOOD up to 3.3V through a 100kΩ resistor, T _J = 25°C		600	720	mV
	V _{OL_10}	V _{IN} = 0V, pull PGOOD up to 3.3V through a 10kΩ resistor, T _J = 25°C		700	820	
Thermal Protection (TP)						
TP fault rising threshold ⁽⁸⁾	T _{SD_Rise}	4Fh = A0h		160		°C
TP fault falling threshold ⁽⁸⁾	T _{SD_Fall}	4Fh = A0h, D6h[2:1] = 2b'00		140		°C
TP warning rising threshold ⁽⁸⁾	T _{WARN_Rise}	51h = 8Ch		140		°C
TP warning falling threshold ⁽⁸⁾	T _{WARN_Fall}	51h = 8Ch, D6h[2:1] = 2b'00		120		°C
Min TP warning temp ⁽⁸⁾	T _{SD_WARN_MIN}			35		°C
Max TP warning temp ⁽⁸⁾	T _{SD_WARN_MAX}			160		°C
Monitoring Parameters						
Output voltage monitor accuracy ⁽⁸⁾	M _{VOUT_ACC}	V _{OUT} =0.6V	0.588	0.6	0.612	V
Output voltage bit resolution ⁽⁸⁾				1.25		mV
Output current monitor accuracy ⁽⁸⁾	M _{IOUT_ACC}	V _{OUT} = 1.2V, fs = 600kHz, I _{OUT} = 20A	18	20	22	A
Output current bit resolution ⁽⁸⁾				62.5		mA
Input voltage monitor accuracy	M _{IN_ACC}		11.76	12	12.24	V
Input voltage bit resolution ⁽⁹⁾				25		mV

ELECTRICAL CHARACTERISTICS (continued)

$V_{IN} = 12V$, $T_J = -40^{\circ}C$ to $125^{\circ}C$ ⁽⁸⁾, typical value is tested at $T_J = 25^{\circ}C$, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
PMBus DC Characteristics (SDA, SCL, ALERT) ⁽⁸⁾						
Input high voltage	V_{IH}		2.1			V
Input low voltage	V_{IL}				0.8	V
Output low voltage	V_{OL}	$I_{OL} = 1mA$			0.4	V
Input leakage current	I_{LEAK}	SDA, SCL, ALERT = 3.3V	-10		10	μA
Maximum voltage (SDA, SCL, ALERT, EN)	V_{MAX}	Transient voltage including ringing	-0.3	3.3	3.6	V
Pin capacitance on SDA, SCL	C_{PIN}				10	pF
PMBus Timing Characteristics ⁽⁹⁾						
Min operating frequency				10		kHz
Max operating frequency				1000		kHz
Bus free time		Between stop and start condition	0.5			μs
Holding time			0.26			μs
Repeated start condition set-up time			0.26			μs
Stop condition set-up time			0.26			μs
Data hold time			0			ns
Data set-up time			50			ns
Clock low time out			25		35	ms
Clock low period			0.5			μs
Clock high period			0.26		50	μs
Clock/data fall time		100kHz Class			300	ns
		400kHz Class			300	ns
		1000kHz Class			120	ns
Clock/data rise time		100kHz Class			1000	ns
		400kHz Class			300	ns
		1000kHz Class			120	ns

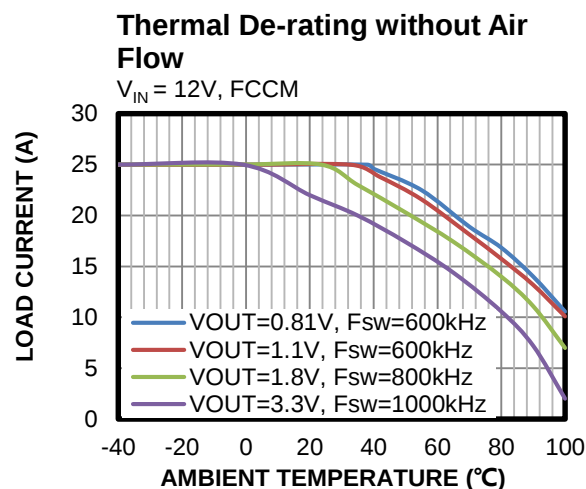
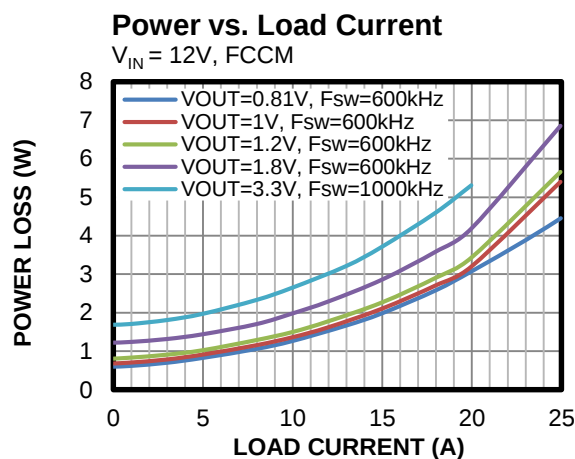
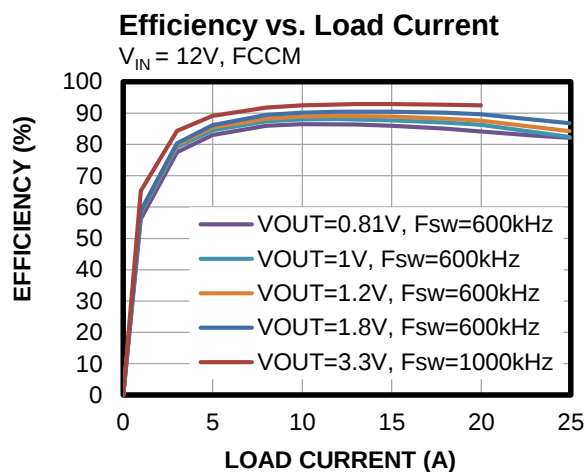
Notes:

8) Guaranteed by sample characterization.

9) Guaranteed by sample characterization. Not tested in production. The parameter is tested during parameters characterization.

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN}=12V$, $V_{OUT}=1.2V$, $F_{SW}=600kHz$, $T_A=+25^{\circ}C$, unless otherwise noted.

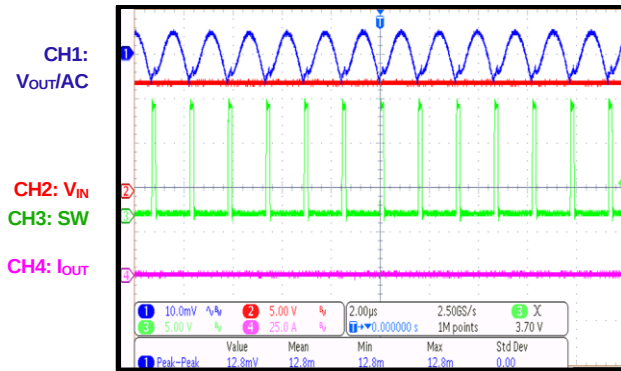


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN}=12V$, $V_{OUT}=1.2V$, $F_{SW}=600kHz$, $T_A=+25^{\circ}C$, unless otherwise noted.

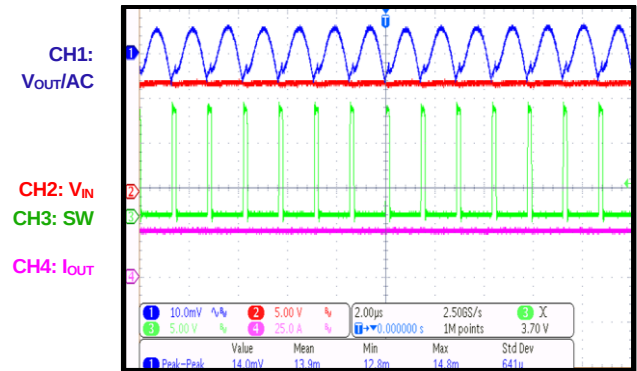
Output Voltage Ripple

$I_{OUT} = 0A$



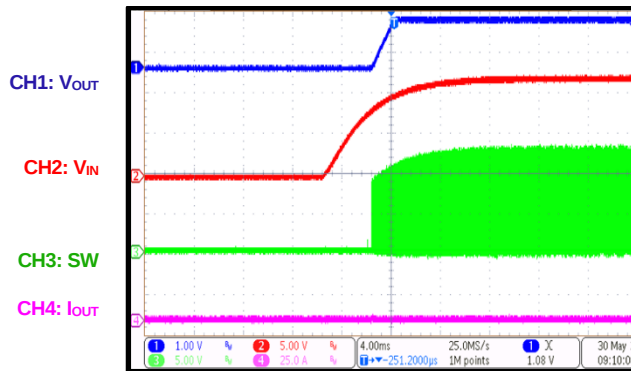
Output Voltage Ripple

$I_{OUT} = 25A$



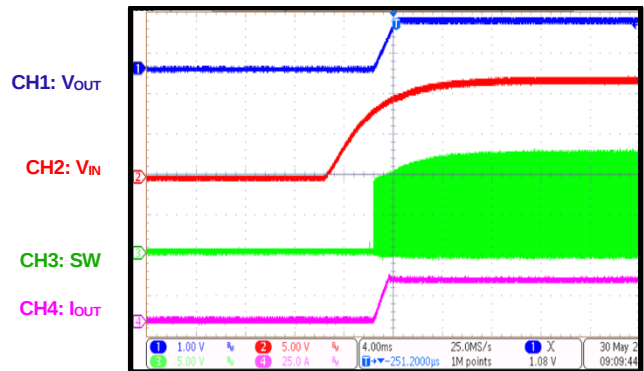
V_{IN} Start-Up

$I_{OUT} = 0A$



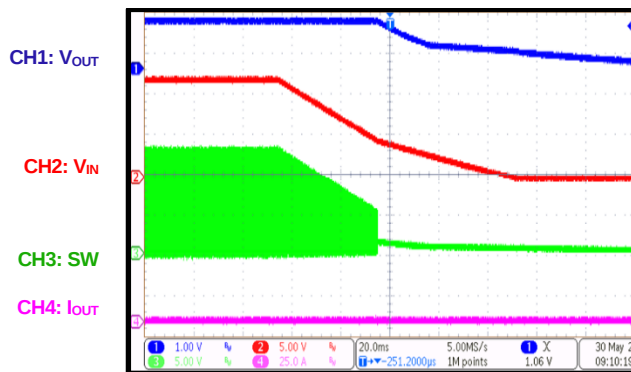
V_{IN} Start-Up

$I_{OUT} = 25A$



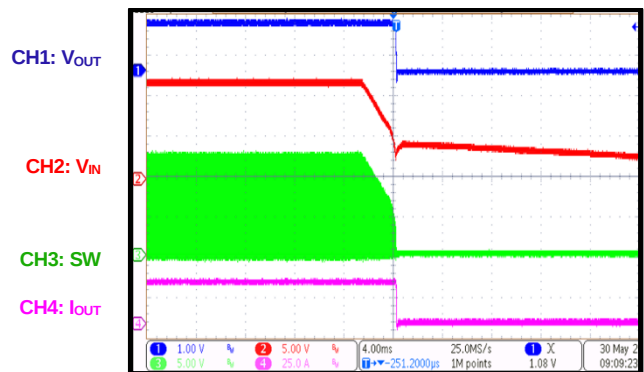
V_{IN} Shutdown

$I_{OUT} = 0A$



V_{IN} Shutdown

$I_{OUT} = 25A$

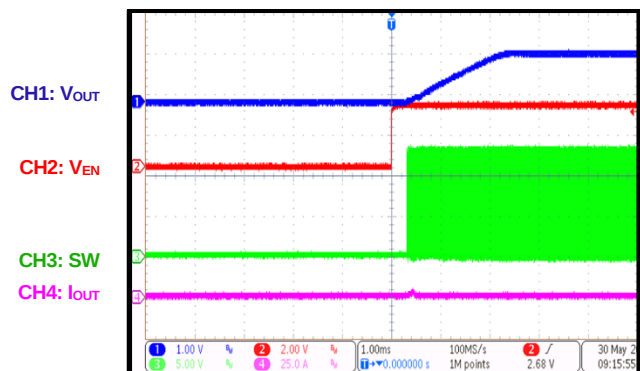


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN}=12V$, $V_{OUT}=1.2V$, $F_{SW}=600kHz$, $T_A=+25^{\circ}C$, unless otherwise noted.

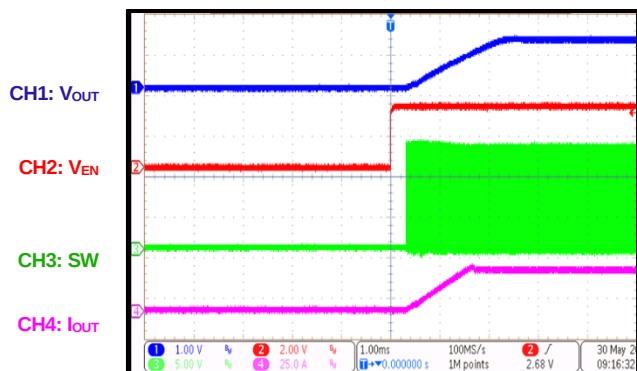
EN Start-Up

$I_{OUT} = 0A$



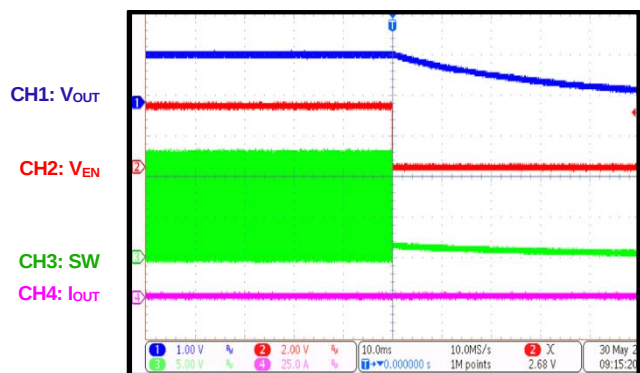
EN Start-Up

$I_{OUT} = 25A$



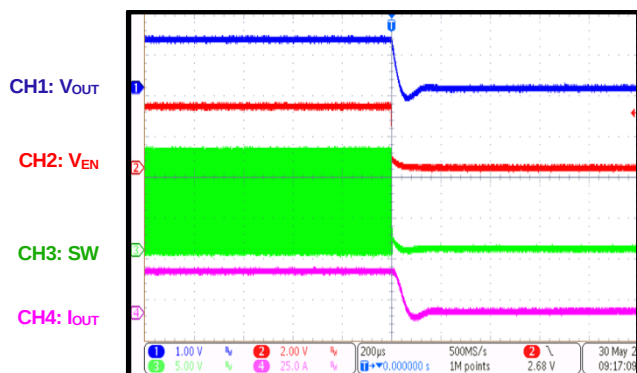
EN Shutdown

$I_{OUT} = 0A$



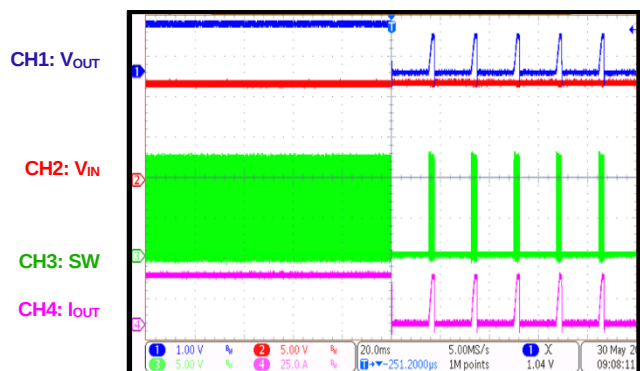
EN Shutdown

$I_{OUT} = 25A$



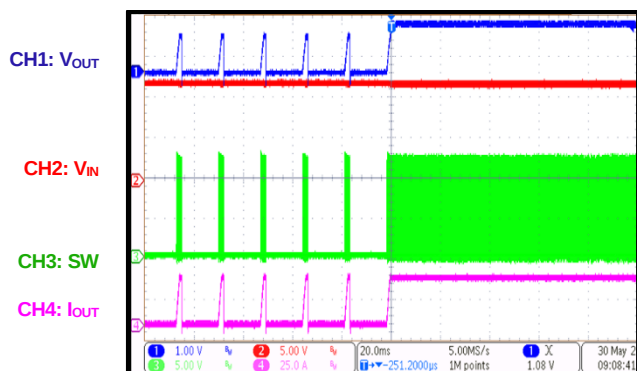
OCP Entry

$I_{OUT} = 25A$



OCP Recovery

$I_{OUT} = 25A$

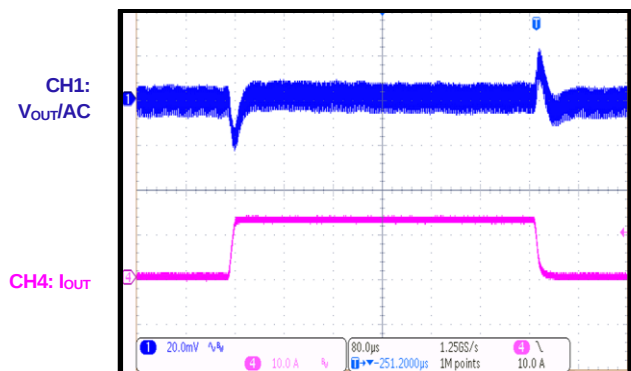


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN}=12V$, $V_{OUT}=1.2V$, $F_{SW}=600kHz$, $T_A=+25^{\circ}C$, unless otherwise noted.

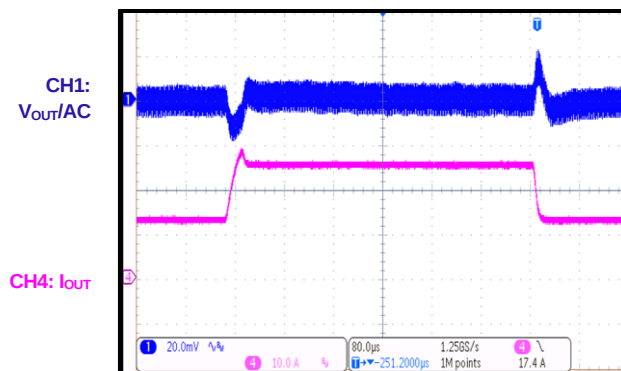
Load Transient

0-12.5A Load Step, 2.5A/ μs



Load Transient

12.5-25A Load Step, 2.5A/ μs



BLOCK DIAGRAM

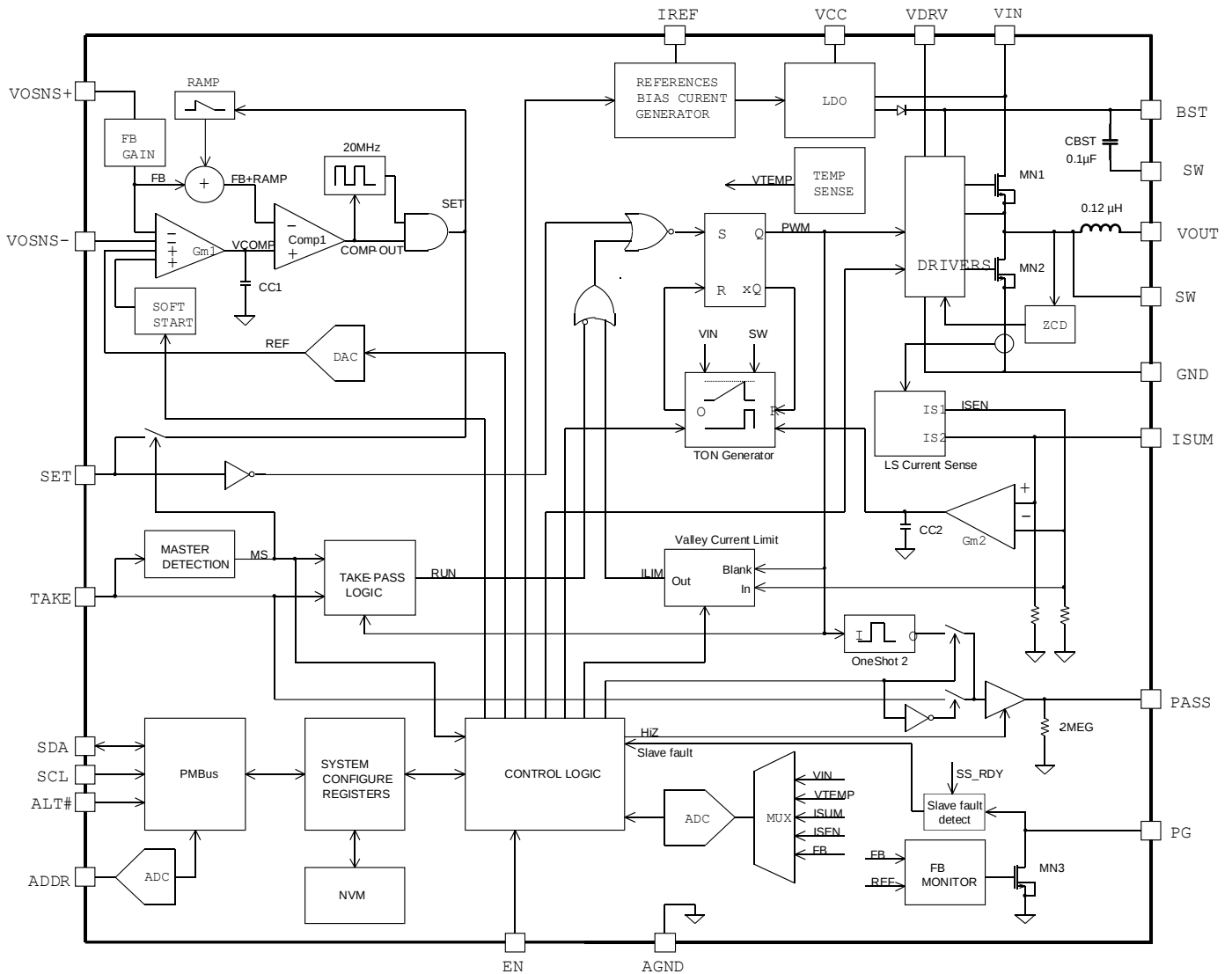


Figure 1: Functional Block Diagram

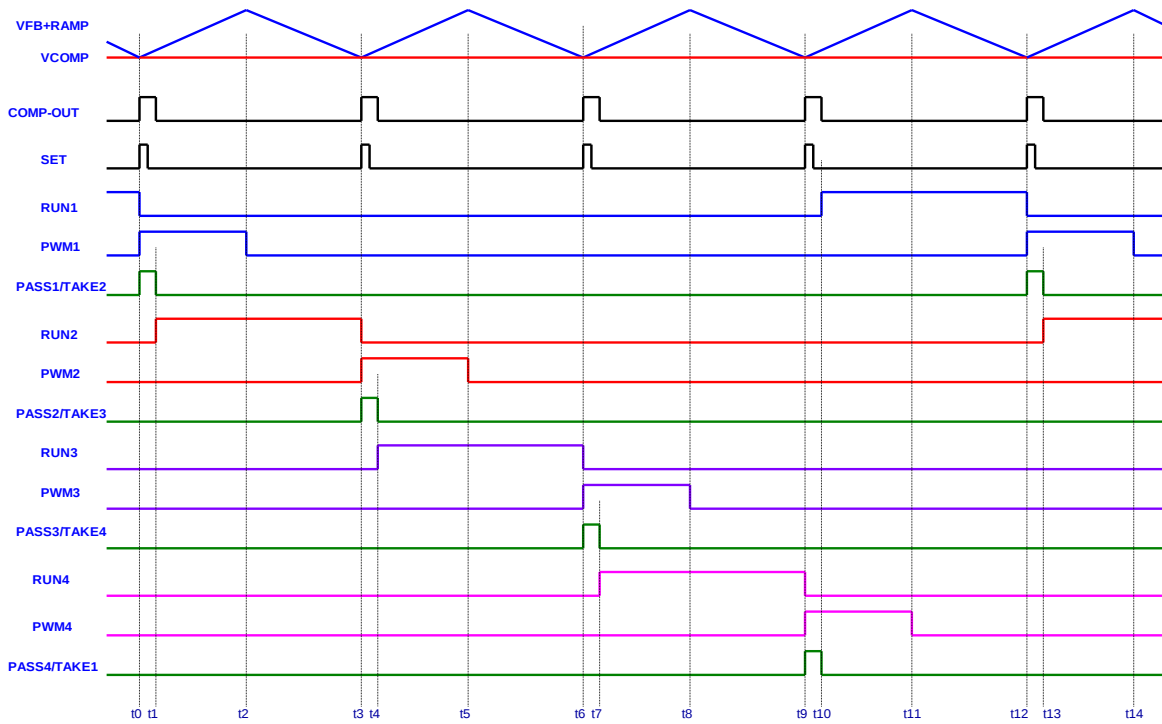


Figure 2: Multi-Phase Operation Timing Diagram (Steady State)

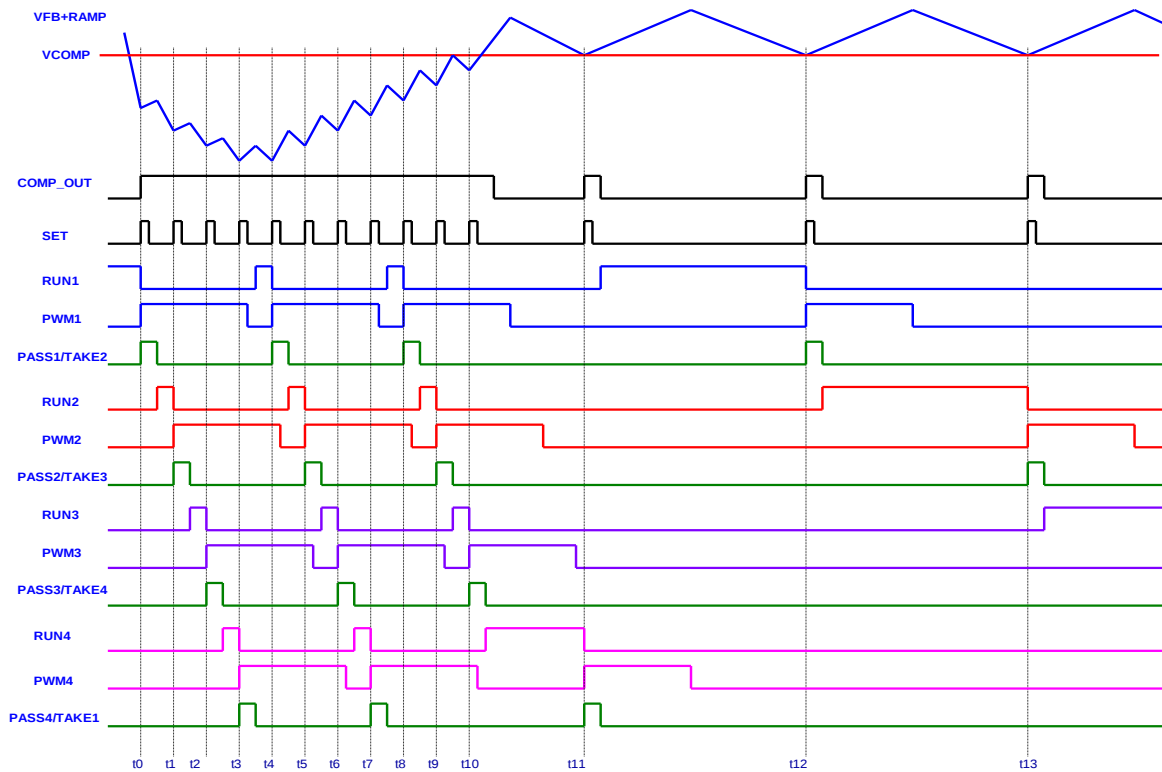


Figure 3: Multi-Phase Operation Timing Diagram (Transient)

OPERATION

The MPM3695-20 is a fully integrated power solution with up to 25A output current in a 5x6x4.4mm ECLGA package. For applications that require more than 25A, the MPM3695-20 can be connected in parallel to provide a higher output current. The MPM3695-20 employs constant-on-time (COT) control to provide fast transient response. The internal ramp compensation guarantees stable operation for applications using zero-ESR ceramic output capacitors.

Multi-Phase Operation

In a multi-phase configuration, one master phase and up to five slave phases are connected in parallel. The output current is shared equally among all phases. The typical application circuit illustrates four MPM3695-20s in a multi-phase configuration. The TAKE pin of the master phase is required to be pulled up to a voltage source through a resistor. The MPM3695-20 detects its master/slave configuration by monitoring the state of the TAKE pin during start-up. The PASS and TAKE pins of all phases are connected in a cascaded manner (See Typical Application circuit). The PASS pin of the last slave-phase is connected back to the TAKE pin of the master phase.

MCOT Operation-Master Phase

A master phase performs the following functions:

- Accepts both write and read commands through PMBus from a host
- Generates the SET signal
- Manages the start-up, shut-off, and all the protections
- Monitors fault alerts from the slave phases through the PG pin
- Generates the first ON pulse
- Generates the ON pulse when receiving RUN and SET signals
- Dynamically adjusts its on-time to ensure equal current sharing
- Generates the PASS signal

MCOT Operation-Slave Phases

The slave phase performs the following functions:

- Accepts write commands through PMBus from a host
- Receives the SET signal from a master
- Sends an OV/UV/OT fault alert to a master phase through the PG pin
- Starts the ON pulse when receiving RUN and SET signals
- Dynamically adjusts its on-time to ensure equal current sharing with its own phase based on the per-phase and total current
- Generates the PASS signal

Figure 2 illustrates MCOT operation. At t₀, a SET pulse is generated by the master phase when (VFB+RAMP) drops below the reference level (VCOMP). All the phases receive this SET signal, but only the phase (the MASTER) that has an active RUN signal will take action, so the MASTER turns on the High-Side-FET (HS-FET). Meanwhile, it generates a fixed width-pulse on the PASS pin, and passes it to the TAKE pin of SLAVE1.

At t₁, the falling edge of the TAKE pin of SLAVE1 activates the RUN signal. This enables the SLAVE1 to wait for the SET signal to turn on its HS-FET.

At t₂, the ON time of the PWM signal of the MASTER phase expires and the HS-FET is turned off. The ON time of the PWM signal is fixed for any given input voltage, output voltage and switching frequency. The ON time of each phase is fine-tuned based on the per phase and the total current to ensure equal current sharing among phases.

At t₃, the (VFB+RAMP) drops below the reference level (VCOMP) in the MASTER phase again, only SLAVE1 has an active RUN signal, so it turns on its HS-FET. All other phases ignore this SET signal. Meanwhile, the SLAVE1 generates a pulse with fixed width on the PASS pin, and passes it to the TAKE pin of SLAVE2.

The MPM3695-20 keeps above MCOT operation and each phase turns on its HS-FET one by one for a fixed ON time. The operation is similar to a relay race and the RUN signal is like the baton. The relay is carried on through the PASS/TAKE loop. Only the phase that has the baton (RUN signal) will turn on the HS-FET when the SET signal is ready.

The MPM3695-20 benefits from MCOT control to achieve extremely fast load transient response. The SET signal is generated more frequently during a load transient compared to steady state (See Figure 3). Consequently, energy is delivered to the load at a higher rate, which minimizes the output deviation during a load transient event. With the MPM3695-20, the SET pulses are generated with a minimum 50ns interval, i.e., the next phase can be turned on as fast as 50ns after the turn-on of the previous phase.

RAMP Compensation

The MPM3695-20 guarantees stable operation with zero-ESR ceramic output capacitors by using internal RAMP compensation. A triangular RAMP signal is generated internally and is superimposed on the FB signal. The triangular RAMP signal starts to rise once RAMP+FB drops below the REF signal, and a SET pulse is generated. The rise time of the RAMP signal is fixed. The amplitude of the RAMP compensation is selectable through the PMBus command of D0h[3:1] to support wide operation configurations. There is a trade-off between the stability and load transient response. A larger RAMP signal provides higher stability but a slower load transient response and vice versa. Consequently, it is necessary to optimize the RAMP compensation selection based on the design criteria for each application.

APPLICATION INFORMATION

Operation Mode Selection

The MPM3695-20 provides both forced CCM and pulse skip operations in a light-load condition. Four switching frequencies are available for the MPM3695-20. The selection of operation mode in a light-load condition and the switching frequency is done through the PMBus.

CCM Operation

When the output current is high and the inductor current is always above zero amps, it is called continuous-conduction-mode (CCM). The CCM mode operation is shown in Figure 3 shown. When V_{FB} is below V_{EAO} , HS-MOSFET is turned on for a fixed interval which is determined by one-shot on-timer. When the HS-MOSFET is turned off, the LS-MOSFET is turned on until next period.

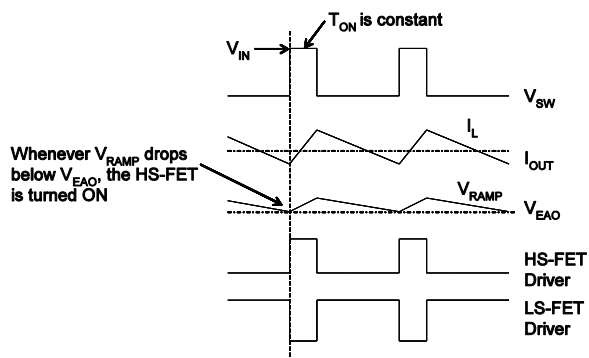


Figure 3: Heavy Load Operation

In CCM mode operation, the switching frequency is fairly constant and it is called PWM mode.

Pulse Skip Mode (PSM)

When the MPM3695-20 works in pulse skip mode (PSM) during light-load operation, the MPM3695-20 reduces the switching frequency to maintain high efficiency, and the inductor current drops near zero. When the inductor current reaches zero, the LS-FET driver goes into tri-state (high Z) as shown in Figure 4. Therefore, the output capacitors discharge slowly to GND through LS-FET and load. This operation greatly improves device efficiency when the output current is low.

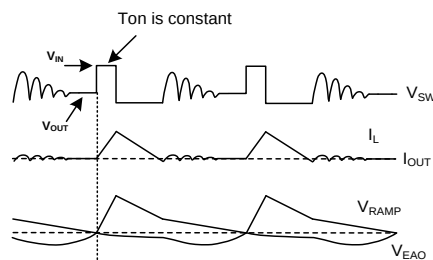


Figure 4, Light Load Operation

PSM is also called discontinuous conduction mode or pulse-frequency modulation (PFM) because the HS-FET does not turn on as frequently as during CCM. The frequency at which the HS-FET turns on is a function of the output current. As the output current increases, the current modulator regulation period becomes shorter, and the HS-FET turns on more frequently. This is the increasing on the switching frequency.

Output Voltage Setting

The MPM3695-20 offers two methods for adjusting the output voltage: either through the internal resistor voltage divider or via the external resistor divider. In addition, the output voltage can be adjusted within a certain range through PMBus by adjusting the internal reference voltage of the PWM controller (V_{REF}). The reference voltage, which has a default value of 0.6V, can be adjusted between 0.5V to 0.672V.

Internal Voltage Setting

Figure 4 shows the configuration of the internal voltage divider. VOSNS+ and VOSNS- are connected directly to the output voltage sense point.

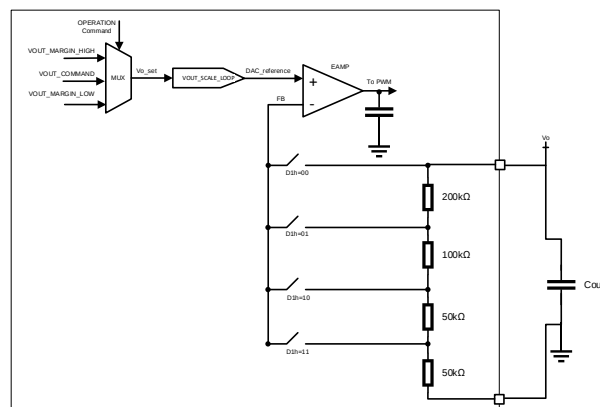


Figure 4: Output Voltage Set by Internal Resistors Divider

Select the appropriate output voltage range when using the internal resistor divider. The feedback gain plays a crucial role in regulating the output voltage during load transient. A higher feedback gain typically leads to faster response times to load transients. However, excessively high gains can introduce instability or overshoot. Table 1 shows the internal voltage divider options throughout the MFR_CTRL_VOUT (D1h).

Table 1 VOUT_SCALE_LOOP vs MFR_CTRL_VOUT

FB Divider	VOUT_SCALE_LOOP (29h)	MFR_CTRL_VOUT (D1h[1:0])
External	29h = RFB2 / (RFB1 + RFB2)	D1h[1:0] = 2'b00: VREF / VO = 1, VO = 0.4V to 5.5V
Internal	29h = 0x01F4	D1h[1:0] = 2'b01: VREF / VO = 0.5, VO = 0.4V to 1.344V
	29h = 0x00FA	D1h[1:0] = 2'b10: VREF / VO = 0.25, VO = 0.7V to 2.688V
	29h = 0x007D	D1h[1:0] = 2'b11: VREF / VO = 0.125, VO = 1.3V to 5.376V

External Voltage Setting

A feedback resistor divider is required to set the proper feedback gain. Figure 5 shows the configuration of an external voltage divider used. VOSNS+ and VOSNS- are connected to the output voltage sense point through a resistor divider (R1 and R2).

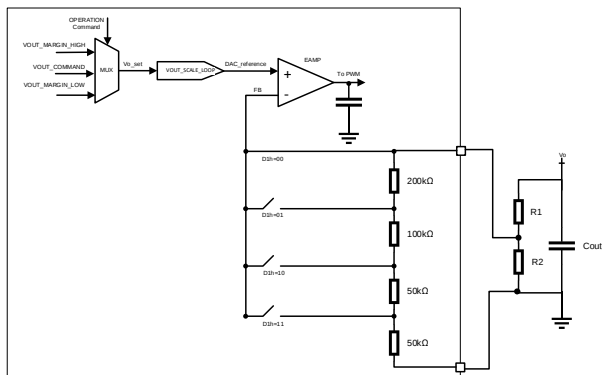


Figure 5: Output Voltage Set by External Resistors Divider

The values of the feedback resistors are determined using equation 1:

$$R_2(k\Omega) = \frac{0.6}{V_O - 0.6} \times R_1(k\Omega) \quad (1)$$

where V_{OUT} is the output voltage. The output voltage feedback gain is determined with equation 2:

$$G_{FB} = \frac{R_2}{R_1 + R_2} \quad (2)$$

To optimize the load transient response, a feed-forward capacitor (C_{FF}) is required to be placed in parallel with R_1 . Table 2 lists the values of the feedback resistors and the feedforward capacitor for common output voltages.

Table 2: Common Output Voltages

V _{OUT} (V)	R ₁ (kΩ)	R ₂ (kΩ)	C _{FF} (nF)	VOUT_SCALE_LOOP (29h)
0.9	0.5	1	33	0.67
1.2	1	1	33	0.50
1.8	2	1	33	0.33
3.3	4.53	1	4.7	0.18
5	7.32	1	4.7	0.12

For a given feedback resistor network, the upper and lower limits of the output voltage are determined with equation 3a and equation 3b:

$$V_{o,max} = \frac{0.672}{G_{FB}} \quad (3a)$$

$$V_{o,min} = \frac{0.5}{G_{FB}} \quad (3b)$$

Three steps need to be followed to program the output voltage through PMBus:

1. The MFR_CTRL_VOUT (D1h) can only be set to D1[1:0] = 2'b00, see Table 1.
2. Write G_{FB} value determined by Equation 2 to register VOUT_SCALE_LOOP (29h)
3. Write the output voltage command to register VOUT_COMMAND (21h)

V_{REF} is updated automatically based on the output voltage command and G_{FB}

Output voltage monitoring through PMBus is enabled by setting the register

VOUT_SCALE_LOOP (29h) with a value that matches the G_{FB} calculated with Equation 2.

For applications where a PMBus interface is not required, $V_{REF}=0.6V$ is used by default, and the MPM3695-20 operates in analog mode. The feedback resistors should be determined based on Equation 1.

Soft Start

The soft start (SS) time can be programmed through PMBus. The default SS time is 2ms. Figure 6 shows the timing parameters that can be programmed through PMBus interface during the start-up and shutdown.

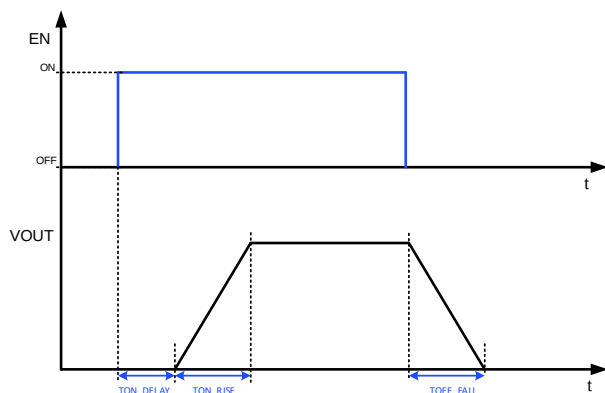


Figure 6 Soft Start and Shutdown

Pre-Bias Start-Up

The MPM3695-20 is designed for monotonic startup into pre-biased loads. If the output voltage is pre-biased to a certain voltage during startup (see Figure 7), both the high-side and low-side switches are disabled until the internal reference voltage exceeds the sensed output voltage.

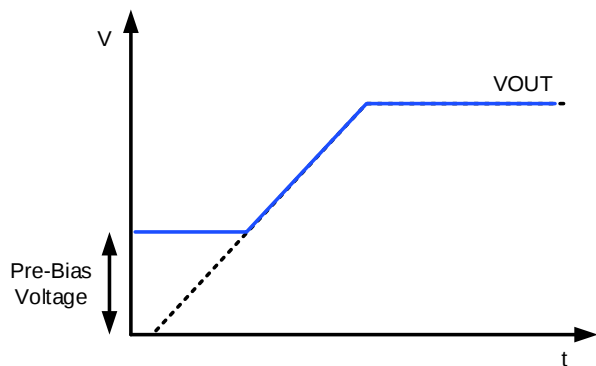


Figure 7: Pre-Bias Output Voltage

Output Voltage Discharge

The output voltage discharge mode will be enabled if the MPM3695-20 is disabled through the EN pin. Figure 8 shows the behaviour of the output voltage when the output discharge is enabled. In such a case, both the high-side and low-side switches are latched off. A discharge FET connected between SW and GND is turned on to discharge the output capacitor. A typical on-resistance of the discharge FET is 60Ω. Once the sensed output voltage drops below 10% of the reference output voltage, the discharge FET is turned off.

This feature can be enabled or disabled through the MFR_CTRL_VOUT (D1h) command.

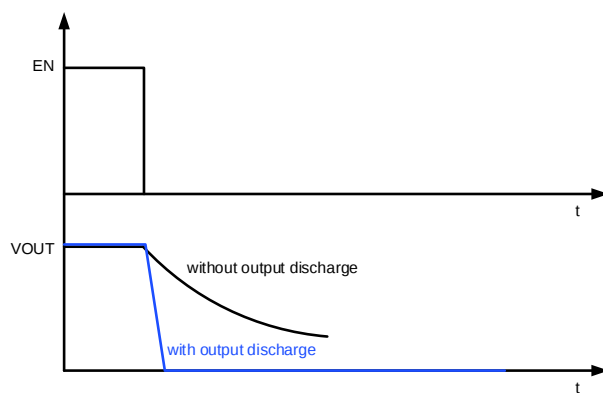


Figure 8 Output Voltage Discharge Function Current Sense and Over-Current Protection (OCP)

The MPM3695-20 features on-die current sense and a programmable positive current limit threshold.

The MPM3695-20 provides both inductor valley current limits (set by register D7h).

Inductor Valley Over-Current Protection (D7h)

During the LS-FET ON state, the inductor current is sensed and monitored cycle-by-cycle. The HS-FET will only be allowed to turn ON if over-current is not detected during the LS-FET ON-state. If there are 31 consecutive cycles of an OC condition detected, OCP is triggered.

During an over-current condition or output short-circuit condition, if the output voltage drops below the under-voltage protection (UVP) threshold, the MPM3695-20 enters OCP immediately.

Once OCP is triggered, it either enters HICCUP mode or latch-off mode, depending on the register. It should be noted that a power-recycle of the Vcc or EN is required to re-enable the MPM3695-20 once it latches-off.

The inductor valley over-current limit can be programmed through register D7h, which sets the per-phase inductor valley current limit for both single and multi-phase operation. Figure 9 shows the behavior of the output voltage when the OCP is triggered and HICCUP mode is selected.

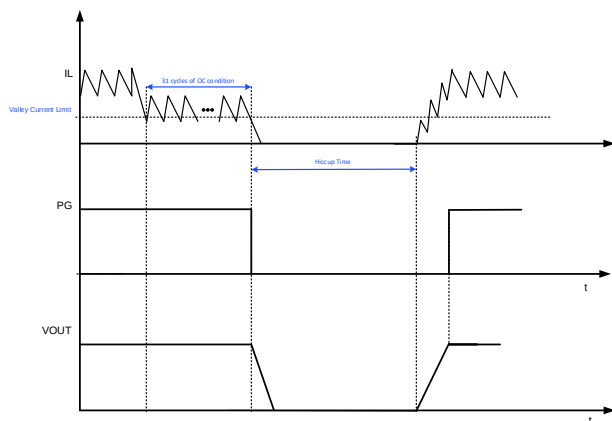


Figure 9 Valley Current Limit with Hiccup Mode Enabled

Negative Inductor Current limit

When the LS-FET detects a negative current lower than the limit (-13A), the part will turn off its LS-FET for a period of time to limit the negative current. The period is set through register D5h[3].

Under -Voltage Protection (UVP)

The MPM3695-20 monitors the output voltage through the VONSNS+/- pins to detect an under-voltage condition. If the internal FB voltage drops below the UVP threshold (set through register VOUT_UV_FAULT_LIMIT), the UVP is triggered. After UVP is triggered, the MPM3695-20 enters either HICCUP or latch-off mode, depending on the PMBus selection. Please note that a power-recycle of the Vcc or EN is required to re-enable the MPM3695-20 once it latches off.

Over-Voltage Protection (OVP)

The MPM3695-20 monitors the output voltage using the VOSNS+/- pins connected to the tap of a resistor divider to detect an over-voltage condition. Please refer to the register VOUT_OV_FAULT_RESPONSE section for additional information on OVP.

Output Sinking Mode (OSM)

The MPM3695-20 enters the OSM when the output voltage is more than 5% higher than the reference and below the OVP threshold. Once the OSM is triggered, the MPM3695-20 runs in forced CCM. The MPM3695-20 exits OSM mode when the HS-FET turns back on. OSM mode can be enabled or disabled by configuring register 0xEA[9].

Over-Temperature Protection (OTP)

The MPM3695-20 monitors the junction temperature. If the junction temperature exceeds the threshold value (set by register OT_FAULT_LIMIT), the converter enters either HICCUP or latch-off mode depending on the PMBus selection. Please note that a power-recycle of the Vcc or EN is required to re-enable the MPM3695-20 once it latches off.

Power Good (PG)

The MPM3695-20 has an open-drain power-good (PG) output. The PG pin can be configured as an output only or input and output pin by bit [0] of register MRF_CTRL_COMP (D0h). For single-phase configuration, the PG pin should be configured as output only. For multi-phase operation, the PG pin should be configured as an input and output pin to detect faults from the slave phases. The PG pin must be pulled high, to Vcc or a voltage source, with less than 3.6V through a pull-up resistor (typically 100kΩ).

PG is pulled low initially once input voltage is applied to the MPM3695-20. After the internal FB voltage reaches the threshold set by register POWER_GOOD_ON, the PG pin is pulled high after a delay set by the register MFR_CTRL_VOUT, see Figure 10.

PG is latched low if any fault occurs, and the relevant protection feature is triggered (e.g., UV, OV, OT, UVLO, etc.). After the PG is latched low, it cannot be pulled high again unless a new soft-start is initialized.

If the input supply fails to power the MPM3695-20, the PG is latched low.

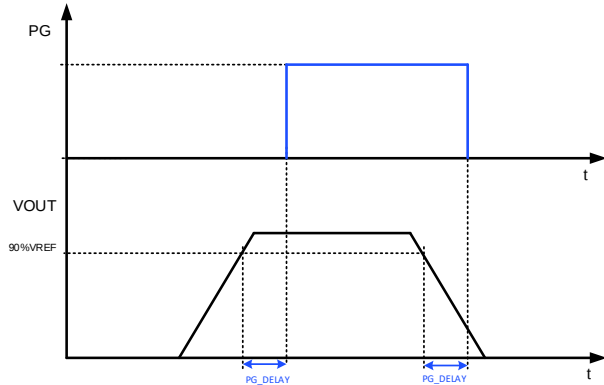


Figure 10 Power Good Delay Time

Input Capacitor

The input current to a buck converter is discontinuous, and therefore, requires a capacitor to supply the AC current to the step-down module while maintaining the DC input voltage. Use ceramic capacitors for the best performance. During layout, place the input capacitors as close to the V_{IN} pin as possible.

The capacitance can vary significantly with temperature. Use capacitors with X5R and X7R ceramic dielectrics, because they are fairly stable over a wide temperature range.

The capacitors must also have a ripple current rating that exceeds the converter's maximum input ripple current. Estimate the input ripple current using equation 4:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (4)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (5)$$

For simplification, choose an input capacitor with an RMS current rating that exceeds half the maximum load current.

The input capacitance value determines the converter input voltage ripple. Select a capacitor value that meets any input voltage ripple requirements.

Estimate the input voltage ripple using equation 6:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (7)$$

Output Capacitor

The output capacitor maintains the DC output voltage. Use ceramic capacitors or POSCAPs. Estimate the output voltage ripple using equation 8:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}\right) \quad (8)$$

Where the module internal inductor is 0.36μH.

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency. The capacitance also dominates the output voltage ripple. For simplification, estimate the output voltage ripple using equation 9:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

The ESR dominates the switching-frequency impedance for POSCAPs, so the output voltage ripple is determined by the ESR value.

For simplification, the output ripple can be approximated using equation 10:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (10)$$

PCB Layout Guidelines

PCB layout plays an important role to achieve stable operation. For optimal performance, follow the guidelines below:

1. Place the input ceramic capacitors as close to the V_{IN} and PGND pins as possible on the same layer of the MPM3695-20. Maximize the V_{IN} and PGND copper plane to minimize the parasitic impedance. Place a $1\mu F$ capacitor close to PIN14.
2. Place V_{IN} vias at least 1cm from the part to minimize noise coupling from input pulsating current.
3. Connect AGND to a solid ground plane through a single point.
4. Place sufficient output GND vias close to the GND pins to minimize both parasitic impedance and thermal resistance.
5. Keep the ISUM trace as short as possible. The ISUM trace should be away from the V_{IN} copper in a multi-phase configuration. Vias should be avoided whenever possible.
6. VOSNS+ and VOSNS- should be routed as differential signals no matter remote sense is used or not. When modules are paralleled, all VOSNS+ of master and slaves should be connected, and all VOSNS- of master and slaves should be connected. Avoid routing VOSNS+/- traces close to input plane and high speed signals.
7. When external resistor divider is used for remote sense, the external resistor divider is recommended to place close to MPM3695-20.

Signal traces should avoid the area directly beneath the SW pad unless a PGND layer is used to provide shielding.

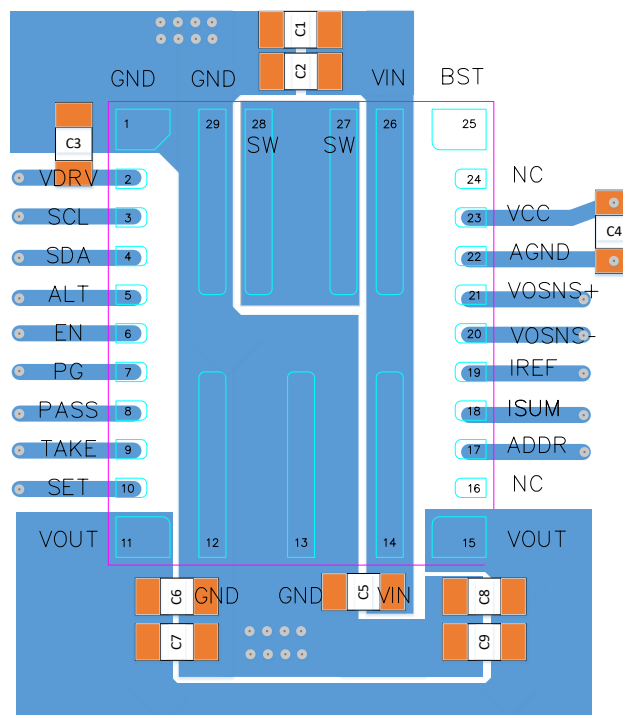


Figure 11: Example Layout - Top Layer

PMBUS INTERFACE

PMBus Serial Interface Description

The power management bus (PMBus) is a two-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are “idle”. Connecting to the line, a master device generates the SCL signal and device address and arranges the communication sequence. It is based on the principles of I²C operation. The MPM3695-20 interface is a PMBus slave, which will support both the standard mode (100kHz) and fast mode (400kHz and 1000KHz). The PMBus interface adds flexibility to the power supply solution.

Device Address

To manage multiple MPM3695-20s through the same PMBus, use the ADDR pin to program the device address for the MPM3695-20s; there is a 8μA current flow out of the ADDR pin. Connect a resistor between the ADDR pin and AGND to set the ADDR voltage. The internal ADC converts the pin voltage to set the PMBus address. A maximum of 18 addresses can be set by the ADDR pin. The MFR_ ADDR_ PMBUS (D3h) register can be used to set the PMBus address digitally.

IREF is a reference current generator amplifier output. This pin is used to select I2C address. Connect a 60.4kΩ resistor when I2C address is selected between 0x30h to 0x3Fh or 180kΩ resistor when I2C address is selected between 0x40h to 0x4Fh. The 60.4kΩ or 180kΩ resistor connected at IREF is required to be 1% or higher accuracy.

After the address is selected, each device must have a unique address during normal operation. For multi-phase operation same address resistor must be used for all phases.

Table 3 shows ADDR resistor values versus the PMBus address.

Table3: PMBus Address vs. ADDR Resistor

R _{ADDR} (kΩ)	Device Address (R _{IREF} = 60.4kΩ)	Device Address (R _{IREF} = 180kΩ)
4.99	30h	40
15	31h	41
24.9	32h	42
34.8	33h	43
45.3	34h	44
54.9	35h	45
64.9	36h	46
75	37h	47
200	3Fh	4F

Start and Stop Conditions

The START/STOP are signaled by the master device, which signifies the beginning and the end of the PMBus data transfer. The START condition is defined as the SDA signal transitioning from HIGH to LOW while the SCL is HIGH. The STOP condition is defined as the SDA signal transitioning from LOW to HIGH while the SCL is HIGH (See Figure 2).

The master then generates the SCL clocks, and transmits the device address and the read/write direction bit R/W on the SDA line. Data is transferred in 8 bit bytes by the SDA line. Each byte of data is followed by an acknowledge bit.

PMBus Update Sequence

The MPM3695-20 requires a start condition, a valid PMBus address, a register address byte, and a data byte for a single data packet update. After receipt of each byte, the MPM3695-20 acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid PMBus address selects the MPM3695-20. The MPM3695-20 performs an update on the falling edge of the LSB byte.

Protocol Usage

All PMBus transactions on the MPM3695-20 are done using defined bus protocols. The following protocols are implemented:

- Send byte with PEC
- Receive byte with PEC
- Write byte with PEC
- Read byte with PEC
- Write word with PEC
- Read word with PEC
- Block read with PEC

PMBus Bus Message Format

In figures a-g below, unshaded cells indicate that the bus host is actively driving the bus; shaded cells indicate that the MPM3695-20 is driving the bus.

S = start condition

Sr = repeated start condition

P = stop condition

R = read bit

$\overline{W}$ = write bit

A = acknowledge bit (0)

$\overline{A}$ = acknowledge bit (1)

“A” represents the ACK (acknowledge) bit. The ACK bit is typically active low (Logic 0) if the transmitted byte is successfully received by a device. However, when the receiving device is the bus master, the acknowledge bit for the last byte read is a Logic 1, indicated by $\overline{A}$.

Packet Error Checking (PEC)

The MPM3695-20 PMBus interface supports the use of the packet error checking (PEC) byte. The PEC byte is transmitted by the MPM3695-20 during a read transaction or sent by the bus host to the MPM3695-20 during a write transaction.

The PEC byte is used by the bus host or the MPM3695-20 to detect errors during a bus transaction, depending on whether the transaction is a read or a write. If the host determines that the PEC byte read during a read transaction is incorrect, it can decide to repeat the read. If the MPM3695-20 determines that the PEC byte sent during a write transaction is incorrect, it ignores the command (does not execute it), and it sets a status flag. Within a group command, the host can choose to send or not send a PEC byte as part of the message to the MPM3695-20.

PMBus Alert Response Address (ARA)

The PMBus alert response address (ARA) is a special address that can be used by the bus host to locate any devices that need to talk to it. A host typically uses a hardware interrupt pin to monitor the PMBus ALERT pins of a number of devices. When the host interrupt occurs, the host issues a message on the bus using the PMBus receive byte or receive byte with PEC protocol.

The special address used by the host is 0x0C. Any devices that have a PMBus alert signal return their own 7-bit address as the seven MSBs of the data byte. The LSB value is not used and can be either 1 or 0. The host reads the device address from the received data byte and proceeds to handle the alert condition.

More than one device may have an active PMBus alert signal and attempt to communicate with the host. In this case, the device with the lowest address dominates the bus and succeeds in transmitting its address to the host. The device that succeeds disables its PMBus alert signal. If the host sees that the PMBus alert signal is still low, it continues to read addresses until all devices that need to talk to it have successfully transmitted their addresses.

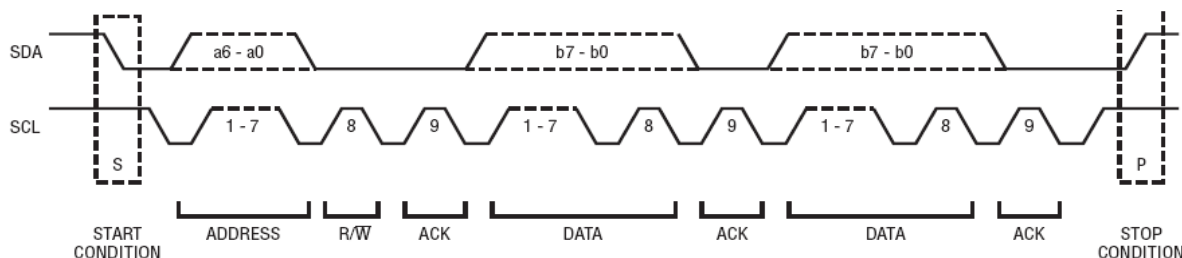
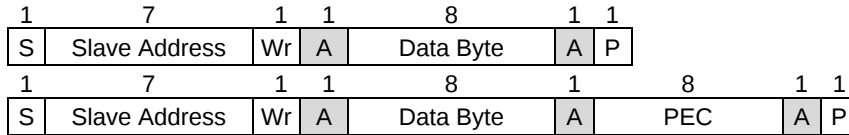
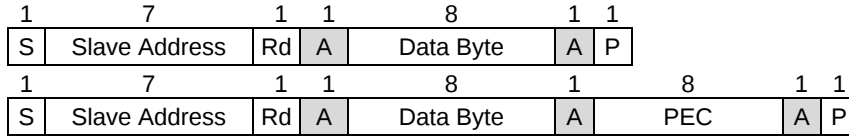


Figure12: Data Transfer over PMBus

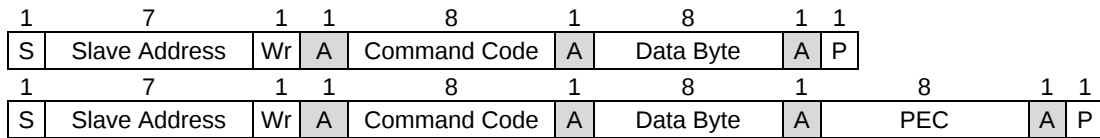
a) Send Byte and Send Byte with PEC



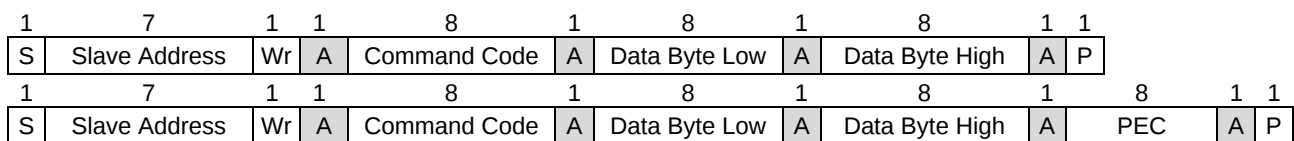
b) Receive Byte and Receive Byte with PEC



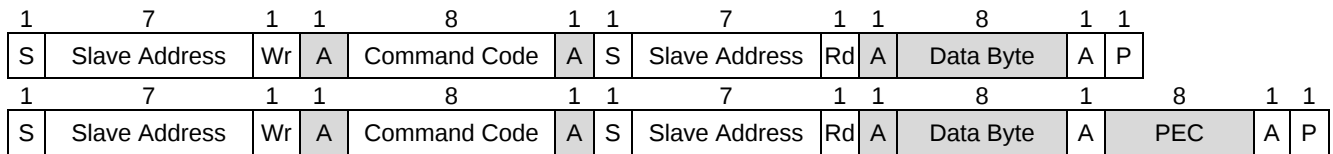
c) Write Byte and Write Byte with PEC



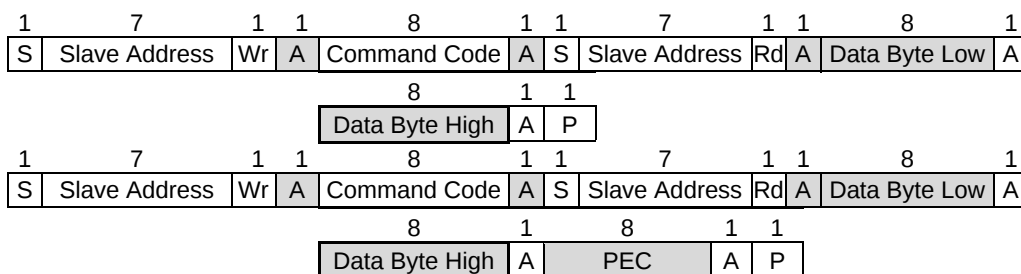
d) Write Word and Write Word with PEC



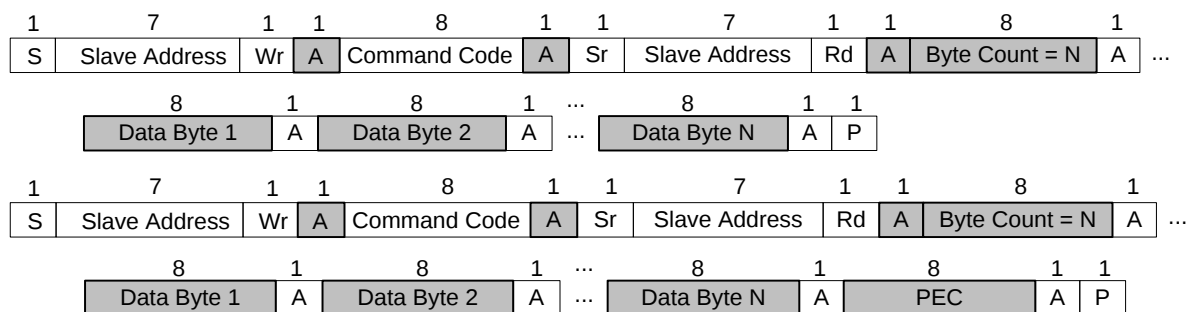
e) Read Byte and Read Byte with PEC



f) Read Word and Read Word with PEC



g) Block Read with PEC



Direct Format Conversion

The MPM3695-20 uses a direct format internally to represent real-world values such as voltage, current, power and temperature.

All numbers with no suffix in this document are decimals unless explicitly designated otherwise.

Numbers in binary format are indicated by the prefix “n'b”, where n is the binary count. For example, 5'b01010 indicates a 5-bit binary data. And the data is 01010.

The suffix “h” indicates a hexadecimal format, which is generally used for the register address number in this document.

The symbol “0x” indicates a hexadecimal format, which is used for the value in the register. For example, 0xA3 is a 1-byte number whose hexadecimal value is A3.

PMBus™ Communication Failure

A data transmission fault occurs when the data is not properly transferred between the devices. There are several data transmission faults as listed below:

- Sending too few data
- Reading too few data
- Sending too many bytes
- Reading too many bytes
- Improperly set read bit in the address byte
- Unsupported command code

PMBus™ Reporting and Status Monitoring

The MPM3695-20 supports real-time monitoring for some operation parameters and status with PMBus™ interface. They are listed on Table4.

Table4: PMBus™ monitored parameters and status Table (-0022 Part)

Parameter/Status	PMBus™
Output voltage	1.25mV/LSB
Output current	62.5mA/LSB
Temperature	1°C/LSB
Input voltage	25mV/LSB
V _{IN} OV	√
V _{IN} UV	√
V _{IN} OV Warn	√
V _{IN} UV Warn	√
V _{OUT} OV	√
V _{OUT} UV	√
Over Temperature (OT)	√
OT Warn	√
V _{OUT} OC	√
V _{OUT} OC Warn	√

MTP Programming

The MPM3695-20 has built-in MTP (Multiple Time Program) cells to store the user configurations. The standard command of 15h (STORE_USER_ALL) is currently not supported by the MPM3695-20. Alternatively, the MTP cells must be programmed through the following commands sequence:

1. Erase: E7h(2000h)
2. Load: E7h(1000h)

Write: E7h(4000h)Add a delay of 1s after each command sequence and to successfully programmed the MTP is required to disable MPM3695-20 through EN pin and adjust VIN > 10V.

The MPS GUI for the MPM3695-20 supports the STORE_USER_ALL command by integrating the above E7h command sequence and naming it 15h (STORE_USER_ALL).

When MTP is being programmed, the VCC voltage may go up as high as 5V. Be cautious if VCC is connected to circuits that can be damaged by such high voltage. The MTP programming usually takes about 300ms. 1μF VCC capacitor is recommended during MTP.

1ms interval is recommended between each command and make sure VIN is larger than 10V during MTP.

REGISTER MAP

Name	Code	Type	Bytes	Default Value (-0022 Part)	MTP
OPERATION	01h	R/W w/PEC	1	80h	YES
ON OFF CONFIG	02h	R/W w/PEC	1	1Eh	YES
CLEAR FAULTS	03h	Send byte w/PEC	0	-	
WRITE_PROTECT	10h	R/W w/PEC	1	00h	YES
STORE_USER_ALL	15h	Send byte w/PEC	0	-	
RESTORE_USER_ALL	16h	Send byte w/PEC	0	-	
CAPABILITY	19h	R w/PEC	1	-	
VOUT_MODE	20h	R w/PEC	1	-	
VOUT_COMMAND	21h	R/W w/PEC	2	0384h (1.8V)	YES
VOUT_MAX	24h	R/W w/PEC	2	0BB8h (6V)	YES
VOUT_SCALE_LOOP	29h	R/W w/PEC	2	014Dh (0.333)	YES
VOUT_MIN	2Bh	R/W w/PEC	2	00FAh (0.5V)	YES
VIN_ON	35h	R/W w/PEC	2	0Ch (3V)	YES
VIN_OFF	36h	R/W w/PEC	2	0Bh (2.75V)	YES
OT_FAULT_LIMIT	4Fh	R/W w/PEC	2	00A0h(160°C)	YES
OT_WARN_LIMIT	51h	R/W w/PEC	2	008Ch (140°C)	YES
VIN_OV_FAULT_LIMIT	55h	R/W w/PEC	2	0024h (18V)	YES
VIN_OV_WARN_LIMIT	57h	R/W w/PEC	2	0022h (17V)	YES
VIN_UV_WARN_LIMIT	58h	R/W w/PEC	2	0001h (0.25V)	YES
TON_DELAY	60h	R/W w/PEC	2	0000h (0ms)	YES
TON_RISE	61h	R/W w/PEC	2	0001h (2ms)	YES
STATUS_BYTE	78h	R w/PEC	1		
STATUS_WORD	79h	R w/PEC	2		
STATUS_VOUT	7Ah	R w/PEC	1		
STATUS_IOUT	7Bh	R w/PEC	1		
STATUS_INPUT	7Ch	R w/PEC	1		
STATUS_TEMPERATURE	7Dh	R w/PEC	1		
STATUS_CML	7Eh	R w/PEC	1		
READ_VIN	88h	R w/PEC	2		
READ_VOUT	8Bh	R w/PEC	2		
READ_IOUT	8Ch	R w/PEC	2		
READ_TEMPERATURE_1	8Dh	R w/PEC	2		
PMBUS_REVISION	98h	R w/PEC	1	33h, ASCII "13" (PMBus 1.3)	
MFR_ID	99h	Block read w/PEC	1(byte)+ 3(data)	4Dh 50h 53h, ASCII "MPS"	
MFR_CTRL_COMP	D0h	R/W w/PEC	1	0Fh	YES
MFR_CTRL_VOUT	D1h	R/W w/PEC	1	40h	YES
MFR_CTRL_OPS	D2h	R/W w/PEC	1	03h	YES
MFR_ADDR_PMBUS	D3h	R/W w/PEC	1	30h	YES
MFR_VOUT_FAULT_LIMIT	D4h	R/W w/PEC	1	03h	YES
MFR_OVP_NOCP_SET	D5h	R/W w/PEC	1	02h	YES
MFR_OT_OC_SET	D6h	R/W w/PEC	1	09h	YES
MFR_OC_PHASE_LIMIT	D7h	R/W w/PEC	1	11h (25.5A)	YES
MFR_PGOOD_ON_OFF	D9h	R/W w/PEC	1	00h	YES
MFR_VOUT_STEP	DAh	R/W w/PEC	1	04h	YES
MFR_CTRL	EAh	R/W w/PEC	1	180h	YES

* For manufactuer WRITE only

COMMANDS

OPERATION (01h)

Format: Unsigned binary

OPERATION is a paged register. The OPERATION command is used to turn the converter output on/off in conjunction with input from the EN pin. It is also used to set the output voltage to the upper or lower MARGIN voltages. The unit stays in the commanded operating mode until a subsequent OPERATION command or a change in the state of the EN pin instructs the converter to change to another mode. This OPERATION command is also used to re-enable the converter after a fault triggered shutdown. Writing an OFF command followed by an ON command will clear all faults. Writing only an ON command after a fault-triggered shutdown will not clear the fault registers.

Bits	Access	Bit Name	Description
7:2	R/W	OPERATION	Selects the operation mode. 6'b 00xx xx: Hi-Z shutdown 6'b 01xx xx: Soft shutdown 6'b 1000 xx: Normal on 6'b 1001 01: Margin low (ignore fault) 6'b 1001 10: Margin low (act on fault) 6'b 1010 01: Margin high (ignore fault) 6'b 1010 10: Margin high (act on fault) "x" means not applicable.
1:0	R	RESERVED	RESERVED

ON_OFF_CONFIG (02h)

Format: Unsigned binary

The ON_OFF_CONFIG command configures the combination of the EN pin input and the PMBus commands needed to turn the converter on and off. This includes how the converter responds when input voltage is applied.

Bits	Access	Bit Name	Description
7:5	R	RESERVED	RESERVED
4	R/W	PON	1'b0: Converter powers up any time the input voltage is present regardless of state of the EN pin 1'b1: Converter does not power up until commanded by the EN pin and OPERATION command
3	R/W	OP	1'b0: Converter ignores the "on" bit in the OPERATION command from the PMBus 1'b1: Converter responds the "on" bit in the OPERATION command from the PMBus
2	R/W	EN	1'b0: Converter ignores the EN pin (on/off controlled only by the OPERATION command). 1'b1: Converter requires the EN pin to be asserted to power up. Depending on the bit[3] op bit, the OPERATION command may also be required to instruct the converter to power up.
1	R/W	POL	This function is disabled. 1'b0: Active low (Pull EN pin low to start the converter) 1'b1: Active high (Pull EN pin high to start the converter)
0	R	DLY	RESERVED

CLEAR_FAULTS (03h)

The CLEAR_FAULTS command is used to reset all stored warning and fault flags. If a fault or warning condition still exists when the CLEAR_FAULTS command is issued, the ALT# signal may not be cleared or will be re-asserted almost immediately. Issuing a CLEAR_FAULTS command will not cause the converter to restart in the event of a fault turn-off. It must be done by issuing an OPERATION command after the fault condition is cleared. This command uses the PMBus to send byte protocol.

WRITE_PROTECT (10h)

The WRITE_PROTECT command is used to control writing to the converter. The intent of this command is to provide protection against accident changes. It's not intended to provide protection against deliberate or malicious changes to the converter's configuration or operation.

All the supported commands may have their parameters read, regardless of the WRITE_PROTECT settings.

Bits	Access	Bit Name	Description
7:5	R/W	WRITE PROTECT	3'b 000: Enable writes to all commands. 3'b 001: Disable all writes except to the WRITE_PROTECT, OPERATION, PAGE, ON_OFF_CONFIG and VOUT_COMMAND commands. 3'b 010: Disable all writes except to the WRITE_PROTECT, OPERATION and PAGE commands. 3'b 100: Disable all writes except to the WRITE_PROTECT command.
4:0	R	RESERVED	RESERVED

STORE_USER_ALL (15h)

Write all the data from the registers to the internal MTPs. This process will operate when the MPM3695-20 receives a STORE_USER_ALL command from the PMBus interface. Currently the MPM3695-20 doesn't support the standard 15h command. However, it can accept a 15h command from the MPS GUI for the MPM3695-20. See the "MTP Programming" section for additional details. The following registers can be stored using STORE_USER_ALL:

OPERATION (01h)	VIN_UV_WARN_LIMIT (58h)
ON_OFF_CONFIG (02h)	TON_DELAY (60h)
WRITE_PROTECT (10h)	TON_RISE (61h)
VOUT_COMMAND (21h)	MFR_CTRL_COMP (D0h)
VOUT_MAX (24h)	MFR_CTRL_VOUT (D1h)
VOUT_MARGIN_HIGH (25h)	MFR_CTRL_OPS (D2h)
VOUT_MARGIN_LOW (26h)	MFR_ADDR_PMBUS (D3h)
VOUT_SCALE_LOOP (29h)	MFR_VOUT_FAULT_LIMIT (D4h)
VOUT_MIN (2Bh)	MFR_OVP_NOCP_SET (D5h)
VIN_ON (35h)	MFR_OT_OC_SET (D6h)
VIN_OFF (36h)	MFR_OC_PHASE_LIMIT (D7h)
OT_FAULT_LIMIT (4Fh)	MFR_PGOOD_ON_OFF (D9h)
OT_WARN_LIMIT (51h)	MFR_VOUT_STEP (DAh)
VIN_OV_FAULT_LIMIT (55h)	MFR_CTRL (EAh)
VIN_OV_WARN_LIMIT (57h)	

RESTORE_USER_ALL (16h)

The RESTORE_USER_ALL command instructs the MPM3695-20 to copy all content of the MTP values to the matching locations in the registers. The values in the registers are overwritten by the value retrieved from the MTP. Any items in the MTPs that do not have matching locations in the operating memory are ignored.

The RESTORE_USER_ALL command can be used while the MPM3695-20 is operating.

Please Note: While the RESTORE_USER_ALL command can be used, the MPM3695-20 may be

unresponsive during the copy operation with unpredictable, undesirable, or even catastrophic results.

This command is write only.

CAPABILITY (19h)

Format: Unsigned binary

The CAPABILITY command returns information about the PMBus functions supported by the MPM3695-20. This command is read with the PMBus read byte protocol.

Bits	Access	Bit Name	Description
7	R	PEC	1'b1: PEC supported
6:5	R	Maximum bus speed	2'b 00: Maximum supported bus speed is 100kHz 2'b 01: Maximum supported bus speed is 1MHz 2'b 10: Maximum supported bus speed is 400kHz 2'b 11: Reserved
4:0	R	RESERVED	Reserved.

VOUT_MODE (20h)

The VOUT_MODE command is used to command and read the output voltage. The 3 most significant bits are used to determine the data format (only a direct format is supported by the MPM3695-20), and the remaining 5 bits represent the exponent used in the output voltage read/write commands

VOUT_COMMAND (21h)

Format: Direct

The VOUT_COMMAND sets the output voltage of the MPM3695-20. The VOUT_COMMAND and the VOUT_SCALE_LOOP together determine the feedback reference voltage: $VOUT_COMMAND * VOUT_SCALE_LOOP$.

Please refer to the “Output Voltage Setting” section to program the output voltage.

Bits	Access	Bit Name	Description
15:12	R	RESERVED	RESERVED
11:0	R/W	VOUT_COMMAND	12'b: 2mV/LSB

The value is unsigned and 1LSB = 2mV. An example of a returned **VOUT_COMMAND** value and conversion to the real-world value is 384h=1.8V.

VOUT_MAX (24h)

Format: Direct

The VOUT_MAX command sets an upper limit on the output voltage the converter can command regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level rather than to be the primary output over-voltage protection.

Bits	Access	Bit Name	Description
15:12	R	RESERVED	RESERVED
11:0	R/W	VOUT_MAX	12'b: 2mV/LSB

If an attempt is made to program the output voltage higher than the limit set by this command, the device shall respond as follows:

- The commanded output voltage shall be set to VOUT_MAX,

- The V_{OUT} bit shall be set in the STATUS_WORD
- The VOUT_MAX_MIN warning bit shall be set in the STATUS_VOUT register
- The device shall notify the host

The value is unsigned and 1LSB=2mV. The minimum value of VOUT_MAX is 0V and the maximum value of VOUT_MAX is 6V. An example of a returned **VOUT_MAX** value and conversion to the real-world value is 3E8h=2V.

VOUT_MARGIN_HIGH (25h)

Format: Direct

Bits	Access	Bit Name	Description
15:12	R	RESERVED	RESERVED
11:0	R/W	VOUT_MARGIN_HIGH	12'b: 2mV/LSB

The value is unsigned and 1LSB = 2mV. The minimum value of VOUT_MARGIN_HIGH is 0.5V while the maximum value is 5.376V. An example of a returned VOUT_MARGIN_HIGH value and conversion to the real-world value is 9C4h=5V.

VOUT_MARGIN_LOW (26h)

Format: Direct

Bits	Access	Bit Name	Description
15:12	R	RESERVED	RESERVED
11:0	R/W	VOUT_MARGIN_LOW	12'b: 2mV/LSB

The value is unsigned and 1LSB = 2mV. The minimum value of VOUT_MARGIN_LOW is 0.5V while the maximum value is 5.376V. An example of a returned VOUT_MARGIN_LOW value and conversion to the real-world value is 2EEh=1.5V.

VOUT_SCALE_LOOP (29h)

Format: Direct

The VOUT_SCALE_LOOP sets the feedback resistor divider ratio. It equals V_{FB}/V_{OUT} . Regardless of the external or internal feedback resistor divider used, the VOUT_SCALE_LOOP should match the actual feedback resistor divider used.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	RESERVED
9:0	R/W	VOUT_SCALE_LOOP	10'b: 0.001/LSB

The value is unsigned and 1LSB = 0.001. An example of a returned **VOUT_SCALE_LOOP** value, when a voltage divider is used, for $V_{out} = 1.8V$ and the resistor divider is set with a top resistor value of $R_1 = 2k\Omega$ and a bottom resistor value of $R_2 = 1k\Omega$, the conversion to the real-world value is 14Dh=0.333

$$Ratio = VOUT_SCALE_LOOP = \frac{R_2}{R_1 + R_2} = 0.333$$

VOUT_MIN (2Bh)

Format: Direct

The VOUT_MIN command sets a lower limit on the output voltage the converter can command regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level rather than to be the primary output under-voltage protection.

Bits	Access	Bit Name	Description
15:12	R	RESERVED	RESERVED

11:0	R/W	VOUT_MIN	12'b: 2mV/LSB
------	-----	----------	---------------

If an attempt is made to program the output voltage lower than the limit set by this command, the device shall respond as follows:

- The commanded output voltage shall be set to VOUT_MIN
- The V_{OUT} bit shall be set in the STATUS_WORD
- The VOUT_MAX_MIN warning bit shall be set in the STATUS_VOUT register
- The device shall notify the host

The minimum value of VOUT_MIN is 0.5V while the maximum value is 8.19V. The value is unsigned and 1LSB=2mV. An example of a returned VOUT_MIN value and conversion to the real-world value is 1F4h=1V.

VIN_ON (35h)

Format: Direct

The VIN_ON command sets the value of the input voltage, in Volts, at which the converter should be turned on if all other required power-up conditions are met. The VIN_ON value should always be set higher than the VIN_OFF value, with enough margin, so that there will be no bouncing between VIN_ON and VIN_OFF during power conversion.

Bits	Access	Bit Name	Description
15:6	R	RESERVED	RESERVED
5:0	R/W	VIN_ON	6'b: 250mV/LSB

The value is unsigned and 1LSB=250mV. The minimum value of VIN_ON is 3V and the maximum value is 15V. An example of a returned VIN_ON value and conversion to the real-world value is 10h=4V.

VIN_OFF (36h)

Format: Direct

The VIN_OFF command sets the value of the input voltage, in Volts, at which the converter, once operation has started, should be turned off. The VIN_OFF value can be set between 2.75V and 14.75V with a 0.25V increment. The VIN_OFF value should be always set lower than VIN_ON value, with enough margin, so that there will be no bouncing between VIN_OFF and VIN_ON during power conversion.

Bits	Access	Bit Name	Description
15:6	R	RESERVED	RESERVED
5:0	R/W	VIN_OFF	6'b: 250mV/LSB

The value is unsigned and 1 LSB=250mV. The minimum value of VIN_OFF is 2.75V and the maximum value is 14.75V. An example of a returned VIN_OFF value and conversion to the real-world value is 10h=4V.

OT_FAULT_LIMIT (4Fh)

Format: Direct

The OT_FAULT_LIMIT is used to configure or read the threshold for the over-temperature fault detection. If the measured temperature exceeds this value, an over-temperature fault will be triggered. The way the MPM3695-20 operates after OTP depends on the MFR_OT_OC_SET (D6h) register; OT fault flags are set in the STATUS_BYTE(78h), STATUS_WORD(79h) respectively, and the ALT# signal is asserted. After the measured temperature falls below the value in this register, the converter will be turned back on with the OPERATION command when the part works in latch off mode. The minimum temperature fault detection time should be less than 20ms. The temperature range is 0 °C to 255°C.

If an OT fault occurs when the temperature rises above this register value, the part will auto-retry when the temperature drops below 20°C (set by register D6h) than this register value when the part works on retry mode.

Bits	Access	Bit Name	Description
15:8	R	RESERVED	RESERVED
7:0	R/W	OT_FAULT_LIMIT	8'b: 1°C /LSB

The value is unsigned and 1LSB=1°C.

The OT_FAULT_LIMIT setting value should be lower than 160°C. If the OT_FAULT_LIMIT value is set higher than 160°C, the register value will be neglected, and the MPM3695-20 will enter thermal shutdown when the junction temperature reaches 160°C.

The table below shows the relationship between the direct value and the real word value.

Direct Value	Real World Value / °C
0000 0000	0
0000 0001	1
1111 1111	+255

OT_WARN_LIMIT (51h)

Format: Direct

The OT_WARN_LIMIT is used to configure or read the threshold for the over-temperature warning detection. If the sense temperature exceeds this value, an over-temperature warning is triggered, the OT warn flags are set in the STATUS_BYTE(78h), STATUS_WORD(79h) respectively, and the ALT# signal is asserted. The minimum temperature warning detection time should be less than 20ms.

Bits	Access	Bit Name	Description
15:8	R	RESERVED	RESERVED
7:0	R/W	OT_WARN_LIMIT	8'b: 1°C /LSB

The value is unsigned and 1LSB=1°C. The minimum value of OT_WARN_LIMIT is 0°C. The OT_WARN_LIMIT setting value should be lower than 160°C. The relationship between the direct value and the real word value is the same with OT_FAULT_LIMIT.

VIN_OV_FAULT_LIMIT (55h)

Format: Direct

The VIN_OV_FAULT_LIMIT command is used to configure or read the threshold for the input over-voltage fault detection. If the measured value of V_{IN} rises above the value in this register, the VIN OV fault flags are set in the respective registers. The power stage of the MPM3695-20 will be disabled. When VIN drops below the VIN_OV_FAULT_LIMIT, the MPM3695-20 will be re-enabled.

Bits	Access	Bit Name	Description
15:6	R	RESERVED	RESERVED
5:0	R/W	VIN_OV_FAULT_LIMIT	6'b: 500mV/LSB

The value is unsigned and 1LSB=500mV. The minimum value of VIN_OV_FAULT_LIMIT is 0V. The VIN_OV_FAULT_LIMIT setting value should not be higher than 18V. An example of a returned VIN_OV_FAULT_LIMIT value and conversion to the real-world value is 1Eh=15V.

VIN_OV_WARN_LIMIT (57h)

Format: Direct

The VIN_OV_WARN_LIMIT command is used to configure or read the threshold for the input over-voltage warning detection. If the measured value of V_{IN} rises above the value in this register, VIN OV warning flags are set in the respective registers, and the ALT# signal is asserted.

Bits	Access	Bit Name	Description
15:6	R	RESERVED	RESERVED
5:0	R/W	VIN_OV_WARN_LIMIT	6'b: 500mV/LSB

The value is unsigned and 1LSB=500mV. The minimum value of VIN_OV_WARN_LIMIT is 0V.

The VIN_OV_WARN_LIMIT setting value should not be higher than 18V. An example of a returned VIN_OV_WARN_LIMIT value and conversion to the real-world value is

20h=16V.

VIN_UV_WARN_LIMIT (58h)

Format: Direct

The VIN_UV_WARN_LIMIT command is used to configure or read the threshold for the input under-voltage fault detection. If the measured value of V_{IN} falls below the value in this register, VIN UV warning flags are set in the respective registers, and the ALT# signal is asserted.

Bits	Access	Bit Name	Description
15:6	R	RESERVED	RESERVED
5:0	R/W	VIN_UV_WARN_LIMIT	6'b: 250mV/LSB

The value is unsigned and 1LSB=250mV. The minimum value of VIN_UV_WARN_LIMIT is 0V. The VIN_UV_WARN_LIMIT setting value should not be higher than 3.3V. An example of a returned VIN_UV_WARN_LIMIT value and conversion to the real-world value is 08h=2V.

TON_DELAY (60h)

Format: Direct

The TON_DELAY command sets the time, in ms, from when a start condition is received (as programmed by the ON_OFF_CONFIG command) until the output voltage starts to rise.

Bits	Access	Bit Name	Description
15:8	R	RESERVED	RESERVED

7:0	R/W	TON_DELAY	8'b: 4ms/LSB
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The value is unsigned and 1LSB=4ms. The minimum value of TON_DELAY is 0ms and the maximum value is 60h=FFh (1020ms). An example of a returned **TON_DELAY** value and conversion to the real-world value is 0Ah=40ms.

TON_RISE (61h)

Format: Direct

The TON_RISE command sets the soft-start time, in ms, from when the output starts to rise until the voltage has reached the regulation point.

Bits	Access	Bit Name	Description
15:3	R	RESERVED	RESERVED
2:0	R/W	TON_RISE	3'b 000: 1ms 3'b 001: 2ms 3'b 010: 4ms 3'b 011: 8ms 3'b 100 and up: 16ms

STATUS BYTE (78h)

The STATUS_BYTE command returns the value of a number of flags indicating the state of the MPM3695-20. Access to this command should use the read byte protocol. To clear bits in this register, the underlying fault should be removed and a CLEAR_FAULTS command issued.

Bits	Name	Behavior	Default Set	Description
7	Reserved	N/A	0	Always read as 0
6	OFF	R Live	0	1'b 0 Part enabled 1'b 1 Part disabled, this can be triggered from: VIN UV/OV fault or the operation command to turn off
5	VOUT_OV	R Latched	0	1'b 0 No output over-voltage fault has occurred. 1'b 1 An output over-voltage fault has occurred.
4	IOUT_OC_FAULT	R Latched	0	1'b 0 No Over-current fault detected 1'b 1 Over-current fault detected
3	VIN_UV	R Latched	0	1'b 0 No VIN_UV fault detected 1'b 1 VIN_UV fault detected
2	OT_FAULT_WARN	R Latched	0	1'b 0 No over-temperature warning or fault detected 1'b 1 Over-temperature warning or fault detected
1	CUMM_ERROR	R Latched	0	1'b 0 No communication error detected 1'b 1 Communication error detected
0	NONE_OF_THE_ABOVE	R Latched	0	1'b 0 No other fault or warning 1'b 1 Fault or warning not listed in bits [7:1] has occurred.

STATUS WORD (79h)

The STATUS_WORD returns the value of a number of flags indicating the state of the MPM3695-20. To clear bits in this register, the underlying fault should be removed and a CLEAR_FAULTS command issued. Any bits in 79h triggered will trigger physical ALT pin.

Bits	Name	Behavior	Default Set	Description
15	VOUT_STATUS	R Latched	0	1'b 0 No output fault or warning 1'b 1 Output fault or warning
14	IOUT_STATUS	R Latched	0	1'b 0 No IOUT fault 1'b 1 IOUT fault

13	VIN_STATUS	R Latched	0	1'b 0 No VIN fault 1'b 1 VIN fault, at the period when V _{IN} starts up, the initial flag is 1 before the V _{IN} passes the UVLO threshold. It is then cleared once the V _{IN} passes UVLO
12	MFR_STATUS	R	0	Always read as 0
11	POWER_GOOD#	R Live	0	1'b 0 Power good signal is asserted 1'b 1 Power good signal is not asserted
10	Reserved	R	0	Always read as 0
9	Reserved	R	0	Always read as 0
8	UNKNOWN	R Latched	0	1'b 0 No other fault has occurred 1'b 1 A fault type not specified in bits [15:1] of the STATUS_WORD has been detected.
Low Byte	STATUS_BYTE	R		The low 8 bits are defined in register 78h

STATUS_VOUT (7Ah)

The STATUS_VOUT command returns one data byte with contents as follows:

Bits	Name	Behavior	Default Set	Description
7	VOUT_OV_FAULT	R Latched	0	1'b 0 No output OV fault 1'b 1 Output OV fault
6	Reserved	R	0	Always read as 0
5	Reserved	R	0	Always read as 0
4	VOUT_UV_FAULT	R Latched	0	1'b 0 No output UV fault 1'b 1 output UV fault
3	VOUT_MAX_MIN	R Latched	0	1'b 0 No VOUT_MAX, VOUT_MIN warning 1'b 1 An attempt has been made to set the output voltage to a value higher than allowed by the VOUT_MAX command or lower than the limit allowed by the VOUT_MIN command.
2	Reserved	R	0	Always read as 0
1	Reserved	R	0	Always read as 0
0	UNKNOWN	R Latched	0	1'b 0 No other fault has occurred 1'b 1 A fault type not specified in bits [15:1] of the STATUS_WORD has been detected.

STATUS_IOUT (7Bh)

Format: Unsigned binary

Bits	Name	Behavior	Default Set	Description
7	IOUT_OC	R Latched	0	1'b 0 No I _{OUT} OC fault 1'b 1 I _{OUT} OC fault
6	IOUT_OC & VOUT_UV	R Latched	0	1'b 0 No I _{OUT} OC & V _{OUT} UV fault 1'b 1 I _{OUT} OC & V _{OUT} UV fault
5	IOUT_OC_WARNING	R Latched	0	1'b 0 No I _{OUT} OC warning 1'b 1 I _{OUT} OC warning
4:0	Reserved	R	0	Reserved

STATUS_INPUT (7Ch)

The STATUS_INPUT returns the value of flags indicating the input voltage status of the MPM3695-20. To clear bits in this register, the underlying fault or warning should be removed and a CLEAR_FAULTS command issued.

Bits	Name	Behavior	Default Set	Description
7	VIN_OV_FAULT	R Latched	0	1'b 0 means no over-voltage detected on the OV pin 1'b 1 means over-voltage detected on the OV pin
6	VIN_OV_WARN	R Latched	0	1'b 0 means over-voltage condition on V _{IN} has not occurred 1'b 1 means over-voltage condition on V _{IN} has occurred
5	VIN_UV_WARN	R Latched	0	1'b 0 means input voltage is higher than VIN_UV_WARN_LIMIT(58h) 1'b 1 means input voltage is lower than VIN_UV_WARN_LIMIT(58h)
4	VIN_UV_Fault	R Latched	0	1'b 0 means input voltage is higher than VIN_OFF(36h) 1'b 1 means input voltage is lower than VIN_OFF(36h)
3:0	Reserved	R	0	Always read as 0000

STATUS_TEMPERATURE (7Dh)

The STATUS_TEMPERATURE returns the value of flags indicating the V_{IN} over-voltage or under-voltage of the MPM3695-20. To clear bits in this register, the underlying fault should be removed and a CLEAR_FAULTS command issued.

Bits	Name	Behavior	Default Set	Description
7	OT_FAULT	R Latched	0	1'b 0 no over-temperature fault has occurred 1'b 1 over-temperature fault has occurred
6	OT_WARNING	R Latched	0	1'b 0 no over-temperature warning has occurred 1'b 1 over-temperature warning has occurred
5:0	Reserved	R	0	Always read as 0

STATUS_CML (7Eh)

Reading non-existing register is triggering 7Eh[7], and read writing only or writing read only registers is triggering 7Eh[6]. If 7Eh[7,6,1] is triggered, 78h[1] will trigger.

Bits	Name	Behavior	Default Set	Description
7	INVALID/UNSUPPORTED COMMAND	R Latched	0	1'b 0 No invalid / unsupported command 1'b 1 Invalid/unsupported command
6	INVALID/UNSUPPORTED DATA	R Latched	0	1'b 0 No invalid / unsupported data 1'b 1 Invalid / unsupported data
5	Reserved	R	0	Always read as 0
4	MEMORY_FAULT	R Latched	0	1'b 0 No memory fault 1'b 1 Memory fault
3	Reserved	R	0	Always read as 0
2	Reserved	R	0	Always read as 0
1	OTHER_FAULT	R Latched	0	1'b 0 No other fault 1'b 1 Other fault
0	MEMORY_BUSY	R Latched	0	1'b 0 No memory busy 1'b 1 Memory busy

READ_VIN (88h)**Format:** Direct

The READ_VIN command returns the 10-bit measured value of the input voltage.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	RESERVED
9:0	R	READ_VIN	10'b: 25mV/LSB

READ_VOUT (8Bh)**Format:** Direct

The READ_VOUT command returns the 13-bit measured value of the output voltage.

Bits	Access	Bit Name	Description
15:13	R	RESERVED	RESERVED
12:0	R	READ_VOUT	13'b: 1.25mV/LSB

READ_IOUT (8Ch)**Format:** Direct

The READ_IOUT command returns the 14-bit measured value of the output current.

Bits	Access	Bit Name	Description
15:14	R	RESERVED	RESERVED
13:0	R	READ_IOUT	14'b: 62.5mA/LSB

For multi-phase operation the master device returns total current for all phases through READ_IOUT.

READ_TEMPERATURE_1 (8Dh)**Format:** Direct

The READ_TEMPERATURE_1 command returns the internal sensed temperature. This value is also used internally for the over-temperature fault and warning detection. This data has a range of -40°C to +215°C.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	RESERVED
9	R/W	SIGN	1'b 0 Positive sign 1'b 1 Negative sign
8:0	R	READ_TEMPERATURE	9'b 1 °C/LSB

READ_TEMPERATURE is a 2-byte, twos complement integer. The bit[9] is the sign bit.

The table below shows the relationship between the direct value and the real word value.

Sign	Direct Value	Real World Value / °C
0	0 0000 0000	0
0	0 0000 0001	1
0	1 1111 1111	+511
1	0 0000 0001	-511
1	1 1111 1111	-1

MFR_CTRL_COMP (D0h)

The MFR_CTRL_COMP command is used to adjust the loop compensation of the MPM3695-20. The control loop parameters can best be understood by reference to Figure 13.

Bits	Access	Bit Name	Default	Description	
7:5	R/W	Reserved	4'b 0000	NA	
4	R/W	Cff	1'b 0	1'b 0: 20pF. 1'b 1: 50pF.	
3:1	R/W	RAMP	3'b 111	EAh[3]=0 (single phase)	EAh[3]=1 (Multi-phase)
				3'b 000: 5.6mV RAMP	3'b 000: 8.6mV RAMP
				3'b 001: 9.8mV RAMP	3'b 001: 15mV RAMP
				3'b 010: 18mV RAMP	3'b 010: 27mV RAMP
				3'b 011: 30mV RAMP	3'b 011: 45mV RAMP
				3'b 100: 8.5mV RAMP	3'b 100: 13mV RAMP
				3'b 101: 15.1mV RAMP	3'b 101: 23mV RAMP
				3'b 110: 27mV RAMP	3'b 110: 41mV RAMP
				3'b 111: 44mV RAMP	3'b 111: 68mV RAMP
0	R/W	Slave Fault Detection	1'b 1	1'b 0:Slave-phase fault detection is enabled; 1'b 1:Slave-phase fault detection is disabled.	

Bit[4] (Cff): Set the feed-forward capacitance when the internal feedback resistor divider is selected.

Bit[3:1]: Set the internal RAMP compensation to stabilize the loop. Cautions should be made that the actual RAMP amplitude is related to the selection of register bit of EAh[3]. Refer to register EAh description for details.

Bit[0]: Enable or disable the slave fault detection function through the PG pin.

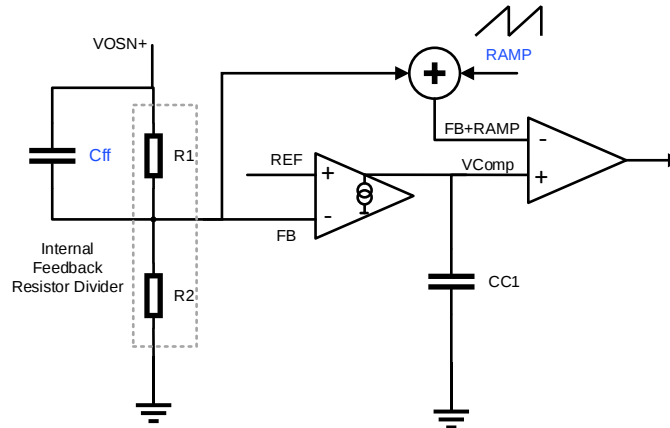


Figure 13 MPM3695-20 Control Loop Programmable Parameters

MFR_CTRL_VOUT (D1h)

The MFR_CTRL_VOUT command is used to adjust the output voltage of the MPM3695-20.

Bits	Access	Bit Name	Default	Description
7	R/W	Reserved	1'b 0	

6	R/W	V _{OUT} discharge	1'b 1	1'b 1: Output voltage discharge at EN low. 1'b 0: No active output voltage discharge.
5:2	R/W	PG delay	4'b 0000	4'b 0000: 2ms 4'b 0001: 3ms 4'b 1110: 16ms 4'b 1111: 1ms
1:0	R/W	VO_RANGE	2'b 00	2'b 00: External voltage divider, V _{ref} =0.5-0.672V 2'b 01: Internal voltage divider: V _{ref} /V _{OUT} =1:2, V _{OUT} =0.4~1.344V 2'b 10: Internal voltage divider: V _{ref} /V _{OUT} =1:4, V _{OUT} =0.7~2.688V 2'b 11: Internal voltage divider: V _{ref} /V _{OUT} =1:8, V _{OUT} =1.3~5.376V

MFR_CTRL_OPS (D2h)

The MFR_CTRL_OPS command is used to set the switching frequency and light-load operation mode of the MPM3695-20.

Bits	Access	Bit Name	Default	Description
7:3	R	Reserved	5'b 00000	Reserved
2:1	R/W	SWITCHING_FREQUENCY	2'b 01	2'b 00: Set the fs to 400KHz. 2'b 01: Set the fs to 600KHz. 2'b 10: Set the fs to 800KHz. 2'b 11: Set the fs to 1000KHz.
0	R/W	SKIP_CCM (SYNC)	1'b 1	1'b 0: Pulse-skip mode at light load. 1'b 1: Forced CCM at light load.

MFR_ADDR_PMBUS (D3h)

Format: Direct

Bits	Access	Bit Name	Default	Description
7	R/W	ENABLE BIT	1'b 0	1'b 1: The address is decided by MFR_ADDR_PMBUS [6:0] 1'b 0: The address is decided by ADDR pin.
6:0	R/W	ADDRESS	7'b 0110000	Address value if MFR_ADDR_PMBUS [7] was set to 1

MFR_VOUT_FAULT_LIMIT (D4h)

This MFR_VOUT_FAULT_LIMIT command sets the thresholds for OVP.

Bits	Access	Bit Name	Default	Description
7:4	R	Reserved	4'b 0000	Reserved
3:2	R/W	OV_EXIT_TH	2'b 01	2'b 00: 10%*V _{REF} 2'b 01: 50%*V _{REF} 2'b 10: 80%*V _{REF} 2'b 11: 102.5%*V _{REF}
1:0	R/W	OV_ENTER_TH	2'b 01	2'b 00: 115%*V _{REF} 2'b 01: 120%*V _{REF} 2'b 10: 125%*V _{REF} 2'b 11: 130%*V _{REF}

The thresholds of OVP are relative values of the reference voltage.

MFR_OVP_NOCP_SET (D5h)

The MFR_OVP_NOCP_SET command sets the responses of the output voltage OVP.

Bits	Access	Bit Name	Default Set	Description
7:4	R	Reserved	4'b 0000	Reserved
3	R/W	DELAY_NOCP	1'b 0	1'b 0: 100ns delay after NOCP 1'b 1: Reserved
2	N/A	Reserved	N/A	Reserved.
1:0	R/W	VOUT_OV_Response	2'b 10	2'b 00: Latch-off with output voltage discharge 2'b 01: Latch-off without output voltage discharge in DCM 2'b 10: HICCUP with output voltage discharge 2'b 11: HICCUP without output voltage discharge in DCM

The bit[1:0] of MFR_VOUT_OVP_NOCP_SET command tells the converter what action to take in response to an output over-voltage fault. The device also does the following:

- Sets the VOUT_OV bit in the STATUS_BYTE
- Sets the V_{OUT} bit in the STATUS_WORD
- Sets the V_{OUT} over-voltage fault bit in the STATUS_VOUT command
- Notifies the host by asserting ALERT pin

There are four OVP response modes. The mode can be chosen through bit[1:0] of MFR_VOUT_OVP_NOCP_SET:

- **Latch-off with output discharge:** Once it hits the OV entry threshold, the LS-FET is ON until it hits NOCP, then it is OFF for a fixed time, and then it is ON again. It operates in this manner until FB drops below the OVP exit threshold set by register D4[3:2], then the LS-FET is off. If FB rises above the OV entry threshold again, the LS-FET is turned on again to discharge the output voltage. However, the converter won't attempt to restart until there is power recycle either in V_{IN}, VCC, or EN.
- **Latch-off without output discharge (only effective in DCM):** Once it hits the OV entry threshold, the LSFET is ON. When the inductor current crosses zero, the converter enters high-z mode (output disabled). The converter stops discharging the output voltage. The converter won't attempt to restart until there is power recycle either in V_{IN}, VCC, or EN.
- **HICCUP with output discharge:** Once it hits the OV entry threshold, the LSFET is ON until it hits NOCP, then it is OFF for a fixed time, and then it is ON again. It operates in this manner until FB drops below the OVP exit threshold set by register D4[3:2], and then the LSFET is OFF. A new SS will be initiated.
- **HICCUP without output discharge:** Once it hits OV, the LSFET is ON until it hits NOCP, then it initiates a new SS.

MFR_OT_OC_SET (D6h)

This command sets the responses of the OCP and the responses and hysteresis of the OTP. It's a 1 byte command.

Bits	Access	Bit Name	Default Set	Description
7:4	R	Reserved	4'b 0000	Reserved
3	R/W	OC_response	1'b 1	1'b 0: Latch-off 1'b 1: Retry
2:1	R/W	OT_hyst	2'b 00	2'b 00: 20°C 2'b 01: 25°C 2'b 10: 30°C 2'b 11: 35°C

0	R/W	OT_Response	1'b 0	1'b 0:Latch-off 1'b 1:Retry after the temp drops by the value set by bits [2:1]
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The MFR_OT_OC_SET command tells the converter what kind of action to take in response to an over-temperature fault and a total output over-current fault.

MFR_OC_PHASE_LIMIT (D7h)

The MFR_OC_PHASE_LIMIT command sets the inductor valley current limit of each individual phase. This is a cycle-by-cycle current limit. After 31 consecutive cycles of OC, it triggers OCP. It's a 1 byte command.

Bits	Access	Bit Name	Default Set	Description
7:5	R	Reserved	3'b 000	Reserved
4:0	R/W	OC_limit	5'b 10001	Current limit. 1.5A/LSB;[00000]=0A.

The value is unsigned and 1LSB=1.5A. An example of a returned MFR_OC_PHASE_LIMIT value and conversion to the real-world value is 10h=24A.

MFR_PGOOD_ON_OFF_LIMIT (D9h)

The MFR_PGOOD_ON_OFF_LIMIT command sets the thresholds for PGOOD on and off.

Bits	Access	Bit Name	Default Set	Description
7:4	R	Reserved	4'b 0000	Reserved
3:2	R/W	PG_OFF	2'b 00	2'b 00:69%*V _{REF} 2'b 01:74%*V _{REF} 2'b 10:79%*V _{REF} 2'b 11:84%*V _{REF}
1:0	R/W	PG_ON	2'b 00	2'b 00:90%*V _{REF} 2'b 01:92.5%*V _{REF} 2'b 10:95%*V _{REF} 2'b 11:97.5%*V _{REF}

D9h[3:2] sets the UVP threshold. When FB drops below the PG_OFF level, the MPM3695-20 enters UVP. The response of UVP is the same as in OCP.

Any fault condition will pull PG low.

MFR_VOUT_STEP (DAh)

The MFR_VOUT_STEP command sets the slew rate of the output voltage transition after soft start finishes. It doesn't determine the slew rate of the output voltage during soft start.

Bits	Access	Bit Name	Default Set	Description
7:4	R	Reserved	4'b 0000	Reserved
3:0	R/W	V _{OUT_Step}	4'b 0100	0000 = 20μs/2mV 1LSB = 2.5μs/2mV The max Vout_step is 40μs/2mV when bit[3:0]=4b'1000.if bit[3:0] is larger than 4b'1000,Vout_step is 30μs/2mV.

When the value of DAh is greater than 0x08, the slew rate will keep 30μs/2mV.

MFR_CTRL (EAh)

The bits of the MFR_CTRL are used to enable/disable the functions below:

Bits	Access	Bit Name	Default Set	Description
15:10	R	Reserved	reserved	For manufacturer use only
9	R/W	OSM	1'b 0	1'b 0: Enable OSM (Output Sink Mode). 1'b 1: Disable OSM

8:4	R	Reserved	reserved	For manufacturer use only
3	R/W	Phase_Operation	1'b 0	1'b 0: For single-phase operation 1'b 1: For multi-phase operation
2:0	R	Reserved	reserved	For manufacturer use only

Bit[9] and bit[3] are user accessible for the MFR_CTRL (EAh). The other bits are reserved for manufacturer use only.

Bit[9] osm enables or disables the Output Sink Mode (OSM) function.

Bit[3] phase operation is used to choose single or multi-phase operation. The selection of this bit will affect the actual RAMP amplitude chosen through register D0h[3:1]. See register description of MFR_CTRL_COMP (D0h).

DEFAULT MTP CONFIGURATION

Table 5: 0022 Suffix Code Configuration

Items	Value
Output Voltage Set Method	External divider
V _{OUT}	1.8V
FB Voltage	0.6V
Soft-Start Time	2mS
Individual Valley Current Limit	25.5A
Light-Load Mode	FCCM
Individual Switching Frequency	600kHz
RAMP	44mV
UVLO Rising	3V
UVLO Falling	2.75V
OT Fault Limit	160°C
OT Warning Limit	140°C
VIN_OV_Fault_Limit	18V
Output current read_back resolution	62.5mA/LSB
Phase	Single

Table6: 0022 Suffix Register Value

Suffix Code	Page	Register	Hex Value	Suffix Code	Page	Register	Hex Value
0022	1	01	80	0022	1	60	0
0022	1	02	1E	0022	1	61	1
0022	1	10	0	0022	1	64	0
0022	1	21	384	0022	1	9B	32
0022	1	24	BB8	0022	1	D0	F
0022	1	25	AC0	0022	1	D1	40
0022	1	26	604	0022	1	D2	3
0022	1	29	14F	0022	1	D3	30
0022	1	2B	FA	0022	1	D4	3
0022	1	35	C	0022	1	D5	2
0022	1	36	B	0022	1	D6	9
0022	1	4F	A0	0022	1	D7	11
0022	1	51	8C	0022	1	D8	0
0022	1	55	24	0022	1	D9	0
0022	1	57	22	0022	1	DA	4
0022	1	58	1	0022	1	EA	180

DEFAULT MTP CONFIGURATION

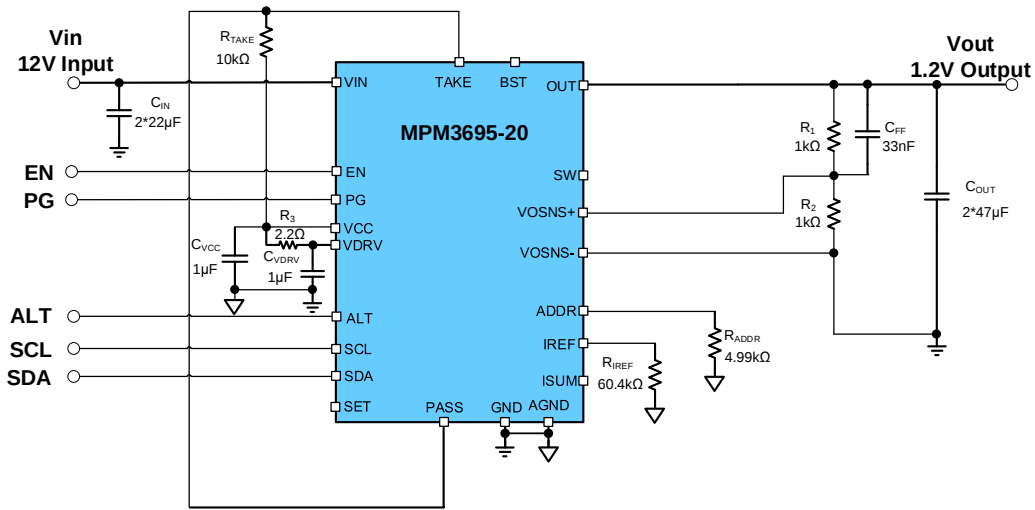
Table7:3333 Suffix Code Configuration

Items	Value
Output Voltage Set Method	External divider
V _{OUT}	3.3V
FB Voltage	0.6V
Soft-Start Time	4mS
Individual Valley Current Limit	30A
Light-Load Mode	FCCM
Individual Switching Frequency	600kHz
RAMP	44mV
UVLO Rising	3V
UVLO Falling	2.75V
OT Fault Limit	160°C
OT Warning Limit	140°C
VIN_OV_Fault_Limit	18V
Output current read_back resolution	62.5mA/LSB
Phase	Multiple

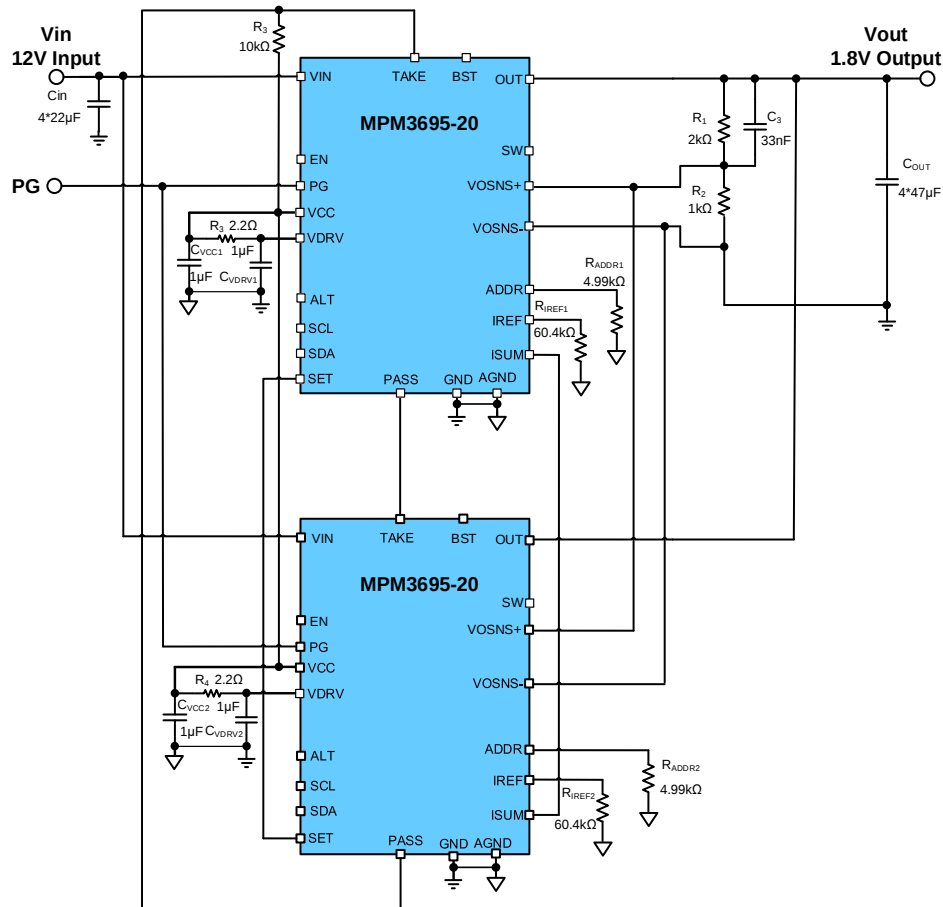
Table 8: 3333 Suffix Register Value

Suffix Code	Page	Register	Hex Value	Suffix Code	Page	Register	Hex Value
3333	1	01	80	3333	1	60	0
3333	1	02	1E	3333	1	61	2
3333	1	10	0	3333	1	64	0
3333	1	21	672	3333	1	9B	32
3333	1	24	BB8	3333	1	D0	F
3333	1	25	6A4	3333	1	D1	40
3333	1	26	640	3333	1	D2	3
3333	1	29	B6	3333	1	D3	30
3333	1	2B	FA	3333	1	D4	3
3333	1	35	C	3333	1	D5	2
3333	1	36	B	3333	1	D6	9
3333	1	4F	A0	3333	1	D7	14
3333	1	51	8C	3333	1	D8	0
3333	1	55	24	3333	1	D9	0
3333	1	57	22	3333	1	DA	4
3333	1	58	1	3333	1	EA	188

TYPICAL APPLICATION CIRCUITS



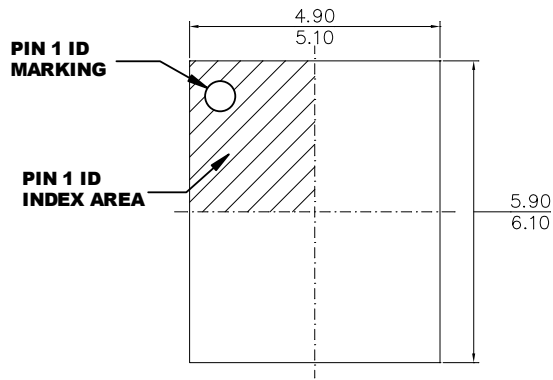
Single Phase Operation



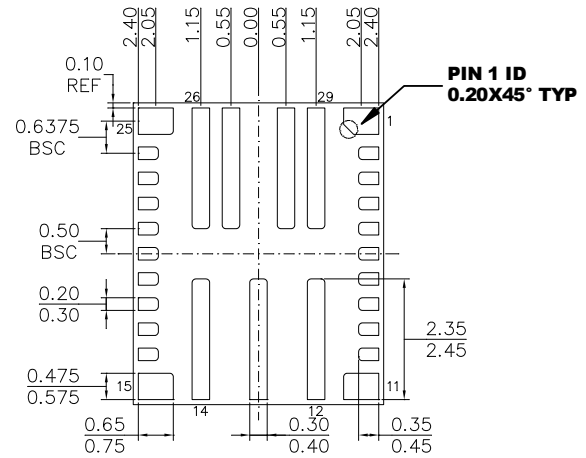
Dual Phase Operation

PACKAGE INFORMATION

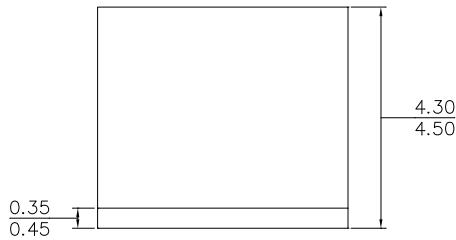
ECLGA-29 (5mmx6mmx4.4mm)



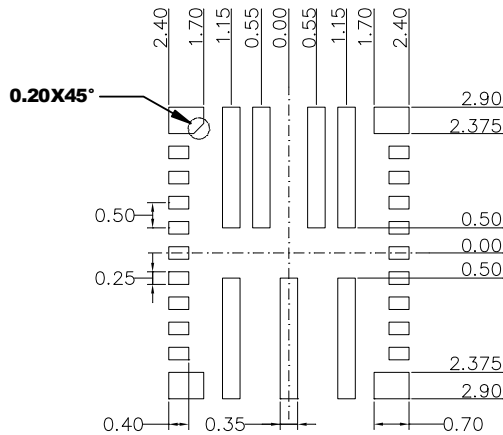
TOP VIEW



BOTTOM VIEW



SIDE VIEW

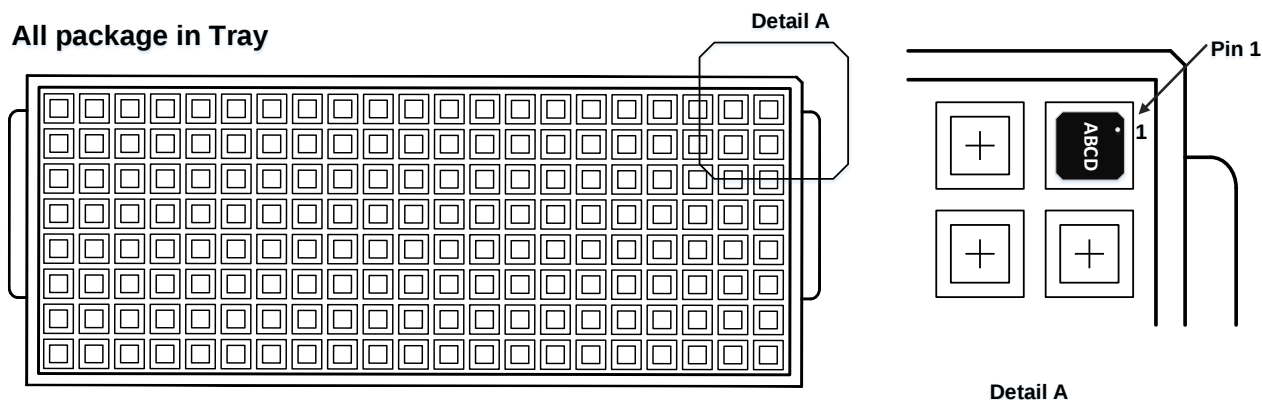


RECOMMENDED LAND PATTERN

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
- 3) JEDEC REFERENCE IS MO-303.
- 4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Note:

This is a schematic diagram of Tray. Different packages correspond to different trays with different length, width and height

Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM3695GPJ-20-xxxx-T	ECLGA-29 (5mmx6mmx4.4mm)	N/A	N/A	360	N/A	N/A	N/A

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/2/2024	Initial Release	-

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