**DESCRIPTION**

The MPM3632S is a synchronous, rectified, step-down, mini-module regulator with built-in power MOSFETs, an inductor, and two capacitors. It offers a compact solution with only input and output capacitors to achieve a 3A continuous output current with excellent load and line regulation over a wide input supply range. The MPM3632S operates in a fixed 2.2MHz switching frequency with constant on-time (COT) control to provide fast load transient response.

Full protection features include output over-voltage protection, over-current protection, and thermal shut down.

The device eliminates design and manufacturing risks while dramatically improving time to market.

The MPM3632S is available in a space-saving EC LGA-10 (3mmx3mmx1.45mm) package.

**FEATURES**

- Wide 4V to 18V Operation Input Range
- Internally Fixed Soft Start Time
- 0.5% Accuracy Output Voltage
- 3A Continuous Output Current
- 2.2MHz Switching Frequency
- Forced CCM Mode
- Power Good Indicator
- Hiccup OCP Protection
- Output Over-Voltage Protection
- Fast Transient Response
- Available in an EC LGA-10 (3mmx3mmx1.45mm) Package

**APPLICATIONS**

- Server Systems
- Medical and Imaging Equipment
- Distributed Power Systems

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**TYPICAL APPLICATION**

![Typical Application Diagram]

**Efficiency vs. Load Current**

\[ V_{OUT} = 3.3V \]

![Efficiency Graph]

- Blue: \( V_{IN}=4V \)
- Gray: \( V_{IN}=12V \)
- Orange: \( V_{IN}=18V \)
**ORDERING INFORMATION**

<table>
<thead>
<tr>
<th>Part Number*</th>
<th>Package</th>
<th>Top Marking</th>
<th>MSL Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPM3632SGPQ</td>
<td>EC LGA-10&lt;br&gt;(3mmx3mmx1.45mm)</td>
<td>See Below</td>
<td>3</td>
</tr>
</tbody>
</table>

* For Tape & Reel, add suffix –Z (e.g. MPM3632SGPQ–Z). For tray, –Z is not required.

**TOP MARKING**

Y: Year code  
W: Week code  
BPE: part number code  
LLL: Lot number

**PACKAGE REFERENCE**

```
TOP VIEW

PG  VCC  AGND

10  9  8

EN  1  7  FB

VIN  2  6  OUT_S

3  4  5

PGND PGND VOUT

EC LGA-10 (3mmx3mmx1.45mm)
```
## PIN FUNCTIONS

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>EN</td>
<td><strong>Enable.</strong> Drive EN high to enable the MPM3632S.</td>
</tr>
<tr>
<td>2</td>
<td>VIN</td>
<td><strong>Supply voltage.</strong> The MPM3632S operates from a 4V to 18V input rail. Requires a ceramic capacitor to decouple the input rail. Connect using a wide PCB trace.</td>
</tr>
<tr>
<td>3, 4</td>
<td>PGND</td>
<td><strong>System ground.</strong> Reference ground of the regulated output voltage. Requires special consideration during PCB layout. Connect to GND with copper traces and vias.</td>
</tr>
<tr>
<td>5</td>
<td>VOUT</td>
<td><strong>Power output pin.</strong></td>
</tr>
<tr>
<td>6</td>
<td>OUT_S</td>
<td><strong>Output voltage sense pin.</strong></td>
</tr>
<tr>
<td>7</td>
<td>FB</td>
<td><strong>Feedback pin.</strong> Set the output voltage with divider resistors.</td>
</tr>
<tr>
<td>8</td>
<td>AGND</td>
<td><strong>Analog ground.</strong></td>
</tr>
<tr>
<td>9</td>
<td>VCC</td>
<td><strong>Internal 3.3V LDO regulator output.</strong> The MPM3632S does not require external connections due to its internal decoupling capacitor.</td>
</tr>
<tr>
<td>10</td>
<td>PG</td>
<td><strong>Power good output.</strong> Open-drain structure. PG switches to an open-drain state when FB is greater than 90%. It switches to low if FB is below 80% of VREF.</td>
</tr>
</tbody>
</table>

## ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IN} )</td>
<td>-0.3V to +20V</td>
</tr>
<tr>
<td>( V_{SW} )</td>
<td>(-0.3V \leq 0.7V \leq +0.7V ) (22V for &lt; 10ns)</td>
</tr>
<tr>
<td>( V_{EN} )</td>
<td>18V</td>
</tr>
<tr>
<td>( V_{OUT} )</td>
<td>6.5V</td>
</tr>
<tr>
<td>( V_{PG} )</td>
<td>5.5V</td>
</tr>
<tr>
<td>All other pins</td>
<td>-0.3V to +4V</td>
</tr>
</tbody>
</table>

Continuous power dissipation (\( T_A = +25^\circ C \)):

\[
P_{D\,(\text{MAX})} = \frac{\left(T_J\,(\text{MAX}) - T_A\right)}{\theta_JA}.
\]

Notes:
1. Exceeding these ratings may damage the device.
2. The maximum allowable power dissipation is a function of the maximum junction temperature \( T_J \), the junction-to-ambient thermal resistance \( \theta_{JA} \), and the ambient temperature \( T_A \). The maximum allowable continuous power dissipation at any ambient temperature is calculated by
   \[
P_{D\,(\text{MAX})} = \frac{T_J\,(\text{MAX}) - T_A}{\theta_{JA}}.
   \]
   Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3. The device is not guaranteed to function outside of its operating conditions.
4. Measured on EVM3632S-PQ-00A, 4-layer PCB.

## Thermal Resistance

<table>
<thead>
<tr>
<th>Package</th>
<th>( \theta_{JA} )</th>
<th>( \theta_{JC} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>EVM3632S-PQ-00A</td>
<td>60</td>
<td>30</td>
</tr>
</tbody>
</table>

Notes:

1. Exceeding these ratings may damage the device.

## ESD Rating

- Human-body model (HBM): 2kV
- Charged-device model (CDM): 1kV

## Recommended Operating Conditions

- Supply voltage \( V_{IN} \): 4V to 18V
- Output voltage \( V_{OUT} \): 0.8V to 5.2V
- Operating junction temp. \( T_J \): -40°C to +125°C
## ELECTRICAL CHARACTERISTICS

\( V_{IN} = 12V, T_A = -40°C \) to \(+125°C \) \(^{(5)}\), unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply current (shutdown)</td>
<td>( I_{IN} )</td>
<td>( V_{EN} = 0V )</td>
<td>15</td>
<td>( \mu A )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply current (quiescent)</td>
<td>( I_q )</td>
<td>No switching, FB = 0.85V</td>
<td>1200</td>
<td>( \mu A )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Switch leakage</td>
<td>( SW_{LKG} )</td>
<td>( V_{EN} = 0V, V_{SW} = 12V )</td>
<td>1</td>
<td>( \mu A )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Switching frequency</td>
<td></td>
<td>( V_{OUT} = 3.3V )</td>
<td>-15%</td>
<td>2200</td>
<td>+15%</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{OUT} = 1.2V )</td>
<td>-15%</td>
<td>2200</td>
<td>+15%</td>
<td>kHz</td>
</tr>
<tr>
<td>Low-side valley current limit (^{(6)})</td>
<td>( I_{LIMIT1} )</td>
<td></td>
<td>3</td>
<td>3.3</td>
<td>3.9</td>
<td>A</td>
</tr>
<tr>
<td>Low-side negative current limit</td>
<td>( I_{LIMIT2} )</td>
<td>Force PWM mode or OVP, need force PWM option</td>
<td>-2.5</td>
<td>A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Minimum on time (^{(6)})</td>
<td>( t_{ON_MIN} )</td>
<td>Reach min ( t_{ON} ), then decrease ( f_{SW} ). Avoid unstable pulse. Simulate 18V to 1V spec.</td>
<td>25</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Minimum off time (^{(6)})</td>
<td>( t_{OFF_MIN} )</td>
<td>Reach min ( t_{OFF} ) then decrease ( f_{SW} ), simulate 4.2V to 3.3V spec.</td>
<td>80</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reference accuracy</td>
<td>( V_{REF} )</td>
<td>( T_J = -40°C ) to +125°C</td>
<td>788</td>
<td>800</td>
<td>812</td>
<td>mV</td>
</tr>
<tr>
<td>Output load regulation (^{(6)})</td>
<td>( V_{OLD_REG} )</td>
<td>( V_{OUT} = 3.3V, I_{OUT} = 0A ) to 3A</td>
<td>-0.5</td>
<td>+0.5</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Output line regulation (^{(6)})</td>
<td>( V_{OL_NREG} )</td>
<td>( V_{OUT} = 3.3V, I_O = 0.1A/1.5A/3A )</td>
<td>-0.5</td>
<td>+0.5</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Output over-voltage threshold</td>
<td>( V_{OVP} )</td>
<td>FB pin OV threshold, monitor Vin OV then hiccup</td>
<td>110%</td>
<td>115%</td>
<td>120%</td>
<td>( V_{REF} )</td>
</tr>
<tr>
<td>OVP hysteresis</td>
<td></td>
<td>OVP is disabled during SS</td>
<td>5</td>
<td>( V_{REF} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OVP delay</td>
<td>( t_{OVP} )</td>
<td></td>
<td>2</td>
<td>( \mu s )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output pin absolute OV</td>
<td>( V_{OVP2} )</td>
<td>Same behavior with FB &gt; 115%</td>
<td>5.7</td>
<td>6</td>
<td>6.3</td>
<td>V</td>
</tr>
<tr>
<td>Absolute OV hysteresis</td>
<td></td>
<td></td>
<td>50</td>
<td>( mV )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PG OV threshold rising</td>
<td>( PGOV_{HI} )</td>
<td>Fault</td>
<td>110%</td>
<td>115%</td>
<td>120%</td>
<td>( V_{REF} )</td>
</tr>
<tr>
<td>PG OV threshold falling</td>
<td>( PGOV_{LO} )</td>
<td>Good</td>
<td>110%</td>
<td>( V_{REF} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PG UV threshold rising</td>
<td>( PGUV_{HI} )</td>
<td>Good</td>
<td>85%</td>
<td>90%</td>
<td>95%</td>
<td>( V_{REF} )</td>
</tr>
<tr>
<td>PG UV threshold falling</td>
<td>( PGUV_{LO} )</td>
<td>Fault</td>
<td>80%</td>
<td>( V_{REF} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power good deglitch time</td>
<td>( PGDe_g )</td>
<td></td>
<td>50</td>
<td>( \mu s )</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### ELECTRICAL CHARACTERISTICS (continued)

VIN = 12V, TA = -40°C to +125°C (5), unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>PG sink current capability</td>
<td>VPG</td>
<td>Sink 4mA</td>
<td>0.4</td>
<td>0.6</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>EN rising threshold</td>
<td>VEN_RISING</td>
<td></td>
<td>1.1</td>
<td>1.20</td>
<td>1.3</td>
<td>V</td>
</tr>
<tr>
<td>EN falling threshold</td>
<td>VEN_FALL</td>
<td></td>
<td>0.96</td>
<td>1.00</td>
<td>1.04</td>
<td>V</td>
</tr>
<tr>
<td>VIN UVLO rising</td>
<td>INUV_Vin</td>
<td></td>
<td>3.2</td>
<td>3.6</td>
<td>3.9</td>
<td>V</td>
</tr>
<tr>
<td>VIN UVLO hysteresis</td>
<td>INUVHYS</td>
<td>Take care</td>
<td></td>
<td></td>
<td>V_CC</td>
<td>LDO dropout</td>
</tr>
<tr>
<td>VCC regulator</td>
<td>VCC</td>
<td></td>
<td>3.3</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VCC load regulation</td>
<td></td>
<td>I_CC = 20mA</td>
<td>3</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>Soft start time (6)</td>
<td>tss</td>
<td>V_OUT from 10% to 90%</td>
<td>1.65</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>Thermal shutdown (6)</td>
<td></td>
<td></td>
<td>150</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Thermal hysteresis (6)</td>
<td></td>
<td></td>
<td>20</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>

**Notes:**

5) Not tested in production and guaranteed by over-temperature correlation.

6) Guaranteed by characterization, not production tested.
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the Design Example section. $V_{\text{IN}} = 12\,\text{V}$, $V_{\text{OUT}} = 3.3\,\text{V}$, $T_{\text{A}} = 25^\circ\text{C}$, unless otherwise noted.

**Efficiency vs. Load Current**

$V_{\text{OUT}} = 5\,\text{V}$

$V_{\text{OUT}} = 3.3\,\text{V}$

**Load Regulation vs. Load Current**

$V_{\text{OUT}} = 5\,\text{V}$

$V_{\text{OUT}} = 3.3\,\text{V}$

**Line Regulation vs. Input Voltage**

$V_{\text{IN}} = 12\,\text{V}$, $V_{\text{OUT}} = 3.3\,\text{V}$

**Temperature Rise vs. Load Current**

$V_{\text{IN}} = 12\,\text{V}$
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the Design Example section. 
\( V_{\text{IN}} = 12\text{V}, V_{\text{OUT}} = 3.3\text{V}, T_A = 25^\circ\text{C}, \) unless otherwise noted.

Thermal Derating

\( V_{\text{IN}} = 12\text{V} \)
TYPICAL PERFORMANCE CHARACTERISTICS (continued)
Performance waveforms are tested on the evaluation board of the Design Example section. \(V_{IN} = 12V\), \(V_{OUT} = 3.3V\), \(T_A = 25^\circ C\), unless otherwise noted.

**V\text{O} Ripple**

\(I_{OUT} = 0A\)

![Waveform Image]

\(I_{OUT} = 3A\)

![Waveform Image]

**VIN Start-Up through Input Voltage**

\(I_{OUT} = 0A\)

![Waveform Image]

\(I_{OUT} = 3A\)

![Waveform Image]

**Shutdown through Input Voltage**

\(I_{OUT} = 0A\)

![Waveform Image]

\(I_{OUT} = 3A\)

![Waveform Image]
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Performance waveforms are tested on the evaluation board of the Design Example section.

\( V_{IN} = 12\text{V}, \quad V_{OUT} = 3.3\text{V}, \quad T_{A} = 25^\circ\text{C} \), unless otherwise noted.

- **Start-Up through Enable**
  - \( I_{OUT} = 0\text{A} \)
  - \( I_{OUT} = 3\text{A} \)

- **Shutdown through Enable**
  - \( I_{OUT} = 0\text{A} \)
  - \( I_{OUT} = 3\text{A} \)

- **Short Circuit Entry**
  - \( I_{OUT} = 0\text{A} \)
  - \( I_{OUT} = 3\text{A} \)
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Performance waveforms are tested on the evaluation board of the Design Example section. $V_{\text{IN}} = 12\text{V}$, $V_{\text{OUT}} = 3.3\text{V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

**Short Circuit Recovery**

- $I_{\text{OUT}} = 0\text{A}$
- $I_{\text{OUT}} = 3\text{A}$

**Short Circuit Steady State**

**Transient Response**

- $I_{\text{OUT}} = 1.5\text{A}$ to $3\text{A}$, $800\text{mA/μs}$

---

**Graphs:**

- Waveforms showing $V_{\text{OUT}}$, $V_{\text{IN}}$, $V_{\text{SW}}$, and $I_{\text{L}}$ for different conditions.
- Scales for each channel are specified.

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FUNCTIONAL BLOCK DIAGRAM

Figure 1: Functional Block Diagram
OPERATION

PWM Operation
The MPM3632S is a fully-integrated, synchronous, rectified, forced CCM mode, step-down switch mode converter. Constant-on-time (COT) control provides fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on if the feedback voltage (VFB) drops below the reference voltage (VREF) due to insufficient output voltage. The output voltage and input voltage determine the on period to ensure the switching frequency stays constant over the input voltage range.

After the on period elapses, the HS-FET turns off. It turns on again when VFB drops below VREF. This repetitive operation regulates the output voltage. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET off to minimize the conduction loss. There is a dead short between input and GND if the HS-FET and LS-FET turn on simultaneously. This is called shoot-through. To avoid shoot-through, a dead time (DT) is internally generated when the HS-FET is off and the LS-FET is on, or when the LS-FET is off and the HS-FET is on.

An internal compensation is applied for COT control to further stabilize the device. When ceramic capacitors are used as output capacitors, this internal compensation then improves the jitter performance without affecting the line or load regulation.

Regular-Load Operation
Continuous-conduction mode (CCM) is when the output current is high and the inductor current is above 0A. Figure 2 shows CCM operation. When VFB is below VREF - VDC_ERROR, the HS-FET turns on for a fixed interval that is set by an internal one-shot on-timer. When the HS-FET turns off, the LS-FET turns on until the next period.

In CCM, the switching frequency is constant and it is also called PWM operation.

DC Auto Tune Loop
The MPM3632S applies a DC auto-tune loop to balance the DC error between VFB and VREF. It adjusts the comparator input-REF to make VFB follow VREF. This is a slow loop that improves load and line regulation without affecting the transient performance. Figure 3 shows the relationship between VFB, VREF, and REF.

Internal Regulator
A 3.3V internal regulator powers most of the internal circuitries. When EN is high, this regulator takes the VIN input and operates in the full VIN range. When VIN exceeds 3.3V, the output of the regulator is in full regulation. When VIN is below 3.3V, the output voltage decreases and follows the input voltage.

Enable Control
EN is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator; drive EN low to turn it off. The EN pin is a high-voltage input node, so connect the EN pin to the input to set auto startup. The EN pin can support an 18V input voltage.

Under-Voltage Lockout (UVLO)
Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The device’s UVLO comparator monitors the voltage of VIN pin. The UVLO rising threshold is about 3.6V, and its falling threshold is 3.1V.
Soft Start

Soft start prevents the converter output voltage from overshooting during start-up. When the chip starts, the internal circuitry generates a soft-start voltage \( V_{SS} \) that ramps up from 0V to 3.3V. When \( V_{SS} \) is lower than \( V_{REF} \), the error amplifier uses \( V_{SS} \) as the reference. When \( V_{SS} \) is higher than \( V_{REF} \), the error amplifier uses \( V_{REF} \) as the reference.

Over-Current Protection and Hiccup

The device has cycle-by-cycle over-current limiting control. The current-limit circuit employs a "valley" current-sensing algorithm. The part uses the \( R_{DS(on)} \) of the low-side MOSFET to sense the current. If the current-sense signal exceeds the current-limit threshold, the PWM does not initiate a new cycle.

The trip level is fixed internally. The inductor current is monitored by the voltage between the GND pin and the SW pin. GND is used as the positive current sensing node, so connect GND to the source terminal of the bottom MOSFET.

Since this value is monitored while the high-side MOSFET is off and the low-side MOSFET is on, the over-current (OC) trip level sets the valley level of the inductor current. The load current at over-current threshold \( I_{OC} \) can be calculated with Equation (1):

\[
I_{OC} = I_{\text{limit}} + \frac{\Delta I_{\text{inductor}}}{2}
\]

In an over-current condition, the current to the load exceeds the current to the output capacitor, and the output voltage falls off. The output voltage drops until \( V_{FB} \) falls below the undervoltage (UV) threshold, which is typically below 50% of \( V_{REF} \). Once UV triggers, the device enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-shorted to ground, and it greatly reduces the average short circuit current to alleviate thermal issues and protect the regulator. The device exits the hiccup mode when the over-current condition is removed.

Over Voltage Protection (OVP)

The MPM3632S monitors the feedback voltage \( V_{FB} \) to detect an over-voltage condition. When \( V_{FB} \) exceeds 115% of the reference voltage \( V_{REF} \), the controller enters a dynamic regulation period. During this period, the IC turns the low-side MOSFET on until a -2.5A negative current limit triggers and turns off the low-side MOSFET for a fixed delay time if the OV conditions persists. This discharges the output and maintains it within the normal range. The part exits dynamic regulation when \( V_{FB} \) falls below 110% of \( V_{REF} \).

If the VOUT pin’s absolute voltage exceeds the 6V threshold, the part enters dynamic regulation mode to discharge the output voltage.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperatures exceeds 150°C, it shuts down the whole chip. When the temperature falls below its lower threshold, (about 130°C), the chip enables again.

PG Indicator

The PG pin is an open-drain output. When \( V_{FB} \) is above the UV threshold and below the OV threshold, EN is high, VIN is OK, and there is no over-temperature condition, this pin is set to high impedance. Otherwise this pin is pulled down to GND. When an external resistor pulls it up to a reliable voltage, this pin can be used for the digital interface.

Floating Driver and Bootstrap Charging

Figure 4 shows an internal bootstrap charging circuit. An internal bootstrap capacitor powers the floating power of the MOSFET driver. This floating driver has its own UVLO protection. This UVLO’s rising threshold is 2.3V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by \( V_{IN} \) through \( D1, M1, C4, L1 \) and \( C2 \). If \( V_{IN} - V_{SW} \) exceeds 3.3V, \( U1 \) regulates \( M1 \) to maintain a 3.3V BST voltage across \( C4 \).

**Figure 4: Internal Bootstrap Charging Circuit**
APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage. Choose the R1 resistance. R2 can be estimated with Equation (2):

\[
R_2 = \frac{R_1}{V_{OUT} - 0.8V}
\]

(2)

Figure 5 shows the feedback circuit.

\[\text{Figure 5: Feedback Network}\]

where \(V_o\) is the output voltage. The output voltage feedback gain is determined by:

\[
G_{FB} = \frac{R_2}{R_1 + R_2}
\]

(3)

To stabilize the system and optimize the load transient response, place a feed-forward capacitor \((C_{FF})\) in parallel with R1. Table 1 shows the values of feedback resistors and feedforward capacitors for common output voltages.

<table>
<thead>
<tr>
<th>(V_{OUT}) (V)</th>
<th>R1 (kΩ)</th>
<th>R2 (kΩ)</th>
<th>C_{FF} (pF)</th>
<th>C_{OUT} (μF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>47</td>
<td>8.87</td>
<td>39</td>
<td>22</td>
</tr>
<tr>
<td>3.3</td>
<td>47</td>
<td>15</td>
<td>39</td>
<td>22</td>
</tr>
<tr>
<td>2.5</td>
<td>47</td>
<td>22</td>
<td>39</td>
<td>22</td>
</tr>
<tr>
<td>1.8</td>
<td>47</td>
<td>37.4</td>
<td>22</td>
<td>22</td>
</tr>
<tr>
<td>1.5</td>
<td>47</td>
<td>53.6</td>
<td>22</td>
<td>22</td>
</tr>
<tr>
<td>1.2</td>
<td>47</td>
<td>93.1</td>
<td>22</td>
<td>22</td>
</tr>
<tr>
<td>1</td>
<td>47</td>
<td>187</td>
<td>22</td>
<td>22</td>
</tr>
</tbody>
</table>

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10μF capacitor suffices.

Since the input capacitor absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be calculated with Equation (4):

\[
I_{C1} = \frac{I_{LOAD}}{2} \times \left( \frac{V_{OUT}}{V_{IN}} \left( 1 - \frac{V_{OUT}}{V_{IN}} \right) \right)
\]

(4)

The worst-case condition occurs at \(V_{IN} = 2 \times V_{OUT}\) shown in Equation (5):

\[
I_{C1} = \frac{I_{LOAD}}{2}
\]

(5)

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, place a small, high-quality ceramic capacitor \((0.1 \text{ μF})\) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent an excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (6):

\[
\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_1} \times \frac{V_{OUT}}{V_{IN}} \times \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)
\]

(6)

Selecting the Output Capacitor

An output capacitor \((C2)\) is required to maintain the DC output voltage. Low ESR ceramic capacitors can be used with the device to maintain a low output ripple. A 22μF output ceramic capacitor is sufficient for most cases.
When using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is caused mainly by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (7):

\[
\Delta V_{\text{OUT}} = \frac{V_{\text{OUT}}}{8 f_{\text{SW}} L_1 C_2} \left(1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}ight) \quad (7)
\]

With tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be calculated with Equation (8):

\[
\Delta V_{\text{OUT}} = \frac{V_{\text{OUT}}}{f_{\text{SW}} L_1} \left(1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}ight) R_{\text{ESR}} \quad (8)
\]

Where \(L_1\) is a 0.68\(\mu\)H, integrated inductor.

The characteristics of the output capacitor also affect the stability of the regulation system.

**PCB Layout Guidelines**

Efficient PCB layout is critical for stable operation. For the best results, see Figure 6 and follow the guidelines below:

1. Keep the connection of the input ground and GND as short and wide as possible.
2. Ensure that all feedback connections are short and direct.
3. Place the feedback resistors as close as to the chip as possible.
4. Route sensitive analog areas such as FB away from SW.
5. Place enough vias around the chip to improve thermal performance.

**Notes:**

7) The recommended layout is based on Figure 6.
TYPICAL APPLICATION CIRCUIT

Figure 8: Typical Application Circuit
PACKAGE INFORMATION

EC LGA-10 (3mmx3mmx1.45mm)

TOP VIEW

BOTTOM VIEW

SIDE VIEW

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE x.xx MILLIMETERS MAX.
3) JEDEC REFERENCE IS xxx.
4) DRAWING IS NOT TO SCALE.

RECOMMENDED LAND PATTERN
## CARRIER INFORMATION 1

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package Description</th>
<th>Quantity/ Reel</th>
<th>Quantity/ Tube</th>
<th>Quantity/ Tray</th>
<th>Reel Diameter</th>
<th>Carrier Tape Width</th>
<th>Carrier Tape Pitch</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPM3632SGPQ-Z</td>
<td>EC LGA (3mmx3mmx1.45mm)</td>
<td>2500</td>
<td>N/A</td>
<td>N/A</td>
<td>13in.</td>
<td>12mm</td>
<td>8mm</td>
</tr>
</tbody>
</table>

## CARRIER INFORMATION 2

Note:
This is a schematic diagram of Tray. Different packages correspond to different trays with different length, width and height.

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package Description</th>
<th>Quantity/ Reel</th>
<th>Quantity/ Tube</th>
<th>Quantity/ Tray</th>
<th>Reel Diameter</th>
<th>Carrier Tape Width</th>
<th>Carrier Tape Pitch</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPM3632SGPQ</td>
<td>EC LGA (3mmx3mmx1.45mm)</td>
<td>N/A</td>
<td>N/A</td>
<td>490</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
</tbody>
</table>

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