MPM3593

High-Efficiency, 45V, 3A, Digitally Calibrated, Synchronous Step-Down Module

DESCRIPTION

The MPM3593 is a high-frequency, synchronous, rectified, step-down module with an I²C control interface and a multi-page one-time programmable (OTP) memory. It can achieve up to 3A of continuous output current (I_{OUT}), with excellent load and line regulation across a wide input voltage (V_{IN}) range.

The MPM3593 integrates an internal high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET) to achieve high efficiency without requiring an external Schottky diode. With internal compensation and a feedback divider, the device provides a very compact solution that requires a minimal number of readily available, standard external components.

The MPM3593 is flexibly designed to support a 0.8V to 12V output voltage (V_{OUT}) that can be adjusted on the fly via an I²C serial interface. The voltage slew rate, switching frequency (f_{SW}), enable, and power-save mode are also configurable via the I²C interface. This allows the user to optimize each output for different specifications.

During bench evaluations, different configurations can be easily obtained via the I²C interface instead of reworking external components. Once the desired optimal configuration is achieved, a multi-page OTP memory can permanently store the settings.

Current mode operation provides fast transient response and eases loop stabilization. Full protection features include under-voltage lockout (UVLO), over-voltage protection (OVP), over-current protection (OCP), and over-temperature protection.

The MPM3593 is available in a QFN-41 (6mmx8mm) package.

FEATURES

- Wide 3.5V to 45V Operating V_{IN} Range
- 3A Continuous Output Current (I_{OUT}) at V_{OUT} ≤ 5V and 2A Continuous I_{OUT} at V_{OUT} > 5V
- 12V V_{OUT} at V_{IN} ≤ 24V and 8V V_{OUT} at V_{IN} > 24V
- High-Efficiency, Synchronous Mode Module
- Power Good (PG) and Fault Indications
- OVP, OCP, and Over-Temperature Protection
- Internal Soft Start (SS)
- Configurable Address via Resistor
- Configurable Parameters via I²C Interface Include:
  - 0.8V to 12V V_{OUT} Range
  - Switching Frequency (f_{SW})
  - Compensation Network
  - Slope Compensation
  - Enable (EN) Threshold
  - Input UVLO Threshold
  - PG Threshold
  - AAM Mode and CCM Selection
  - Light-Load Mode Threshold
  - SCP Mode Selection
  - Current Limit Threshold
  - OVP Mode Selection
  - Input and Output OVP Threshold
  - Over-Temperature Protection Threshold
  - Switching Slew Rate
  - Output Slew Rate (SS Time, t_{SS})
  - SYNC Input and Output Selection
  - Phase Shift
  - Frequency Dithering for Low-EMI Operation
- Multi-Page One-Time Programmable (OTP) Memory for Permanent Storage
- Available in a QFN-41 (6mmx8mm) Package

APPLICATIONS

- Industrial Power Systems
- Automotive Power Systems
- Telecommunication Systems

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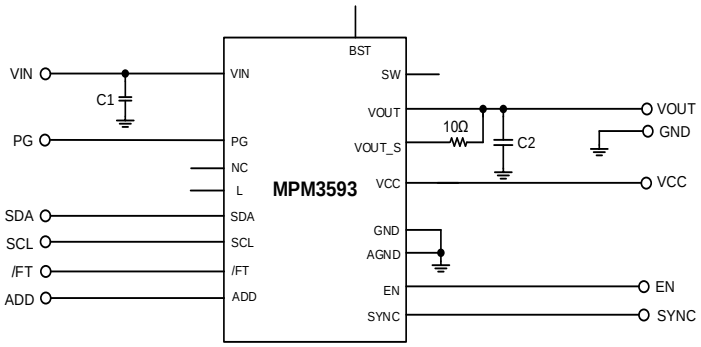
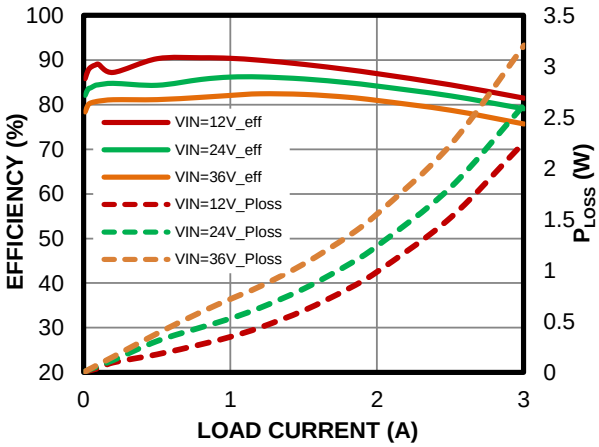
TYPICAL APPLICATION



Efficiency and Power Loss vs. Load Current

V_{OUT} = 3.3V



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPM3593GQY-xxxx**	QFN-41 (6mmx8mm)	*See Below*	3
MPM3593GQY-0001	QFN-41 (6mmx8mm)	*See Below*	3
EVKT-M3593	-	-	-

* For tray, add suffix -T (e.g. MPM3593GQY-0001-T).

** “xxxx” is the configuration identifier for the register settings stored in the OTP memory. Each “x” can be a hexadecimal value between 0 and F. “0001” is the default configuration code. For more details on the configuration information, see Table 2 and Table 3 on page 29 based on the suffix code “0001”.

TOP MARKING

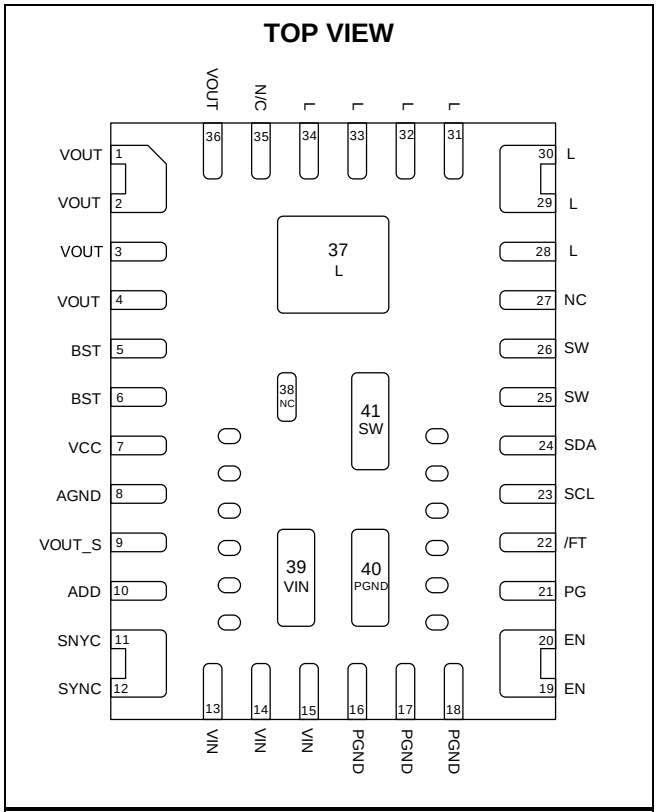
MPSYYWW

MP3593

LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP3593: Part number
LLLLLLLLL: Lot number

PACKAGE REFERENCE



QFN-41 (6mmx8mm)

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PIN FUNCTIONS

Pin #	Name	Description
1, 2, 3, 4, 36	VOUT	**Module output.**
5,6	BST	**Bootstrap.** A 0.1µF capacitor connected internally between the SW and BST pins forms a floating supply across the high-side MOSFET (HS-FET) switch driver. BST can also be floated.
7	VCC	**Internal 5V low-dropout (LDO) regulator output.** A 1µF capacitor connected internally decouples the VCC pin. VCC can also be floated.
8	AGND	**Signal ground.** The AGND pin is the internal logic and signal circuit's ground. AGND is not internally connected to the power ground. Ensure AGND is connected to the power ground in the PCB layout.
9	VOUT_S	**Output voltage (V_{OUT}) sense.**
10	ADD	**Address setting for the I^2C.**
11,12	SYNC	**Synchronized to external clock signal.** The SYNC pin can be configured via the I^2C to the sync input (SYNCIN) or sync output (SYNCO).
13, 14, 15, 39	VIN	**Supply voltage.** The VIN pin supplies power to the entire module. To reduce switching spikes, connect a decoupling capacitor from VIN to ground, placed as close as possible to the IC. Connect VIN using a wide PCB trace.
16, 17, 18, 40	PGND	**Power ground.** The PGND pin is the regulated V_{OUT}'s reference ground. For the best thermal results, connect PGND to larger copper areas.
19, 20	EN	**Enable.** Pull the EN pin high to turn on the MPM3593; pull EN low to turn off the MPM3593. EN cannot be floated.
21	PG	**Power good indicator.** The PG pin's output is an open drain. If used, connect a resistor to a pull-up power source.
22	/FT	**Fault indicator.** If any fault or warning occurs, the /FT pin is pulled down.
23	SCL	**I^2C serial clock.**
24	SDA	**I^2C serial data.**
25, 26, 41	SW	**Module switch output.** Internally connect to the internal inductor.
27, 35, 38	NC	**Not connected.** Float the NC pin. Do not connect the NC pins together in the PCB layout.
28, 29, 30, 31, 32, 33, 34, 37	L	**N/A.**

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) .....-0.3V to +48V
SW voltage (V_{SW}) ..... -0.3V (-10V for <3ns)
.....to V_{IN} + 0.3V (+50V for <3ns)
EN voltage (V_{EN}) .....-0.3V to +48V
BST voltage (V_{BST}) ..... V_{SW} + 5.5V
VCC voltage (V_{CC}).....-0.3V to +5.5V
Output voltage (V_{OUT}).....-0.3V to +15V
All other pins .....-0.3V to +5V
Continuous power dissipation (T_A = 25°C) (2) (5)
QFN-41 (6mmx8mm) 4.8W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings (3)

Human body model (HBM) .....±2KV
Charged device model (CDM) ..... ±750V

Recommended Operating Conditions (4)

V_{IN}.....3.5V to 45V
V_{OUT}.....0.8V to 12V (V_{IN} ≤ 24V)
.....0.8V to 8V (V_{IN} > 24V)
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

EVM3593-QY-00B (5)	26	12.6 °C/W
JESD51-7 (6)	33.6	26.2 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) HBM, per JEDEC specification JESD22-A114; CDM, per JEDEC specification JESD22-C101, AEC specification AEC-Q100-011. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
4) The device is not guaranteed to function outside of its operating conditions. See the Typical Application Circuits section on page 28.
5) Measured on EVM3593-QY-00B, 4-layer PCB, 64mmx64mm.
6) Measured on JESD51-7, 4-layer PCB. The θ_{JA} value given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C, typical values refer to T_J = 25°C [8], unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN_UVLO_VTH}$	05h, bits[3:1] = 0b000	2.9	3.2	3.4	V
V_{IN} UVLO threshold hysteresis	$V_{IN_UVLO_HYS}$	05h, bit[0] = 0b1		4		%
V_{IN} UVLO threshold DAC range	$V_{IN_UVLO_DAC}$		3.2		7.4	V
V_{IN} quiescent current	I_Q	00h, bits[7:0] = 0x64; 01h, bits[1:0] = 0b01; V_{OUT} = 5V		600	1000	µA
V_{IN} shutdown current	I_{SD}	V_{EN} = 0V, T_J = 25°C			1	µA
Default output voltage	$V_{OUT_DEFAULT}$	00h, bits[7:0] = 0x64; 01h, bits[1:0] = 0b01; T_J = 25°C	4.95	5	5.05	V
		T_J = -40°C to +125°C	4.925	5	5.075	V
Operating V_{OUT} range	V_{OUT}	V_{IN} ≤ 24V	0.8		12	V
		V_{IN} > 24V	0.8		8	V
Default switching frequency	$f_{SW_DEFAULT}$	02h, bits[5:0] = 0b001010, T_J = 25°C	450	500	550	kHz
Configurable frequency range	f_{SW}		250		2500	kHz
Sync frequency range	f_{SYNC}		250		2500	kHz
Sync high threshold	V_{SYNC_HIGH}		2			V
Sync low threshold	V_{SYNC_LOW}				0.4	V
Minimum on time [7]	t_{ON_MIN}	Peak current mode		80		ns
Minimum off time [7]	t_{OFF_MIN}			380		ns
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)_H}$	V_{BST} - V_{SW} = 5V		95	180	mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)_L}$			50	100	mΩ
Default rising switching slew rate [7]	$SR_{R_DEFAULT}$	09h, bits[2:1] = 0b00		1		V/ns
Rising switching slew rate range [7]	SR_R		1		4	V/ns
Default falling switching slew rate [7]	$SR_{F_DEFAULT}$	09h, bits[4:3] = 0b00		1		V/ns
Falling switching slew rate range [7]	SR_F		1		4	V/ns
BST to SW refresh UVLO	V_{BST_UVLO}			2.4	2.8	V
BST to SW refresh UVLO hysteresis	$V_{BST_UVLO_HYS}$			0.2		V
Default soft-start time	$t_{SS_DEFAULT}$	04h, bits[7:6] = 0b01		1		ms
t_{SS} range	t_{SS}		0.5		4	ms
Default EN voltage threshold	$V_{EN_DEFAULT}$	05h, bits[6:5] = 0b01	1.2	1.4	1.6	V
EN voltage threshold range	V_{EN}		1.2		2	V

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C, typical values refer to T_J = 25°C [8], unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Default EN voltage hysteresis	$V_{EN_HYS_DEFAULT}$	05h, bit[4] = 0b0		220		mV
EN voltage hysteresis range	V_{EN_HYS}		220		420	mV
Default PG upper trip rising threshold	$V_{PG_U_DEFAULT}$		108	110	112	% of V_{OUT}
PG upper trip rising threshold range	$V_{PG_U_RANGE}$		110		115	%
Default PG lower trip rising threshold	$V_{PG_L_DEFAULT}$		86	89	92	% of V_{OUT}
PG lower trip threshold range	$V_{PG_L_RANGE}$		84		89	%
Default PG trip threshold hysteresis	$V_{PG_HYS_DEFAULT}$			5.5		%
PG trip threshold hysteresis range	V_{PG-HYS}		3		5.5	%
PG low output voltage	V_{PG_SINK}	I_{SINK} = 1mA		0.1	0.3	V
PG rising deglitch time	$t_{PG_DELAY_RISING}$			30		µs
PG falling deglitch time	$t_{PG_DELAY_FALLING}$			30		µs
VCC regulator	V_{CC}	I_{CC} = 0mA	4.7	5	5.3	V
Default peak current limit [7]	$I_{PEAK_LIMIT_DEFAULT}$	06h, bits[5:3] = 0b000	4.2	5	5.8	A
Peak current limit range	I_{PEAK_LIMIT}		2		8	A
Default valley current limit [7]	$I_{VALLEY-LIMIT_DEFAULT}$	06h, bits[2:1] = 0b10	3	4	5.2	A
Valley current limit range	I_{VALEY_LIMIT}		2		4	A
Default output over-voltage protection (OVP) threshold	$V_{OVP_DEFAULT}$	07h, bits[2:1] = 0b01	115	120	125	% of V_{OUT}
Output OVP threshold range	V_{OVP_RANGE}		110		130	%
Default output OVP hysteresis	$V_{OVP_HYS_DEFAULT}$	07h, bit[0] = 0b0		5.7		% of V_{OUT}
Output OVP hysteresis range	$V_{OVP_HYS_RANGE}$		3.2		5.7	%
Input OVP threshold range	$V_{IN_OVP_RANGE}$		28		40	V
Input OVP threshold accuracy	$V_{IN_OVP_ACC}$	01h, bits[3:2] = 0b10	32	34	36	V
Default input OVP hysteresis	$V_{IN_OVP_HYS_DEFAULT}$	01h, bit[4] = 0b1		3.5		% of V_{IN_OVP}
Input OVP hysteresis range	$V_{IN_OVP_HYS_RANGE}$		3.5		5.5	%
Default thermal shutdown [7]	$T_{SD_DEFAULT}$	07h, bits[7:6] = 0b10		175		°C
Thermal shutdown range [7]	T_{SD}		125		175	°C
Default thermal shutdown hysteresis [7]	$T_{SD_SYS_DEFAULT}$	07h, bit[5] = 0b0		25		°C
Thermal shutdown hysteresis range [7]	T_{SD_SYS}		25		50	°C

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I²C PORT SIGNAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C, typical values refer to T_J = 25°C [8], unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
I²C Interface Specifications						
Input logic low	V_{IL}		0		0.4	V
Input logic high	V_{IH}		1.3			V
Output logic low	V_{OL}	I_{LOAD} = 3mA			0.4	V
SCL clock frequency	f_{SCL}				400	kHz
SCL high time	t_{HIGH}		0.6			µs
SCL low time	t_{LOW}		1.3			µs
Data set-up time	t_{SU_DAT}		100			ns
Data hold time	t_{HD_DAT}		0		0.9	µs
Set-up time for a repeated start condition	t_{SU_STA}		0.6			µs
Hold time for a start condition	t_{HD_STA}		0.6			µs
Bus free time between a start and stop condition	t_{BUF}		1.3			µs
Set-up time for a stop condition	t_{SU_STO}		0.6			µs
Rise time of SCL and SDA	t_R		20 + 0.1 x C_B		120	ns
Fall time of SCL and SDA	t_F		20 + 0.1 x C_B		120	ns
Pulse width of suppressed spike	t_{SP}		0		50	ns
Capacitance bus for each bus line	C_B				400	pF

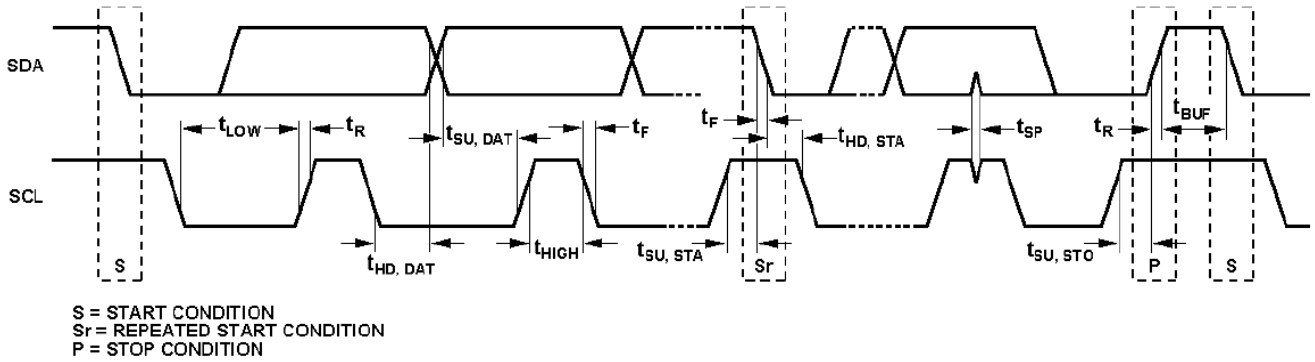

Figure 1: I²C-Compatible Interface Timing Diagram

Notes:

7) Derived from characterization test. Not tested in production.
8) Derived from engineering sample test. Not tested in production.

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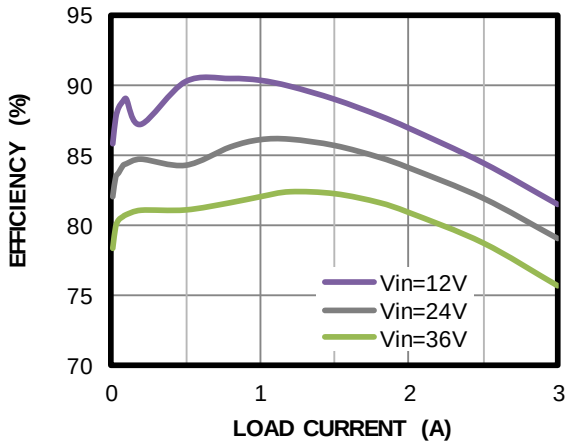
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board, V_{IN} = 24V, AAM mode, T_A = 25°C, unless otherwise noted.

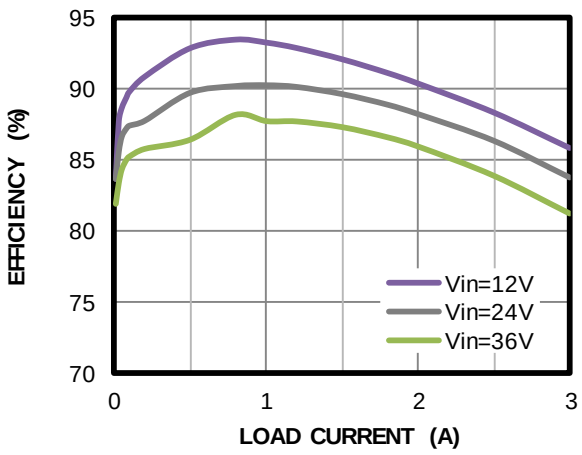
Efficiency vs. Load Current

V_{OUT} = 3.3V



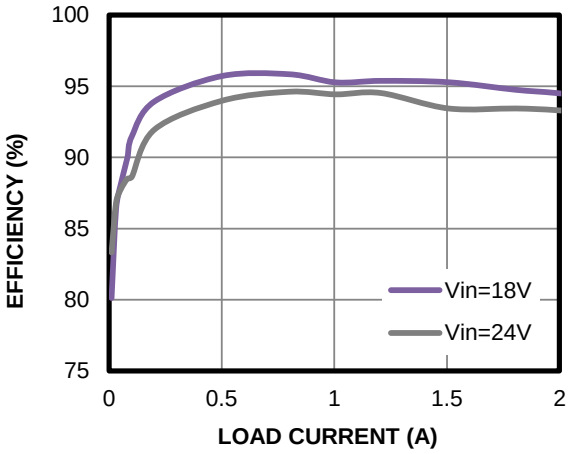
Efficiency vs. Load Current

V_{OUT} = 5V



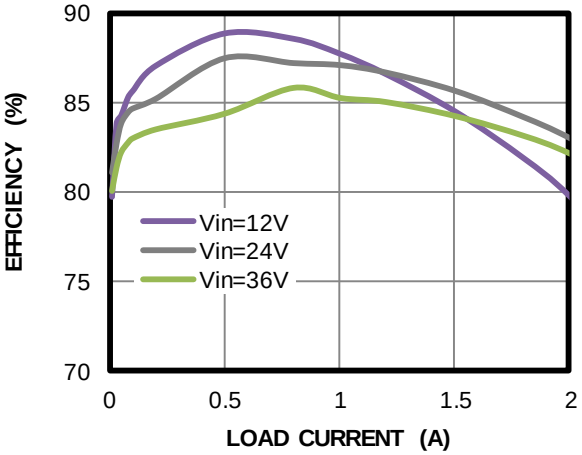
Efficiency vs. Load Current

V_{OUT} = 12V



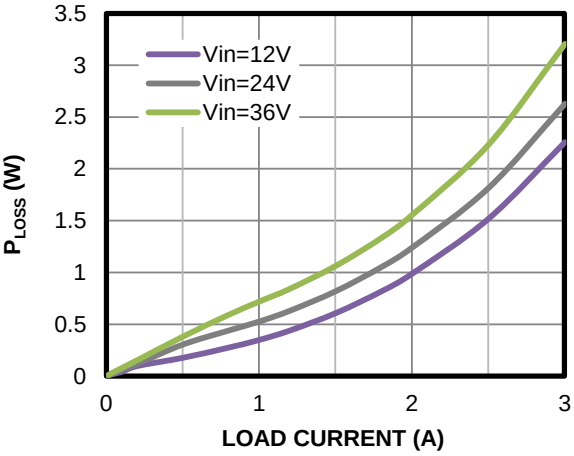
Efficiency vs. Load Current

V_{OUT} = -5V



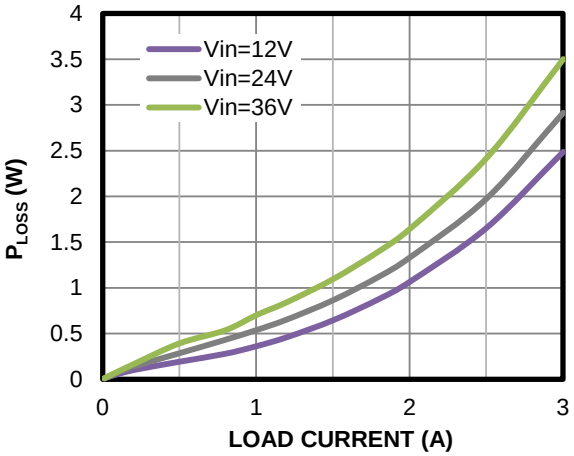
Power Loss vs. Load Current

V_{OUT} = 3.3V



Power Loss vs. Load Current

V_{OUT} = 5V



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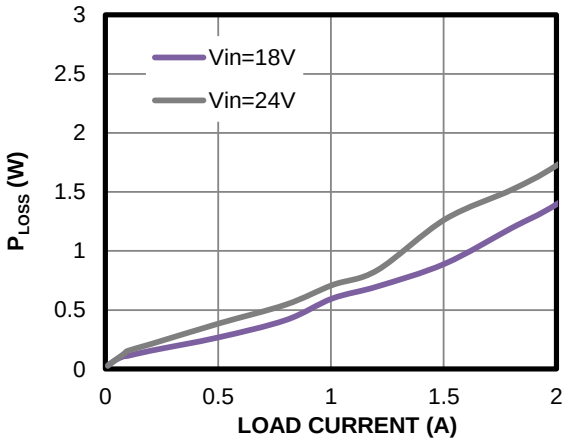
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board, V_{IN} = 24V, AAM mode, T_A = 25°C, unless otherwise noted.

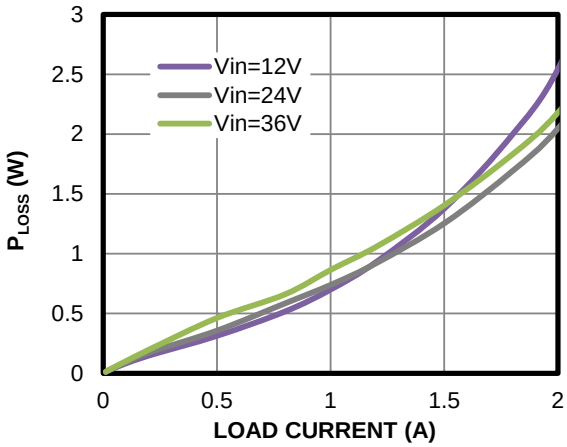
Power Loss vs. Load Current

V_{OUT} = 12V



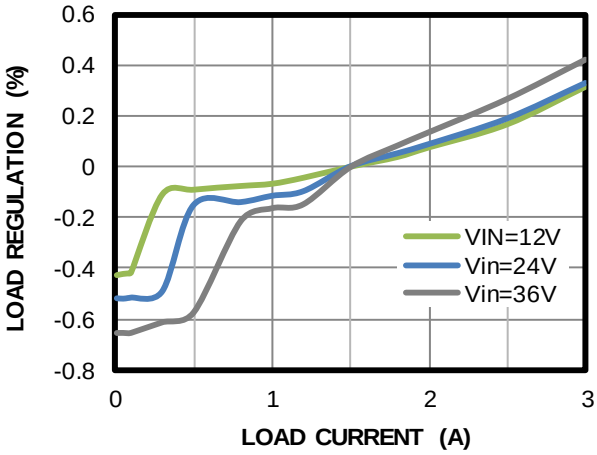
Power Loss vs. Load Current

V_{OUT} = -5V



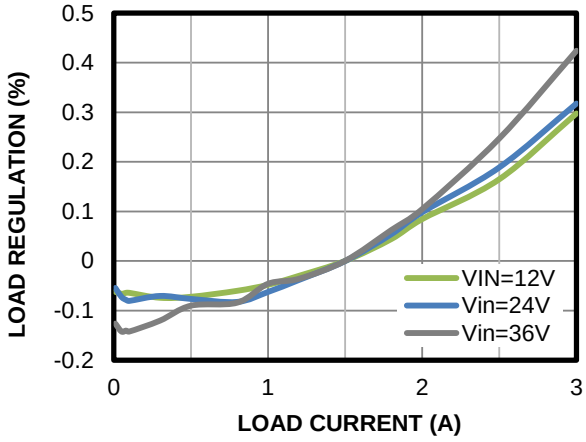
Load Regulation

V_{OUT} = 3.3V



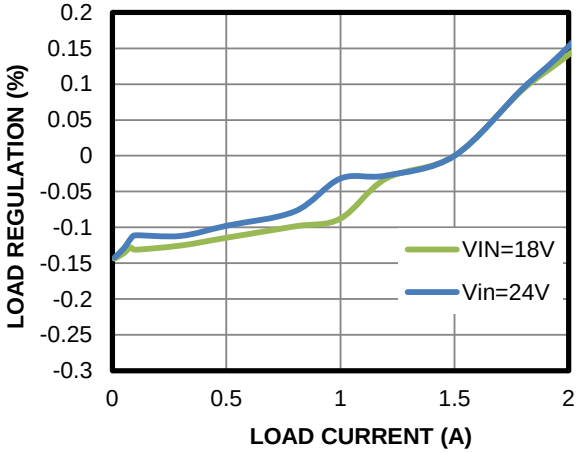
Load Regulation

V_{OUT} = 5V



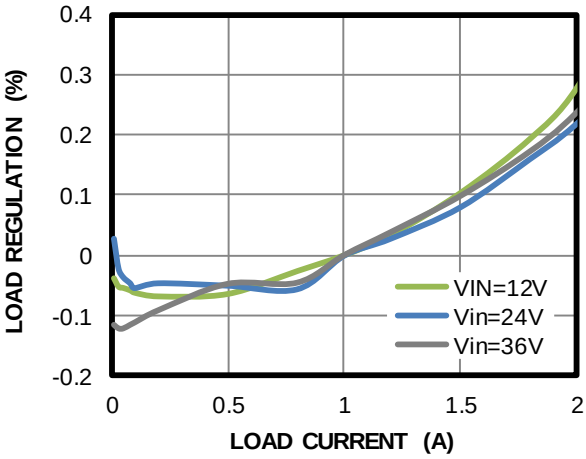
Load Regulation

V_{OUT} = 12V



Load Regulation

V_{OUT} = -5V



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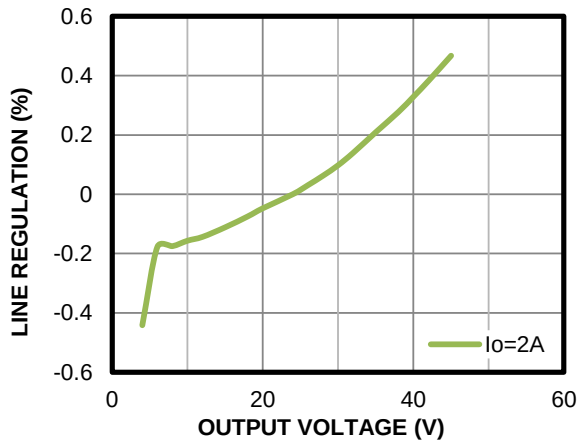
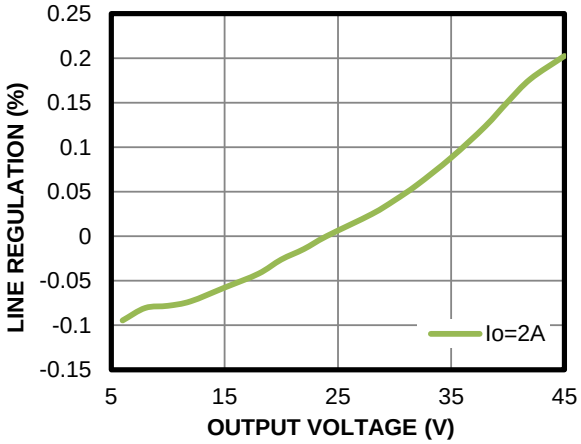
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V_{IN} = 24V, AAM mode, T_A = 25°C, unless otherwise noted.

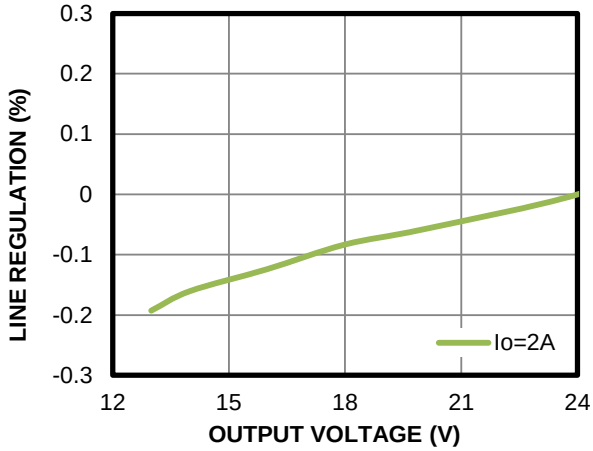
Line Regulation
V_{OUT} = 3.3V



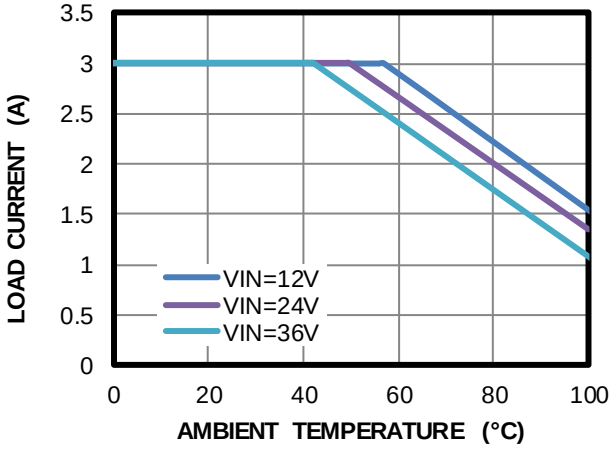
Line Regulation
V_{OUT} = 5V



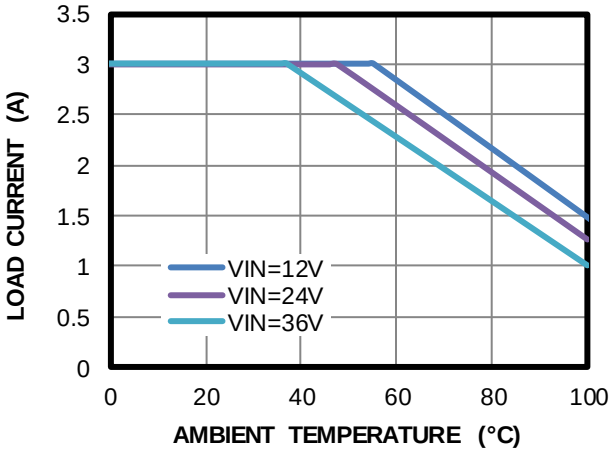
Line Regulation
V_{OUT} = 12V



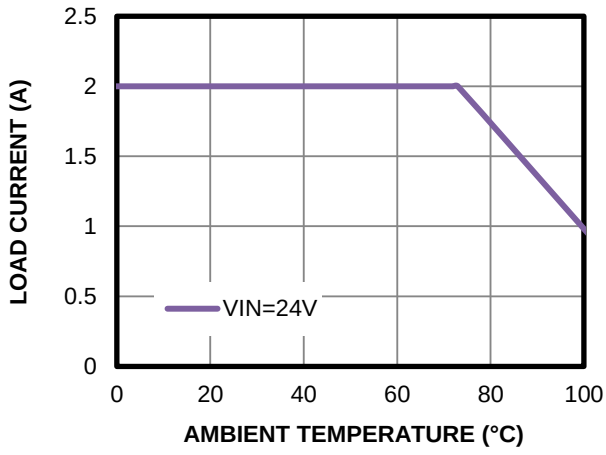
Thermal Derating
V_{OUT} = 3.3V



Thermal Derating
V_{OUT} = 5V



Thermal Derating
V_{OUT} = 12V



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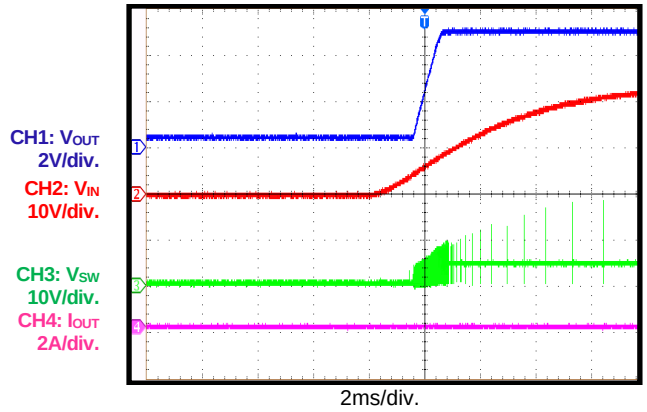
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V_{IN} = 24V, AAM mode, T_A = 25°C, unless otherwise noted.

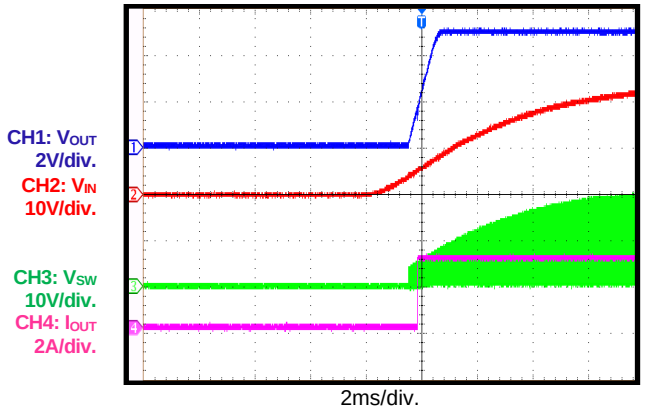
Start-Up through VIN

V_{OUT} = 5V, I_{OUT} = 0A



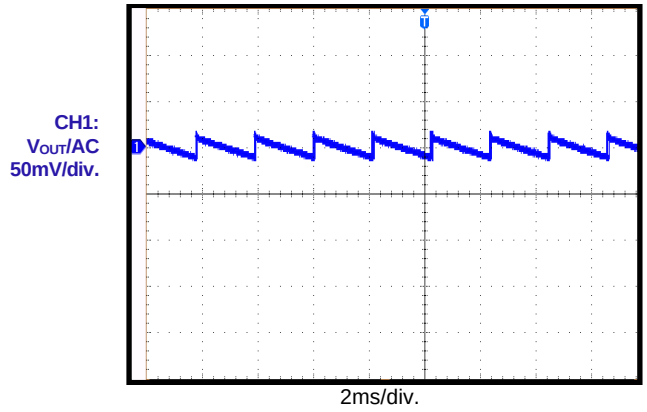
Start-Up through VIN

V_{OUT} = 5V, I_{OUT} = 3A



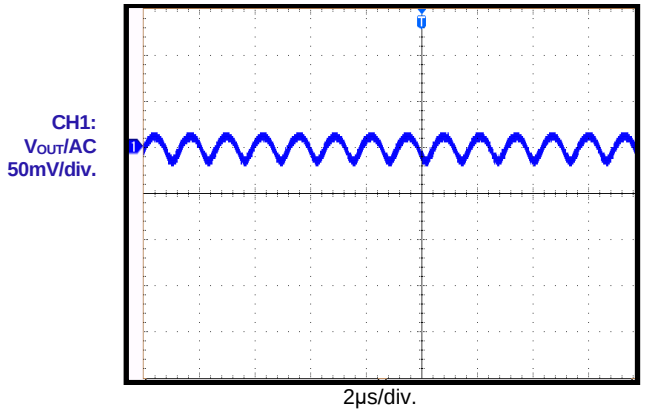
Output Voltage Ripple

V_{OUT} = 5V, I_{OUT} = 0A, 3 x 22µF capacitor



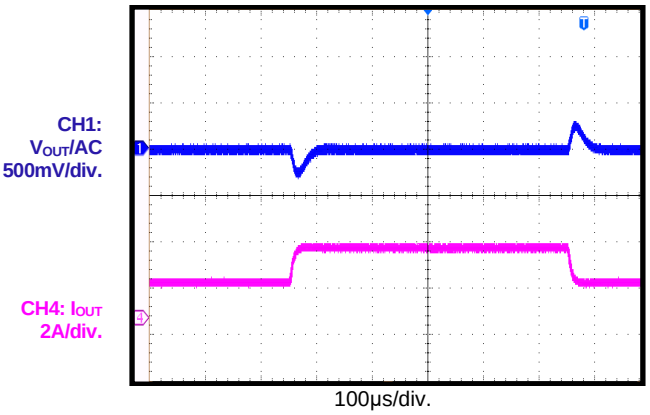
Output Voltage Ripple

V_{OUT} = 5V, I_{OUT} = 3A, 3 x 22µF capacitor



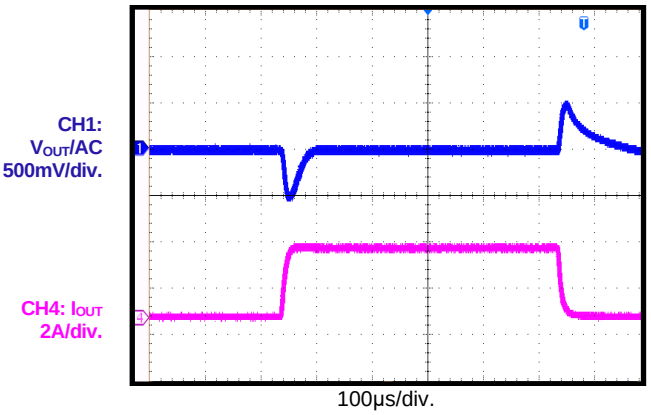
Load Transient Response

V_{OUT} = 5V, 1.5A to 3A, 3 x 22µF capacitor



Load Transient Response

V_{OUT} = 5V, 0A to 3A, 3 x 22µF capacitor



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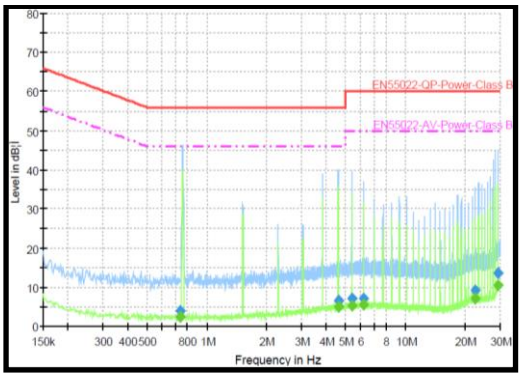
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V_{IN} = 24V, AAM mode, T_A = 25°C, unless otherwise noted.

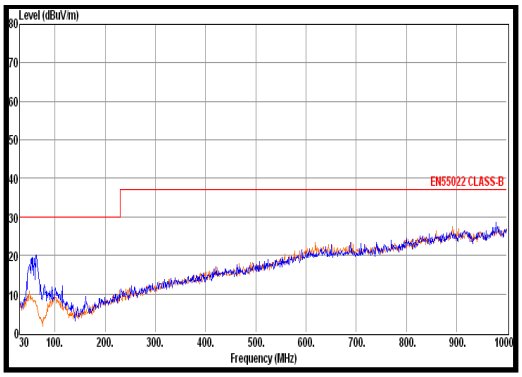
Conducted Emissions, EV55022 Class B

V_{OUT} = 3.3V, I_{OUT} = 3A, input Pi filter: 10µF, 4.7µH, or 10µF



Radiated Emissions, EV55022 Class B

V_{OUT} = 3.3V, I_{OUT} = 3A, 10µF input Pi filter



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EMI TEST CIRCUIT

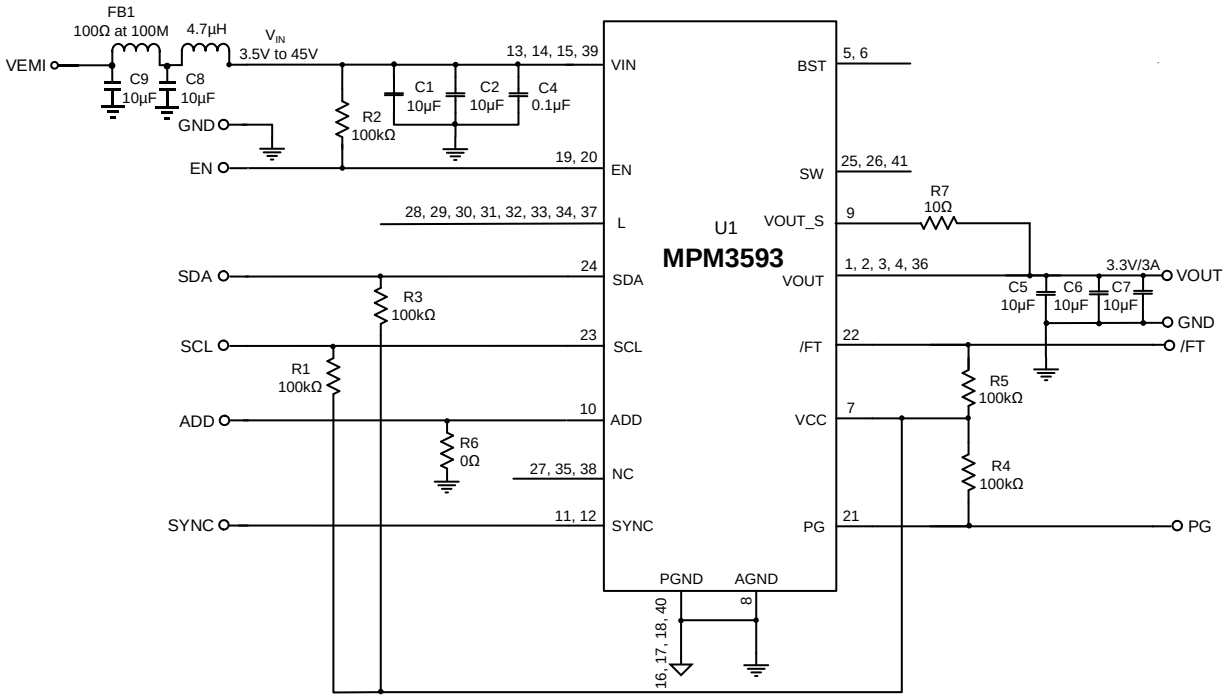

Figure 2: EMI Test Circuit

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FUNCTIONAL BLOCK DIAGRAM

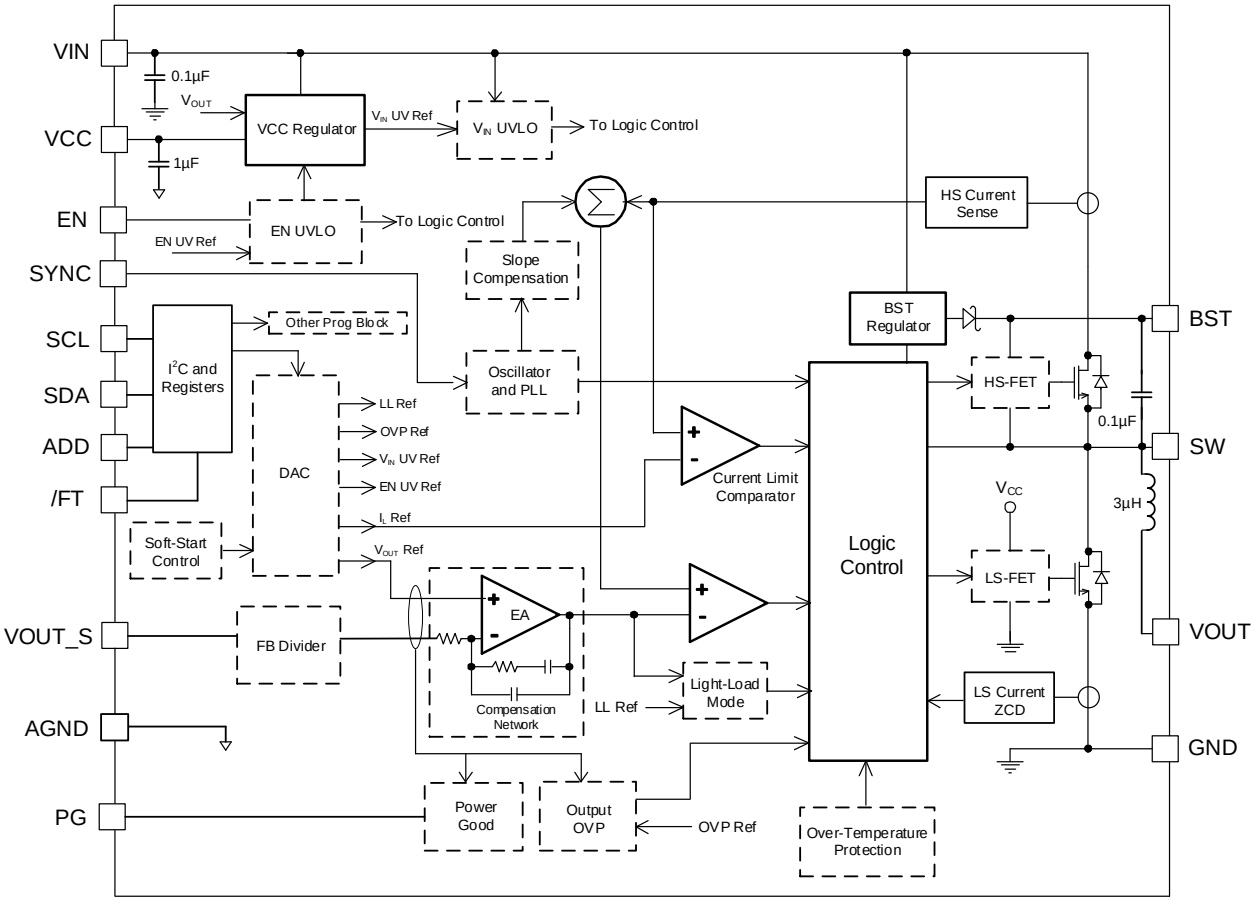

Figure 3: Functional Block Diagram (9)

Note:

9) The blocks with dashed lines are configurable.

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OPERATION

The MPM3593 is a high-frequency, synchronous step-down module with built-in power MOSFETs. The device can achieve up to 3A of continuous output current (I_{OUT}) across a wide 3.5V to 45V input voltage (V_{IN}) range, with excellent load and line regulation.

Pulse-Width Modulation (PWM) Control

At moderate-to-high output currents, the MPM3593 operates in fixed-frequency, peak current control mode to regulate the output voltage (V_{OUT}). A pulse-width modulation (PWM) cycle is initiated by the internal clock. At the clock's rising edge, the high side MOSFET (HS-FET) turns on and the inductor current (I_L) increases linearly to provide energy to the load. The HS-FET remains on until its current reaches the COMP voltage (V_{COMP}), which is the internal error amplifier (EA)'s output.

The EA compares the feedback (FB) voltage (V_{FB}) to the internal, high-precision reference voltage (V_{REF}) and generates an output voltage (V_{EA}) that is proportional to the difference between the two voltages. V_{EA} is then used to determine the amount of energy that should be transferred to the load. V_{COMP} is proportional to the load current, where a higher load current results in a higher V_{COMP}. The FB divider ratio and FB reference voltage can be adjusted via the I^2C, which makes it easy to adjust different V_{OUT} values.

When the HS-FET is off, the low-side MOSFET (LS-FET) turns on immediately and remains on until the next clock begins. During this time, I_L flows through the LS-FET. To avoid shoot-through, a dead time (DT) is inserted to prevent the HS-FET and LS-FET from turning on at the same time.

If the current in the HS-FET does not reach the value set by COMP within one PWM period, then the HS-FET remains on and saves a turn-off operation.

Mode Selection (AAM Mode and FCCM)

The MPM3593 provides two modes that can be selected via the I^2C: advanced asynchronous modulation (AAM) mode or forced continuous conduction mode (FCCM) (see Figure 4).

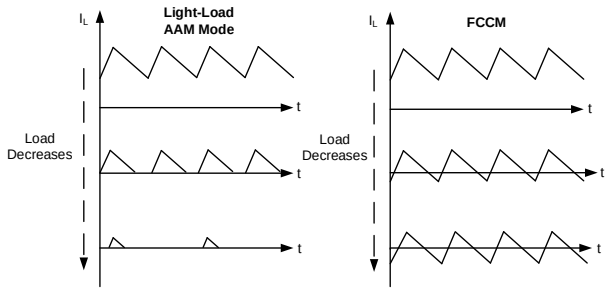

Figure 4: AAM Mode and FCCM

AAM mode optimizes efficiency under light-load or no-load conditions, meanwhile FCCM maintains a constant switching frequency (f_{SW}) and smaller output ripple, with the disadvantage of lower efficiency under light loads.

When the load decreases with AAM mode enabled, the MPM3593 first enters discontinuous conduction mode (DCM) with a fixed frequency until I_L approaches 0A. If the load decreases further, or there is no load that makes the peak I_L (I_{L_PEAK}) lower than the AAM mode threshold set via the I^2C, then the MPM3593 enters sleep mode and consumes a very low quiescent current (I_Q) to further improve light-load efficiency.

In sleep mode, the internal clock is blocked and V_{FB} is below V_{REF}. As a result, the MPM3593 skips some pulses and V_{COMP} ramps up until I_{L_PEAK} exceeds the AAM mode threshold. The internal clock is then reset and the crossover time becomes the benchmark for the next clock. This control scheme helps achieve high efficiency by scaling down the frequency, which reduces the switching and gate driver losses.

As the output current (I_{OUT}) increases under light-load conditions, V_{COMP} and f_{SW} increase. If I_{OUT} exceeds the critical level set by V_{COMP}, then the MPM3593 resumes fixed-frequency PWM control.

When FCCM is enabled, the MPM3593 operates in fixed-frequency, peak current control mode to regulate V_{OUT}, regardless of I_{OUT}.

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Internal Regulator (VCC)

Most of the internal circuitry is powered by the internal 5V regulator. This regulator uses V_{IN} as its input and operates across the full V_{IN} range. When V_{IN} exceeds 5V, the regulator's output is in full regulation. A lower V_{IN} results in a lower output voltages.

Once V_{IN} exceeds its under-voltage lockout (UVLO) threshold and the EN pin is pulled high, the regulator is enabled. During EN shutdown, the VCC regulator is disabled to reduce power dissipation.

For improved thermal performance, V_{OUT} bias function can be enabled via the I²C. When V_{OUT} exceeds 5V, VCC and the internal circuit are powered by V_{OUT}. The bias function only works when the MPM3593 is set to AAM mode; the bias function does not work in continuous conduction mode (CCM) even when V_{OUT} bias is enabled. If an external FB divider is used, do not enable the bias function. For improved output regulation, do not enable the bias function when V_{OUT} exceeds 9V.

Enable (EN) Control

EN is a digital control pin that turns the regulator, including the I²C block, on and off. Pull EN high to turn on the regulator; pull EN low to turn off the regulator. The EN threshold can be configured via the I²C. Do not float EN. To adjust the parameters via the I²C, the EN voltage (V_{EN}) must exceed 2V. When V_{EN} is low, the I²C interface is blocked to achieve lower current consumption, and the RAM registers are reset to the default value.

Switching Frequency (f_{SW})

The MPM3593's frequency is set to 500kHz by default and can be configured between 250kHz and 2.5MHz via the I²C.

SYNCIN and SYNCO

The SYNC pin can be configured via the I²C to the sync input or sync output (SYINC and SYNCO, respectively). SYNCO outputs the sync signal in phase with the internal switching clock. SYNCIN synchronizes the internal f_{SW} via an external clock using the SYNC pin, where the phase shift can be set between 0 and 180 degrees according to register 02h, bit[6] in the I²C register.

At start-up, the MPM3593 operates at the internally set frequency, then synchronizes quickly to the external clock once soft start (SS) is ready. To drive the internal logic, ensure the SYNC clock's high amplitude exceeds 2V, and the low amplitude is below 0.4V. The external SYNC frequency is recommended to be between 250kHz and 2.5MHz.

Under-Voltage Lockout (UVLO)

The MPM3593 provides V_{IN} under-voltage lockout (UVLO) protection to ensure reliable output power. If EN is active and V_{IN} exceeds the UVLO rising threshold, then the MPM3593 starts up. If V_{IN} drops below the UVLO falling threshold, then the MPM3593 shuts down. The UVLO threshold can be set between 3.2V and 7.4V via the I²C. UVLO is a non-latch protection that prevents the device from operating at an insufficient voltage.

Soft Start (SS)

When EN is pulled high, the MPM3593 implements built-in SS to ramp up V_{OUT} in a controlled slew rate, avoiding overshoot during start-up. When the MPM3593 starts up, the internal circuitry generates a SS voltage (V_{SS}) that ramps up slowly. If V_{SS} is below V_{REF}, V_{SS} overrides V_{REF} as the EA reference; if V_{SS} exceeds V_{REF}, V_{REF} acts as the EA reference. Once V_{REF} acts as the EA reference, SS completes and the MPM3593 enters steady state.

The SS time (t_{SS}) is set internally by default to 1ms. t_{SS} can also be configured to 0.5ms, 2ms, or 4ms via the I²C. When V_{OUT} is shorted to GND, V_{FB} decreases and V_{SS} is discharged. The MPM3593 resumes soft start and begins normal operation.

Pre-Biased Start-Up

If V_{FB} exceeds V_{SS} at start-up, meaning the output has a pre-biased voltage, neither the HS-FET or LS-FET turn on until V_{SS} exceeds V_{FB}.

Power Good (PG) Indicator

The MPM3593 includes an open-drain power good (PG) output. Pull PG up to a voltage source via a resistor (e.g. 100kΩ). If V_{IN} is present, PG is pulled to GND before SS is ready. If V_{OUT} is within the default ±10% rated voltage window, PG is pulled high after a delay (typically 30µs).

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If V_{OUT} moves outside the default ±10% range with a hysteresis, PG is pulled low to indicate a failure output status. The PG threshold and hysteresis can be configured via the I^2C.

FAULT Indicator

The /FT pin is open-drain output. Pull /FT up to a voltage source via a resistor (e.g. 100kΩ). During normal operation, /FT is pulled high. If any fault or warning occurs, /FT is pulled low to indicate a fault status, including input and output over-voltage protection (OVP), short-circuit protection (SCP), and thermal shutdown.

Over-Current Protection (OCP)

The MPM3593 supports cycle-by-cycle over-current protection (OCP). I_L is monitored when HS-FET is turned on. Once I_{L_PEAK} exceeds the set current limit threshold, the HS-FET immediately turns off. Then the LS-FET turns on to discharge the energy and I_L decreases. The HS-FET remains off until I_L drops below the valley current limit. OCP helps prevent I_L runaway and potential damage to the components. I_{L_PEAK} and the valley current threshold can be configured via the I^2C.

When I_L triggers the peak current limit, the OCP timer starts immediately. During the OCP timer, if I_L reaches the current limit in each cycle, then SCP operation is triggered and is set to hiccup mode by default.

Short-Circuit Protection (SCP)

If a short circuit occurs, the MPM3593 immediately hits its current limit, while V_{OUT} quickly drops to the UVLO threshold (default 50% of the set V_{OUT}, V_{OUT_SET}), which is recognized as an output dead short. This directly triggers SCP. There are three SCP modes that are selectable via the I^2C: hiccup mode (default), switching with non-hiccup mode, and latch-off mode.

In hiccup mode, the MPM3593 disables its output power stage and resets V_{SS}, then initiates a SS procedure. t_{SS} and hiccup duty determine the hiccup off time, which can be set via the I^2C. If the short-circuit condition still holds after SS completes, the device repeats this operation until the short circuit is removed and the output returns to regulation. SCP significantly reduces the average short-circuit current by periodically restarting the device, which alleviates thermal issues and protects the regulator. In switching with non-hiccup mode, the MPM3593 continues switching with I_L, where I_L is limited by the peak and valley current limit. In latch-off mode, the MPM3593 stops operating once SCP occurs until the device is re-enabled or powered up again.

Output Over-Voltage Protection (OVP)

The MPM3593 monitors V_{OUT} using the VOUT_S pin to detect V_{OUT} over-voltage (OV) conditions. When V_{OUT} exceeds the OVP threshold (default 120% of V_{OUT_SET}), OVP is triggered. There are three OVP modes that are selectable via the I^2C: discharge mode (default), stop switching mode, and latch-off mode.

In discharge mode, LS-FET turns on to discharge V_{OUT} when a OV fault is detected. LS-FET remains on until its current reaches the negative current limit. In stop switching mode, the MPM3593 stops switching when an OV fault is detected and resumes switching once the fault is removed. In latch-off mode, the MPM3593 stops operating when OVP is triggered until the device starts up again.

Input Over-Voltage Protection (OVP)

The MPM3593 offers an optional input OVP. The OVP threshold can be set to 28V, 34V, or 40V. If V_{IN} exceeds the OVP threshold, then the MPM3593 stops switching. The device resumes normal operation once the input OVP is removed. OVP is a non-latch protection. The input OVP threshold and hysteresis can be set via the I^2C interface.

Thermal Shutdown

The MPM3593 provides over-temperature protection by monitoring the IC temperature internally. Over-temperature protection prevents the chip from operating at an exceedingly high temperature. If the junction temperature (T_J) exceeds the threshold, the MPM3593 shuts down. Once T_J drops with a hysteresis (default 25°C), the device resumes operation by initiating a SS. Over-temperature protection is a non-latch protection. The over-temperature protection threshold and hysteresis can be set via the I^2C interface.

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Floating Driver and Bootstrap (BST) Charging

An internal bootstrap (BST) capacitor (C_{BST}) supplies the floating power MOSFET driver. The floating driver has its own UVLO protection with a 2.4V rising threshold and 200mV hysteresis. When the LS-FET is on, the C_{BST} voltage is charged to about 5V from VCC via a P-channel MOSFET pass transistor.

When the voltage from BST to SW (V_{BST-SW}) drops below the UVLO threshold, the HS-FET turns off and the LS-FET turns on with a high-side (HS) minimum off time to conduct and refresh the charge on C_{BST}.

Low-Dropout Operation (BST Refresh)

To improve dropout, the MPM3593 is designed to operate at close to 100% duty cycle if V_{BST-SW} exceeds its UVLO threshold. When V_{IN} drops, the HS-FET remains on and close to 100% duty cycle to maintain output regulation until V_{BST-SW} falls below the UVLO threshold.

Since the supply current sourced from C_{BST} is low, the BST charge refresh occurs infrequently and the HS-FET can remain on for more switching cycles. Thus, the switching regulator's effective duty cycle is high. During the regulator's dropout, the effective duty cycle is mainly influenced by the voltage drops across the power MOSFET, inductor resistance, low-side (LS) diode, and PCB resistance.

I²C Control and Default Output Voltage (V_{OUT})

When the MPM3593 is enabled, EN is pulled high and V_{IN} exceeds UVLO. The MPM3593 starts up to a default V_{OUT}, after which the I²C bus can communicate with the master to set the internal configuration using valid I²C commands.

Configure V_{OUT} by adjusting V_{REF} and the output FB divider ratio. Before adjusting V_{OUT} or changing any other register value, write 0x00 to register 0h to send an operation off command from the master controller, which disables the output. Then send commands to adjust the necessary parameters. After that, the MPM3593 resumes operation by receiving an operation on command. The MPM3593 does not support adjusting the internal RAM parameters on the fly, including V_{OUT} (see Figure 9 on page 22). It is recommended to exclusively use the MPS communication interface and GUI to get access to the MPM3593. If access through a local microcontroller unit (MCU) is required, contact MPS for more application information.

Frequency Dithering for Low EMI

The MPM3593 supports frequency dithering to reduce EMI, especially for EMI-sensitive applications. By using spread-spectrum modulation, the converter's frequency spectrum is spread, which in turn spreads the energy of the switching harmonics across a wider band. This reduces the switching harmonic amplitude and helps meet stringent EMI requirements. The frequency dithering range and cycle can be set via the I²C interface.

Multi-Page One-Time Programmable (OTP) Memory (10)

The MPM3593 includes three pages of one-time programmable (OTP) memory to permanently store the desired settings.

To ensure long-term reliability, a differential OTP cell is used instead of a single-ended OTP cell. Data is stored on two floating-gate avalanche-injection metal-oxide semiconductor (FAMOS) devices, and output comparators are used for differential reading.

The first page of the multi-page OTP memory is configured with the manufacturer default values. The second and third pages can be configured using MPS's GUI. Once the device is enabled, the default values on the first page set the control parameters in the registers. If there is data on other pages, the newest configuration is automatically loaded into the I²C registers. The GUI checks whether the part is completely configured as well as the remaining blank pages. For more information about the I²C register configuration, see the Register Map section on page 23 and the Register Description section on page 25.

Note:

10) The V_{OUT} bias function must be disabled before configuring the MPM3593's multi-page OTP memory.

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I²C INTERFACE

I²C Serial Interface

The I²C is a two-wire, bidirectional serial interface that consists of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage (V_{BUS}) when they are idle. A master device connected to the line generates the SCL signal and device address, then arranges the communication sequence. The MPM3593 interface is an I²C slave that supports fast mode (400kHz), which adds flexibility to the power supply solution. The MPM3593's SDA and SCL can be pulled up from 1.8V to 5V for different systems. V_{OUT}, the transition slew rate, or other interesting parameters can be instantaneously controlled via the I²C interface.

Data Validity

A clock pulse is generated for each transferred data bit. The data on the SDA line must be stable during the clock's high period. The data line's high or low state can only change when the SCL line's clock signal is low (see Figure 5).

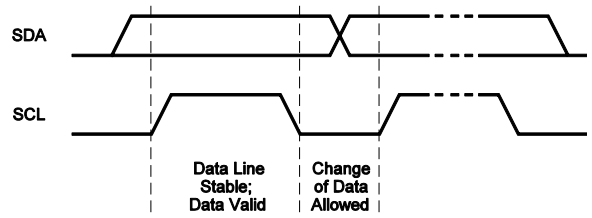

Figure 5: Bit Transfer on the I²C Bus

Start and Stop Commands

The start (S) and stop (P) commands are signaled by the master device, indicating the beginning and the end of the I²C transfer. In the start condition, the SDA signal transitions from high to low while the SCL remains high. In the stop condition, the SDA signal transitions from low to high while the SCL remains high (see Figure 6).

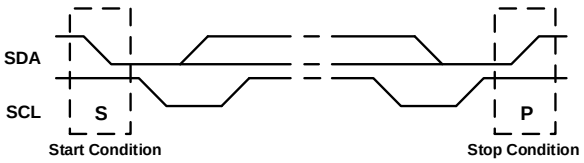

Figure 6: Start and Stop Conditions

The master always generates the start and stop commands. After the start command, the bus is busy and is not free until at least 4.7µs after the stop command. If a repeated start (Sr) command is generated instead of a stop command, then the bus stays busy. The start and repeated start conditions are functionally identical.

Transfer Data

Each byte on the SDA line must be 8 bits long and followed by an acknowledge (ACK) bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse, so that it remains stable and low during the clock pulse's high period.

Figure 7 shows a complete data transfer.

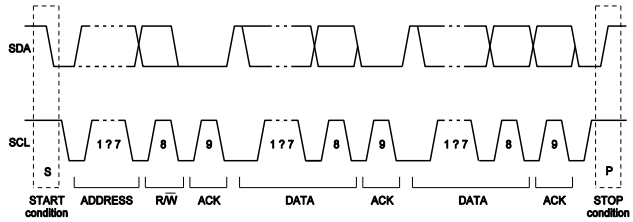

Figure 7: A Complete Data Transfer

After the start command, a 7-bit slave address is sent, followed by an 8th data direction bit (R/W), where 1 = read to indicate a data request, and 0 = write to indicate a transmission. A data transfer is always terminated by a stop command generated by the master. However, if a master wants to continue communicating on the bus, it can generate a repeated start command and address another slave without having to generate a stop command.

I²C Update Sequence

The MPM3593 requires a start command, valid I²C address, register address byte, and data byte for a single data update. The MPM3593 acknowledges receiving each byte by pulling the SDA line low during a single clock pulse's high period. A valid I²C address selects the MPM3593. The MPM3593 performs an update on the least significant bit (LSB) byte's falling edge.

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I²C Chip Address

The I²C address is configured via the ADD pin. The MPM3593 supports eight addresses for up to eight voltage rails that are configured via the ADD resistor (R_{ADD}). The master sends a 7-bit address, followed by an 8th data direction bit to indicate a read/write (R/W) operation.

Table 1 shows I²C address setting details.

Table 1: I²C Address Setting

1% Resistor (kΩ)	I²C Address
0 to 20	21h
23 to 45	22h
49 to 71.5	23h
73.5 to 97.3	24h
100 to 124	25h
127 to 147	26h
150 to 174	27h
>178	28h

I²C Interface Diagram Block

MPS's GUI can send I²C commands to the MPM3593 to generate the OTP interface time that controls the OTP to process RAM/ROM operation. Figure 8 shows the I²C interface diagram block.

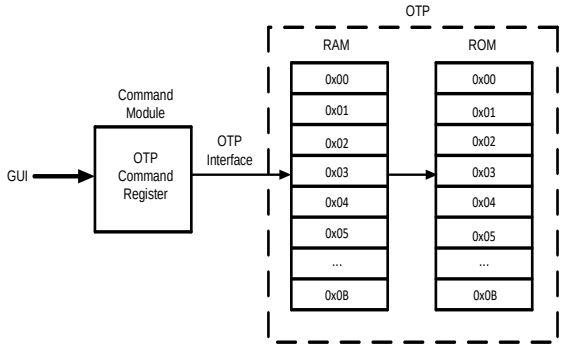

Figure 8: I²C Interface Diagram Block

Note that the registers included in the Register Map section on page 23 are not directly addressed via the I²C. The MPM3593 uses an internal command module to access user registers. These commands are supported by the GUI and are not fully described in this datasheet. Please contact MPS or visit the MPS website to download the GUI. In addition, users can access the RAM and ROM with a customized controller. If a local MCU is required to write, read, or configure the device, please contact MPS for more application information. Figure 9 and Figure 10 on page 22 show the R/W operation of the RAM registers.

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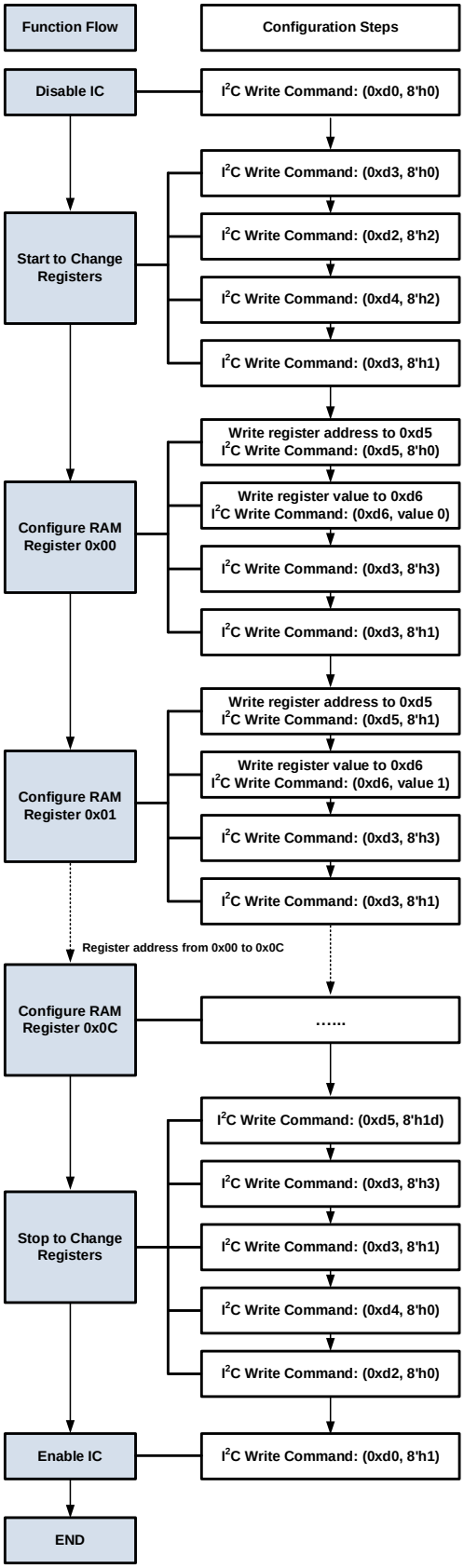

Figure 9: MPM3593 RAM Registers Write Operation Process

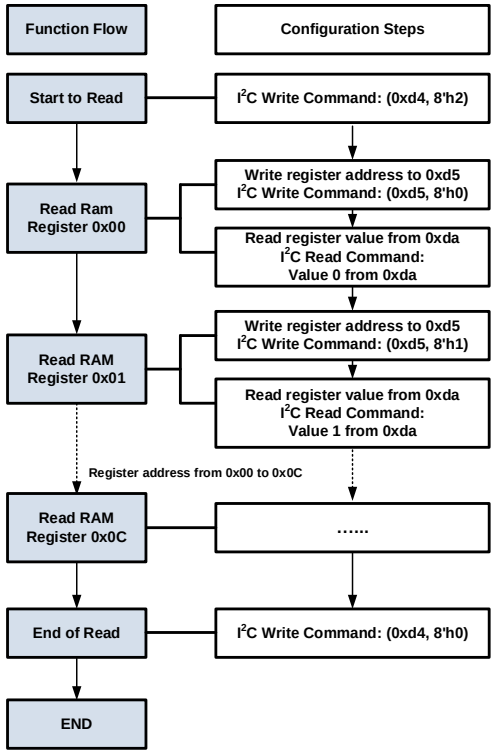

Figure 10: MPM3593 RAM Registers Read Operation Process

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REGISTER MAP

Add	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00h	R/W	REFERENCE_VOLTAGE (DAC)							
01h	R/W	FREQUENCY_ DITHERING (EN disabled)	FREQUENCY _DITHERING (dithering cycle)	FREQUENCY _DITHERING (dithering range)	INPUT_OVP_ HYSTERESIS	INPUT_OVP_ THRESHOLD	FB_DIVIDER_RATIO		
02h	R/W	N/A	PHASE_ SHIFT	SWITCHING_FREQUENCY					
03h	R/W	COMPENSATION (C_{COMP2})		COMPENSATION (R_T)			COMPENSATION (R_{COMP})		
04h	R/W	SOFT_START_TIME		SLOPE_COMPENSATION			COMPENSATION (C_{COMP1})		
05h	R/W	N/A	EN_RISING_THRESHOLD		EN_RISING_ HYSTERESIS	VIN_UVLO_RISING_ THRESHOLD			VIN_UVLO_ HYSTERESIS
06h	R/W	SCP_MODE		PEAK_CURRENT_LIMIT_THRESHOLD			VALLEY_CURRENT_ LIMIT_THRESHOLD		N/A
07h	R/W	OVER-TEMPERATURE_PROTECTION_ RISING_THRESHOLD		OTP_ HYSTERESIS	OUTPUT_OVP_MODE		OUTPUT_OVP_RISING _THRESHOLD		OUTPUT_OVP _HYSTERESIS
08h	R/W	PG_LOWER_ HYSTERESIS	PG_LOWER_ RISING_ THRESHOLD	PG_UPPER_ HYSTERESIS	PG_UPPER_ RISING_ THRESHOLD	SCP_ DETECTION_ TIME	SCP_ TRIGGERED_ FB_VOLTAGE		N/A
09h	R/W	/FT_SETTING	SYNCIN/OUT	HICCUP_ DUTY	SWITCHING_SLEW_ RATE (falling)		SWITCHING_SLEW_ RATE (rising)		N/A
0Ah	R/W	N/A							AAM/CCM
0Bh	R/W	AAM_MODE_THRESHOLD				PKC	VOUT_BIAS		NA

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REGISTER DESCRIPTION

Register Description	Add	Bits	Default Code	Default Value	Range/Values	Min Value	Max Value	Resolution /LSB	Units
Reference Voltage (DAC)	0x00	D[7:0]	01100100	1	0.6V to 2.55V	0.60	2.55	0.01	V
FB Divider Ratio	0x01	D[1:0]	01	1/5	1/2, 1/5, 1/5, 1	1/5	1	-	-
Input OVP Threshold	0x01	D[3:2]	00	No OVP	No OVP, 28V, 34V, 40V	28	40	-	V
Input OVP Hysteresis	0x01	D[4]	1	3.5	5.5, 3.5	3.5	5.5	-	% of V_{IN}
Frequency Dithering (Range)	0x01	D[5]	1	3/48	3/28, 3/48	3/48	3/28	-	f_{SW}
Frequency Dithering (Cycle)	0x01	D[6]	1	150	120, 150	120	150		µs
Frequency Dithering	0x01	D[7]	0	Disable	Disable, enable	-	-	-	-
Switching Frequency	0x02	D[5:0]	001010	500	250 to 2500	250	2500	50	kHz
Phase Shift	0x02	D[6]	0	0	0, 180	0	180	-	°
Reserved	0x02	D[7]	0	N/A	-	-	-	-	-
Compensation, (R_{COMP})	0x03	D[2:0]	011	700	400, 500, 600, 700, 800, 900, 1000, 1100	400	1100	-	kΩ
Compensation (R_T)	0x03	D[5:3]	011	60	0, 20, 40, 60, 80, 100, 120, 140	0	140	-	kΩ
Compensation (C_{COMP2})	0x03	D[7:6]	00	0.5	0.5			-	pF
Compensation (C_{COMP1})	0x04	D[2:0]	000	40	40, 45	40	45	-	pF
Slope Compensation	0x04	D[5:3]	000	750	750, 600, 450, 300, 750, 900, 1050, 1200	300	1200	-	mV
Soft-Start Time	0x04	D[7:6]	01	1	0.5, 1, 2, 4	0.5	4	-	ms
V_{IN} UVLO Hysteresis	0x05	D[0]	1	4	2, 4	2	4	-	% of $V_{IN_UVLO_VTH}$
V_{IN} UVLO Rising Threshold	0x05	D[3:1]	000	3.2	3.2, 3.8, 4.4, 5, 5.6, 6.2, 6.8, 7.4	3.2	7.4	-	V
EN Rising Hysteresis	0x05	D[4]	0	220	220, 420	220	420	-	mV
EN Rising Threshold	0x05	D[6:5]	01	1.4	1.2, 1.4,1.6, 2	1.2	2	-	V
Reserved	0x05	D[7]	0	N/A	-	-	-	-	-
Reserved	0x06	D[0]	0	N/A	-	-	-	-	-
Valley Current Limit Threshold	0x06	D[2:1]	10	4	2, 3, 4	2	4	-	A
Peak Current Limit Threshold	0x06	D[5:3]	000	5	5, 6, 7, 8, 4, 3, 2	2	8	-	A
SCP Mode	0x06	D[7:6]	00	Hiccup	Hiccup, latch, switching with non-hiccup, switching with non-hiccup	-	-	-	-
Output OVP Hysteresis	0x07	D[0]	0	5.7	5.7, 3.2	3.2	5.7	-	% of V_{OUT_SET}
Output OVP Rising Threshold	0x07	D[2:1]	01	120	110, 120, 130	110	130	-	% of V_{OUT_SET}
Output OVP Mode	0x07	D[4:3]	01	Stopping switching	Discharge, stopping switching, latch, latch	-	-	-	-

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REGISTER DESCRIPTION *(continued)*

Register Description	Add	Bits	Default Code	Default Value	Range/Values	Min Value	Max Value	Resolution /LSB	Units
Over-Temperature Protection Hysteresis	0x07	D[5]	0	25	25, 50	25	50	-	°C
Over-Temperature Protection Rising Threshold	0x07	D[7:6]	10	175	125, 150, 175	125	175	-	°C
Reserved	0x08	D[0]	0	N/A	-	-	-	-	-
SCP Triggered FB Voltage	0x08	D[1]	0	50	50, 75	50	75	-	% of V_{REF}
SCP Detection Time	0x08	D[3:2]	01	128	256, 128, 64, 32	32	256	-	f_{SW}
PG Upper Rising Threshold	0x08	D[4]	0	110	110, 115	110	115	-	% of V_{OUT_SET}
PG Upper Hysteresis	0x08	D[5]	0	5.5	5.5, 3	3	5.5	-	% of V_{OUT_SET}
PG Lower Rising Threshold	0x08	D[6]	0	89	89, 84	84	89	-	% of V_{OUT_SET}
PG Lower Hysteresis	0x08	D[7]	0	5.5	5.5, 3	3	5.5	-	% of V_{OUT_SET}
Reserved	0x09	D[0]	0	N/A	-	-	-	-	
Switching Slew Rate (Rising) (11)	0x09	D[2:1]	00	1	1, 2, 3, 4	1	4	-	V/ns
Switching Slew Rate (Falling) (11)	0x09	D[4:3]	00	1	1, 2, 3, 4	1	4	-	V/ns
Hiccup Duty (On Time)	0x09	D[5]	0	10	10, 20	10	20	-	%
SYNC In/Out	0x09	D[6]	1	SYNC in	SYNC out, SYNC in	-	-	-	-
/FT Setting	0x09	D[7]	1	Auto-reset	EN must restart to reset the fault status; Auto-reset when fault is removed	-	-	-	
AAM/CCM Control	0x0A	D[0]	0	AAM mode	AAM mode, CCM	-	-	-	
Reserved	0x0A	D[7:1]	0101000	N/A	-	-	-	-	
Reserved	0x0B	D[0]	0	N/A	-	-	-	-	
V_{OUT} BIAS	0x0B	D[2:1]	00	BIAS	No BIAS, BIAS, BIAS in sleep mode only	-	-	-	
PKC	0x0B	D[3]	1	PKC	PKC	-	-	-	
AAM Threshold (PKC)	0x0B	D[7:4]	1000	530	Disable, 605, 680, 755, 830, 905, 980, 1055, 530, 455, 380, 305, 225, 150, 75, 0	0	1055	-	mA

Note:

11) To limit the SW spike, do not use a switching slew rate above 2V/ns when the input exceeds 30V.

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APPLICATION INFORMATION

Setting the Output Voltage (V_{OUT})

The MPM3593 has two options for setting V_{OUT}: internal divider mode and external divider mode. In internal divider mode, the internal FB reference voltage (V_{FB}) and output FB divider ratio (D_{FB}) are adjusted via the I^2C. Based on REG00h, D[7:0], set V_{FB} between 0.6 and 2.55V at 10mV/LSB. Based on REG01h, D[0:1], set D_{FB} to 1/5, 1/2, and 1. V_{OUT} depends on V_{FB} and D_{FB}, and can be calculated with Equation (1):

$$V_{OUT} = \frac{V_{FB}}{D_{FB}} \quad (1)$$

For example, if V_{FB} is 1V and D_{FB} is 1/5, then V_{OUT} is 5V.

In external divider mode, D_{FB} should be set to 1 and V_{FB} can be set between 0.6V and 2.55V. Adjust the values of the external divider resistors connected to VOUT to set V_{OUT} (see Figure 11).

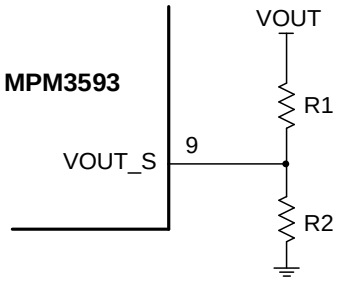

Figure 11: External Divider Mode

V_{OUT} in external divider mode can be calculated with Equation (2):

$$V_{OUT} = \frac{R1+R2}{R2} \times V_{FB} \quad (2)$$

The external divider resistance is recommended to be between 10kΩ and 100kΩ.

Selecting the Input Capacitor (C_{IN})

The step-down converter has a discontinuous input current (I_{IN}), and requires a capacitor to supply AC current to the converter while maintaining the DC V_{IN}. For the best performance, it is recommended to use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are strongly recommended due to their low ESR and small temperature coefficients.

For most applications, a 4.7µF to 10µF capacitor at the input is sufficient. To absorb high-frequency switching noise, it is strongly recommended to use another lower-value capacitor (e.g. 0.1µF) with a small package size (0603). Place the small-size capacitor as close to the VIN and GND pins as possible.

The input capacitor (C_{IN}) requires an adequate ripple current rating to absorb the switching I_{IN}. C_{IN}'s RMS current can be estimated with Equation (3):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (3)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (2):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (4)$$

For simplification, choose a C_{IN} with an RMS current rating that exceeds half of the maximum load current.

C_{IN} can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, place a small, high-quality, ceramic capacitor (e.g. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that the capacitor has sufficient capacitance to prevent excessive voltage ripple at input. The input voltage ripple (ΔV_{IN}) caused by the capacitance can be estimated with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

Selecting the Output Capacitor (C_{OUT})

The output capacitor (C_{OUT}) maintains the DC V_{OUT}. It is recommended to use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, low-ESR capacitors are recommended to effectively limit the output voltage ripple (ΔV_{OUT}). ΔV_{OUT} can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \cdot (1 - \frac{V_{OUT}}{V_{IN}}) \cdot (R_{ESR} + \frac{1}{8 f_{SW} \times C_{OUT}}) \quad (6)$$

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Where L is the fixed inductance at 3µH, and R_{ESR} is the C_{OUT}'s equivalent series resistance (ESR).

When using ceramic capacitors, the capacitance dominates the impedance at f_{SW} and causes the majority of ΔV_{OUT}. For simplification, ΔV_{OUT} can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be approximated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (8)$$

The C_{OUT} characteristics also affect the stability of the regulation system. The MPM3593 can be optimized for a wide range of capacitance and ESR values.

PCB Layout Guidelines

PCB layout is critical for stable operation. A 4-layer layout is recommended to improve thermal performance. For the best results, refer to Figure 12 and follow the guidelines below:

1. Keep the C_{IN} power loop as small as possible.
2. Connect a large ground plane directly to PGND. If the bottom layer is a ground plane, add vias near PGND.
3. Ensure that the high-current paths at GND and VIN have short, direct, and wide traces.
4. Place the ceramic C_{IN}, especially the small-size bypass C_{IN} ,as close to VIN and PGND as possible to minimize high-frequency noise.
5. Connect VIN, VOUT, and GND to a large copper area to cool the chip, which improves thermal performance and long-term reliability.
6. Place an integrated GND at the mid-layer or bottom layer.
7. Use multiple vias to connect the power planes to the mid-layers.

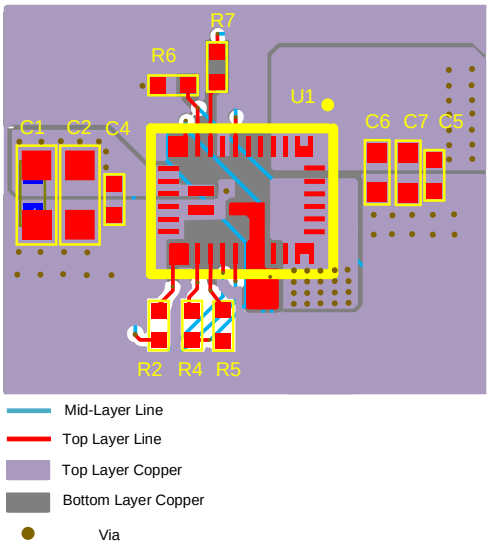

Figure 12: Recommended PCB Layout (12)

Note:

12) This PCB layout covers a full range of specs. For specific cases such as having a higher f_{SW}, lower V_{IN}, or lower I_{OUT}, a much smaller layout size can also be achieved by selecting smaller packages for the capacitors.

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TYPICAL APPLICATION CIRCUITS (13) (14)

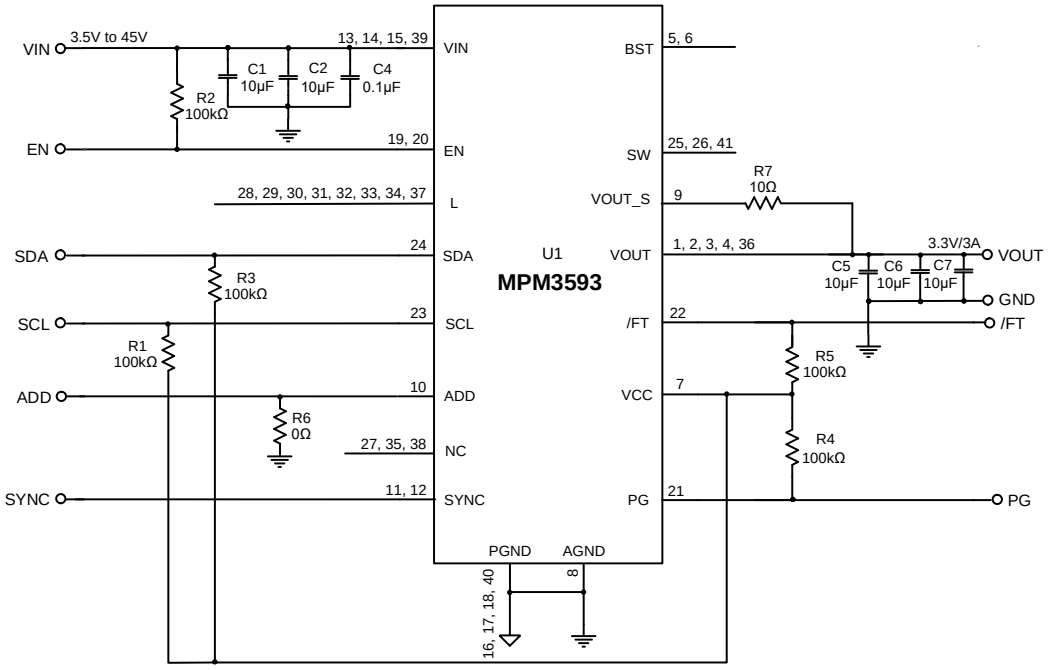

Figure 12: Typical Application Circuit (V_{OUT} = 3.3V/5V/12V, I_{OUT} = 3A)

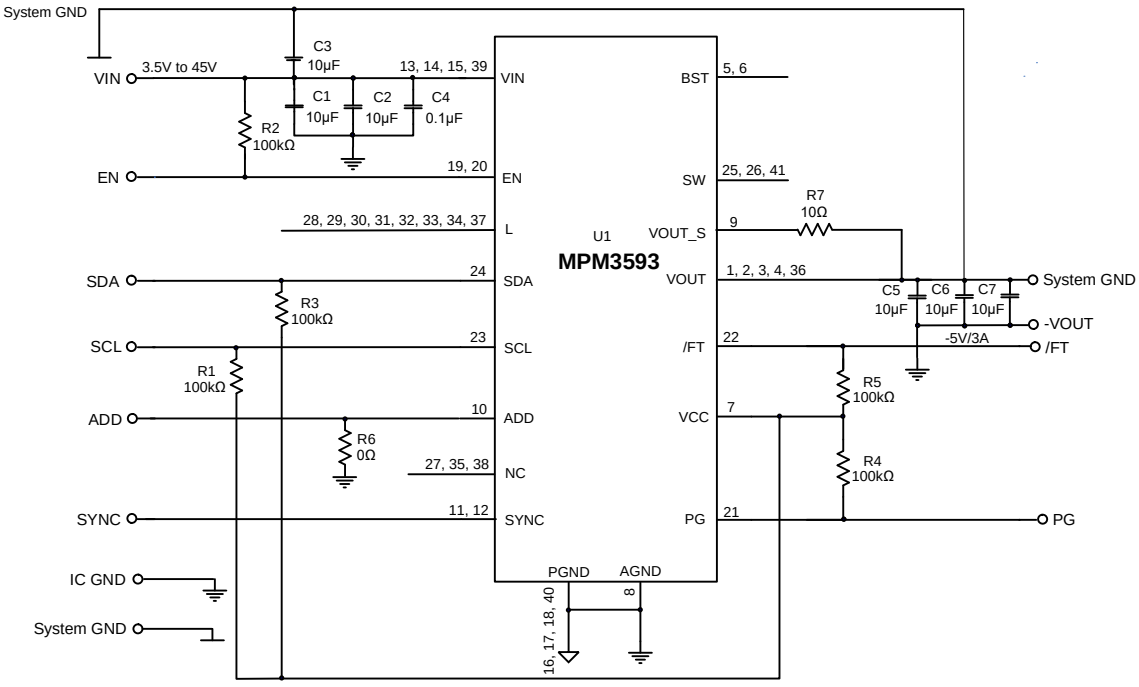

Figure 13: Typical Application Circuit (V_{OUT} = -5V, I_{OUT} = 3A)

Notes:

13) If V_{OUT} exceeds 9V, use a 100Ω resistor for R7 and ensure that the V_{OUT} bias function is disabled.
14) If V_{OUT} exceeds 8V, ensure that V_{IN} does not exceed 24V.

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DEFAULT OTP CONFIGURATION

Table 2: MPM3593GQY-0001 Suffix Code Configuration

OTP Items	Values
Reference Voltage (DAC)	1V
FB Divider Ratio	1/5
Output Voltage	5V
Mode	AAM Mode
SCP Mode	Hiccup
Soft-Start Time	1ms
Switching Slew Rate (Rising)	1V/ns
Switching Slew Rate (Falling)	1V/ns
Valley Current Limit	4A
Peak Current Limit	5A
Switching Frequency	500kHz
OTP Rising Threshold	175°C
OTP Configuration Code	0x0001

Table 3: MPM3593GQY-0001 Suffix Code Register Value

Suffix Code	Register	Hex Value
0001	0x00	64h
0001	0x01	71h
0001	0x02	0Ah
0001	0x03	1Bh
0001	0x04	40h
0001	0x05	21h
0001	0x06	04h
0001	0x07	8Ah
0001	0x08	04h
0001	0x09	C0h
0001	0x0A	50h
0001	0x0B	88h
0001	0x0C	FFh

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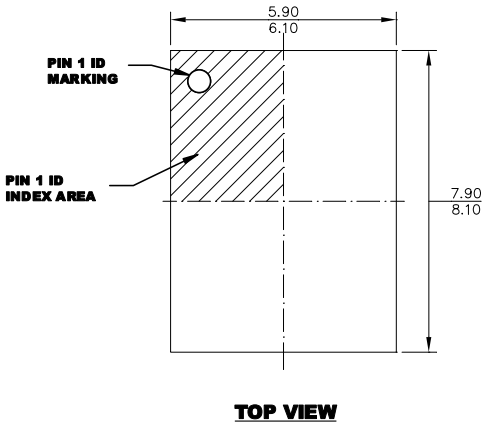
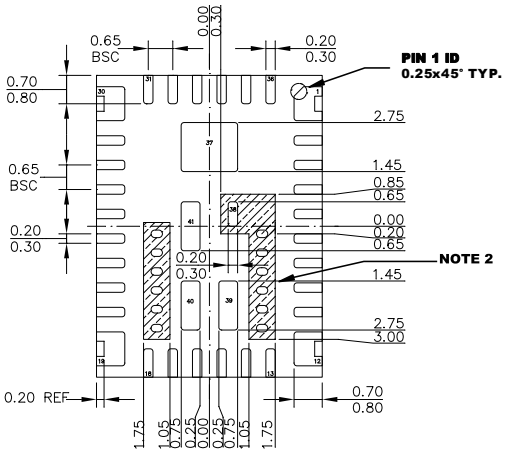
PACKAGE INFORMATION

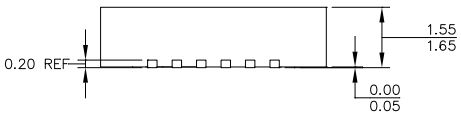
QFN-41 (6mmx8mm)



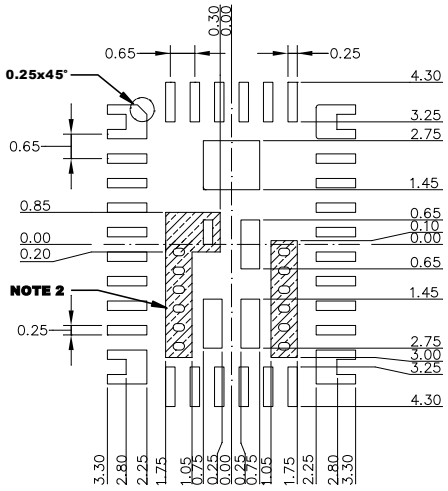
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) SHADED AREA IS THE KEEP-OUT ZONE. ANY PCB METAL TRACE AND VIA ARE NOT ALLOWED TO CONNECT TO THIS AREA ELECTRICALLY OR MECHANICALLY.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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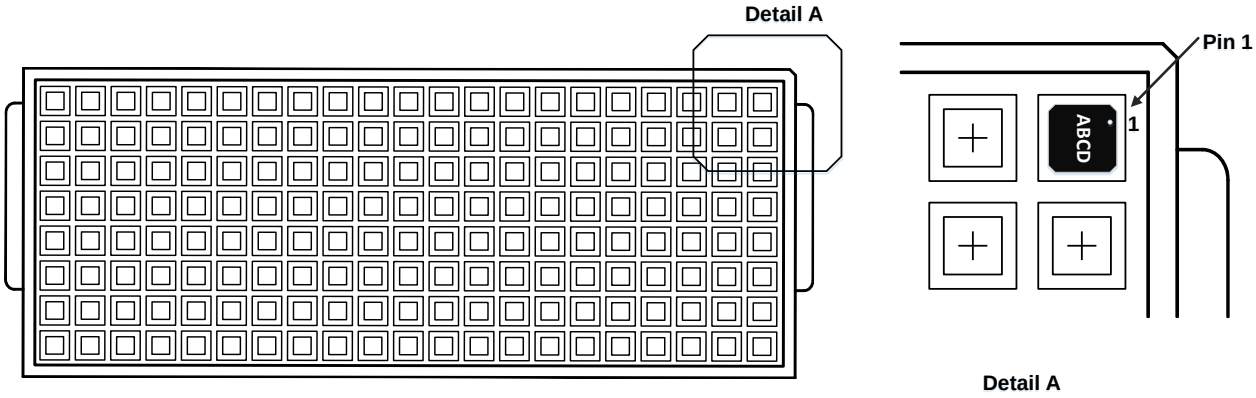
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM3593GQY-T	QFN-41 (6mmx8mmx 1.6mm)	N/A	N/A	128	N/A	N/A	N/A

Note:

15) This is a schematic diagram of a tray. Different packages correspond to different trays with different lengths, widths, and heights.

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/5/2022	Initial Release	-
1.1	4/1/2024	Updated the Ordering Information section from reel to tray	3
		Updated the Carrier Information from reel to tray: • Updated image • Updated carrier information • Added Note 15	31

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