



MPF52000-AEC2

Dual USB PD Controller for Source Port, Supporting Firmware Update and Advanced PDP Management, AEC-Q100 Qualified

DESCRIPTION

The MPF52000-AEC2 is a highly integrated, dual-channel USB power delivery (PD) controller for a source port. The device integrates a 32-bit ARM Cortex-M0 microcontroller, up to 36MHz operation frequency, USB Type-C port controller, and legacy charging protocol management. In addition, the CC lines support a firmware update feature.

The dual USB Type-C ports support USB PD revision 3.1 with programmable power supply (PPS) and Qualcomm quick charge 3/4/4+ technology. These ports are also backward compatible with dedicated charging port (DCP) schemes for battery charging specification (BC1.2), Apple divider mode, and Huawei FCP/SCP protocols without the need for outside user interaction.

Power sharing functionality supports dynamic power budget management between the two USB PD ports. Power data object (PDO) capabilities are reduced when the car battery voltage is low, or when an over-temperature warning is triggered.

Fault condition protections includes bus voltage (V_{BUS}) over-voltage protection (OVP) and under-voltage protection (UVP), and thermal shutdown. The high-voltage I/O pins support short-to-battery and short-to-VBUS protection.

The MPF52000-AEC2 requires a minimal number of readily available, standard external components. The MPF52000-AEC2 is available in a QFN-24 (4mmx4mm) package and is available in AEC-Q100 Grade 2.

FEATURES

- 3.3V to 21V Bus Voltage (V_{BUS}) Range in Standard Power Range (SPR) Mode with Discharge Function
- Supports Up to 48V V_{BUS} in Extended Power Range (EPR) Mode with External V_{BUS} Resistor Divider
- 4.6V to 5.5V Input Voltage (V_{IN}) Range
- 150 μ A Low I_{DRLP} Mode in Detached State

FEATURES (continued)

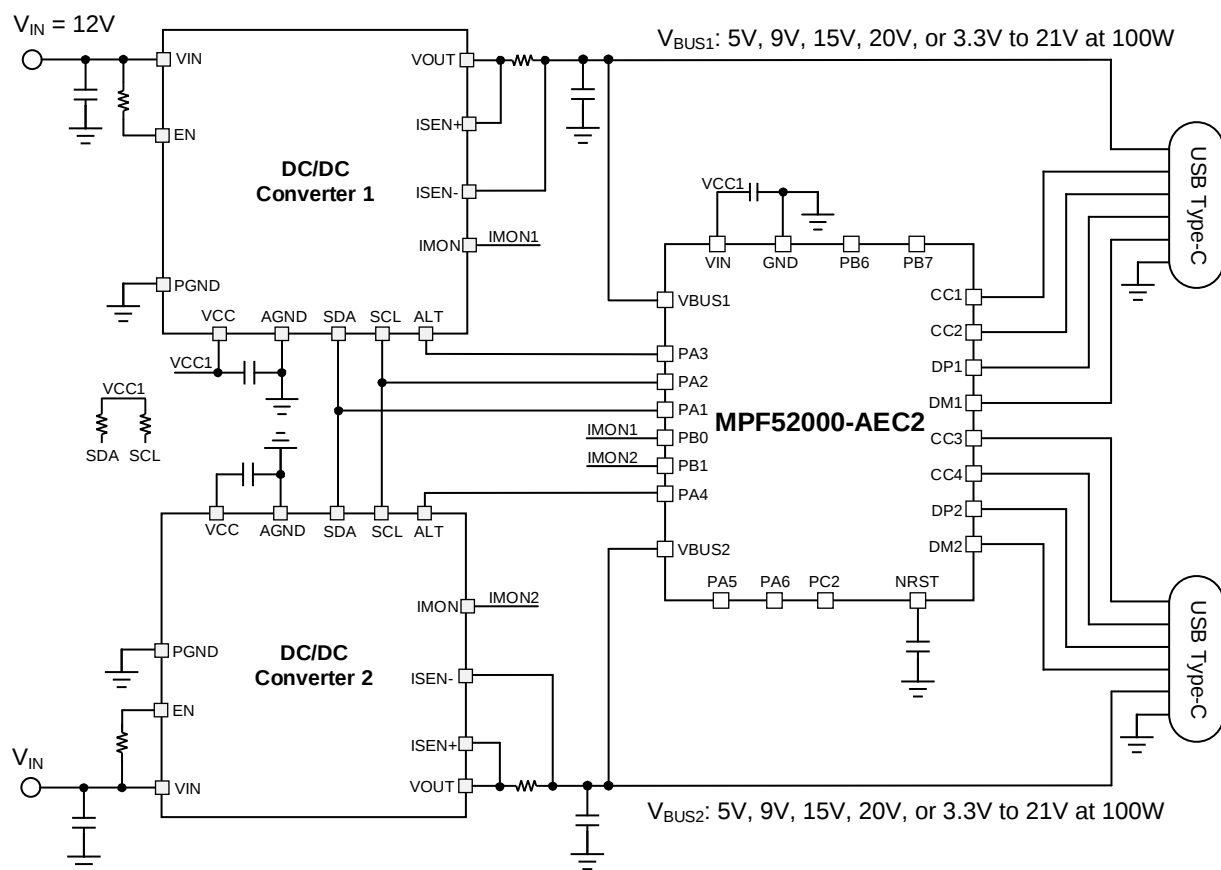
- Dual USB PD Controller for Source Port
 - Complies with USB PD3.1 with PPS, USB Type-C 2.1, and TCPC 2.0 Supporting Firmware Update
 - Passed USB PD3.1 Certification Test with PPS (TID: 8467)
 - Supports USB PD Alternate Mode for Display Port
 - Integrated V_{CONN} Power Switch and Over-Current Protection (OCP)
 - Dynamic Power Sharing Function
 - Load-Shedding Function at High Temperature or Low Battery Voltage
- Other Charging Protocols:
 - Supports Qualcomm Quick Charge 3/4/4+
 - Legacy Charging Protocol Supports BC1.2, Apple 3A Divider Mode, Huawei FCP/SCP, and UFCS
- 32-Bit ARM Cortex-M0 Microcontroller
 - Integrated 12MHz and 8kHz RC Oscillator
 - 128kB Flash with ECC, 12kB SRAM and 4kB ROM
 - Three 16-Bit Timers with PWM Function
 - 12-Bit Analog-to-Digital Converter (ADC)
 - Watchdog Timer (WDT)
 - UART and Serial Wire Debug (SWD)
 - Two I²C Master/Slave Interfaces
- Protections:
 - High-Voltage CCx/DP/DM I/O and Short-to-Battery/VBUS/GND Protection
 - Thermal Shutdown Protection
- Available in a QFN-24 (4mmx4mm) Package
- Available in AEC-Q100 Grade 2

APPLICATIONS

- USB Power Delivery Charging Ports
- USB Power Delivery Hubs

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TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPF52000GRE-0000-AEC2	QFN-24 (4mmx4mm)	See Below	1
MPF52000GRE-0001-AEC2			
MPF52000GRE-xxxx-AEC2**			
EVKT-MPF52000-AEC2	Evaluation kit	-	-

* For Tape & Reel, add suffix -Z (e.g. MPF52000GRE-xxxx-AEC2-Z).

** “xxxx” is the configuration code identifier for the register setting stored in the flash. Each “x” can be a hexadecimal value between 0 and F. “0000” is the default configuration code supporting 60W for a single port without power sharing. “0001” is the standard code supporting 120W of total shared power and 100W for a single port. The firmware can be updated multiple times with the PDFU communication interface.

TOP MARKING

MPSYWW
M52000
LLLLLL
E

MPS: MPS prefix

Y: Year code

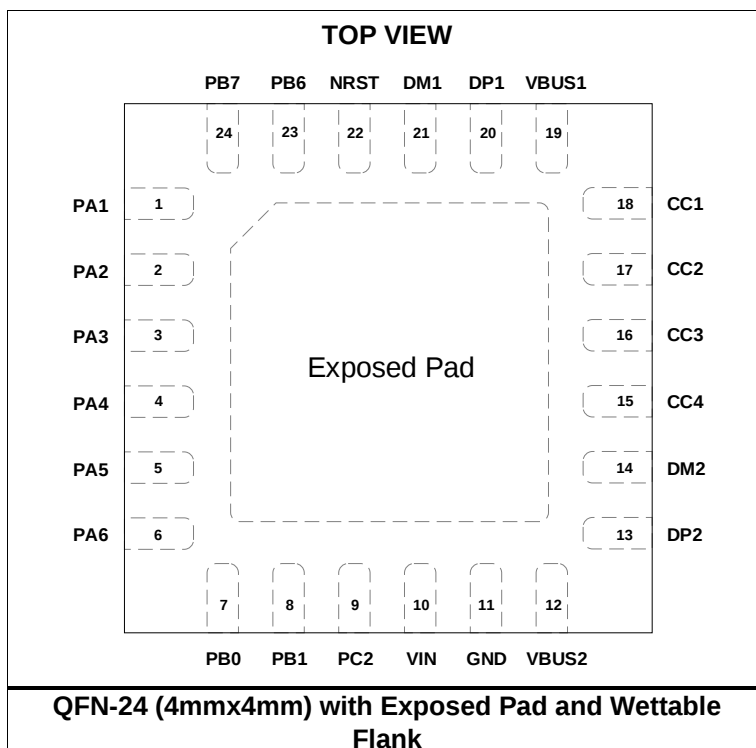
WW: Week code

M52000: Product code of MPF52000GRE-AEC2-Z

LLLLLL: Lot number

E: Wettable flank package

PACKAGE REFERENCE



EVALUATION KIT (EVKT-MPF52000-AEC2)

EVKT-MPF52000-AEC2 kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EVF52000-4263-R-00B	EVF52000-4263-R-00B evaluation board	1
2	PDFU-RE-00A	PDFU communication interface	1
3	MPF52000GRE-0001-AEC2	Supports 120W total shared power and 100W for single port	2

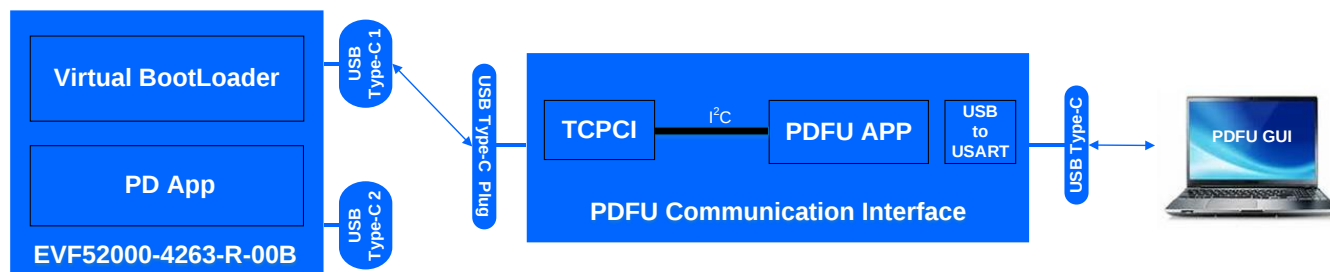


Figure 1: EVKT-MPF52000-AEC2 Connection

PIN FUNCTIONS

Pin #	Name	I/O	Description	Default Status
1	PA1	Bidirectional	Multi-functional pin. <u>Default:</u> PA1 (general-purpose input and output) <u>Alternate:</u> I2C0_SDA (I2C0 data), and TIMER16_CH0 (TIMER16 channel 0)	Low
2	PA2	Bidirectional	Multi-functional pin. <u>Default:</u> PA2 (general-purpose input and output) <u>Alternate:</u> I2C0_SCL (I2C0 clock), TIMER16_CH1 (TIMER16 channel 1), and ADC_IN1 (ADC channel 1 input)	Hi-Z
3	PA3	Bidirectional	Multi-functional pin. During start-up, PA3 must be floated or pulled high. <u>Default:</u> BOOT0. The BOOT0 and BOOT1 voltages can set different boot modes. <u>Alternate:</u> PA3 (general-purpose input and output), I2C1_SDA (I2C1 data), and TIMER18_CH0 (TIMER18 channel 0)	-
4	PA4	Bidirectional	Multi-functional pin. During start-up, PA4 must be floated or pulled high. <u>Default:</u> BOOT1. The BOOT0 and BOOT1 voltages can set different boot modes. <u>Alternate:</u> PA4 (general-purpose input and output), I2C1_SCL (I2C1 clock), and TIMER18_CH1 (TIMER18 channel 1)	-
5	PA5	Bidirectional	Multi-functional pin. <u>Default:</u> PA5 (general-purpose input and output) <u>Alternate:</u> ADC_IN2 (ADC channel 2 input), CLK_OUT (internal clock output function), I2C0_SDA (I2C0 data), TIMER17_CH0 (TIMER17 channel 0), and UART_TX (UART transmit data)	Hi-Z
6	PA6	Bidirectional	Multi-functional pin. <u>Default:</u> PA6 (general-purpose input and output) <u>Alternate:</u> ADC_IN3 (ADC channel 3 input), I2C0_SCL (I2C0 clock), TIMER17_CH1 (TIMER17 channel 1), and UART_RX (UART receive data)	Hi-Z
7	PB0	Bidirectional	Multi-functional pin. <u>Default:</u> PB0 (general-purpose input and output) <u>Alternate:</u> UART_TX (UART transmit data), I2C1_SDA (I2C1 data), ADC_IN6 (ADC channel 6 input), and TIMER16_CH0 (TIMER16 channel 0)	Hi-Z
8	PB1	Bidirectional	Multi-functional pin. <u>Default:</u> PB1 (general-purpose input and output) <u>Alternate:</u> UART_RX (UART receive data), I2C1_SCL (I2C1 clock), ADC_IN7 (ADC channel 7 input), and TIMER16_CH1 (TIMER16 channel 1)	Hi-Z
9	PC2	Bidirectional	Multi-functional pin. <u>Default:</u> PC2 (general-purpose input and output) <u>Alternate:</u> UART_TX (UART transmit data), and ADC_IN8 (ADC channel 8 input)	Hi-Z

PIN FUNCTIONS *(continued)*

Pin #	Name	I/O	Description	Default Status
10	VIN	Power	5V power supply for all internal circuitry. The MPF52000-AEC2 operates from a 4.6V to 5.5V input voltage (V_{IN}). A 0.47 μ F to 4.7 μ F ceramic input capacitor (C_{IN}) must supply the internal circuitry.	-
11	GND	Ground	Ground.	-
12	VBUS2	Power	Bus voltage sensing and discharge pin of USB Type-C port 2.	-
13	DP2	Bidirectional	D+ data line to USB Type-C port 2. The DP and DM pins are the input/output used for handshaking with portable devices.	-
14	DM2	Bidirectional	D- data line to USB Type-C port 2. The DP and DM pins are the input/output used for handshaking with portable devices.	-
15	CC4	Bidirectional	Configuration channel (CC). CC4 is used for the discovery, configuration, and management of connections across a USB Type-C cable.	-
16	CC3	Bidirectional	Configuration channel (CC). CC3 is used for the discovery, configuration, and management of connections across a USB Type-C cable.	-
17	CC2	Bidirectional	Configuration channel (CC). CC2 is used for the discovery, configuration, and management of connections across a USB Type-C cable.	-
18	CC1	Bidirectional	Configuration channel (CC). CC1 is used for the discovery, configuration, and management of connections across a USB Type-C cable.	-
19	VBUS1	Power	Bus voltage sensing and discharge pin of USB Type-C port 1.	-
20	DP1	Bidirectional	D+ data line to USB Type-C port 1. The DP and DM pins are the input/output used for handshaking with portable devices.	-
21	DM1	Bidirectional	D- data line to USB Type-C port 1. The DP and DM pins are the input/output used for handshaking with portable devices.	-
22	NRST	Input	External reset pin. Pull the NRST pin low to reset the microcontroller (MCU); pull it high to enable the MCU. In typical applications, it is recommended to connect a 100nF capacitor from NRST to GND. NRST is connected to VIN with an internal, 10k Ω pull-up resistor.	-
23	PB6	Bidirectional	Multi-functional pin. <u>Default:</u> SWDIO (serial write data input and output) <u>Alternate:</u> PB6 (general-purpose input and output), and I2C1_SCL (I2C1 clock)	High
24	PB7	Bidirectional	Multi-functional pin. <u>Default:</u> SWCLK (serial wire clock) <u>Alternate:</u> PB7 (general-purpose input and output), and I2C1_SDA (I2C1 data)	Low
Exposed pad	-	-	Exposed pad. Connect the exposed pad to ground when designing the PCB layout.	-

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Supply voltage (V_{IN})	-0.3V to +6V
VBUS1, VBUS2, DP1, DP2, DM1, DM2	-0.3V to +22.5V
CC1~CC4	-0.3V to +21V
All other pins	-0.3V to +6V
Continuous power dissipation ($T_A = 25^{\circ}\text{C}$)	
QFN-24 (4mmx4mm) ^{(2) (4)}	3W
Junction temperature (T_J)	125°C
Lead temperature	260°C
Storage temperature	-65°C to +150°C

ESD Ratings ⁽³⁾

Human body model (HBM)	±2000V
Charged-device model (CDM)	±750V

Recommended Operating Conditions

Supply voltage (V_{IN})	5V
Supply current (I_{IN})	60mA
Operating junction temp (T_J)	-40°C to +125°C

Thermal Resistance ⁽⁴⁾	θ_{JA}	θ_{JC}
QFN-24 (4mmx4mm)	33.8	39... °C/W

Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA} , and the ambient temperature, T_A . The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = $(T_J$ (MAX) - T_A) / θ_{JA} . Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- HBM, per the JEDEC specification JESD22-A114; CDM, per the JEDEC specification JESD22-C101, and the AEC specification AECQ100-011. The JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that a 250V CDM allows safe manufacturing with a standard ESD control process.
- Measured on a JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

$V_{IN} = 5V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$, typical value is tested at $T_J = 25^{\circ}C$, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (deep sleep)	$I_{DSL P}$	V_{IN} current, 36MHz clock is off, 8kHz clock is on		150		μA
Supply current (on)	I_{ON}	V_{IN} current, 36MHz clock is on, 8kHz clock is on, $T_J = 25^{\circ}C$		15	20	mA
Supply current (IDDQ) ⁽⁵⁾	I_{DDQ}			7		μA
Thermal shutdown ⁽⁵⁾	T_{OTP_R}			150		$^{\circ}C$
Thermal hysteresis ⁽⁵⁾	T_{OTP_HYS}			20		$^{\circ}C$
1.5V LDO regulator	V_{DD}		-5%	+1.5	+5%	V
1.5V LDO load regulation ⁽⁵⁾	V_{DD_REG}	$I_{LOAD} = 30mA$		5		%
Input voltage (V_{IN}) under-voltage lockout (UVLO) rising threshold	V_{CC_RS}		3.6	4.2	4.58	V
V_{IN} UVLO hysteresis	V_{CC_HYS}			600		mV
Clock Frequency						
IRC12M oscillator frequency accuracy, factory-trimmed	f_{IRC12M}		-4%	12	+4%	MHz
IRC12M oscillator duty cycle ⁽⁵⁾	D_{IRC12M}		45	50	55	%
IRC12M oscillator start-up time ⁽⁵⁾	$t_{SUIRC12M}$				2	μs
Low-speed internal oscillator (IRC8K) frequency	f_{IRC8K}			8		kHz
IRC8K oscillator start-up time ⁽⁵⁾	t_{IRC8K}				50	μs
PLL output clock frequency ⁽⁵⁾	f_{PLLOUT}		-5%	144	+5%	MHz
PLL lock time ⁽⁵⁾	t_{LOCK}				200	μs
Timer						
TIMER resolution time ⁽⁵⁾	t_{RES}	36MHz operation frequency		27.8		ns
TIMER resolution ⁽⁵⁾	RES			16		bit
Counter period ⁽⁵⁾	$t_{COUNTER}$		1		65536	t_{CLK}
PWM output accuracy	ACC _{PWM}	FREQ = 1MHz	-5		+5	%
WDGT						
Timeout	$t_{TIMEOUT}$	32-bit counter, set system clock prescaler to 1 (range is between 1 and 255), clock = 8kHz		125		μs
Flash Memory						
Number of guaranteed program / erase flash cycles ⁽⁵⁾	N_{CYCLE}		100,000			cycles
Data retention time ⁽⁵⁾	t_{DR}	$T_J = 25^{\circ}C$	100			years
	$t_{DR_HI_TEMP}$	$T_J = 125^{\circ}C$	10			years

ELECTRICAL CHARACTERISTICS (continued)

$V_{IN} = 5V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$, typical value is tested at $T_J = 25^{\circ}C$, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Byte program time ⁽⁵⁾	t_{PROG}		6		7.5	μs
Sector erase time ⁽⁵⁾	t_{SE}		4		5	ms
Chip erase time ⁽⁵⁾	t_{CE}		30		40	ms
Analog-to-Digital Converter (ADC)						
ADC positive reference voltage	V_{REF+}	$T_J = 25^{\circ}C$	-0.5%	+3.3	+0.5%	V
ADC negative reference voltage	V_{REF-}			0		V
ADC sampling rate	f_{ADC_SR}	12-bit	257		571	kSPS
ADC input voltage range	V_{ADC}		0		3.3	V
ADC clock ⁽⁵⁾	f_{ADC}			28.8		MHz
Total conversation time ⁽⁵⁾	t_{CON}				14	$1/f_{ADC}$
Start-up time ⁽⁵⁾	t_{SU}				5	μs
Total unadjusted error	L_{TUE}	$T_J = 25^{\circ}C$	-16		+16	LSB
NRST Pin						
NRST internal pull-up resistor	R_{NRST}			10		k Ω
NRST input low voltage	V_{NRST_L}				1	V
NRST input high voltage	V_{NRST_H}		3.5			V
GPIO						
Standard I/O input low level threshold	V_{IL}				$0.3 \times V_{IN}$	V
Standard I/O input high level threshold	V_{IH}		$0.6 \times V_{IN}$			V
Standard I/O output low level threshold	V_{OL}	$I_{IO} = 16mA$ or $8mA$			0.5	V
Standard I/O output high level threshold	V_{OH}	$I_{IO} = 16mA$ or $8mA$	$V_{IN} - 0.8$			V
Pull-up/pull-down resistance ⁽⁵⁾	$R_{UP/DOWN}$		20		100	k Ω
I/O input capacitance ⁽⁵⁾	C_{IN}				10	pF
Leakage	I_{LKG}				1	μA
I²C Slave						
Input logic high	V_{IL}		$0.6 \times V_{IN}$			V
Input logic low	V_{IH}				$0.3 \times V_{IN}$	V
Output voltage logic low	V_{OUT_L}				0.6	V
SCL clock frequency	f_{SCL}		100	400	1000	kHz
SCL high time ⁽⁵⁾	t_{HIGH}		260			ns
SCL low time ⁽⁵⁾	t_{LOW}		500			ns
Data set-up time ⁽⁵⁾	t_{SU_DAT}		50			ns

ELECTRICAL CHARACTERISTICS (continued)

$V_{IN} = 5V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$, typical value is tested at $T_J = 25^{\circ}C$, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Set-up time for repeated start (5)	t_{SU_STA}		260			ns
Hold time for (repeated) start (5)	t_{HD_STA}		260			ns
Bus free time between a start and a stop command (5)	t_{BUF}		500			ns
Set-up time for stop command (5)	t_{SU_STO}		260			ns
Rising time of SCL and SDA(5)	t_R				120	ns
Falling time of SCL and SDA(5)	t_F				120	ns
Capacitance for each bus line (5)	C_B				400	pF
UART						
Baud	f_{CLK}				115200	bps
VBUS Voltage (V_{BUS})						
Standard power range (SPR) V_{BUS} under-voltage (UV) falling threshold	V_{BUS_UV1}	$VBUS_UV_THLD = 0001b$	-5%	+2.97	+5%	V
		$VBUS_UV_THLD = 0011b$	-2.5%	+4.75	+2.5%	
		$VBUS_UV_THLD = 0111b$	-2.5%	+19	+2.5%	
SPR V_{BUS} over-voltage (OV) rising threshold	$V_{BUS_OV_R1}$	$VBUS_OV_THLD = 0001b$	-2.5%	+6	+2.5%	V
		$VBUS_OV_THLD = 1000b$	22	23	24	
SPR V_{BUS} OV falling threshold	$V_{BUS_OV_F1}$	$VBUS_OV_THLD = 0001b$	-2.5%	5.5	+2.5%	V
		$VBUS_OV_THLD = 1000b$	21	22	23	
SPR V_{BUS} present falling threshold	V_{BUS_PRES}		-5%	+3.5	+5%	V
Extended power range (EPR) V_{BUS} UV falling threshold	V_{BUS_UV2}	$VBUS_UV_THLD = 1000b$	-5%	+13.5	+5%	V
		$VBUS_UV_THLD = 1001b$	-2.5%	+26.6	+2.5%	V
EPR V_{BUS} OV falling threshold	$V_{BUS_OV_R2}$	$VBUS_OV_THLD = 1001b$	-2.5%	+32.5	+2.5%	V
EPR V_{BUS} OV falling threshold	$V_{BUS_OV_F2}$	$VBUS_OV_THLD = 1001b$	-2.5%	+30.6	+2.5%	V
VBUS force discharge resistor	R_{FORCE_DISC}			600		Ω
BC1.2 Dedicated Charging Port (DCP) Mode						
DP and DM short resistance	$R_{DP_DM_SHORT}$	$V_{DP} = 0.8V$, $I_{DM} = 1mA$		120	200	Ω
Divider Mode						
DP output voltage	$V_{DIVIDER_DP}$	$V_{OUT} = 5V$	2.55	2.7	2.8	V
DM output voltage	$V_{DIVIDER_DM}$	$V_{OUT} = 5V$	3.15	3.3	3.45	V
DP output impedance	$R_{DIVIDER_DP}$		20	25	30	k Ω

ELECTRICAL CHARACTERISTICS (continued)

$V_{IN} = 5V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$, typical value is tested at $T_J = 25^{\circ}C$, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
1.2V/1.2V Mode						
DP/DM output voltage	$V_{DP_DM_1.2V}$	$V_{OUT} = 5V$	1.12	1.20	1.28	V
DP/DM output impedance	$R_{DP_DM_1.2V}$			230		k Ω
Quick Charge (QC) 3.0 Mode						
DP/DM low voltage	V_{QC_LOW}		0.25	0.3	0.4	V
DP/DM high voltage	V_{QC_HIGH}		1.8	2	2.2	V
DP output impedance	R_{DP_QC}		300	400	1500	k Ω
DM output impedance	R_{DM_QC}			20		k Ω
DM low glitch time ⁽⁵⁾	t_{GLITCH_DM}			10		ms
DP high glitch time ⁽⁵⁾	t_{GLITCH_DP}		1000		1500	ms
Output voltage change glitch time ⁽⁵⁾	$t_{GLITCH_V_CHANGE}$		20	40	60	ms
Bus voltage step ⁽⁵⁾	$V_{BUS_CONT_STEP}$		150	200	250	mV
Time for VBUS to discharge to 5V when DP < 0.6V ⁽⁵⁾	t_{V_UNPLUG}				500	ms
FCP Mode						
DP/DM Tx high voltage	V_{TX_H}	$R_{LOAD} = 15k\Omega$	2.55		5	V
DP/DM Tx low voltage	V_{TX_L}	$R_{LOAD} = 15k\Omega$			0.4	V
DP/DM Rx high voltage	V_{RX_H}		1.5		5	V
DP/DM Rx low voltage	V_{RX_L}				1	V
DM pull-low resistance	R_{LD_D-}		12	15	18	k Ω
FCP unit interval of PHY ⁽⁵⁾	t_{UI_FCP}	$f_{CLK} = 125kHz$	144	160	176	μs
USB Type-C – Source Mode						
CC pull-up current 1	I_{RP1}	$V_{BUS} = 5V$ at 3A	-8%	+330	+8%	μA
CC pull-up current 2	I_{RP2}	$V_{BUS} = 5V$ at 1.5A	-8%	+180	+8%	μA
CC voltage to enable VCONN for 3A USB Type-C mode	V_{RA1}				0.75	V
CC voltage to enable VBUS for 3A USB Type-C mode	V_{RD1}		0.85		2.45	V
CC detached threshold for 3A Type-C mode	V_{OPEN1}		2.75			V
CC voltage to enable VCONN for 1.5A USB Type-C mode	V_{RA2}				0.35	V
CC voltage to enable VBUS for 1.5A USB Type-C mode	V_{RD2}		0.45		1.5	V
CC detach threshold for 1.5A USB Type-C mode	V_{OPEN2}		1.65			V
VCONN output power	P_{VCONN}	V_{IN} supplies VCONN, $T_J = 25^{\circ}C$	100			mW
VCONN present voltage falling threshold	V_{VCONN_F}		2.28	2.4	2.52	V
VCONN present voltage rising threshold	V_{VCONN_R}	$V_{CONN_PRESENT} = 1b$	2.375	2.5	2.625	V

ELECTRICAL CHARACTERISTICS *(continued)*

$V_{IN} = 5V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$, typical value is tested at $T_J = 25^{\circ}C$, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
USB Type-C Port Controller (TCPC)						
Unit interval ⁽⁵⁾	t_{UI}		3		3.7	μs
Transmitter						
End drive BMC ⁽⁵⁾	t_{EDBMC}				23	μs
Falling time ⁽⁵⁾	t_{FALL}		300			ns
Rising time ⁽⁵⁾	t_{RISE}		300			ns
Hold low BMC ⁽⁵⁾	t_{HLBMC}		1			μs
Logic high voltage	V_{LH}		1.05		1.2	V
Logic low voltage	V_{LL}				70	mV
Output impedance ⁽⁵⁾	R_{TX}		33		75	Ω
Receiver						
CC receiver capacitance ⁽⁵⁾	$C_{RECEIVER}$				600	pF
Transitions for signal detection ⁽⁵⁾	$N_{TRANSITION}$		3			edges
Rx bandwidth limiting filter ⁽⁵⁾	t_{RX_FILTER}		100			ns
Time window for detecting non-idle ⁽⁵⁾	$t_{TRANSITION_WINDOW}$		12		20	μs
Receiver input impedance ⁽⁵⁾	R_{BMC_RX}		1			M Ω

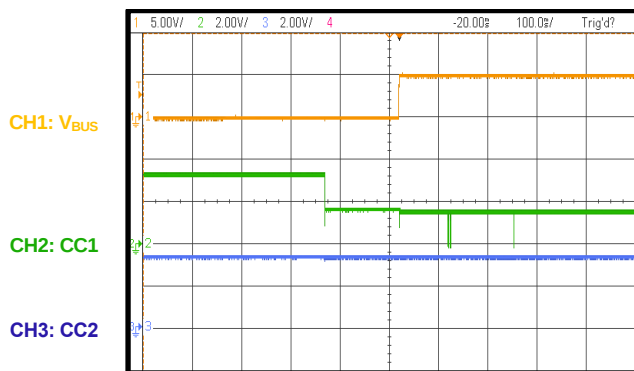
Notes:

5) Guaranteed by engineering sample characterization.

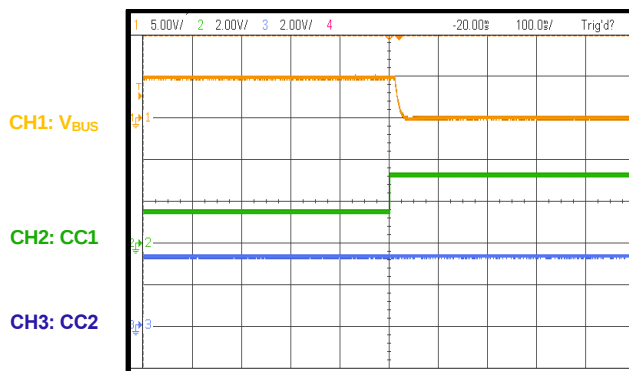
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN_SYS} (DC/DC converter's V_{IN}) = 12V, MPF52000-AEC2 is supplied by an MPS DC/DC converter's VCC, V_{BUS} = 3.3V to 21V, T_A = 25°C, unless otherwise noted.

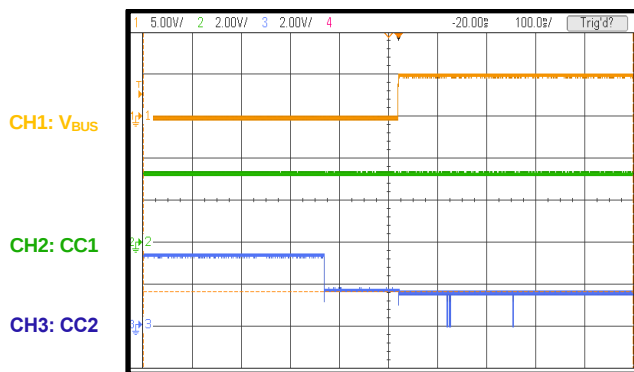
CC1 Attached Rd to Enable VBUS



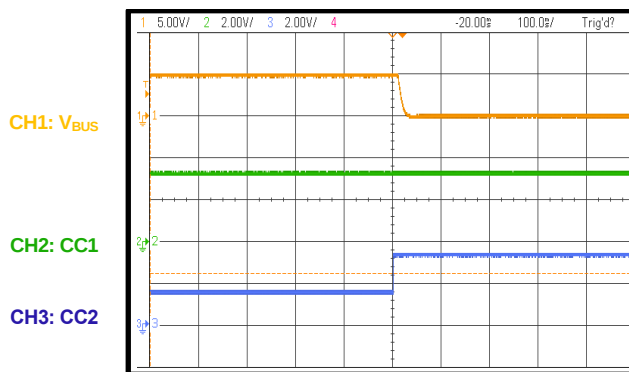
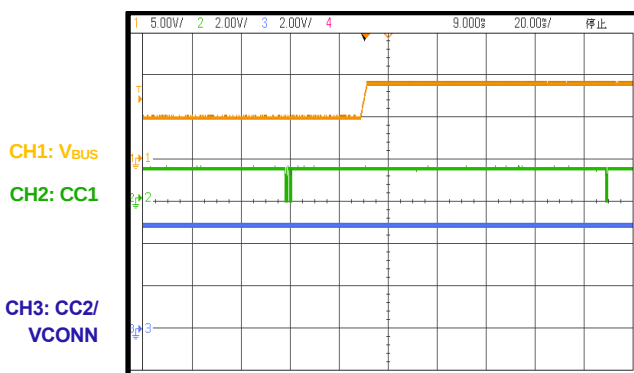
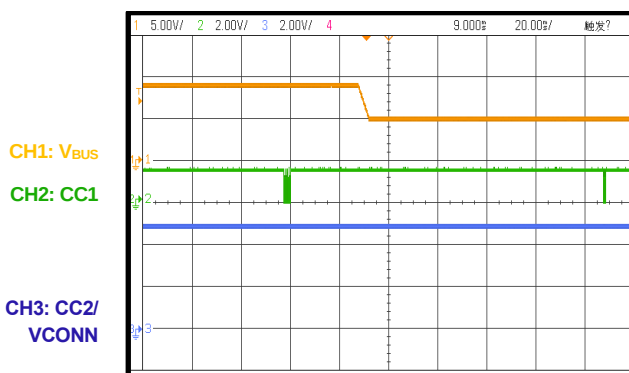
CC1 Detached Rd to Disable VBUS



CC2 Attached Rd to Enable VBUS



CC2 Detached Rd to Disable VBUS

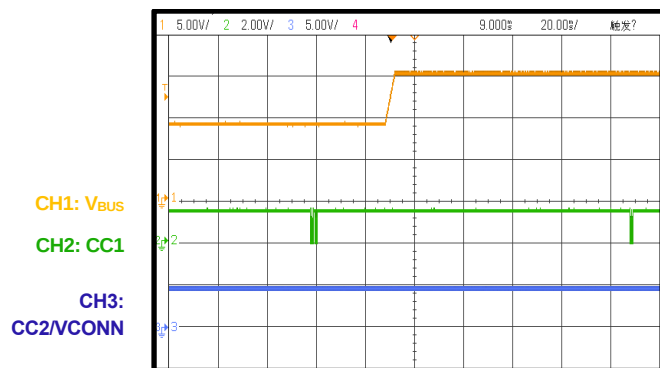

PDO Transition
5V PDO to 9V PDO

PDO Transition
9V PDO to 5V PDO


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN_SYS} (DC/DC converter's V_{IN}) = 12V, MPF52000-AEC2 is supplied by an MPS DC/DC converter's VCC, V_{BUS} = 3.3V to 21V, T_A = 25°C, unless otherwise noted.

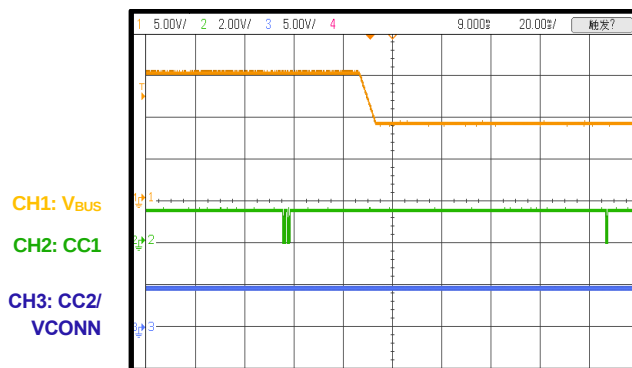
PDO Transition

9V PDO to 15V PDO



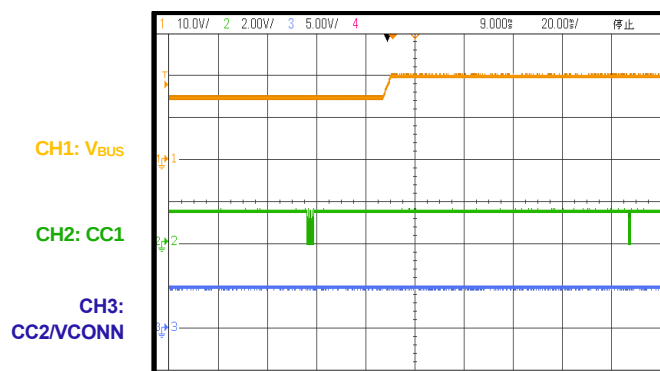
PDO Transition

15V PDO to 9V PDO



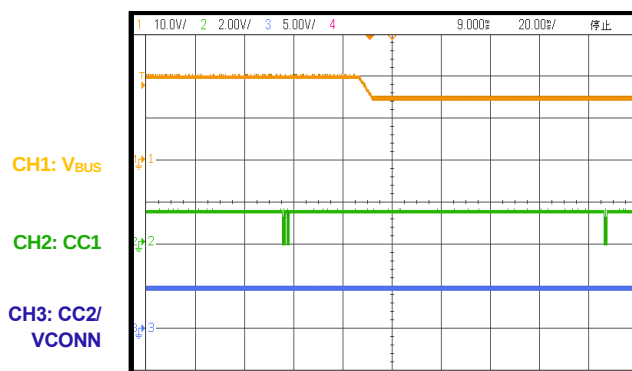
PDO Transition

15V PDO to 20V PDO



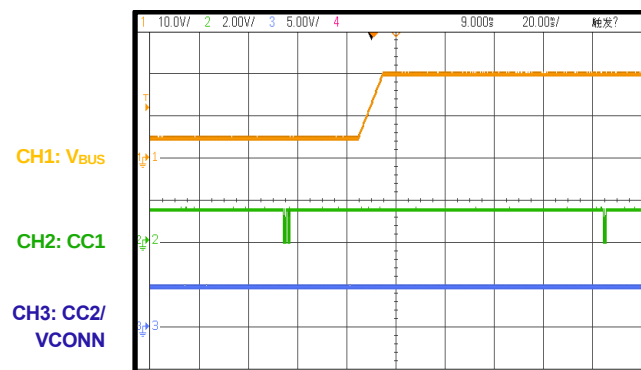
PDO Transition

20V PDO to 15V PDO



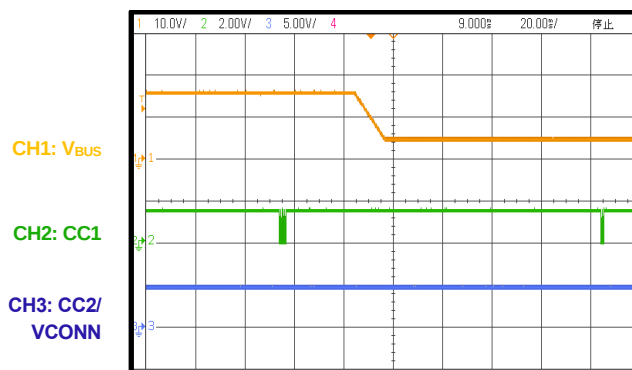
PDO Transition

5V PDO to 20V PDO



PDO Transition

20V PDO to 5V PDO

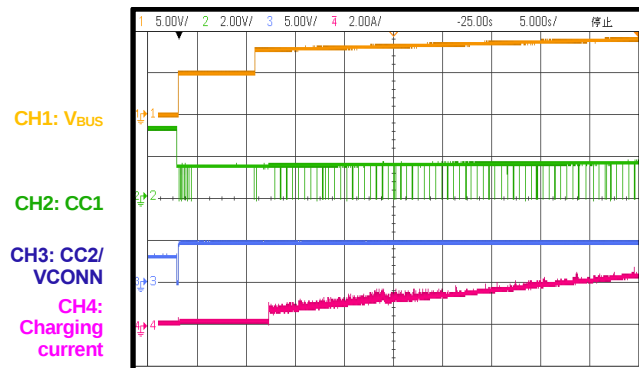


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN_SYS} (DC/DC converter's V_{IN}) = 12V, MPF52000-AEC2 is supplied by an MPS DC/DC converter's VCC, V_{BUS} = 3.3V to 21V, T_A = 25°C, unless otherwise noted.

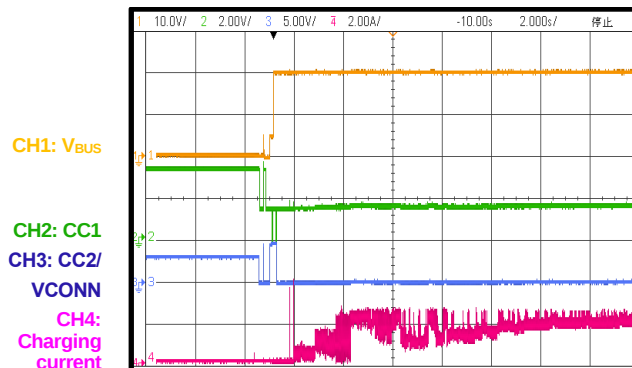
Mobile Phone Charging Test

Phone requests 3.3V to 21V APDO



Laptop Charging Test

Laptop requests 20V PDO



FUNCTIONAL BLOCK DIAGRAM

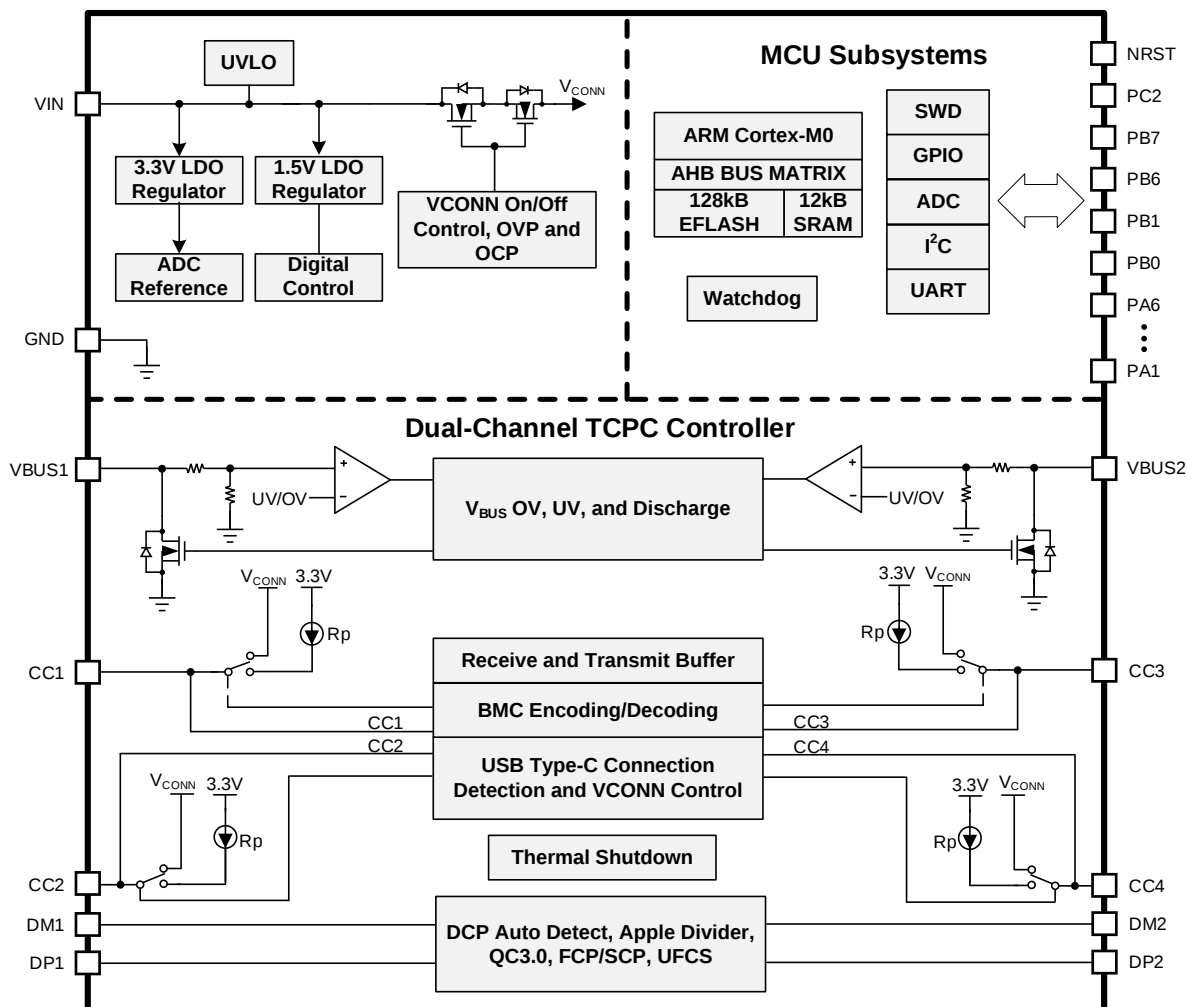


Figure 2: Functional Block Diagram

OPERATION

V_{IN} Under-Voltage Lockout (UVLO)

The MPF52000-AEC2 operates from a 4.6V to 5.5V power supply. The VIN pin is the power supply input pin, and it is biased by an external DC/DC converter's low-dropout (LDO) output. Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MPF52000-AEC2's UVLO comparator monitors the VIN input voltage (V_{IN}). The UVLO rising threshold is 4.2V, and the falling threshold is 3.6V. The VIN pin should have a 0.47μF to 4.7μF decoupling capacitor.

3.3V and 1.5V Regulator

The 3.3V internal regulator uses V_{IN} as the input. It is used as the analog-to-digital converter (ADC) reference voltage.

The 1.5V internal regulator uses V_{IN} as the input. It supplies power to the internal digital circuitry, including the microcontroller (MCU) and flash.

MICROCONTROLLER (MCU)

ARM Cortex-M0 Core

The Arm Cortex-M0 processor is 32 bits and developed to provide a low-cost, low-power consumption platform that offers high performance and meets the application requirement. The M0 processor can operate the Thumb command and is compliant with other Cortex M series processors.

The MPF52000-AEC2's integrated Arm Cortex-M0 processor features one nested, vectored interrupt controller (NVIC), AHB-lite bus interface, and debug access port (DAP). The Arm Cortex-M0 processor has an operating frequency up to 36MHz and can achieve a fast response associated with different peripherals.

Boot Modes

When V_{IN} exceeds its UVLO threshold and NRST is enabled, the MPF52000-AEC2 starts up and runs the boot codes in the ROM. Different BOOT0 and BOOT1 voltages can set different boot modes. These two pins have a one-shot, 40kΩ, internal pull-up resistor during start-up. When using PA3_BOOT0 and PA4_BOOT1 as general-purpose input/output (GPIO) pins or for other functions, the two pins' initial states cannot be pulled low during start-up; otherwise MCU will

falsely enter a different boot mode. The boot modes are defined below:

- If BOOT0 = BOOT1 = 1, boot from the main flash memory (default).
- If BOOT0 = 0 and BOOT1 = 1, boot from the ROM, then configure the flash memory by using UART on the PA5 and PA6 pins.

Embedded Memory

The MPF52000-AEC2 supports up to 128kB of embedded Flash memory, 4kB of ROM, and 12kB of SRAM memory. It provides sufficient storage to store the configurations, boot loader, and data. Table 1 shows the memory map address.

Table 1: Memory Map Address

Item	Address	Size
ROM	0x0000_0000~0x0000_27FF	4kB
RAM	0x2000_0000~0x2000_2FFF	12kB
SYSCON FIG	0x4000_0000~0x4000_0FFF	4kB
IOCONFI G	0x4000_1000~0x4000_17FF	2kB
UART	0x4000_3000~0x4000_37FF	2kB
I2C0	0x4000_4000~0x4000_47FF	2kB
I2C1	0x4000_6000~0x4000_67FF	2kB
ADC	0x4000_8000~0x4000_87FF	2kB
TIM16	0x4000_B800~0x4000_BFFF	2kB
TIM17	0x4000_C000~0x4000_C7FF	2kB
TIM18	0x4000_C800~0x4000_CFFF	2kB
EFLASH Control	0x4000_D000~0x4000_D7FF	2kB
WATCHD OG	0x4000_E000~0x4000_E7FF	2kB
GPIO	0x4002_0000~0x4002_FFFF	64kB
EFLASH_ REMAP	0x2200_0000~0x2201_FFFF	128kB

System Clock

The MPF52000-AEC2 integrates two basic oscillator circuits to provide 12MHz and 8kHz IRC clock sources. The 12MHz oscillator is selected as the default CPU for clock-on reset. The 12MHz clock can be used as the input clock of PLL. The maximum PLL clock output is up to 144MHz. The PLL clock can be used by the MCU and other peripherals, but the maximum operation frequency should be limited.

The internal 8kHz clock is always enabled, but the 12MHz and PLL clock can be disabled in deep sleep mode for the lowest power consumption.

There are different clock prescalers that can be configured to operate the frequency of the ADC, PWM, watchdog, and advanced high-performance bus (AHB) domains. Table 2 shows the maximum prescaler values.

Table 2: Clock Source Prescaler Value

Name	Bit Size	Maximum Value in Decimal
AHBCLKDIV	4-Bit	15
PWMCLKDIV	8-Bit	255
SYSTICKCLKDIV	8-Bit	255
WDTCLKDIV	8-Bit	255
OUTCLKDIV	8-Bit	255

The CPU, AHB, and advanced peripheral bus (APB) share the same clock domains, and the maximum frequency is 36MHz. Each I²C, timer, and UART has its own prescaler based on the APB clock. OUTCLKDIV is the prescaler of the PA5 clock-out function. After setting CLKOUT_EN equal to 1, the clock is output through the PA5 pin if the PA5 pin is configured for the CLK_OUT function (see Figure 3).

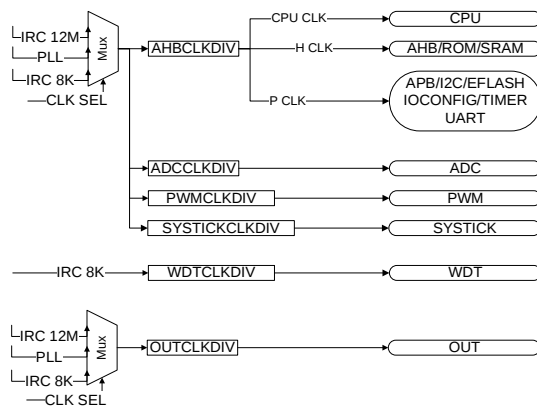


Figure 3: Clock Tree

Deep Sleep Mode

In deep sleep mode, the IRC 12MHz and PLL are disabled, which means that only the 8kHz clock is enabled. This function achieves very low power consumption while retaining the contents of the SRAM and registers. The device can be woken up by the watchdog or a USB Type-C attach interrupt.

When the MPF52000-AEC2 is woken up by a watchdog, there are two modes that can be selected. When WDRESET = 0, the CPU recovers to its previous state and continues running; when WDRESET = 1, the CPU is reset, then reloads the program and starts operating again.

User Configuration Protection

To prevent the MCU flash content from being read and rewritten, the MPF52000-AEC2 provides read/write protection. This protection disables the serial wire debug (SWD) function in boot 1 mode and the serial port update function in boot 2 mode.

Analog-to-Digital Converter (ADC)

The MPF52000-AEC2 integrates one 12-bit, high-accuracy, multi-channel ADC. It supports up to 6 conversation channels. The 6 channels are multiplexed with the external GPIOx. The ADC reference voltage can be selected to 3.3V. Its input voltage is between 0V and 3.3V, and the maximum operation frequency is fixed to 28.8MHz.

An ADC interrupt can be triggered from the events generated by the internal, general timers (TIMER16_CH0 and CH1, then TIMER17_CH0 and TIMER18_CH0) and external signals (PA5, PA6, PB0, PB1, and PC2). The external signal trigger mode can be set as the rising edge, falling edge, and rising/falling edge.

The ADC can be configured for continuous trigger mode and single trigger mode. When the ADC is in continuous trigger mode, the 6 ADC converters (1 for each channel) must finish sequentially when this mode is triggered once. In single trigger mode, each ADC configured ADC channel is converted once when the signal is triggered.

General-Purpose Inputs and Outputs (GPIOs)

The MPF52000-AEC2 supports up to 11 multifunctional GPIO pins (PA1~PA6, PB0, PB1, PB6, PB7, and PC2). Each of the GPIO ports has its own control and configuration registers to meet different applications.

Each of the GPIO pins can be configured as pull-up, pull-down, push-pull and open-drain functions, or as peripheral alternate functions

(ADC, I2C, SWD, UART, and TIMER Input/Output).

See the Pin Functions section on page 5 for more details.

All GPIOs support external interrupt lines, but there are only 6 interrupt vectors that can be used for 11 GPIOs. This means that certain GPIOs must share the same interrupt vector, though they cannot be used at the same time (see Table 3).

The GPIO interrupt trigger mode can be set to rising edge, falling edge, rising/falling edge, high level, and low level.

General-Purpose Timers

The MPF52000-AEC2 supports three general-purpose timers: TIMER16 (CH0 and CH1), TIMER17 (CH0 and CH1), and TIMER18 (CH0 and CH1). The three timers feature 16-bit reload up/down counter, AHB clock domain, and 16-bit clock prescaler from 1 to 65536.

Each timer has two independent channels for input capturing, output comparing, PWM output, or single pulse generation.

Independent Watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 32-bit counter. It is clocked from an independent, 8kHz, internal clock. Because IWDG operates independently from the main clock, it can also operate in a deep sleep mode.

When the watchdog timer expires, IWDG generates a non-maskable interrupt. This interrupt cannot be masked.

Universal Asynchronous Receiver-Transmitter (UART)

The MPF52000-AEC2 embeds one universal, asynchronous receiver-transmitter (UART). The UART provides a flexible, full-duplex data exchange using asynchronous transfer. The working principle is to transmit each bit of the transmitted data bit by bit.

Serial Wire Debug Port (SWD)

The MPF52000-AEC2 integrates one serial wire debug port. The PB6 and PB7 default functions are SWDIO and SWCLK, respectively. They can be used for configuration debugging.

Extended Interrupt Controller (EXTI)

The MPF52000-AEC2 can handle up to 1 non-maskable interrupt and 17 external interrupts (see Table 3).

Each GPIOx interrupt can be independently configured to select the trigger event (high level, low level, rising edge, falling edge, or rising/falling edge) and can be masked independently.

Table 3: Interrupt Vector Description

EXTI Number	Interrupt Trigger Source	Description
0	EFLASH_IRQ	Flash ECC error interrupt
1	TIM16_IRQ	Timer 16 interrupt
2	TIM17_IRQ	Timer 17 interrupt
3	UART_IRQ	UART interrupt
4	I2C0_IRQ	I2C0 interrupt
5	I2C1_IRQ	I2C1 interrupt
6	TIM18_IRQ	Timer 18 interrupt
7	ADC_IRQ	ADC interrupt
8	BOD_IRQ	V _{IN} voltage is too low
9	PB0	GPIOx interrupt
10	PA1/PB1	
11	PA2/PC2	
12	PA3/PA4	
13	PA5/PA6	
14	PB6/PB7	
15	ATTACH1	Channel 1 sink is attached
16	ATTACH2	Channel 2 sink is attached

I²C Transfer Data

Every byte on the SDA line must be 8 bits long. Each byte has to be followed by an acknowledge bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable low during the high period of this clock pulse.

Figure 4 shows the data transfer format. After the start command (S), a slave address is sent. This address is 7 bits long, followed by an eighth bit, which is a data direction bit (R/W).

A 0 indicates a transmission (write), while a 1 indicates a request for data (read).

A data transfer is always terminated by a stop command (P), which is generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated start command (Sr) and address another slave without generating a stop command.

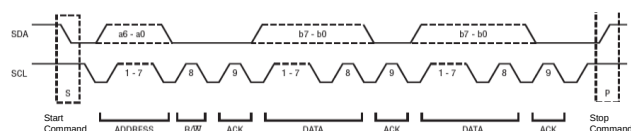


Figure 4: Complete Data Transfer

The MPF52000-AEC2 includes a full I²C slave controller. The I²C slave fully complies with the I²C specification requirements. It requires a start command, a valid I²C address, a register address byte, and a data byte for a single data update. After receiving each byte, the MPF52000-AEC2 acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MPF52000-AEC2. The MPF52000-AEC2 performs an update on the falling edge of the least significant byte.

Reset (NRST)

NRST is an active low pin. Pull the NRST pin low to reset the microcontroller (MCU); pull it high to enable the MCU. In typical applications, it is recommended to connect a 100nF capacitor from NRST to GND. NRST is connected to VIN with an internal 10kΩ pull-up resistor.

USB TYPE-C PORT CONTROLLER

Charging Mode Auto-Detection

Legacy USB 2.0 Mode

The MPF52000-AEC2 integrates a USB dedicated charging port (DCP) auto-detection function that can recognize most mainstream portable devices. It supports the following charging schemes:

- USB battery charging specification BC1.2/ Chinese Telecommunications Industry Standard YD/T 1591-2009

- Apple 3A divider mode
- 1.2V/1.2V mode
- QC3.0 Class A (3.3V to 12V)
- Huawei FCP and SCP
- UFCS

The auto-detection function is a state machine that supports all of the above DCP charging schemes, starting in divider mode. If a device compliant with divider mode is attached, the MPF52000-AEC2 remains in divider mode. Then 3.3V is applied to the DM pin, and 2.7V is applied to the DP pin.

If a device compliant with BC1.2 or YD/T 1591-2009 is attached, the MPF52000-AEC2 operates in 1.2V/1.2V and BC1.2 DCP mode. DM and DP are shorted together with a resistance below 200Ω. The MPF52000-AEC2 remains in that mode until the device releases the data line. Then the device returns to divider mode.

If a QC3.0 or FCP/SCP device (without PD protocol) is attached, the MPF52000-AEC2 enters high-voltage quick charge mode.

USB Type-C Port

The USB Type-C receptacle, plug, and cable solution incorporates a configuration process to detect a downstream-facing port (DFP) to upstream-facing port (UFP) connection for V_{BUS} management, and to determine the host-to-device relationship.

Initially, DFP-to-UFP attachment is detected by a host (DFP) when one of the CC pins at its USB Type-C receptacle senses a specific resistance to GND. Subsequently, UFP-to-DFP detachment is detected when the CC pin that was terminated at its USB Type-C receptacle is no longer connected to GND.

Power is not applied to the USB Type-C host or hub receptacle (V_{BUS} or V_{CONN}) until the DFP detects the presence of an attached device (UFP) port. When a DFP-to-UFP attachment is detected, the DFP enables power to the receptacle and begins normal USB operation with the attached device. When a DFP-to-UFP detachment is detected, the port sourcing V_{BUS} removes power.

The MPF52000-AEC2 is a DFP (provider only), and its power supply capability is rated at 5V/3A

by default. V_{CONN} is provided by the DFP to power the cables and electronics in the plug. V_{CONN} is provided instead of the CC pin if the CC pin is not connected to the cable's configuration channel (CC) wire. V_{CONN} has a maximum power output of 100mW.

V_{CONN} is disabled until R_A is detected. R_A is a pull-down resistor connected from the CC pin to GND, and its resistance should be below 1.2k Ω .

USB Power Delivery (PD)

In USB power delivery (PD), pairs of directly attached ports negotiate the voltage, current, and/or direction of power flow across the USB cable by using the CC wire as the communication channel. The mechanisms that are implemented operate independently of other USB methods that are used to negotiate power.

USB Type-C connectors can support the CC wire as the communication channel. The USB PD engine is disabled until a valid USB Type-C connection is established. Figure 5 shows a USB PD communication stack.

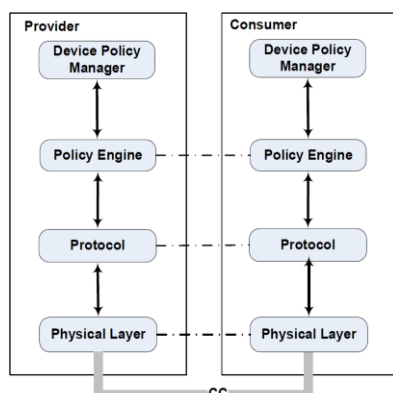


Figure 5: USB PD Communication Stack

PD Contract Handshake

Figure 6 shows the MPF52000-AEC2's PD contract handshake sequence.

#	CH	OS	Power	Data	Cable Plug	Type
0	CC2	SOP'			UFP or DFP	Vendor_Defined
1	CC2	SOP'			Cable Plug	GoodCRC
2	CC2	SOP'			Cable Plug	Vendor_Defined
3	CC2	SOP'			UFP or DFP	GoodCRC
4	CC2	SOP	Source	DFP		Source_Capabilities
5	CC2	SOP	Sink	UFP		GoodCRC
6	CC2	SOP	Sink	UFP		Request
7	CC2	SOP	Source	DFP		GoodCRC
8	CC2	SOP	Source	DFP		Accept
9	CC2	SOP	Sink	UFP		GoodCRC
10	CC2	SOP	Source	DFP		PS_RDY
11	CC2	SOP	Sink	UFP		GoodCRC

Figure 6: PD Contract Handshake

VBUS and VCONN Discharge

When the sink is detached or a hard reset occurs, the MPF52000-AEC2 sends a command to turn off the DC/DC converter's output voltage, and VBUS_P's 600 Ω discharge resistor turns on for 250ms. Meanwhile, the VCONN voltage is discharged with a 1k Ω resistor for 35ms.

V_{BUS} Over-Voltage Protection (OVP) and Under-Voltage Protection (UVP)

The MPF52000-AEC2 supports V_{BUS} over-voltage (OV) and under-voltage (UV) detection and reports the status to the status register. Then the MPF52000-AEC2 can disable the external DC/DC converter from switching, or the device can enter a hard reset state.

The blanking time for over-voltage protection (OVP) and under-voltage protection (UVP) can be set via the TCPC register. To support EPR mode, place a resistor divider with at least 1% tolerance at the VBUS pin and use GPIOx to control the discharge MOSFET (see Figure 7). If there is only SPR mode, the resistor divider is not required.

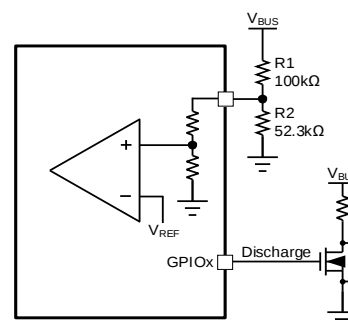


Figure 7: Resistor Divider and Discharge MOSFET for EPR Mode

Table 4 shows the potential V_{BUS} OVP thresholds.

Table 4: V_{BUS} OVP Thresholds

PDO Voltage	VBUS_OV Rising/Falling Threshold (V)	
	Only SPR Mode (R1 = 0Ω, R2 = NS)	EPR Mode (R1 = 100kΩ, R2 = 52.3kΩ)
5V fixed PDO	6/5.5	6/5.5
9V fixed PDO	10.8/9.9	10.8/9.9
12V fixed PDO	14.4/13.2	14.4/13.2
15V fixed PDO	18/16.5	18/16.5
5V prog.	7.08/6.49	7.08/6.49
9V prog.	13.2/12.1	13.2/12.1
15V prog.	19.2/17.6	19.2/17.6
SPR absolute OV	23/22	23/22
28V	-	32.5/30.6
36V	-	39.6/37.8
EPR absolute OV	-	53/52

Table 5 shows the potential V_{BUS} UVP thresholds.

Table 5: V_{BUS} UVP Thresholds

PDO Voltage	VBUS_UV Threshold (V)	
	Only SPR Mode (R1 = 0Ω, R2 = NS)	EPR Mode (R1 = 100kΩ, R2 = 52.3kΩ)
3.3V min PPS	2.97	2.97
5V min PPS	4.5	4.5
5V fixed PDO	4.75	4.75
9V fixed PDO	8.55	8.55
12V fixed PDO	11.4	11.4
15V fixed PDO	14.25	14.25
20V fixed PDO	19	19
15V min PPS	-	13.5
28V fixed PDO	-	26.6
36V fixed PDO	-	34.2
48V fixed PDO	-	45.6

VCONN Over-Current Protection (OCP)

The VIN-to-VCONN switch has a 20Ω resistance and a 50mA over-current protection (OCP) threshold. When V_{CONN} OCP is triggered, the V_{CONN} output latches off. The following actions can re-enable V_{CONN}:

- Cycling power on VIN and EN
- A hard reset
- A VCONN_SWAP
- Detaching and reattaching the USB Type-C device

Start-Up and Shutdown Timing

If the MPF52000-AEC2's V_{IN} exceeds 4.2V, the MCU and PD engine can be enabled. The MPF52000-AEC2 should start up after the DC/DC converter starts up, and it should shut down before the converter shuts down (see Figure 8).

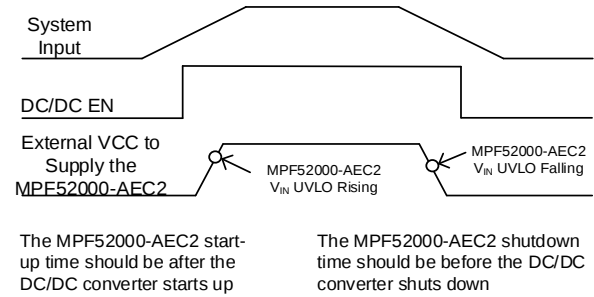


Figure 8: MPF52000-AEC2 Start-Up and Shutdown Timing

Short-to-Battery/V_{BUS}/GND Protection

If a VBUS is shorted to the battery, the VBUS rises to trigger VBUS over-voltage protection (OVP). Details please see VBUS Over-Voltage Protection (OVP).

During a CC pin or DP/DM pin short-to-battery/VBUS condition, the MPF52000-AEC2 can withstand high voltages on the internal components in SPR mode. 0x020C D6 will change to 1, indicating that a battery/VBUS short has been triggered on DP/DM/CCx. And VBUS/CCx/DP/DM supports short to GND protection.

Thermal Shutdown Protection

If the silicon die temperature exceeds 150°C, TCPC is in a thermal shutdown state, MPF52000-AEC2 turns off DC-DC converter. When the silicon die temperature falls below its recovery threshold, (typically 130°C), TCPC is not in a thermal shutdown state, MPF52000-AEC2 returns to normal operation and enable the external DC-DC converter again.

TCPC REGISTER MAP

The MPF52000-AEC2 integrates a dual-channel USB Type-C power controller (TCPC) that handles the BMC message delivery and receiver, CC status reporting, V_{BUS} over-voltage protection (OVP) and under-voltage protection (UVP) detection, V_{BUS} and V_{CONN} discharge, and over-temperature warning threshold selection. Table 6 shows the TCPC base addresses. Table 7 shows the TCPC offset addresses.

Table 6: TCPC Base Address Table

Peripheral Name	Base Address
TCPC1	0x40000000 + 0xE800
TCPC2	0x40000000 + 0xF000

Table 7: TCPC Offset Address Table

Address Offset	Register Name	Type	Reset Value	Definition
TCPC Register (Refer to USB-IF TCPC Specification R2.0 V1.2)				
0x00	VENDOR_ID_L8	R	0xC9	The MPS vendor ID is 0x2CC9
0x04	VENDOR_ID_H8	R	0x2C	
0x08	PRODUCT_ID_L8	R	0x39	Returns the MPS-defined product ID.
0x0C	PRODUCT_ID_H8	R	0x50	
0x10	DEVICE_ID_L8	R	0x00	Returns the MPS-defined device ID.
0x14	DEVICE_ID_H8	R	0x00	
0x18	USBTYPEC_REV_L8	R	0x20	Returns the USB Type-C revision.
0x1C	USBTYPEC_REV_H8	R	0x00	
0x20	USBPD_REV_VER_L8	R	0x12	Returns the USB PD revision.
0x24	USBPD_REV_VER_H8	R	0x30	
0x28	PD_INTERFACE_REV_L8	R	0x10	Returns the PD interface revision.
0x2C	PD_INTERFACE_REV_H8	R	0x20	
0x40	ALERT_L8	R/W	0x00	ALERT register definition.
0x44	ALERT_H8	R/W	0x00	
0x48	ALERT_MASK_L8	R/W	0xFF	ALERT_MASK register definition.
0x4C	ALERT_MASK_H8	R/W	0xFF	
0x50	POWER_STATUS_MASK	R/W	0xFF	POWER_STATUS_MASK register definition.
0x54	FAULT_STATUS_MASK	R/W	0xFF	FAULT_STATUS_MASK register definition.
0x58	EXTENDED_STATUS_MASK	R/W	0xFF	EXTENDED_STATUS_MASK register definition.
0x5C	ALERT_EXTENDED_MASK	R/W	0xFF	ALERT_EXTENDED_MASK register definition.
0x64	TCPC_CONTROL	R/W	0x00	TCPC_CONTROL register definition.
0x68	ROLE_CONTROL	R/W	0x00	ROLE_CONTROL register definition.
0x6C	FAULT_CONTROL	R/W	0x00	FAULT_CONTROL register definition.
0x70	POWER_CONTROL	R/W	0x00	POWER_CONTROL register definition.
0x74	CC_STATUS	R	0x00	CC_STATUS register definition.
0x78	POWER_STATUS	R	0x00	POWER_STATUS register definition.
0x7C	FAULT_STATUS	R	0x00	FAULT_STATUS register definition.
0x80	EXTENDED_STATUS	R	0x00	EXTENDED_STATUS register definition.
0x84	ALERT_EXTENDED	R	0x00	ALERT_EXTENDED register definition.
0x8C	COMMAND	W	0x00	COMMAND register definition.
0x90	DEVICE_CAPABILITIES_1_L8	R	VD	DEVICE_CAPABILITIES_1 register definition.
0x94	DEVICE_CAPABILITIES_1_H8	R	VD	
0x98	DEVICE_CAPABILITIES_2_L8	R	VD	DEVICE_CAPABILITIES_2 register definition.
0x9C	DEVICE_CAPABILITIES_2_H8	R	VD	
0xB8	MESSAGE_HEADER_INFO	R/W	0x00	MESSAGE_HEADER_INFO register definition.
0xBC	RECEIVE_DETECT	R/W	0x00	RECEIVE_DETECT register definition.

0xC0	READABLE_BYTE_COUNT	R	0x00	Indicates the number of bytes in the RX_BUF_BYTE_x registers plus one (for the RX_BUF_FRAME_TYPE).
0xC1	RX_BUF_FRAME_TYPE	R	0x00	Indicates the type of received frame.
0xC2	RX_BUF_BYTE_x	R	0x00	Receive buffer bytes.
0x140	TRANSMIT	R/W	0x00	TRANSMIT register definition.
0x144	I2C_WRITE_BYTE_COUNT	R/W	0x00	Indicates the number of bytes the USB Type-C port manager (TCPM) writes to the TX_BUF_BYTEx.
0x148	TX_BUF_BYTE_x	R/W	0x00	Transmit buffer bytes.
Vendor-Defined Register (Defined by MPS)				
0x200	SYS_CTL1	R/W	0x00	Selects the PD mode and the V _{BUS} OV/UV blanking times.
0x204	SYS_CTL2	R/W	0x00	Selects the legacy charging mode.
0x208	VBUS_OV_UV_THLD_SEL	R/W	0x0F	Selects the VBUS OV/UV thresholds for different PDOs.
0x20C	STATUS1	R/W	0x00	TCPM writes 1 to clear. The TCPC alerts the MCU when the status bit is set to 1.
0x210	STATUS1_MASK	R/W	0xFF	Masks certain faults.
0x218	SYS_CTL3	R/W	0x00	VBUS and VCONN discharge path is controlled by TCPM.
0x220	STATUS2	R/W	0x00	TCPM writes 1 to clear. The MCU is not alerted of this status when this bit is set to 1.
0x360	TOP_STATUS	R/W	0x00	TCPM writes 1 to clear.
0x364	TOP_STATUS_MASK	R/W	0x00	Masks certain faults.

VENDOR-DEFINED REGISTER DESCRIPTION

SYS_CTL1

Address: 0x0200

Type: R/W

The SYS_CTL1 command selects the power delivery modes and sets the V_{BUS} OV/UV blanking times.

Bits	Bit Name	Default	Description
D[31:8]	RESERVED	24'b 0000 0000 0000 0000 0000 0000	Reserved.
D[7]	PD_MODE_SEL	1'b 0	Selects the power delivery mode. 1'b 0: Standard power delivery mode 1'b 1: Extended power delivery mode
D[6:5]	VBUS_UV_BLANK_TIME	2'b 00	Selects the V_{BUS} under-voltage (UV) blanking time. 2'b 00: 2ms 2'b 01: 4ms 2'b 10: 8ms 2'b 11: 16ms
D[4]	VBUS_OV_BLANK_TIME	1'b 0	Selects the V_{BUS} over-voltage (OV) blanking time. 1'b 0: 40ms 1'b 1: 80ms
D[3:0]	RESERVED	1'b 0000	Reserved.

SYS_CTL2

Address: 0x0204

Type: R/W

The SYS_CTL2 command selects the legacy charging mode and the V_{BUS} present threshold.

Bits	Bit Name	Default	Description
D[31:7]	RESERVED	25'b 0000 0000 0000 0000 0000 0000 0	Reserved.
D[6:5]	LEGACY_CHARGING_MODE	2'b 00	Selects the legacy charging mode. 2'b 00: All DCP modes are active. Disable QC in the PD contract 2'b 01: Only BC1.2 is active (no Apple mode and no QC) 2'b 10: Apple mode and BC1.2 mode are active 2'b 11: All DCP modes are active, and enable QC in PD contract
D[4]	VBUS_PRESENT_THLD	1'b 1	Selects the V_{BUS} present threshold. If V_{BUS} falls below this threshold, VBUS_PRESENT should be set 0 to report the alert. 1'b 0: 2.5V falling voltage, 2.8V rising voltage. This is for the PPS state 1'b 1: 3.5V falling voltage, 4V rising voltage. This is for the fixed PDO state
D[3:0]	RESERVED	4'b 0000	Reserved.

VBUS_OV_UV_THLD_SEL

Address: 0x0208

Type: R/W

The VBUS_OV_UV_THLD_SEL command sets the V_{BUS} over-voltage protection (OVP) threshold in SPR mode and the V_{BUS} under-voltage protection (UVP) threshold for different PDOs.

Bits	Bit Name	Default	Description
D[31:8]	RESERVED	24'b 0000 0000 0000 0000 0000 0000	Reserved.
D[7:4]	VBUS_OV_THLD	4'b 0000	Sets the V_{BUS} OVP threshold in SPR mode. See Table 4 on page 23 for more details. 0000b: OVP is disabled 0001b: 5V fixed PDO OV threshold 0010b: 9V fixed PDO OV threshold 0011b: 12V fixed PDO OV threshold 0100b: 15V fixed PDO OV threshold 0101b: 5V APDO OV threshold 0110b: 9V APDO OV threshold 0111b: 15V APDO OV threshold 1000b: Absolute OV threshold in SPR mode 1001b: 28V fixed PDO OV threshold 1010b: 36V fixed PDO OV threshold 1011b: 28V APDO OV threshold 1100b: 36V APDO OV threshold 1101b: Absolute OV threshold in EPR mode
D[3:0]	VBUS_UV_THLD	4'b 0000	Sets the V_{BUS} UVP threshold for different PDOs. See Table 5 on page 24 for more details. 0000b: V_{BUS} UV detection is disabled 0001b: 2.97V V_{BUS} UV is selected for 3.3V minimum PPS voltage 0010b: 4.5V V_{BUS} UV is selected for 5V minimum PPS voltage 0011b: 5V PD V_{BUS} UV 0100b: 9V PD V_{BUS} UV 0101b: 12V PD V_{BUS} UV 0110b: 15V PD V_{BUS} UV 0111b: 20V PD V_{BUS} UV 1000b: 13.5V V_{BUS} UV threshold for 15V PPS voltage 1001b: 28V fixed PDO UV threshold 1010b: 36V fixed PDO UV threshold 1011b: 48V fixed PDO UV threshold

STATUS1

Address: 0x020C

Type: WC

The STATUS1 command returns fault information. To clear these bits, TCPM writes 1 to the corresponding bit. The alert bit is always pulled low until it is cleared to 0.

Bits	Bit Name	Description
D[31:8]	RESERVED	Reserved.
D[7]	TSD	1'b 0: TCPC is not in a thermal shutdown state 1'b 1: TCPC is in a thermal shutdown state
D[6]	BATTERY_SHORT	1'b 0: No battery short has been triggered on DP/DM/CCx 1'b 1: A battery short has been triggered on DP/DM/CCx

D[5]	VBUS_UV	Indicates whether the V _{BUS} under-voltage (UV) threshold has been triggered. 1'b 0: The V _{BUS} UV threshold has not been triggered 1'b 1: The V _{BUS} UV threshold has been triggered.
D[2]	VCONN_OVP	1'b 0: VCONN over-voltage protection (OVP) has not been triggered 1'b 1: VCONN OVP has been triggered
D[1:0]	RESERVED	Reserved.

STATUS1_MASK

Address: 0x0210

Type: R/W

The STATUS1_MASK command can only mask the TCPC's ALT# pin behavior, which means that the STATUS1 register still indicates each event.

Bits	Bit Name	Default	Description
D[31:8]	RESERVED	24'b 0000 0000 0000 0000 0000 0000	Reserved.
D[7]	TSD_MASK	1'b 1	1'b 0: The thermal shutdown mask is enabled 1'b 1: No mask
D[6]	BATTERY_SHORT_MASK	1'b 1	1'b 0: The battery short mask is enabled 1'b 1: No mask
D[5]	VBUS_UV_MASK	1'b 1	1'b 0: The V _{BUS} under-voltage (UV) mask is enabled 1'b 1: No mask
D[2]	VCONN_OVP	1'b 1	1'b 0: The VCONN over-voltage protection (OVP) mask is enabled 1'b 1: No mask
D[1:0]	RESERVED	2'b 00	Reserved.

SYS_CTL3

Address: 0x0218

Type: R/W

The SYS_CTL3 command enables the VCONN discharge path and the VBUS discharge path. The VBUS and VCONN discharge paths can be controlled by the TCPM.

Bits	Bit Name	Default	Description
D[31:8]	RESERVED	24'b 0000 0000 0000 0000 0000 0000	Reserved.
D[7]	VCONN_DISCHG	1'b 0	Enables the VCONN discharge path. The VCONN discharge path is automatically disabled when the VCONN discharge timer's 35ms has expired. 1'b 0: The VCONN discharge path is disabled 1'b 1: The VCONN switch is disabled and the discharge path is enabled
D[6]	VBUS_DISCHG	1'b 0	Enables the V _{BUS} discharge path. The 600Ω VBUS discharge resistor is automatically disabled when the VBUS discharge timer's 250ms has expired. Then this bit is set to 0 automatically. 1'b0: Disabled 1'b1: Enabled
D[5:0]	RESERVED	6'b 0000 00	Reserved.

STATUS2

Address: 0x0220

Type: R/W

The STATUS2 command shows the statuses of TCPM_WRITE_TRANSMIT_NOT_ALLOWED, CPM_WRITE_TRANSMIT_WHEN_TXBUF_EMPTY, and TCPM_WRITE_INVALID_COMMAND. To clear these bits, the TCPM writes 1 to the corresponding bit.

Bits	Bit Name	Default	Description
D[31:3]	RESERVED	29'b 0000 0000 0000 0000 0000 0000 0000 0	Reserved.
D[2]	TCPM_WRITE_TRANSMIT_NOT_ALLOWED	1'b 0	1'b0: A TCPM write transmit is allowed 1'b1: No TCPM write transmit is allowed
D[1]	TCPM_WRITE_TRANSMIT_WHEN_TXBUF_EMPTY	1'b 0	1'b0: Normal 1'b1: The TCPM writes a transmit command when transmit buffer is empty
D[0]	TCPM_WRITE_INVALID_COMMAND	1'b 0	1'b0: Normal 1'b1: The TCPC received an invalid command

TOP_STATUS

Address: 0x0360

Type: R/W

The TOP_STATUS command shows the statuses of ATTACH_STATUS_CHANGE, UFCS detection, and PD_INTERRUPT. To clear these bits, TCPM writes 1 to the corresponding bit.

Bits	Bit Name	Default	Description
D[31:9]	RESERVED	23'b 0000 0000 0000 0000 0000 000	Reserved.
D[8]	ATTACH_STATUS_CHANGE	1'b 0	1'b 0: The ATTACH status has not changed 1'b 1: The ATTACH status has changed.
D[7]	UFCS	1'b 0	1'b 0: UFCS detection has not triggered 1'b 1: UFCS detection has triggered
D[6:1]	RESERVED	6'b 0000 00	Reserved.
D[0]	PD_INTERRUPT	1'b 0	1'b 0: A PD interrupt has not triggered 1'b 1: A PD interrupt has triggered (read-only)

TOP_STATUS_MASK

Address: 0x0364

Type: R/W

The TOP_STATUS_MASK command masks the TCPC's ALT# pin behavior, which means that the STATUS1 register still indicates each event.

Bits	Bit Name	Default	Description
D[31:9]	RESERVED	23'b 0000 0000 0000 0000 0000 000	Reserved.
D[8]	ATTACH_STATUS_CHANGE_MASK	1'b 0	1'b 0: MASK enabled. 1'b 1: No mask
D[7]	UFCS_MASK	1'b 0	1'b 0: MASK enabled. 1'b 1: No mask

D[6:1]	RESERVED	6'b 0000 00	Reserved.
D[0]	PD_INTERRUPT_MASK	1'b 0	1'b 0: MASK enabled. 1'b 1: No mask

APPLICATION INFORMATION

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation and improved ESD performance. A 2-layer or 4-layer layout is recommended. For the best results, refer to Figure 9 and follow the guidelines below:

Place the VIN decoupling capacitor as close to the VIN pins as possible.

1. Put 9 vias on the exposed pad of the IC.
2. Connect the exposed pad to ground.
3. Use short, direct, and wide traces to connect CC1, CC2, CC3, and CC4 to the USB Type-C receptacle.

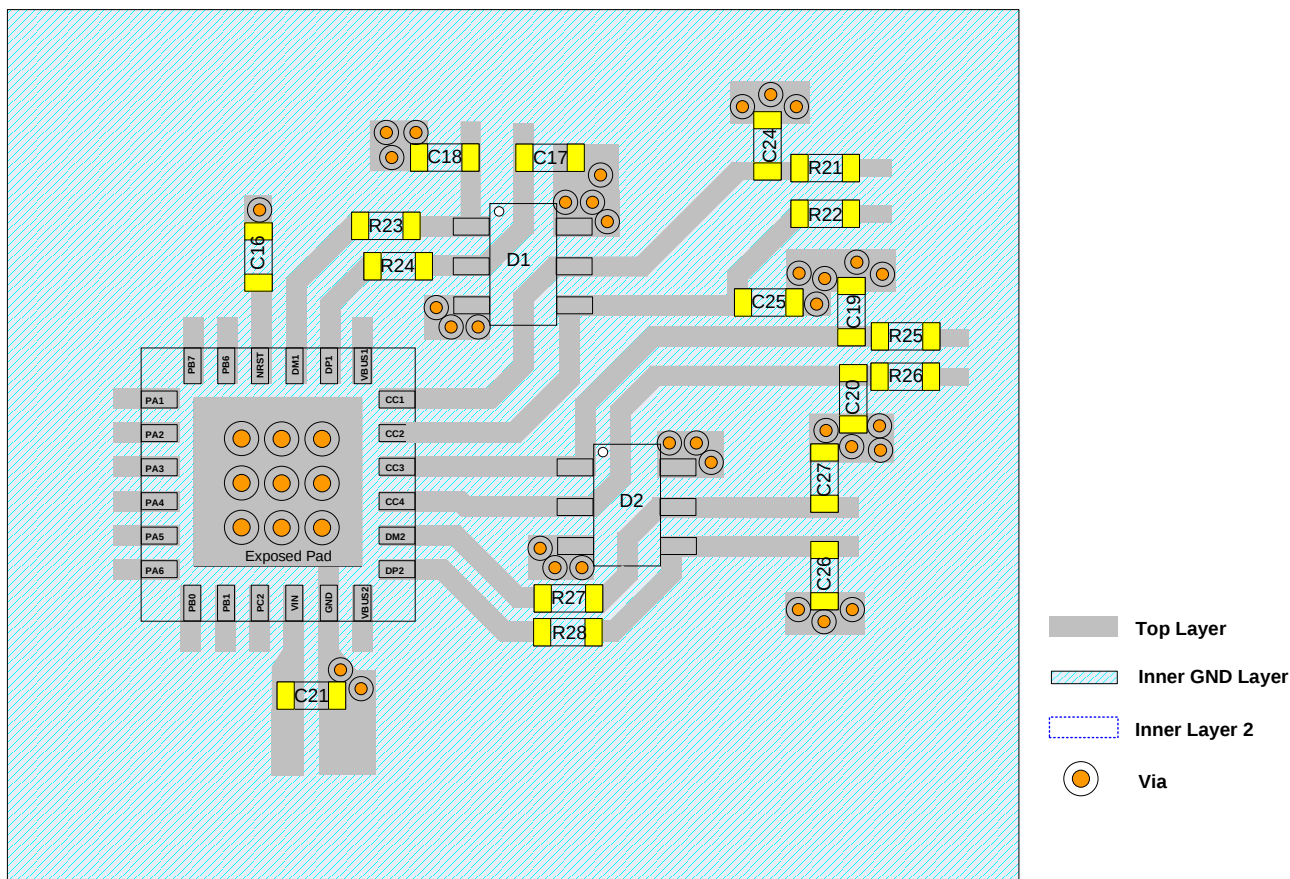


Figure 9: Recommended Layout ⁽⁶⁾

Note:

6) The recommended layout is based on typical application circuit in Figure 10 on page 31.

TYPICAL APPLICATION CIRCUIT

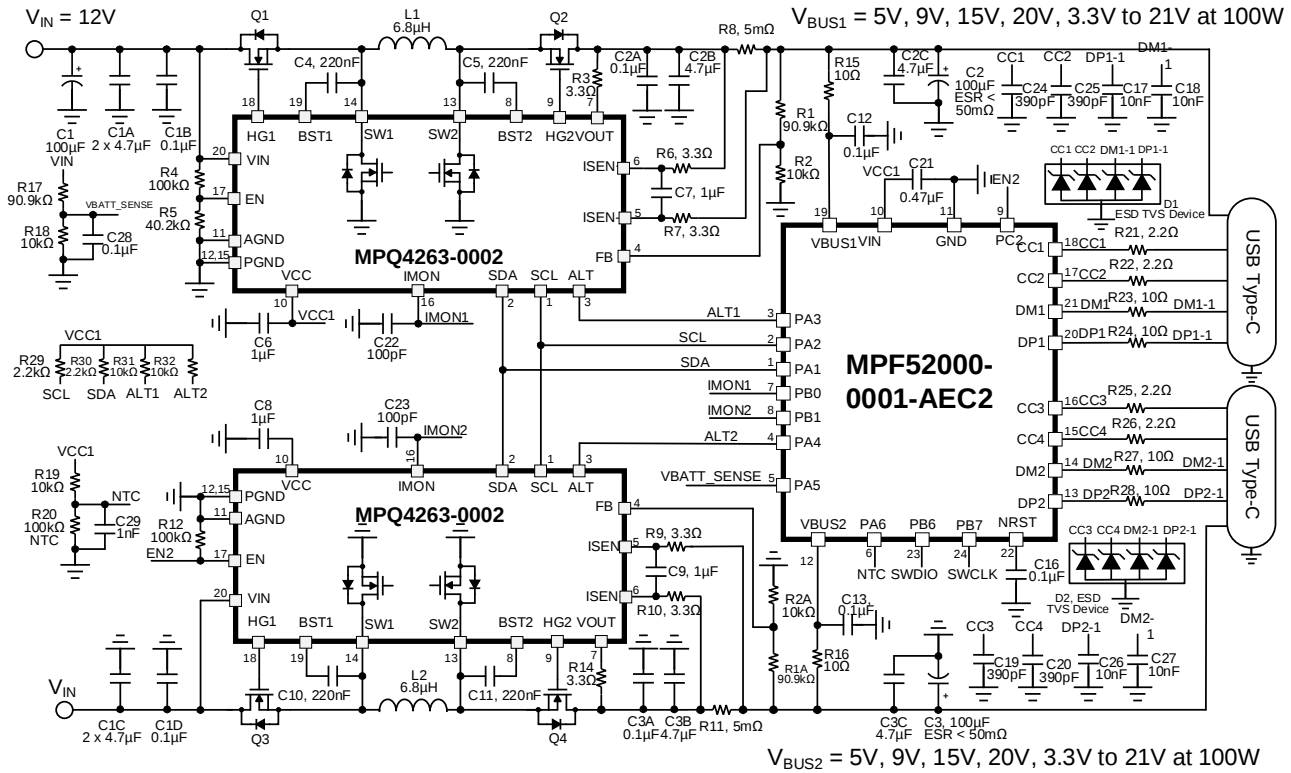
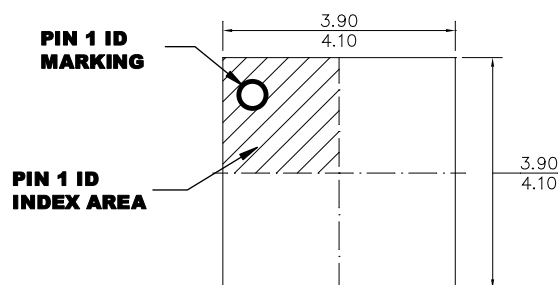


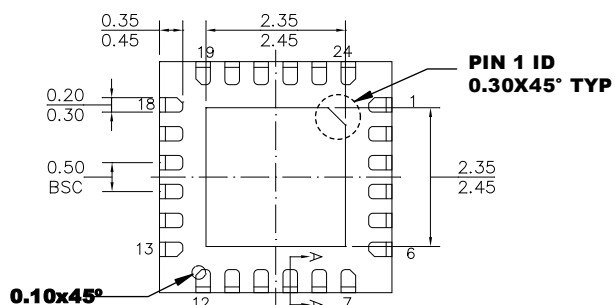
Figure 10: Typical Application Circuit with the MPF52000-AEC2 and MPQ4263 (100W/Each for Dual-Port PD Power Share Application, Total 120W Output Power)

PACKAGE INFORMATION

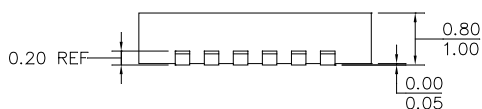
QFN-24 (4mmx4mm)



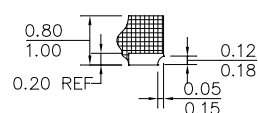
TOP VIEW



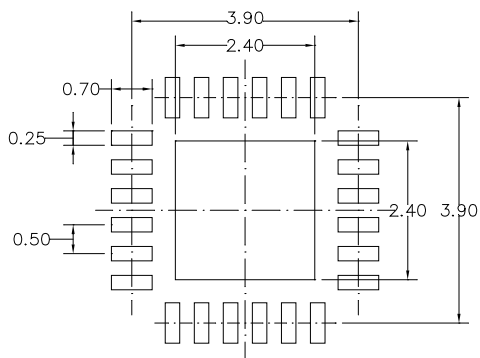
BOTTOM VIEW



SIDE VIEW



SECTION A-A

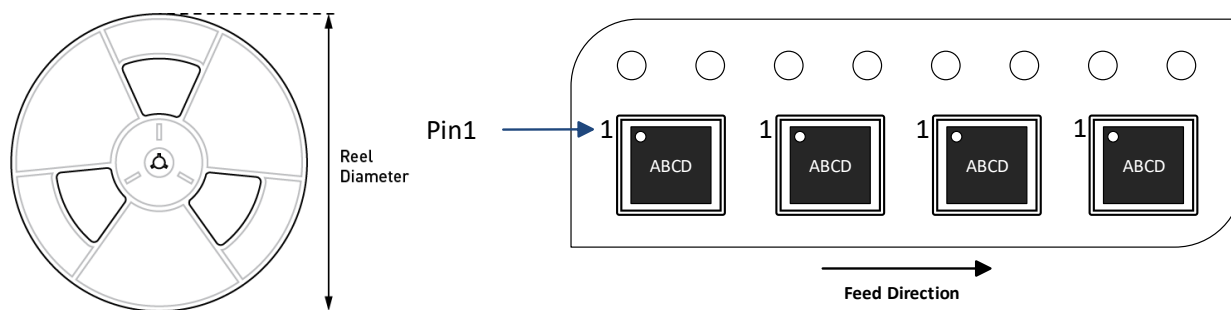


RECOMMENDED LAND PATTERN

NOTE:

- 1) THE LEAD SIDE IS WETTABLE.
- 2) ALL DIMENSIONS ARE IN MILLIMETERS.
- 3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPF52000GRE-xxxx-AEC2-Z	QFN-24 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm
MPF52000GRE-0000-AEC2-Z							
MPF52000GRE-0001-AEC2-Z							

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	7/14/2023	Initial Release	-

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