MPC22168-170

16V, 170A, Dual-Phase Intelli-Module™ with Quiet Switcher™ Technology

DESCRIPTION

The MPC22168-170 is a dual-phase, non-isolated, high-efficiency step-down power module. It integrates driver MOSFETs (DrMOS) and inductors to provide high efficiency and a small footprint, which is ideal for server applications.

The MPC22168-170 has two independent outputs, which can be used separately or in parallel. It can achieve up to 170A (85A/phase) of output current (I_{OUTx}) across a wide input voltage (V_{IN}) range.

The MPC22168-170 offers many features to simplify system design. The device works with tri-state pulse-width modulation (PWM) signal controllers, has Accu-Sense™ current sensing to monitor the inductor current (I_L), and it has temperature sensing to report the junction temperature (T_J).

The MPC22168-170 is available in an LGA-72 (9mmx9.9mmx7.65mm) package.

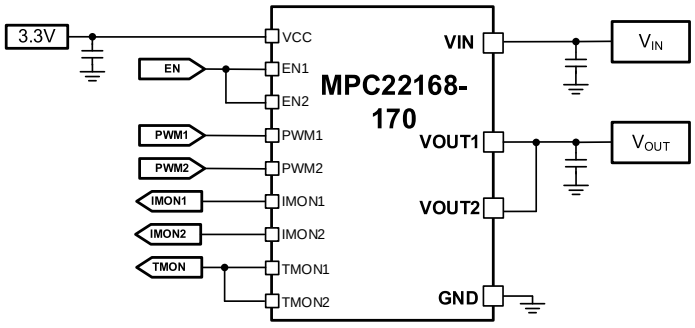
FEATURES

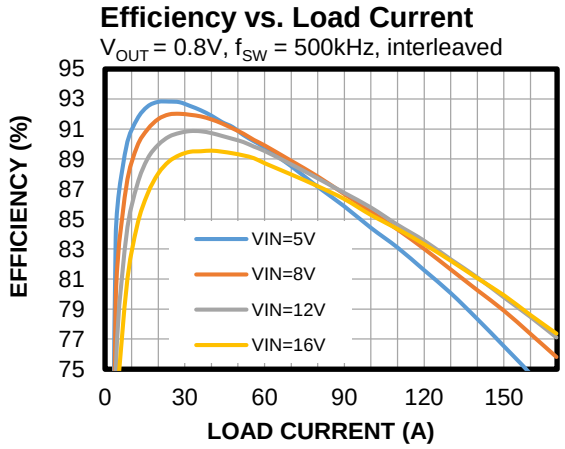
- Quiet Switcher™ Technology (QST) Limits Peak Switching Voltages
- Wide 4V to 16V Input Voltage (V_{IN}) Range
- Up to 170A Continuous Output Current (I_{OUTx})
- Accu-Sense™ Current Sense (CS)
- Temperature Sense
- Compatible with Tri-State Pulse-Width Modulation (PWM) Signals
- Over-Current Protection (OCP)
- Over-Temperature Protection (OTP)
- Fault Reporting
- Typical Weight: 3.5g
- Available in an LGA-72 (9mmx9.9mmx7.65mm) Package

APPLICATIONS

- Servers and Computing
- Field-Programmable Gate Arrays (FPGAs) and ASIC Core Power
- Graphic Card Core Regulators

TYPICAL APPLICATION





ORDERING INFORMATION

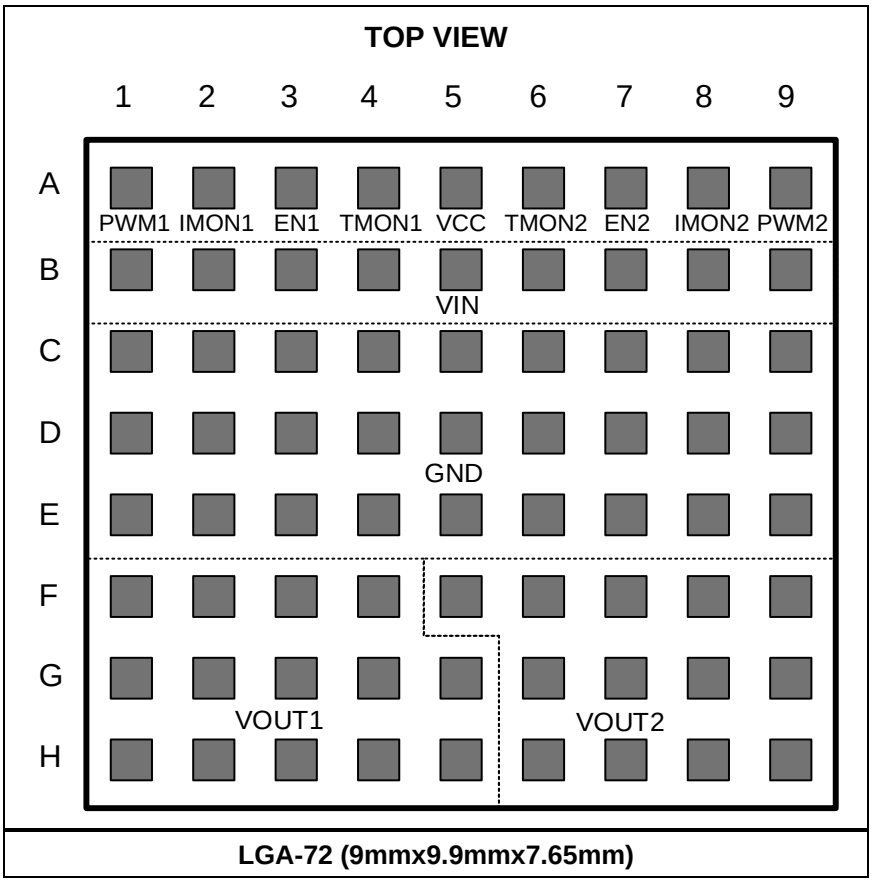
Part Number	Package	Side Label	MSL Rating
MPC22168-170	LGA-72 (9mmx9.9mmx7.65mm)	*See Below*	3

* For Tray, add suffix -T (e.g. MPC22168-170-T).

SIDE LABEL

Date Code
Vendor's Serial Number
LOT ID

PACKAGE REFERENCE



LGA-72 (9mmx9.9mmx7.65mm)

PIN FUNCTIONS

Pin #	Name	Description
A1	PWM1	**Channel 1 pulse-width modulation (PWM) input.** Float the PWM1 pin or pull PWM1 to a middle-state to force the channel 1 driver MOSFET (DrMOS1) into a high-impedance (Hi-Z) state.
A2	IMON1	**Channel 1 current-sense output.** The IMON1 pin is a bidirectional current output proportional to channel 1's inductor current (I_{L1}). Connect IMON1 to the pulse-width modulation (PWM) controller's current-sense input. Connect a resistor to a common-mode voltage to have the differential voltage be proportional to I_{L1}.
A3	EN1	**Channel 1 enable.** Pull the EN1 pin low to disable DrMOS1.
A4	TMON1	**Channel 1 single-pin temperature sense and fault reporting.** If a fault occurs, the TMON1 pin is pulled up to the driver voltage (V_{CC}).
A5	VCC	**Driver voltage.** Connect the VCC pin to a 3.3V supply.
A6	TMON2	**Channel 2 single-pin temperature sense and fault reporting.** If a fault occurs, the TMON2 pin is pulled up to VCC.
A7	EN2	**Channel 2 enable.** Pull the EN2 pin low to disable the channel 2 driver MOSFET (DrMOS2).
A8	IMON2	**Channel 2 current-sense output.** The IMON2 pin is a bidirectional current output proportional to channel 2's I_{L2}. Connect IMON2 to the PWM controller's current-sense input. Connect a resistor to a common-mode voltage to have the differential voltage be proportional to I_{L2}.
A9	PWM2	**Channel 2 PWM input.** Float the PWM2 pin or pull PWM2 to a middle-state to force the DrMOS2 into a Hi-Z state.
B1, B2, B3, B4, B5, B6, B7, B8, B9	VIN	**Input voltage.** Place the ceramic input capacitors (C_{IN}) close to the module's VIN and GND pins. It is recommended to use at least six 4.7µF capacitors (0805) rated for 25V.
C1, C2, C3, C4, C5, C6, C7, C8, C9, D1, D2, D3, D4, D5, D6, D7, D8, D9, E1, E2, E3, E4, E5, E6, E7, E8, E9	GND	**Power ground.**
F1, F2, F3, F4, G1, G2, G3, G4, G5, H1, H2, H3, H4, H5	VOUT1	**Channel 1 output voltage.** Place the ceramic output capacitors (C_{OUT1}) close to the module's VOUT1 and GND pins. It is recommended to use at least three 22µF capacitors (0805) rated for 6.3V.
F5, F5, F7, F8, F9, G6, G7, G8, G9, H6, H7, H8, H9	VOUT2	**Channel 2 output voltage.** Place the ceramic output capacitors (C_{OUT2}) close to the module's VOUT2 and GND pins. It is recommended to use at least three 22µF capacitors (0805) rated for 6.3V.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} to GND .....-0.3V to +20V
V_{OUT1} to GND .....-0.3V to V_{IN} + 0.3V
V_{OUT2} to GND .....-0.3V to V_{IN} + 0.3V
V_{CC}. .....-0.3V to +4V
All other pins .....-0.3V to V_{CC} + 0.3V
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

Recommended Operating Conditions (2)

Input voltage (V_{IN}) .....4V to 16V
Output voltage (V_{OUT1}, V_{OUT2}) .....0.5V to 2V
Driver voltage (V_{CC}).....3.0V to 3.6V
Operating junction temp (T_J).... -40°C to +105°C

Thermal Resistance (3) θ_{JC_TOP} θ_{JC_BOT}

LGA-72 (9mmx9.9mmx7.65mm)……
……1.8.....5.3.. °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) θ_{JC_TOP} is the thermal resistance from the junction to the top of the DrMOS package. θ_{JC_BOT} is the thermal resistance from the junction of the DrMOS to the bottom of the module's package (soldering pad). θ_{JC_TOP} and θ_{JC_BOT} are calculated from the thermal resistance matrix at V_{IN} = 12V, V_{OUT} = 0.8V, I_{OUTx} = 30A, and f_{SW} = 500kHz.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{CC} = V_{EN1} or V_{EN2} = 3.3V, f_{SW} = 500kHz, T_A = 25°C for typical values, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Module Quiescent Current						
Input quiescent current (I_Q)	I_{VIN_Q}	EN1 and EN2 are low		10		μA
VCC I_Q	I_{VCC_Q}	EN1 and EN2 are low		820		μA
Single Phase Parameters						
Input voltage (V_{IN}) under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_RISING}$			2.5	3	V
V_{IN} UVLO hysteresis				200		mV
Input current (I_{IN}) at no load	$I_{IN\_NO\_LOAD}$	I_{OUTx} = 0A, PWMx duty = 0.8/12		50		mA
Continuous output current (I_{OUTx}) (4)	I_{OUTx_DC}	PWMx duty = 0.8/12, T_J ≤ 105°C		85		A
VCC voltage (V_{CC}) UVLO rising threshold	$V_{CC\_UVLO\_RISING}$			2.75	2.95	V
V_{CC} UVLO hysteresis				200		mV
VCC current at no load	$I_{VCC\_NO\_LOAD}$	I_{OUTx} = 0A, PWMx duty = 0.8/12		30		mA
High-side MOSFET (HS-FET) current limit (4)	I_{LIMIT_HS}	Cycle-by-cycle, up to 10 cycles		120		A
Low-side MOSFET (LS-FET) current limit (4)	I_{LIMIT_LS}	I_{LIMIT_NEG}, cycle-by-cycle, no fault report		-50		A
Negative current limit (I_{LIMIT_NEG}) LS-FET off time (4)	t_{LIMIT_NEG}			200		ns
High-side current limit shutdown counter (4)	t_{LIMIT_HS}			10		times
ENx logic high voltage			1.4			V
ENx logic low voltage					0.85	V
IMONx gain (4)				5		μA/A
IMONx gain accuracy (4)			-4		+4	%
TMONx gain (4)				8		mV/°C
TMONx offset (4)		T_J = 25°C		800		mV
Over-temperature protection (OTP) and fault flag (4)				160		°C
TMONx voltage (V_{TMONx}) when a fault occurs (4)				V_{CC}		V
PWMx source current		V_{PWMx} = 0V		500		μA
PWMx sink current		V_{PWMx} = 3.3V		-500		μA
PWMx high-impedance (Hi-Z) voltage		PWMx is in a Hi-Z state		1.6		V
PWM logic high voltage			2.6			V
PWM tri-state range			1.1		2.1	V
PWM logic low voltage					0.6	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{CC} = V_{EN1} or V_{EN2} = 3.3V, f_{SW} = 500kHz, T_A = 25°C for typical values, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Minimum PWMx pulse width (4)				15		ns
PWMx high to DrMOS switching node (SW) rising delay (4)	t_{RISING}			15		ns
PWMx low to SW falling delay (4)	$t_{FALLING}$			15		Ns
PWMx tri-state to SW Hi-Z delay (4)	t_{LT}			40		ns
	t_{TL}			20		ns
	t_{HT}			40		ns
	t_{TH}			20		ns

Note:

4) Guaranteed by design or characterization data. Not tested in production.

PWM TIMING DIAGRAM

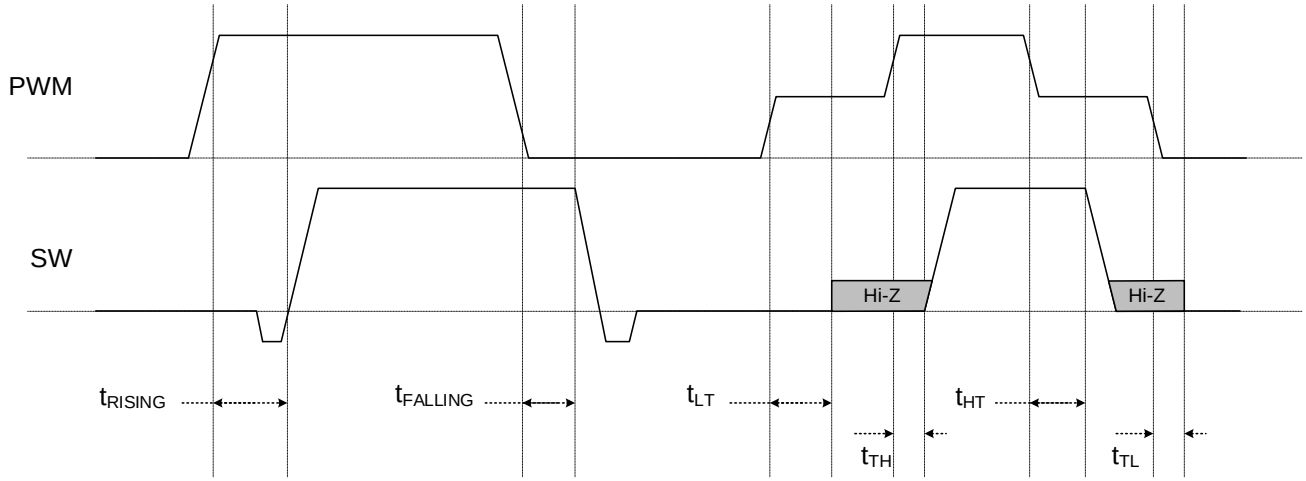


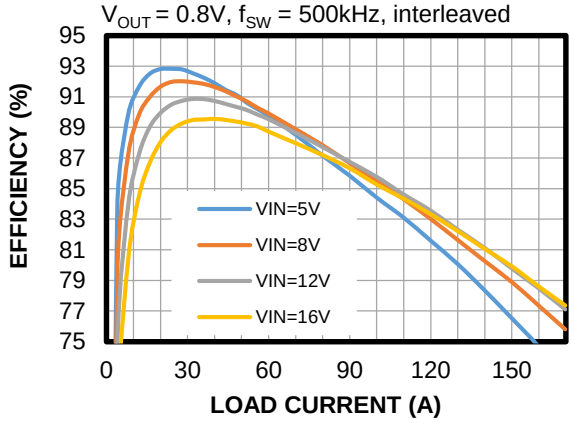
Figure 1: PWM Timing Diagram

TYPICAL CHARACTERISTICS

Performance waveforms are tested on the evaluation board. V_{CC} = 3.3V, external C_{IN} = 18 x 10µF, C_{OUT} = 18 x 22µF, T_A = 25°C, unless otherwise noted.

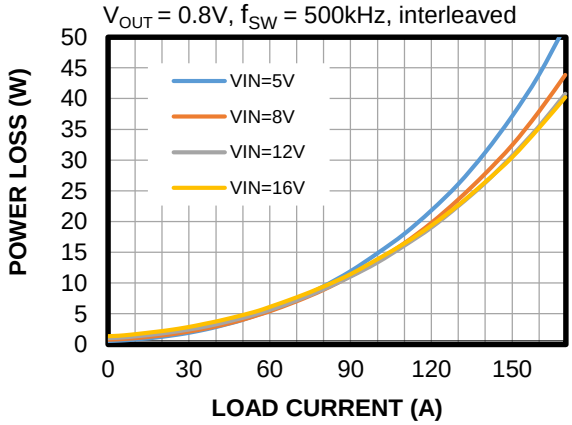
Efficiency vs. Load Current

V_{OUT} = 0.8V, f_{SW} = 500kHz, interleaved



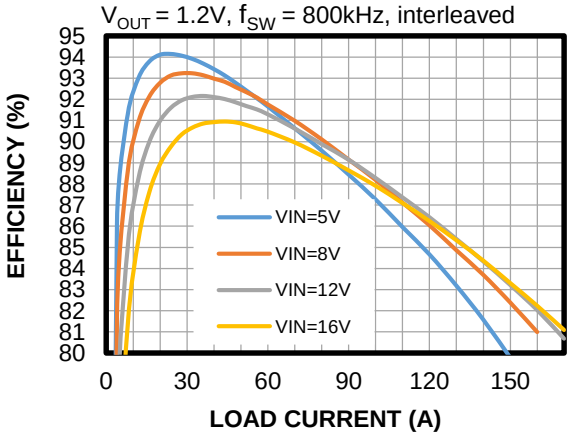
Power Loss vs. Load Current

V_{OUT} = 0.8V, f_{SW} = 500kHz, interleaved



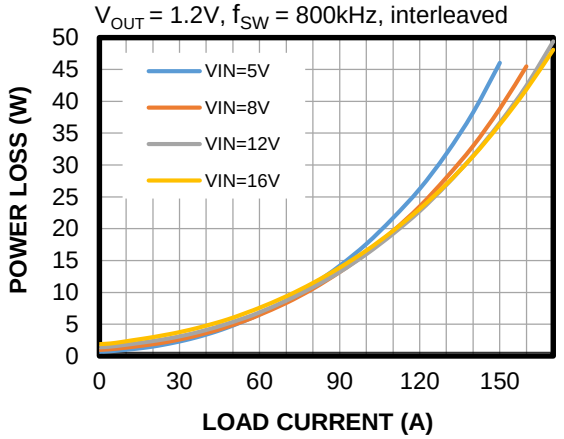
Efficiency vs. Load Current

V_{OUT} = 1.2V, f_{SW} = 800kHz, interleaved



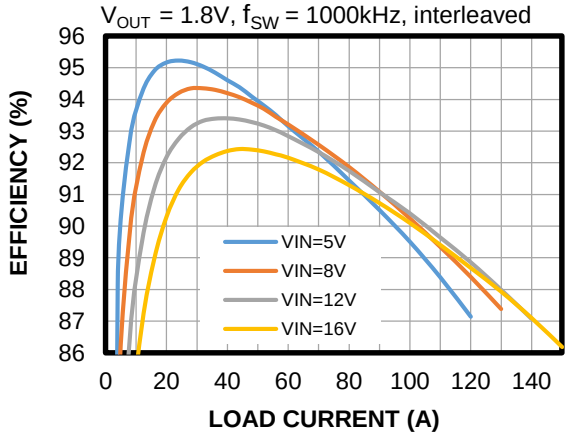
Power Loss vs. Load Current

V_{OUT} = 1.2V, f_{SW} = 800kHz, interleaved



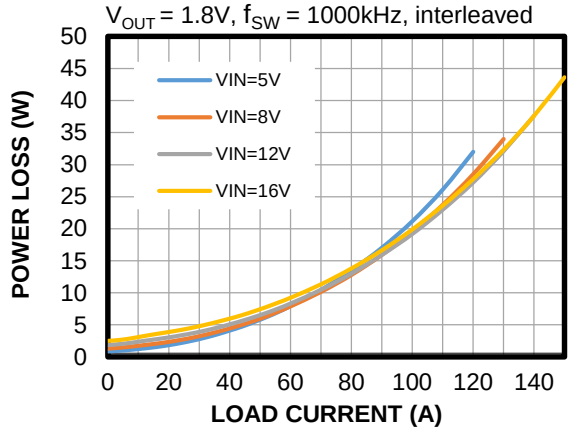
Efficiency vs. Load Current

V_{OUT} = 1.8V, f_{SW} = 1000kHz, interleaved



Power Loss vs. Load Current

V_{OUT} = 1.8V, f_{SW} = 1000kHz, interleaved

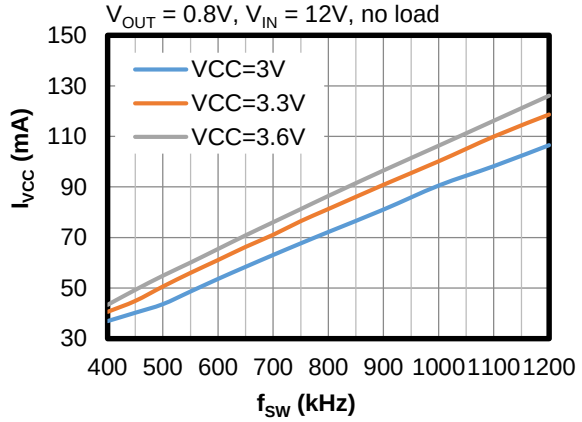


TYPICAL CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V_{CC} = 3.3V, external C_{IN} = 18 x 10µF, C_{OUT} = 18 x 22µF, T_A = 25°C, unless otherwise noted.

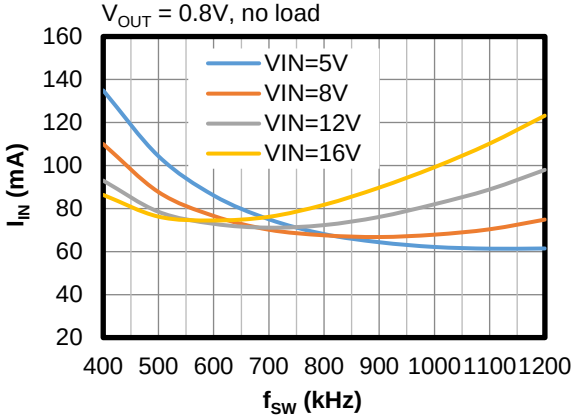
VCC Current vs. Switching Frequency

V_{OUT} = 0.8V, V_{IN} = 12V, no load



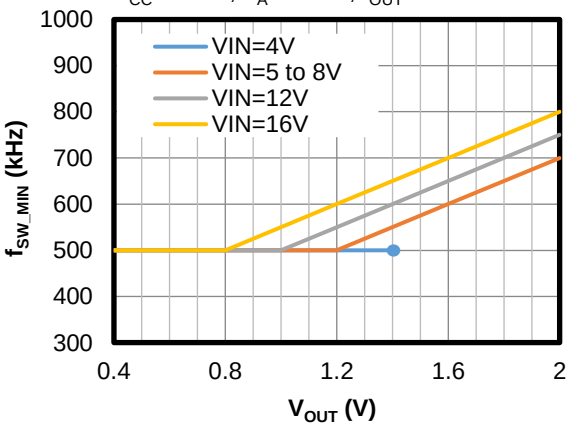
Input Current vs. Switching Frequency

V_{OUT} = 0.8V, no load



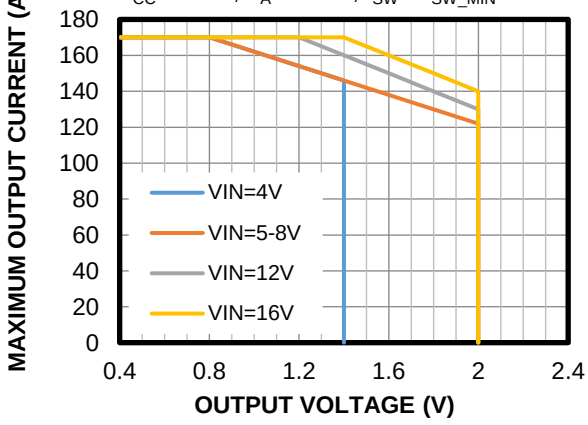
Minimum Switching Frequency vs. Output Voltage (5)

V_{CC} = 3.3V, T_A = 25°C, I_{OUT} = 170A



Maximum Output Current vs. Output Voltage (6)

V_{CC} = 3.3V, T_A = 25°C, $f_{SW} \geq f_{SW\_MIN}$



Note:

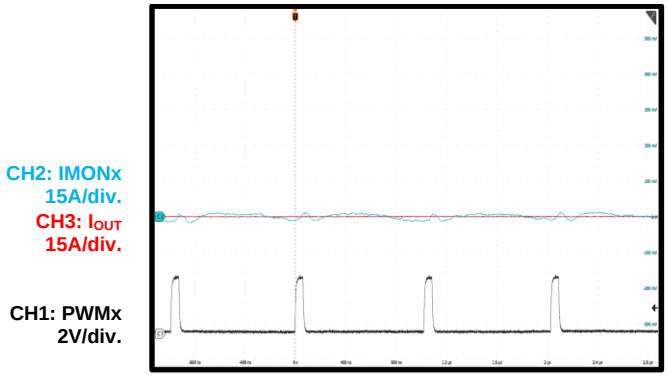
5) The minimum switching frequency (f_{SW}) limits the ripple current and prevents the DrMOS from triggering OCP.
6) The maximum output current is defined by the module's thermal capacity. The output current (I_{OUTx}) can be at a larger value when operating under excellent heat dissipation conditions.

TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board. V_{CC} = 3.3V, external C_{IN} = 18 x 10µF, C_{OUT} = 18 x 22µF, T_A = 25°C, unless otherwise noted.

Steady State

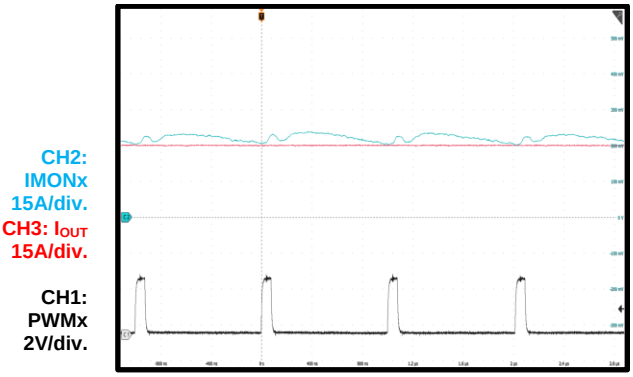
IMON reporting, single-phase, R_{CS} = 1.5kΩ, V_{IN} = 12V, V_{OUT} = 0.8V, PWM = 500kHz, I_{OUT} = 0A



400ns/div.

Steady State

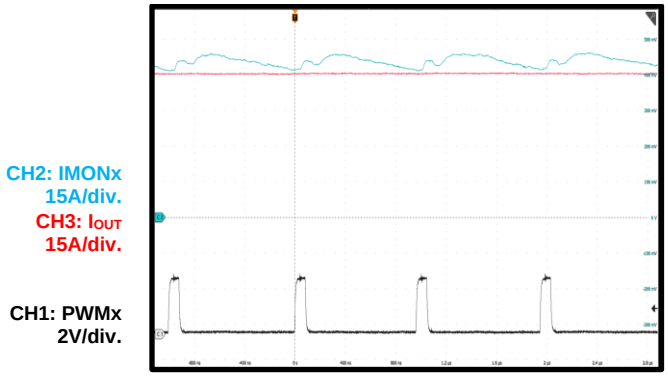
IMON reporting, single-phase, R_{CS} = 1.5kΩ, V_{IN} = 12V, V_{OUT} = 0.8V, PWM = 500kHz, I_{OUT} = 30A



400ns/div.

Steady State

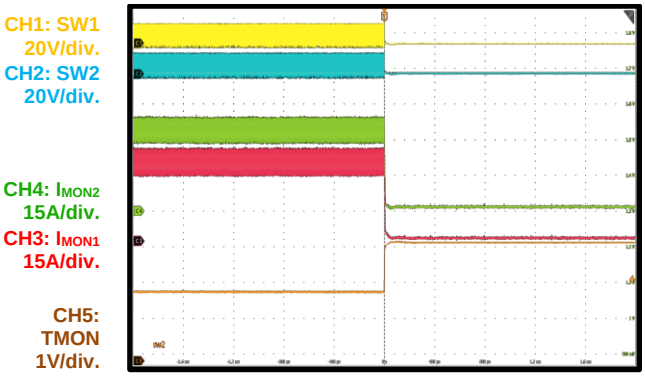
IMON reporting, single-phase, R_{CS} = 1.5kΩ, V_{IN} = 12V, V_{OUT} = 0.8V, PWM = 500kHz, I_{OUT} = 60A



400ns/div.

Over-Temperature Protection

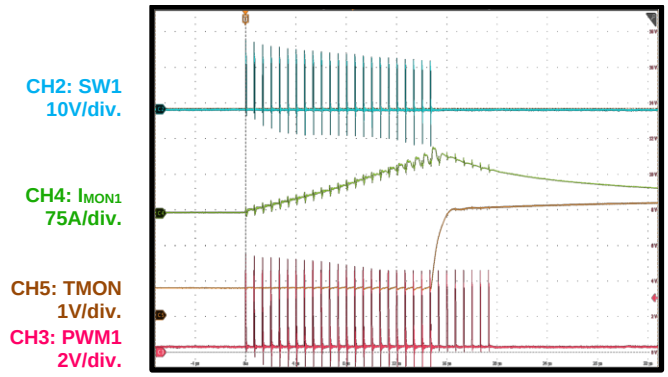
Dual-phase, V_{IN} = 12V, I_{OUT} = 80A, PWM = 500kHz



400µs/div.

Over-Current Protection

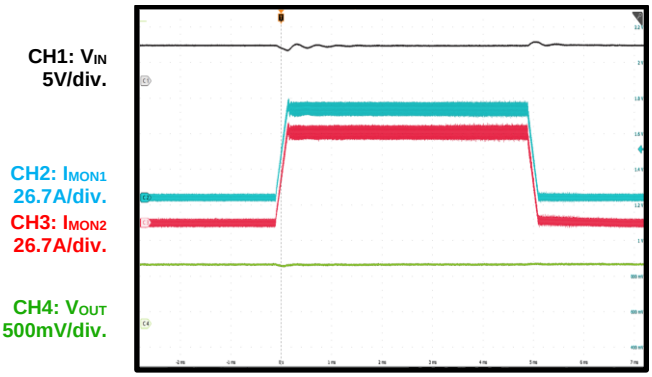
Single-phase, V_{IN} = 16V, output short, PWM = 1500kHz, 50ns, 30 period pulse



4µs/div.

Load Transient Response

Dual-phase interleaved, V_{IN} = 4V, V_{OUT} = 0.8V, I_{OUT} = 0A to 130A to 0A, f_{SW} = 700kHz



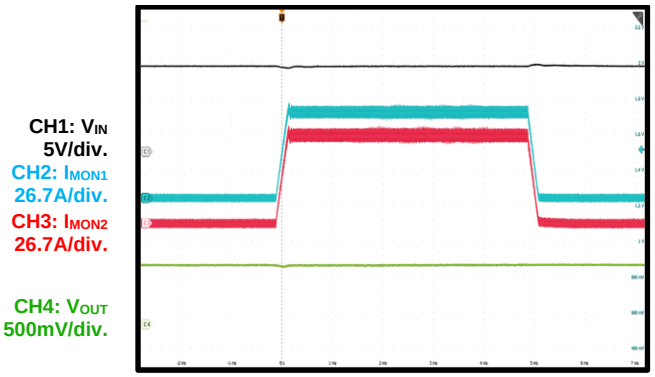
1ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V_{CC} = 3.3V, external C_{IN} = 18 x 10µF, C_{OUT} = 18 x 22µF, T_A = 25°C, unless otherwise noted.

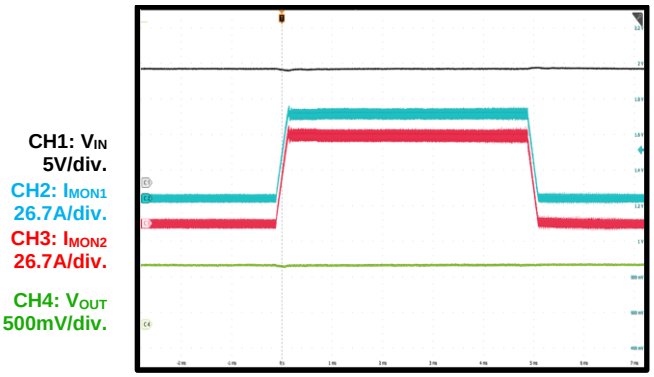
Load Transient Response

Dual-phase interleaved, V_{IN} = 12V, V_{OUT} = 0.8V, I_{OUT} = 0A to 130A to 0A, f_{SW} = 700kHz



Load Transient Response

Dual-phase interleaved, V_{IN} = 16V, V_{OUT} = 0.8V, I_{OUT} = 0A to 130A to 0A, f_{SW} = 700kHz



FUNCTIONAL BLOCK DIAGRAM

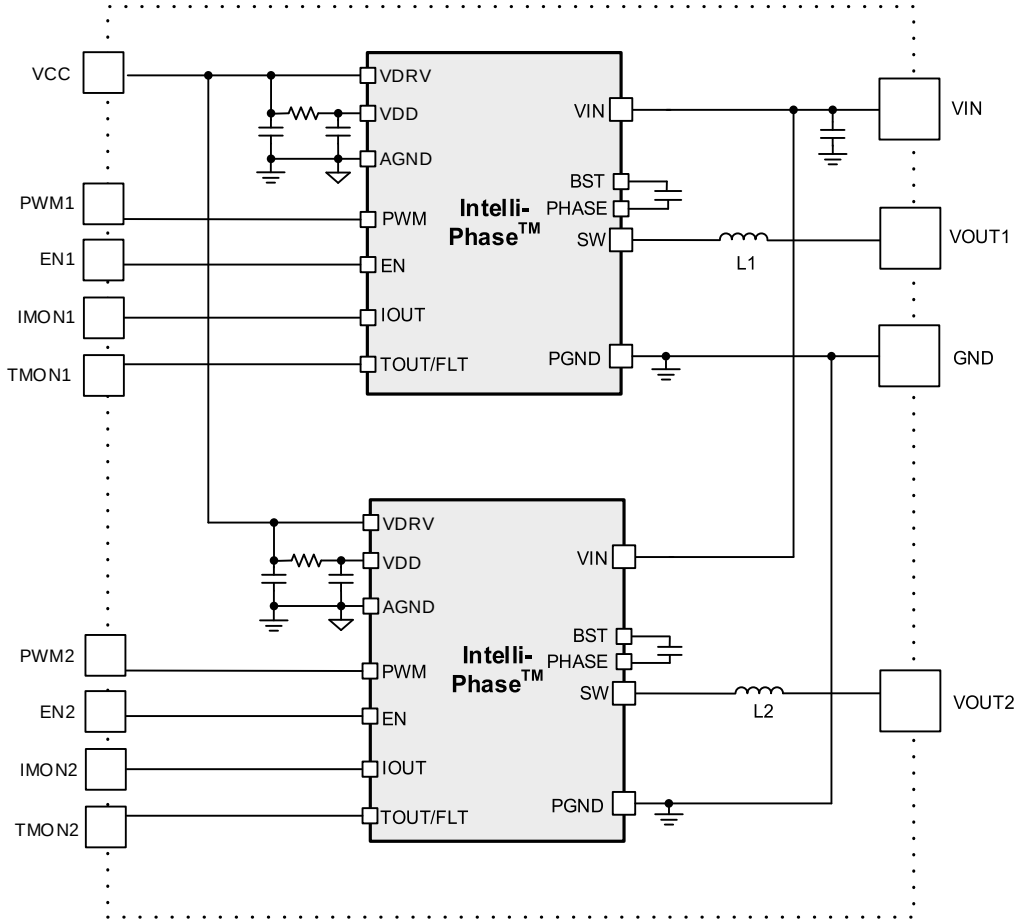


Figure 2: Functional Block Diagram

OPERATION

The MPC22168-170 is a fully integrated, dual-phase power module with up to 170A of continuous output current (I_{OUTx}) in a small LGA-72 (9mmx9.9mmx7.65mm) package. If more current is required, several MPC22168-170s can be connected in parallel.

Dual-Phase Architecture

The MPC22168-170 integrates two sets of half-bridges with inductors. The two half-bridges share an input voltage (V_{IN}) and input capacitors (C_{IN}). In dual-phase applications, the two phases can be connected in parallel. Since the two phases can operate independently, they can provide different output voltages (V_{OUT1} and V_{OUT2}, respectively).

Quiet Switcher™ Technology (QST)

Quiet Switcher™ Technology (QST) is a proprietary feedback control architecture that controls the effect of parasitic kickback in the circuit. This suppresses the level of voltage overshoot during fast switching at frequencies up to 3MHz.

Pulse-Width Modulation (PWMx)

The pulse-width modulation (PWMx) pin can operate as a tri-state input. If the PWM input signal is within the tri-state threshold window (t_{HT} or t_{LT}) for a set time (typically 40ns), the high-side MOSFET (HS-FET) turns off and the low-side MOSFET (LS-FET) enters diode emulation mode. The LS-FET operates in diode emulation mode until zero-current detection (ZCD).

The tri-state PWM input can come from a forced middle-voltage PWM signal or by floating the PWMx pin. The internal current source charges the signal to a middle voltage. See Figure 1 on page 6 for the propagation delay definition between the PWMx pin and the switching node (SW).

Diode Emulation Mode

In diode emulation mode, PWMx is in a tri-state input. If the inductor current (I_L) is positive, then the LS-FET turns on. If I_L is negative or if I_L crosses the ZCD threshold, the LS-FET turns off. Pull PWMx to a middle voltage or float PWMx to enable diode emulation mode.

Current-Sense Output (IMON1 and IMON2)

IMONx is a bidirectional current source proportional to I_L. The current-sense gain (G_{CS}) is 5μA/A. If necessary, use a resistor to configure the voltage gain so that it is proportional to I_L.

The IMONx pin's output has two states (see Table 1).

Table 1: IMONx Output States

PWMx	ENx	IMONx
PWM	High	Active
x	Low	Hi-Z

An IMONx voltage (V_{IMONx}) between 0.7V and 2.1V is required to achieve accurate I_{OUTx} reporting. A resistor (R_{CS}) is typically connected between the IMONx pin and an external reference voltage (V_{CM}) that is capable of sinking small currents, which provides a sufficient voltage to meet the required operating voltage range.

V_{CM} can be calculated with Equation (1):

$$0.7V < I_{MONx} \times R_{CS} + V_{CM} < 2.1 \quad (1)$$

I_{MONx} can be estimated with Equation (2):

$$I_{MONx} = I_L \times G_{CS} \quad (2)$$

The Intelli-Phase™ current-sense output is used by the controller to accurately monitor I_{OUTx}. The cycle-by-cycle current information from the IMONx pin can be used for phase-current balancing, over-current protection (OCP), and active voltage positioning (output voltage droop).

Positive and Negative Inductor Current Limit

If an HS-FET over-current (OC) fault is detected, then the HS-FET turns off for one PWM cycle. If an HS-FET OC fault is detected for ten consecutive cycles, then the HS-FET latches off, TMONx is pulled up to the driver voltage (V_{CC}), and the LS-FET turns on until ZCD. Release the fault latch by toggling ENx or cycling the power on VIN or VCC.

If the LS-FET detects a -50A current, then the LS-FET turns off and the HS-FET turns on for 200ns to limit the negative current. The LS-FET negative current limit does not trigger a fault report.

Temperature-Sense Output with Fault Indicator (TMONx)

The TMONx pin has dual functions. It acts as the device's junction temperature (T_J) sense and fault detection. These functions are described below.

Junction Temperature Sense

If the part is active and V_{CC} has exceeded its UVLO rising threshold, then the TMONx pin voltage (V_{TMONx}) output is proportional to T_J. The gain is 8mV/°C with an 800mV offset at 25°C. For example, V_{TMONx} is 0.8V at T_J = 25°C, and is 1.6V at T_J = 125°C.

Fault Function

If a fault occurs, TMONx is pulled to V_{CC} (typically 3.3V, 3V minimum) to report the fault, regardless of T_J. After a 200ns delay, PWMx's resistance changes to indicate the fault event.

Table 2 shows the PWMx resistance for each fault event.

Table 2: PWMx Resistance for Each Fault Event

Fault Type	PWMx
Over-current (OC) fault	10kΩ to AGND
Over-temperature (OT) fault	20kΩ to AGND
SW to PGND short	1kΩ to VCC

TMONx monitors three different fault events: OC, over-temperature (OT), and SW-to-PGND short. These events are described in greater detail below;

1. OC fault: Ten consecutive current-limit faults trigger an OC fault. Once a fault occurs, the part latches off to turn off the HS-FET. The LS-FET turns on, then turns off once I_L reaches 0A. The PWMx pin uses a 10kΩ resistor connected to AGND to indicate this fault event.
2. OT fault: At T_J > 160°C, the part latches off to turn off the HS-FET. The LS-FET turns on, then turns off once I_L reaches 0A. PWMx uses a 20kΩ resistor connected to AGND to indicate this fault event.
3. SW-to-PGND short: If this fault occurs, the part latches off to turn off the HS-FET. PWMx is pulled high via a 1kΩ resistor connected to VCC to indicate this fault event.

Release a fault latch by toggling EN or by cycling the power on VIN or VCC.

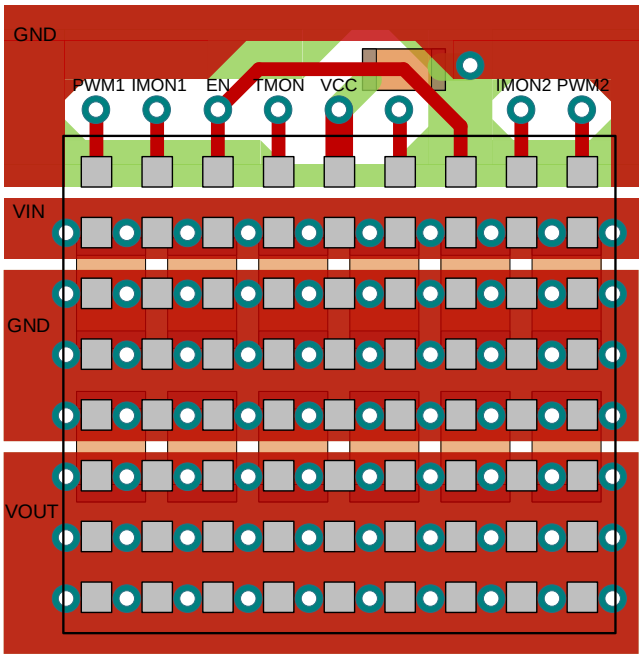
For multi-phase operation, connect the TMONx pin of each DrMOS together (see Figure 4 on page 15).

APPLICATION INFORMATION

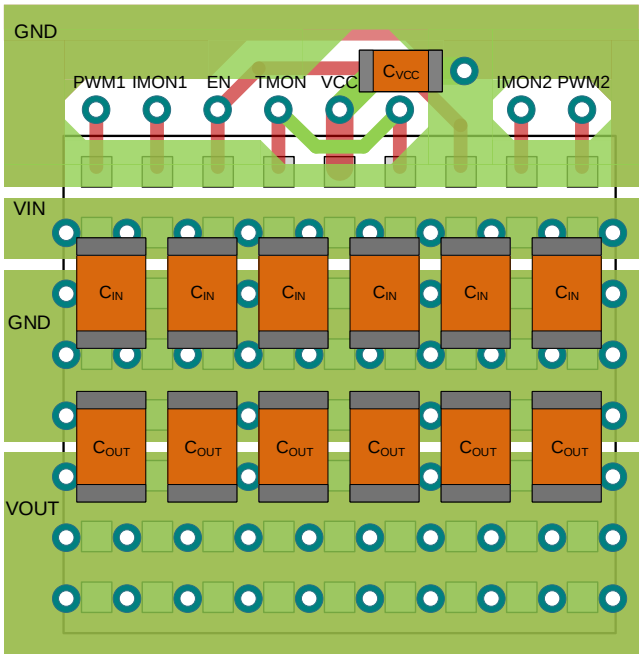
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 3 and follow the guidelines below:

1. Place the modules' outputs close to the load to reduce output network resistance.
2. Place the major MLCC input and output capacitors on the bottom side of the module.
3. Place the MLCC input and output capacitors along the boundary between VIN, VOUTx, and PGND.
4. Place a 1μF to 4.7μF VCC capacitor close to the VCC pin.
5. Route the VCC path using a ≥20mils trace width.
6. Place a VIN copper plane on the mid-layer to form the PCB stack (positive/negative/positive) to reduce parasitic impedance from the MLCC input capacitor to the module.
7. Place as many VIN, VOUTx, and GND vias as possible underneath the package to reduce parasitic impedance and thermal resistance.
8. Avoid placing mechanical vias on the module's land pattern to prevent soldering defects. Copper-filled or laser vias can be placed on the land pattern.
9. Place a VOUTx copper plane to form the PCB stack (positive/negative/positive) to reduce parasitic impedance from the module to the load.
10. Route sensitive signal traces on the mid-layer next to the GND layer.
11. Route all signal traces (PWMx, IMONx, TMONx, and ENx) away from high-current paths, such as VIN.
12. Route the PWMx signal trace away from any other signals.



Top Layer



Bottom Layer

Figure 3: Recommended PCB Layout

Input Capacitor: 0805 Package
Output Capacitor: 0805 Package
VCC Capacitor: 0603 Package
Via Size: 20mils/10mils

TYPICAL APPLICATION CIRCUIT

Figure 4 shows a typical application circuit for multiple MPC22168-170 devices operating in parallel. *n* represents the number of modules and *x* represents the *x*th module. The phase shift between two PWMx pins is 360/2n°. Connect PWMx and PWM(x + n) to each module, so that the two phases on each module have a 180° phase shift.

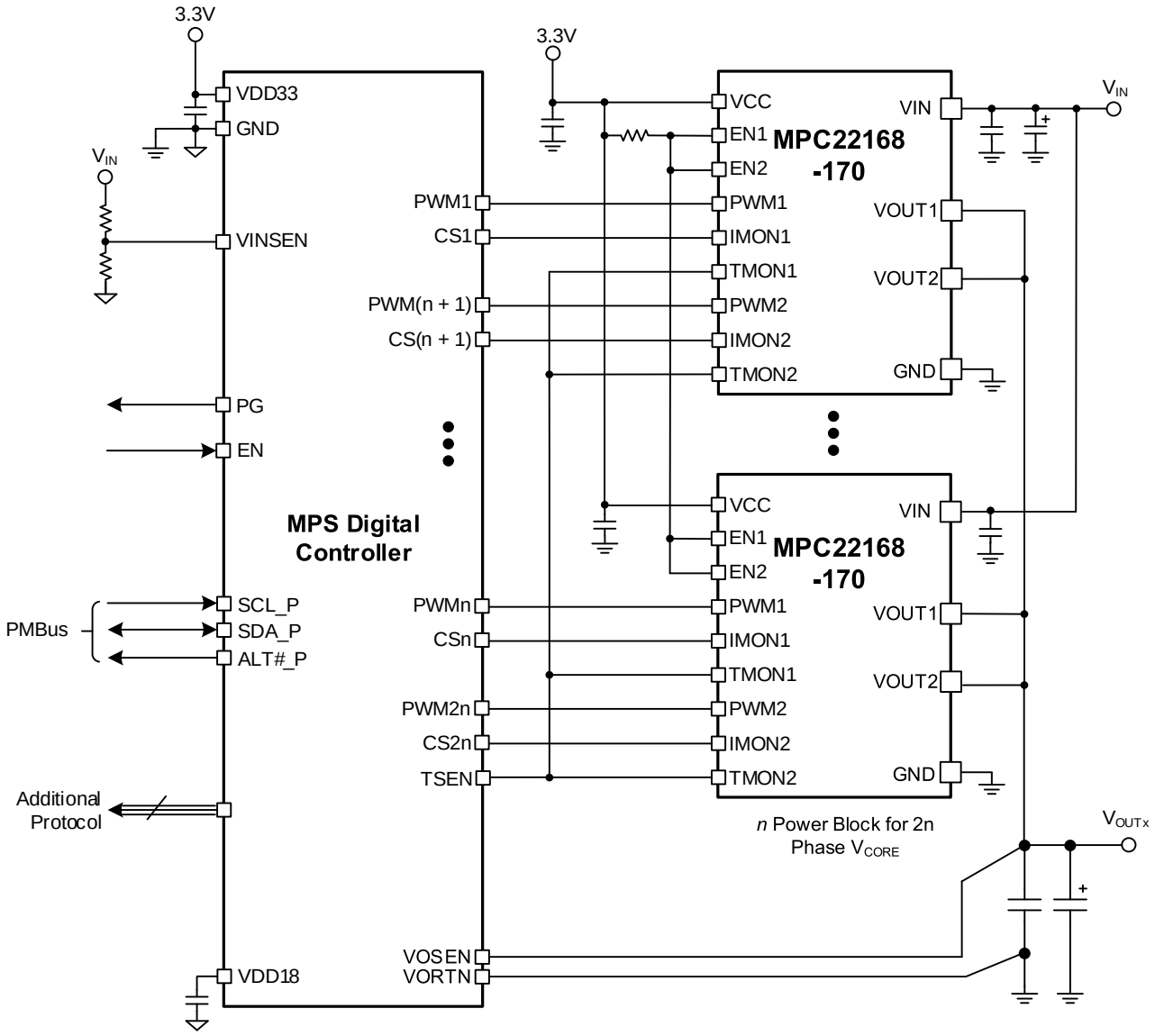
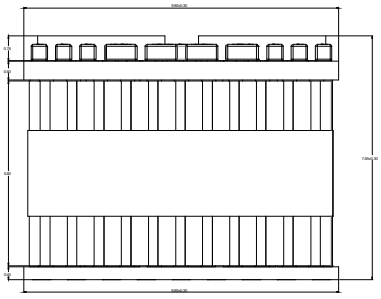


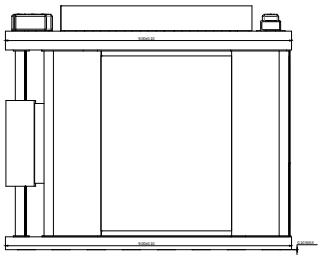
Figure 4: Typical Application Circuit for Multiple MPC22168-170 Devices in Parallel

PACKAGE INFORMATION

LGA-72 (9mmx9.9mmx7.65mm)

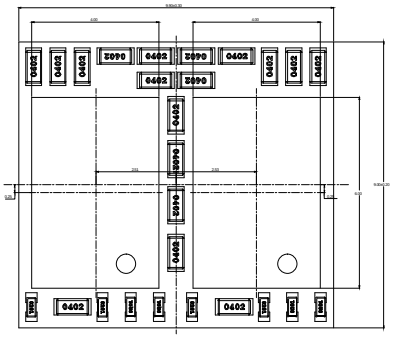


FRONT VIEW

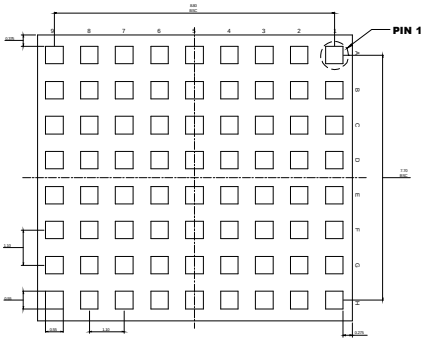


SIDE VIEW

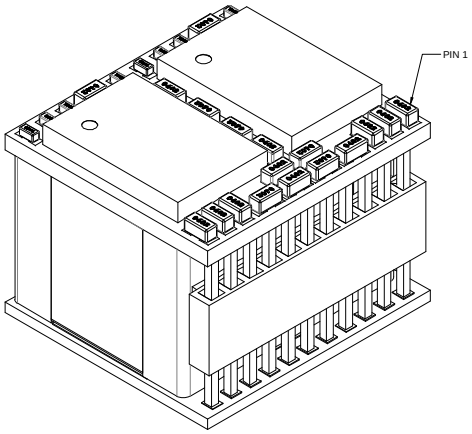
*Note:
(1)ALL DIMENSIONS ARE IN MILLIMETERS
(2)LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX



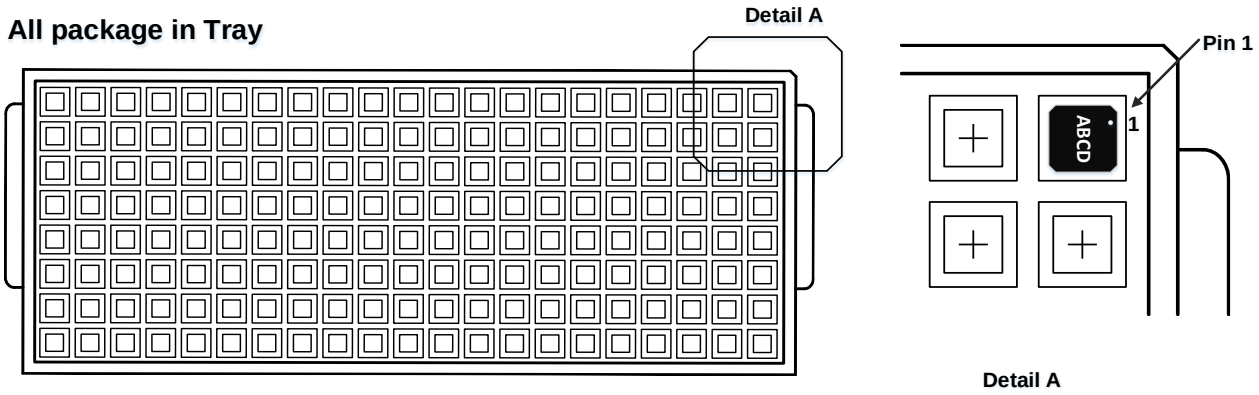
TOP VIEW



BOTTOM VIEW



CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPC22168-170-T	LGA-72 (9mmx9.9mmx 7.65mm)	N/A	N/A	160	N/A	N/A	N/A

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	7/5/2024	Initial Release	-