DESCRIPTION
The MP9943 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. It offers a very compact solution to achieve a 3A peak output current with excellent load and line regulation over a wide input supply range. The MP9943 has synchronous mode operation for higher efficiency over the output current load range.

Current-mode operation provides fast transient response and eases loop stabilization.

Full protection features include over-current protection and thermal shutdown.

The MP9943 requires a minimal number of readily-available standard external components, and is available in a space-saving QFN-8 (3mmx3mm) package.

FEATURES
- Wide 4V to 36V Continuous Operating Input Range
- 85mΩ/55mΩ Low RDS(on) Internal Power MOSFETs
- High-Efficiency Synchronous Mode Operation
- 410kHz Switching Frequency
- Synchronizes from 200kHz to 2.2MHz External Clock
- High Duty Cycle for Automotive Cold-crank
- Internal Power-Save Mode
- Internal Soft-Start
- Power Good Indicator
- Over Current Protection and Hiccup
- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in an QFN-8 (3mmx3mm) package

APPLICATIONS
- General Consumer
- Multi-Function Printers (MFP)
- Distributed Power Systems

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**ORDERING INFORMATION**

<table>
<thead>
<tr>
<th>Part Number*</th>
<th>Package</th>
<th>Top Marking</th>
</tr>
</thead>
<tbody>
<tr>
<td>MP9943GQ</td>
<td>QFN-8 (3mmx3mm)</td>
<td>See Below</td>
</tr>
</tbody>
</table>

* For Tape & Reel, add suffix –Z (e.g. MP9943GQ–Z);

**TOP MARKING**

AMGY
LLL

AMG: product code of MP9943GQ;
Y: year code;
LLL: lot number;

**PACKAGE REFERENCE**

![QFN-8 (3mmx3mm) Top View Diagram]

QFN-8 (3mmx3mm)
ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ............................................... -0.3V to 40V
V_{SW} ............................................... -0.3V to 41V
V_{BS} ............................................. V_{SW}+6V
All Other Pins .................................. -0.3V to 6V (2)

Continuous Power Dissipation (T_A = +25°C) (3)
QFN-8 (3mmx3mm) .................................. 2.27W
Junction Temperature .......................... 150°C
Lead Temperature ............................... 260°C
Storage Temperature ..................... -65°C to 150°C

Recommended Operating Conditions (4)
Continuous Supply Voltage V_{IN} .......... 4V to 36V
Output Voltage V_{OUT} .................. 0.8V to D_{MAX}V_{IN}
Operating Junction Temp (T_J) .......... -40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}
QFN-8 (3mmx3mm) .......................... 55 ....... 13... °C/W

Notes:
1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) About the details of EN/SYNC pin's ABS MAX rating, please refer to page 12, Enable/Sync control section.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operation condition.
5) Measured on JESD51-7, 4-layer PCB.
## ELECTRICAL CHARACTERISTICS

$V_{IN} = 12V$, $T_j = +25^\circ C$, unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Current (Shutdown)</td>
<td>$I_{SHDN}$</td>
<td>$V_{EN} = 0V$</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>Supply Current (Quiescent)</td>
<td>$I_Q$</td>
<td>$V_{EN} = 2V, V_{FB} = 1V$</td>
<td>0.5</td>
<td>0.7</td>
<td>0.7</td>
<td>mA</td>
</tr>
<tr>
<td>HS Switch-ON Resistance</td>
<td>$R_{ON_HS}$</td>
<td>$V_{BST-SW}=5V$</td>
<td>85</td>
<td>105</td>
<td>105</td>
<td>mΩ</td>
</tr>
<tr>
<td>LS Switch-ON Resistance</td>
<td>$R_{ON_LS}$</td>
<td>$V_{CC}=5V$</td>
<td>55</td>
<td>75</td>
<td>75</td>
<td>mΩ</td>
</tr>
<tr>
<td>Switch Leakage</td>
<td>$I_{LKG_SW}$</td>
<td>$V_{EN} = 0V, V_{SW}=12V$</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>Current Limit</td>
<td>$I_{LIMIT}$</td>
<td>Under 40% Duty Cycle</td>
<td>3.2</td>
<td>4.4</td>
<td>5.5</td>
<td>$A$</td>
</tr>
<tr>
<td>Oscillator Frequency</td>
<td>$f_{SW}$</td>
<td>$V_{FB}=750mV$</td>
<td>320</td>
<td>410</td>
<td>500</td>
<td>kHz</td>
</tr>
<tr>
<td>Fold-Back Frequency</td>
<td>$f_{FB}$</td>
<td>$V_{FB}&lt;400mV$</td>
<td>70</td>
<td>100</td>
<td>130</td>
<td>kHz</td>
</tr>
<tr>
<td>Maximum Duty Cycle</td>
<td>$D_{MAX}$</td>
<td>$V_{FB}=750mV, 410kHz$</td>
<td>92</td>
<td>95</td>
<td>95</td>
<td>%</td>
</tr>
<tr>
<td>Minimum ON Time</td>
<td>$t_{ON_MIN}$</td>
<td></td>
<td>70</td>
<td>70</td>
<td>70</td>
<td>ns</td>
</tr>
<tr>
<td>Sync Frequency Range</td>
<td>$f_{SYNC}$</td>
<td></td>
<td>0.2</td>
<td>2.4</td>
<td>2.4</td>
<td>MHz</td>
</tr>
<tr>
<td>Feedback Voltage</td>
<td>$V_{FB}$</td>
<td></td>
<td>778</td>
<td>792</td>
<td>806</td>
<td>mV</td>
</tr>
<tr>
<td>Feedback Current</td>
<td>$I_{FB}$</td>
<td>$V_{FB}=820mV$</td>
<td>10</td>
<td>100</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td>EN Rising Threshold</td>
<td>$V_{EN_RISING}$</td>
<td></td>
<td>1.15</td>
<td>1.4</td>
<td>1.65</td>
<td>V</td>
</tr>
<tr>
<td>EN Falling Threshold</td>
<td>$V_{EN_FALLING}$</td>
<td></td>
<td>1.05</td>
<td>1.25</td>
<td>1.45</td>
<td>V</td>
</tr>
<tr>
<td>EN Threshold Hysteresis</td>
<td>$V_{EN_HYS}$</td>
<td></td>
<td>150</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>EN Input Current</td>
<td>$I_{EN}$</td>
<td>$V_{EN}=2V$</td>
<td>4</td>
<td>6</td>
<td>6</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$V_{EN}=0$</td>
<td></td>
<td></td>
<td>0</td>
<td>0.2</td>
<td>0.2</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>VIN Under-Voltage Lockout Threshold-Rising</td>
<td>$INUVRISING$</td>
<td></td>
<td>3.3</td>
<td>3.5</td>
<td>3.7</td>
<td>V</td>
</tr>
<tr>
<td>VIN Under-Voltage Lockout Threshold-Falling</td>
<td>$INUVFALLING$</td>
<td></td>
<td>3.1</td>
<td>3.3</td>
<td>3.5</td>
<td>V</td>
</tr>
<tr>
<td>VIN Under-Voltage Lockout Threshold-Hysteresis</td>
<td>$INUVHYS$</td>
<td></td>
<td>200</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>VCC Regulator</td>
<td>$V_{CC}$</td>
<td>$I_{CC}=0mA$</td>
<td>4.6</td>
<td>4.9</td>
<td>5.2</td>
<td>V</td>
</tr>
<tr>
<td>VCC Load Regulation</td>
<td></td>
<td>$I_{CC}=5mA$</td>
<td>1.5</td>
<td>4</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>Soft-Start Period</td>
<td>$t_{SS}$</td>
<td>From 10% to 90%</td>
<td>0.45</td>
<td>1.5</td>
<td>2.55</td>
<td>ms</td>
</tr>
<tr>
<td>Thermal Shutdown $^{(6)}$</td>
<td>$T_{SD}$</td>
<td></td>
<td>150</td>
<td>170</td>
<td></td>
<td>$^\circ C$</td>
</tr>
<tr>
<td>Thermal Hysteresis $^{(6)}$</td>
<td>$T_{SD_HYS}$</td>
<td></td>
<td>30</td>
<td></td>
<td></td>
<td>$^\circ C$</td>
</tr>
<tr>
<td>PG Rising Threshold</td>
<td>$PG_{Vih_RISING}$</td>
<td>as percentage of $V_{FB}$</td>
<td>86</td>
<td>90</td>
<td>94</td>
<td>%</td>
</tr>
<tr>
<td>PG Falling Threshold</td>
<td>$PG_{Vih_FALLING}$</td>
<td>as percentage of $V_{FB}$</td>
<td>80</td>
<td>84</td>
<td>88</td>
<td>%</td>
</tr>
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</table>
## ELECTRICAL CHARACTERISTICS (continued)

$V_{\text{IN}} = 12V$, $T_J = +25^\circ\text{C}$, unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>PG Threshold Hysteresis</td>
<td>$PG_{V_{th,\text{HYS}}}$</td>
<td>as percentage of $V_{FB}$</td>
<td>6</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>PG Rising Delay</td>
<td>$PG_{T_{d,\text{RISING}}}$</td>
<td></td>
<td>40</td>
<td>90</td>
<td>160</td>
<td>$\mu$s</td>
</tr>
<tr>
<td>PG Falling Delay</td>
<td>$PG_{T_{d,\text{FALLING}}}$</td>
<td></td>
<td>30</td>
<td>55</td>
<td>95</td>
<td>$\mu$s</td>
</tr>
<tr>
<td>PG Sink Current Capability</td>
<td>$V_{PG}$</td>
<td>Sink 4mA</td>
<td>0.1</td>
<td>0.3</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>PG Leakage Current</td>
<td>$I_{LKG,\text{PG}}$</td>
<td></td>
<td>10</td>
<td>100</td>
<td></td>
<td>nA</td>
</tr>
</tbody>
</table>

**Notes:**
6) Derived from bench characterization. Not tested in production.
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 12\, \text{V}$, $V_{OUT} = 3.3\, \text{V}$, $L = 10\, \mu\text{H}$, $R_{BST}=20\, \Omega$, $T_A = +25^\circ\text{C}$, unless otherwise noted.

**Efficiency vs. Load Current**

- $V_{OUT}=3.3\, \text{V}$
- $V_{OUT}=5\, \text{V}$

**Thermal Rise**

- $V_{IN}=12\, \text{V}$
- $V_{IN}=24\, \text{V}$

**Load Regulation**

- $I_{OUT}=0\, \text{A}$
- $I_{OUT}=1.5\, \text{A}$
- $I_{OUT}=3\, \text{A}$

**Line Regulation**

- $V_{IN}=24\, \text{V}$
- $V_{IN}=12\, \text{V}$

$V_{OUT}=3\, \text{V}$, $L = 10\, \mu\text{H}$, $R_{BST}=20\, \Omega$, $T_A = +25^\circ\text{C}$, unless otherwise noted.
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 12V$, $V_{OUT} = 3.3V$, $L = 10\mu H$, $R_{BST}=20\Omega$, $T_A = +25^\circ C$, unless otherwise noted.

Steady State

Steady State

Steady State

Startup Through $V_{IN}$

Startup Through $V_{IN}$

Shutdown Through $V_{IN}$

Startup Through $EN$

Startup Through $EN$

Startup Through $EN$
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 12\text{V}$, $V_{OUT} = 3.3\text{V}$, $L = 10\mu\text{H}$, $R_{BST}=20\Omega$, $T_A = +25^\circ\text{C}$, unless otherwise noted.
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 12\text{V}$, $V_{OUT} = 3.3\text{V}$, $L = 10\mu\text{H}$, $R_{BST}=20\Omega$, $T_A = +25^\circ\text{C}$, unless otherwise noted.

Cold-Crank

$V_{OUT}=5\text{V}$, $I_{OUT}=3\text{A}$
## PIN FUNCTIONS

<table>
<thead>
<tr>
<th>Package Pin #</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 FB</td>
<td>Feedback. Connect to the tap of an external resistor divider from the output to GND, to set the output voltage. The frequency fold-back comparator lowers the oscillator frequency when the FB voltage is below 660mV to prevent current limit runaway during a short-circuit fault condition.</td>
<td></td>
</tr>
<tr>
<td>2 VCC</td>
<td>Bias Supply. Decouple with 0.1μF-to-0.22μF capacitor. Select a capacitor that does not exceed 0.22μF</td>
<td></td>
</tr>
<tr>
<td>3 EN/SYNC</td>
<td>Enable/Synchronize. EN/SYNC high to enable the MP9943. Apply an external clock to the EN/SYNC pin to change the switching frequency.</td>
<td></td>
</tr>
<tr>
<td>4 BST</td>
<td>Bootstrap. Requires a capacitor connected between SW and BST pins to form a floating supply across the high-side switch driver. A 20Ω resistor placed between SW and BST cap is strongly recommended to reduce SW spike voltage.</td>
<td></td>
</tr>
<tr>
<td>5 GND</td>
<td>System Ground. This pin is the reference ground of the regulated output voltage, and PCB layout requires special care. For best results, connect to GND with copper traces and vias.</td>
<td></td>
</tr>
<tr>
<td>6 SW</td>
<td>Switch Output. Connect with a wide PCB trace.</td>
<td></td>
</tr>
<tr>
<td>7 IN</td>
<td>Supply Voltage Input. The MP9943 operates from a 4V to 36V input rail. Requires C1 to decouple the input rail. Connect using a wide PCB trace.</td>
<td></td>
</tr>
<tr>
<td>8 PG</td>
<td>Power Good. The output of this pin is an open drain and goes high if the output voltage exceeds 90% of the nominal voltage.</td>
<td></td>
</tr>
</tbody>
</table>
Figure 1: Functional Block Diagram
OPERATION

The MP9943 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. It offers a very compact solution to achieve 3A peak output current with excellent load and line regulation over a wide input supply range.

When MP9943 operates in a fixed-frequency, peak-current-control mode to regulate the output voltage. An internal clock initiates a PWM cycle. The integrated high-side power MOSFET turns on and remains on until its current reaches the value set by the COMP voltage. When the power switch is off, it remains off until the next clock cycle starts. If the current in the power MOSFET does not reach the current value set by COMP within 95% of one PWM period, the power MOSFET will be forced to turn off.

Internal Regulator

The 5V internal regulator power most of the internal circuitries. This regulator is supplied by the V_IN input and operates in the full V_IN range: When V_IN exceeds 5.0V, the output of the regulator is in full regulation; when V_IN falls below 5.0V, the output of the regulator decreases following the VIN. A 0.1uF decoupling ceramic capacitor is needed at the pin.

Error Amplifier

The error amplifier compares the FB pin voltage against the internal 0.8V reference (REF) and outputs a COMP voltage—this COMP voltage controls the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies the control loop design.

Power Save Mode for Light Load Condition

The MP9943 has AAM (Advanced Asynchronous Modulation) power-save mode for light load. The AAM threshold is fixed internally. Under the heavy load condition, the V_COMP is higher than V_AAM. When the clock goes high, the high-side power MOSFET turns on and remains on until V_Lsense reaches the value set by the COMP voltage. The internal clock resets every time when V_COMP is higher than V_AAM.

Under the light load condition, the value of V_COMP is low. When V_COMP is less than V_AAM and V_FB is less than V_REF, V_COMP ramps up until it exceeds V_AAM. During this time, the internal clock is blocked, thus the MP9943 skips some pulses for PFM (Pulse Frequency Modulation) mode and achieves the light load power save.

Enable/SYNC control

EN/SYNC is a digital control pin that turns the regulator on and off. Drive EN/SYNC high to turn on the regulator, drive it low to turn it off. An internal 500kΩ resistor from EN/SYNC to GND allows EN/SYNC to be floated to shut down the chip.

The EN/SYNC pin is clamped internally using a 6.5V series Zener diode, as shown in Figure 3. Connect the EN/SYNC input pin through a pullup resistor to any voltage connected to the VIN pin—the pullup resistor limits the EN/SYNC input current to less than 150µA.

For example, with 12V connected to V_IN, R_PULLUP ≥ (12V – 6.5V) ÷ 150µA = 36.7kΩ.

Connecting the EN/SYNC pin directly to a voltage source without any pullup resistor requires limiting voltage amplitude to ≤6V to prevent damage to the Zener diode.
Under-Voltage Lockout
Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP9943 UVLO comparator monitors the output voltage of the internal regulator, VCC. The UVLO rising threshold is about 3.5V while its falling threshold is 3.3V.

Internal Soft-Start
The soft-start prevents the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) that ramps up from 0V to 1.2V. When SS is lower than REF, SS overrides REF so the error amplifier uses SS as the reference. When SS exceeds REF, the error amplifier uses REF as the reference. The SS time is internally set to 1.5ms.

Over-Current Protection and Hiccup
The MP9943 has cycle-by-cycle over current limit when the inductor current peak value exceeds the set current limit threshold. If the output voltage starts to drop until FB is below the Under-Voltage (UV) threshold—typically 84% below the reference—the MP9943 enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-shorted to ground. The average short-circuit current is greatly reduced to alleviate the thermal issue and to protect the regulator. The MP9943 exits the hiccup mode once the over-current condition is removed.

Thermal Shutdown
Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 170°C, it shuts down the whole chip. When the temperature drops below its lower threshold (typically 140°C) the chip is enabled again.

Floating Driver and Bootstrap Charging
An external bootstrap capacitor power the floating-power-MOSFET driver. A dedicated internal regulator (see Figure 4) charges and regulates the bootstrap capacitor voltage to ~5V. When the voltage between the BST and SW nodes drops below regulation, a PMOS pass transistor connected from V_IN to BST turns on. The charging current path is from V_IN, BST and then to SW. The external circuit should provide enough voltage headroom to facilitate charging. As long as V_IN is significantly higher than SW, the bootstrap capacitor remains charged. When the HS-FET is on, V_IN ≈ V_SW, so the bootstrap capacitor can't be charged. When the LS-FET is on, V_IN=V_SW reaches its maximum for fast charging. When there is no inductor current, V_SW=V_OUT, so the difference between V_IN and V_OUT can charge the bootstrap capacitor. The floating driver has its own UVLO protection, with a rising threshold of 2.2V and hysteresis of 150mV. A 20Ω resistor placed between SW and BST cap is strongly recommended to reduce SW spike voltage.

Figure 4: Internal Bootstrap Charging Circuit

Startup and Shutdown
If both V_IN and V_EN/SYNC exceed their appropriate thresholds, the chip starts: The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries.

Three events can shut down the chip: V_EN/SYNC low, V_IN low, and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

Power Good
The MP9943 has power good (PG) output. The PG pin is the open drain of a MOSFET. It should be connected to VCC or some other voltage source through a resistor (e.g. 100kΩ). In the presence of an input voltage, the MOSFET turns on so that the PG pin is pulled to low before SS
is ready. After $V_{FB}$ reaches 90%×REF, the PG pin is pulled high after a delay, typically 90μs. When $V_{FB}$ drops to 84%×REF, the PG pin is pulled low. Also, PG is pulled low if thermal shutdown or EN/SYNC is pulled low.
APPLICATION INFORMATION

Setting the Output Voltage
The external resistor divider sets the output voltage (see Typical Application on page 1). Choose R7 around 41.2kΩ. R8 is then given by:

\[ R8 = \frac{R7}{\frac{V_{OUT}}{0.792V} - 1} \]

The T-type network—as shown in Figure 5—is highly recommended when V_{OUT} is low.

![Figure 5: T-Type Network](image)

RT+R7 is used to set the loop bandwidth. Basically, higher RT+R7, lower bandwidth. To ensure the loop stability, it strongly recommended to limit the bandwidth lower than 40kHz based on the 410kHz default fsw. Table 1 lists the recommended T-type resistors value for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

<table>
<thead>
<tr>
<th>V_{OUT} (V)</th>
<th>R7 (kΩ)</th>
<th>R8 (kΩ)</th>
<th>RT (kΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3</td>
<td>41.2 (1%)</td>
<td>13 (1%)</td>
<td>51 (1%)</td>
</tr>
<tr>
<td>5</td>
<td>41.2 (1%)</td>
<td>7.68 (1%)</td>
<td>51 (1%)</td>
</tr>
</tbody>
</table>

Notes:
7) The recommended parameters is basing on 410kHz switching frequency. Different input voltage, output inductor value and output capacitor value may affect the select of R7, R8 and RT. For other components' parameters, please refer to TYPICAL APPLICATION CIRCUITS on page 19.

Selecting the Inductor
Use a 1µH-to-10µH inductor with a DC current rating of at least 25% percent higher than the maximum load current for most applications. For highest efficiency, an inductor with small DC resistance is recommended. For most designs, the inductance value can be derived from the following equation.

\[ L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_{L} \times f_{OSC}} \]

Where \( \Delta I_{L} \) is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current is:

\[ I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_{L}}{2} \]

Use a larger inductor for improved efficiency under light-load conditions—below 100mA.

VIN UVLO Setting
MP9943 has internal fix under voltage lock out (UVLO) threshold: rising threshold is 3.5V while falling threshold is about 3.3V. For the application needs higher UVLO point, external resistor divider between EN/SYNC and IN as shown in Figure 6 can be used to get higher equivalent UVLO threshold.

![Figure 6: Adjustable UVLO using EN/SYNC divider](image)

The UVLO threshold can be computed from below two equations:

\[ I_{NUV, RISING} = (1 + \frac{R_{EN_UP}}{500k/R_{EN_DOWN}}) \times V_{EN, RISING} \]

\[ I_{NUV, FALLING} = (1 + \frac{R_{EN_UP}}{500k/R_{EN_DOWN}}) \times V_{EN, FALLING} \]

Where \( V_{EN, RISING}=1.4V \), \( V_{EN, FALLING}=1.25V \).

When choose \( R_{EN_UP} \), make sure it is big enough to limit the current flows into EN/SYNC pin lower than 150µA.
Selecting the Input Capacitor
The input current to the step-down converter is discontinuous, therefore requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Use ceramic capacitors with X5R or X7R dielectrics for best results because of their low ESR and small temperature coefficients.

For most application, a 22µF ceramic capacitor is sufficient to maintain the DC input voltage. It is strongly recommended to use a lower value capacitor (e.g. 1µF) to absorb high frequency switching noise. Make sure the small size capacitor is close to IN and GND pins as possible (see PCB LAYOUT section).

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

\[ I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)} \]

The worse case condition occurs at \( V_{IN} = 2V_{OUT} \), where:

\[ I_{C1} = \frac{I_{LOAD}}{2} \]

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high quality ceramic capacitor (e.g. 1µF) placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

\[ \Delta V_{in} = \frac{I_{LOAD}}{f_6 \times C1} \times \left( 1 - \frac{V_{OUT}}{V_{IN}} \right) \]

Selecting the Output Capacitor
The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated by:

\[ \Delta V_{OUT} = \frac{V_{OUT}}{f_6 \times L_1} \times \left( 1 - \frac{V_{OUT}}{V_{IN}} \right) \times \left( R_{ESR} + \frac{1}{8 \times f_6 \times C2} \right) \]

Where \( L_1 \) is the inductor value and \( R_{ESR} \) is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be approximated to:

\[ \Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_6 \times L_1 \times C2} \times \left( 1 - \frac{V_{OUT}}{V_{IN}} \right) \]

The characteristics of the output capacitor also affect the stability of the regulation system. The MP9943 can be optimized for a wide range of capacitance and ESR values.

The characteristics of the output capacitor also affect the stability of the regulation system. The MP9943 can be optimized for a wide range of capacitance and ESR values.

BST Resistor and External BST Diode
A 20Ω resistor in series with BST capacitor is recommended to reduce the SW spike voltage. Higher resistance is better for SW spike reduction, but will compromise the efficiency on the other hand.

BST voltage may become insufficient at some particular specs. In this case an external bootstrap diode can enhance the efficiency of the regulator and avoid BST voltage insufficient at light load PFM operation. The BST voltage insufficient is more likely to happen at given either of following conditions:
- $V_{IN}$ is below 5V
- $V_{OUT}$ is 5V or 3.3V; and Duty cycle is high:
  \[ D = \frac{V_{OUT}}{V_{IN}} > 65\% \]

In these cases, if BST voltage insufficient happens, the output ripple voltage may become extremely large at light load condition, add an external BST diode from the VCC pin or $V_{OUT}$ to BST pin, as shown in Figure 7.

![Figure 7: Optional External Bootstrap Diode to Enhance Efficiency](image)

The recommended external BST diode is 1N4148, and the BST capacitor value is 0.1µF to 1µF.

**PCB Layout**

PCB layout, especially the input capacitor and VCC capacitor placement, is very important to achieve stable operation. For the best results, follow these guidelines:

1) Place the ceramics input capacitor as close to IN and GND pins as possible, especially the small package size (0603) input bypass capacitor. Keep the connection of input capacitor and IN pin as short and wide as possible.
2) Place the VCC capacitor to VCC pin and GND pin as close as possible. Make the trace length of VCC pin-VCC capacitor anode-VCC capacitor cathode-chip GND pin as short as possible.
3) Use large ground plane directly connect to GND pin. Add vias near the GND pin if bottom layer is ground plane.
4) Route SW, BST away from sensitive analog areas such as FB.
5) Place the T-type feedback resistor close to chip to ensure the trace which connects to FB pin as the short as possible.

![Figure 8: Recommended PCB Layout](image)
Design Example
Below is a design example following the application guidelines for the specifications:

<table>
<thead>
<tr>
<th>Table 2: Design Example</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>V\text{IN}</strong></td>
</tr>
<tr>
<td><strong>V\text{OUT}</strong></td>
</tr>
<tr>
<td><strong>I\text{OUT}</strong></td>
</tr>
</tbody>
</table>

The detailed application schematic is shown in Figure 9. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device applications, please refer to the related Evaluation Board Datasheets.
TYPICAL APPLICATION CIRCUITS

Figure 9: 12V<sub>IN</sub>, 5V/3A Peak Output

Figure 10: 12V<sub>IN</sub>, 3.3V/3A Peak Output
PACKAGE INFORMATION

QFN-8 (3mm x 3mm)

TOP VIEW

BOTTOM VIEW

SIDE VIEW

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

RECOMMENDED LAND PATTERN

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