MP9929

100V Input, Current-Mode, Synchronous Step-Down Controller

DESCRIPTION

The MP9929 is a high-voltage, synchronous, step-down, switching regulator controller that can directly step down voltages from up to 100V. The MP9929 uses pulse-width modulation (PWM) current control architecture with accurate cycle-by-cycle current limiting. It can drive dual N-channel MOSFET switches.

Advanced asynchronous modulation (AAM) mode enables asynchronous operation and pulse-skip mode (PSM) to optimize light-load efficiency.

The MP9929's operating frequency can be configured via an external resistor or synchronized to an external clock for noise-sensitive applications. Fault protections are available, including a precision output over-voltage protection (OVP), output over-current protection (OCP), and thermal shutdown.

The MP9929 is available in a QFN-26 (4mmx6mm) package.

FEATURES

- Up to 100V of Input Voltage (V_{IN})
- 7V to 18V VDRV Voltage (V_{DRV}) Range
- Dual N-Channel MOSFET Driver
- Low-Dropout (LDO) Operation: Maximum Duty Cycle at 99.5%
- Configurable Frequency Range: 100kHz to 1000kHz
- 180° Out-of-Phase SYNCO
- External Soft Start (SS) and PG Pin
- Selectable Cycle-by-Cycle Current Limit
- Output Over-Voltage Protection (OVP)
- Configurable Continuous Conduction Mode (CCM), Advanced Asynchronous Modulation (AAM) Mode, and Pulse-Skip Mode (PSM)
- Over-Temperature Protection (OTP)
- Available in a QFN-26 (4mmx6mm) Package

MPL Optimized Performance with MPS Inductor MPL-AY1265 Series

APPLICATIONS

- Power Delivery (PD) Power Supply in Power over Ethernet (PoE) Systems
- USB Dedicated Charging Ports (DCPs)
- Energy Storage Systems (ESS)
- Industrial Control Systems
- Power Supply for Linear Chargers

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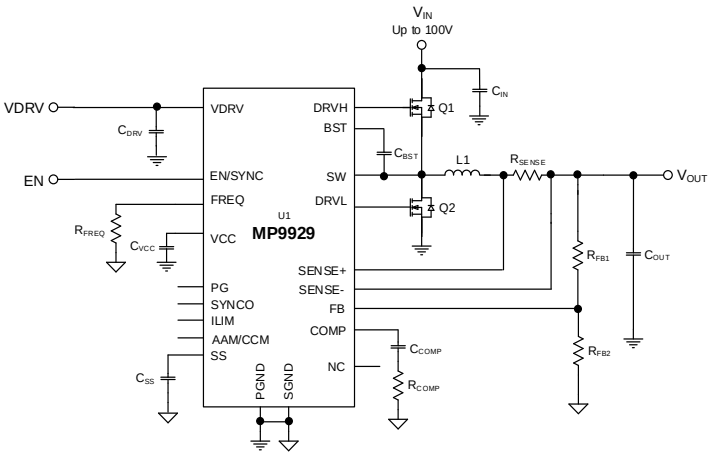
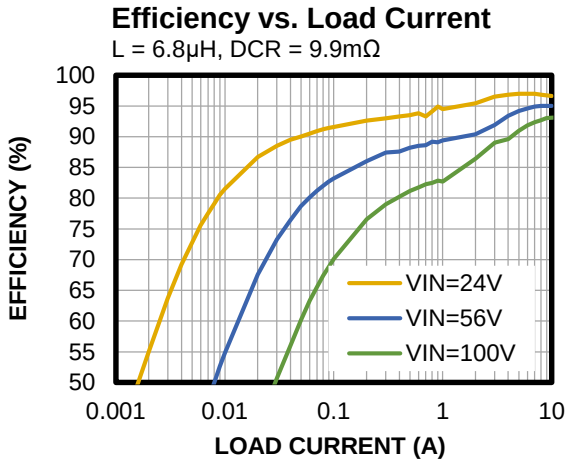
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP9929GQW	QFN-26 (4mmx6mm)	*See Below*	2

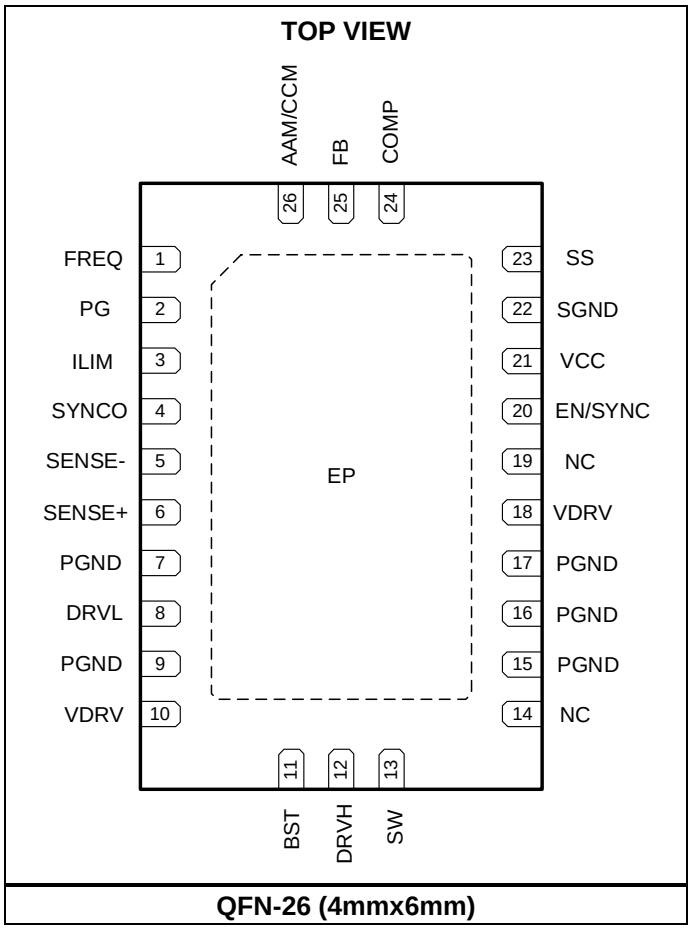
* For Tape & Reel, add suffix -Z (e.g. MP9929GQW-Z).

TOP MARKING

MPSYWW
MP9929
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP9929: Part number
LLLLLL: Lot number

PACKAGE REFERENCE



QFN-26 (4mmx6mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	FREQ	**Switching frequency selection.** Connect a resistor between the FREQ and SGND pins to set the switching frequency (f_{SW}).
2	PG	**Power good output.** The PG pin has an open-drain output.
3	ILIM	**Current limit selection.** The voltage at the ILIM pin (V_{ILIM}) sets the nominal sense voltage at the maximum output current. There are three fixed options: float ILIM, connect ILIM to VCC, or connect ILIM to SGND.
4	SYNCO	**Synchronous signal output.** When the MP9929 works in continuous conduction mode (CCM) or discontinuous conduction mode (DCM) for dual-channel operation, the SYNCO pin outputs a clock that is 180° out-of-phase with the internal oscillator clock or external synchronous clock. SYNCO outputs a DC voltage under certain conditions including sleep mode, low-dropout (LDO) mode, and fault protections.
5	SENSE-	**Negative input for the current sense.** The sensed inductor current (I_L) limit threshold is determined by the ILIM pin's status.
6	SENSE+	**Positive input for the current sense.** The sensed I_L limit threshold is determined by the ILIM pin's status.
7, 9, 15, 16, 17	PGND	**Power ground.** The PGND pin is the power ground reference for the internal low-side MOSFET (LS-FET) driver.
8	DRVL	**Bottom gate driver output.** Connect the DRVL pin to the of the synchronous N-channel MOSFET.
10, 18	VDRV	**Driver power supply and internal circuit supply**. A ceramic capacitor is required at each VDRV pin to prevent large voltage spikes at the input.
11	BST	**Bootstrap.** The BST pin is the positive power supply for the internal, floating high-side MOSFET (HS-FET) driver. Connect a bypass capacitor between the BST and SW pins.
12	DRVH	**High-side (HS) gate driver output.** The DRVH pin drives the gate of the top N-channel MOSFET. The DRVH driver draws power from the BST capacitor (C_{BST}), then returns the power to the SW pin, providing a true floating drive to the top N-channel MOSFET.
13	SW	**Switch node.** The SW pin is the reference for the BST pin voltage (V_{BST}) supply and high current returns for the bootstrapped switch.
14, 19	NC	**Not connected.** Float the NC pins.
20	EN/SYNC	**Enable.** The EN/SYNC pin can be used to implement an input under-voltage lockout (UVLO) function externally. If an external synchronous clock is applied to EN/SYNC, an internal clock follows the synchronous frequency (f_{SYNC}).
21	VCC	**Internal bias supply.** Decouple the VCC pin with a minimum 1µF ceramic capacitor. The capacitance must not exceed 4.7µF.
22	SGND	**Low-noise signal ground reference.**
23	SS	**Soft-start control input.** The SS pin configures the soft-start period (t_{SS}) with an external capacitor connected between the SS and SGND pins.
24	COMP	**Low-impedance output of the internal error amplifier (EA).** The COMP pin compensates for the regulation control loop. Connect an RC network between the COMP and SGND pins to compensate for the regulation control loop.
25	FB	**Feedback.** The FB pin is the input to the EA. An external resistor divider connected between the output and SGND is compared to the internal 0.8V reference voltage (V_{REF}) to set the regulation voltage.

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PIN FUNCTIONS *(continued)*

Pin #	Name	Description
26	AAM/CCM	**Advanced asynchronous modulation (AAM) mode or continuous conduction mode (CCM) setting.** Connect the AAM/CCM pin to VCC or float the pin to enable the MP9929 to work in CCM. Connect a suitable external resistor between the AAM/CCM and SGND pins to set AAM mode at a low level, which enables the part to work in AAM mode. The AAM mode voltage (V_{AAM}) must be a minimum of 480mV.
-	EP	**Thermal exposed pad.** Solder the EP pin to PGND to reduce thermal resistance.

ABSOLUTE MAXIMUM RATINGS (1)

Gate driver voltage (V_{DRV}) ..... -0.3V to +20V
EN/SYNC..... -0.3V to +50V
SW ..... -5V to +105V
BST ..... -0.3V to +110V
BST to SW..... -0.3V to +18V
PG……-0.3V to +6V
SENSE± ..... -0.3V to +28V
Differential sense (SENSE+ to SENSE-).....
..... -0.7V to +0.7V
DRVH to SW..... -0.3V to V_{BST-SW} + 0.3V
DRVL to PGND..... -0.3V to V_{DRV} + 0.3V
All other pins..... -0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2) (3)
QFN-26 (4mmx6mm).....2.3W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) .....±1000V
Charged-device model (CDM) .....±750V

Recommended Operating Conditions (4)

Gate driver voltage (V_{DRV})..... 7V to 18V
SW voltage (V_{SW})..... -1V to +100V
SW slew rate .....<50V/ns
Output voltage (V_{OUT}, R_{SENSE} connected to PGND)……..……≤V_{IN} x D_{MAX}
Output voltage (V_{OUT}, R_{SENSE} connected to V_{OUT})
……..≤24V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance	***θ_{JA}***	***θ_{JC}***
QFN-26(4mmx6mm)		
JESD51-7 (3)……	43.....	9....°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The θ_{JA} value given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.
4) The device is not guaranteed to function outside of its operating conditions.

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ELECTRICAL CHARACTERISTICS

VDRV = 12V, EN = 2V, T_J = -40°C to +125°C (5), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VDRV Supply						
V_{DRV} under-voltage lockout (UVLO) rising threshold	$V_{DRV_UVLO_RISING}$		6.2	6.6	7	V
V_{DRV} UVLO falling threshold	$V_{DRV_UV_FALLING}$		5.6	6	6.4	V
V_{DRV} UVLO hysteresis	$V_{DRV_UVLO_HYS}$			600		mV
VDRV continuous conduction mode (CCM) quiescent current	I_{Q_CCM}	V_{AAM} = 5V, V_{FB} = 0.84V, SENSE+ = SENSE- = 0.3V			1200	µA
VDRV advanced asynchronous modulation (AAM) mode quiescent current	I_{Q_AAM}	V_{AAM} = 0.6V, V_{FB} = 0.84V, SENSE+ = SENSE- = 0.3V			550	µA
VDRV shutdown current	I_{SHDN}	V_{EN} = 0V			400	µA
VCC Regulator						
VCC regulator output voltage from V_{IN}	V_{CC_VIN}	V_{DRV} > 7V		5		V
Reference voltage (V_{REF})						
Reference voltage	V_{REF}	7V ≤ V_{DRV} ≤ 18V, T_J = 25°C	0.792	0.8	0.808	V
		7V ≤ V_{DRV} ≤ 18V, T_J = -40°C to +125°C	0.788	0.8	0.812	V
FB current	I_{FB}	V_{FB} = 0.84V		10		nA
Enable (EN)						
EN rising threshold	V_{EN_RISING}		1.16	1.22	1.28	V
EN falling threshold	$V_{EN_FALLING}$		1.03	1.09	1.15	V
EN threshold hysteresis	V_{EN_TH}			130		mV
EN input current	I_{EN}	V_{EN} = 2V		2		µA
EN turn-off delay	t_{OFF}		10	20		µs
Oscillator and Synchronous Signal						
Operating frequency	f_{SW}	R_{FREQ} = 65kΩ	240	300	360	kHz
Foldback operating frequency	$f_{SW_FOLDBACK}$	V_{FB} = 0.1V		50		% of f_{SW}
Maximum configurable frequency	f_{SWH}		1000			kHz
Minimum configurable frequency	f_{SWL}				100	kHz
EN/SYNC frequency range	f_{SYNC}		100		1000	kHz
EN/SYNC rising threshold	V_{SYNC_RISING}		2			V
EN/SYNC falling threshold	$V_{SYNC_FALLING}$				0.35	V

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ELECTRICAL CHARACTERISTICS *(continued)*

VDRV = 12V, EN = 2V, T_J = -40°C to +125°C (5), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Current Sense						
Current-sense common-mode voltage range	$V_{SENSE±}$		0		24	V
Current limit sense voltage	V_{ILIMIT}	I_{LIM} = SGND, V_{SENSE+} = 3.3V	15	25	35	mV
		I_{LIM} = VCC, V_{SENSE+} = 3.3V	40	50	60	mV
		I_{LIM} = float, V_{SENSE+} = 3.3V	65	75	85	mV
Reverse current limit sense voltage	V_{REV_ILIMIT}	I_{LIM} =SGND, V_{SENSE+} = 3.3V		8		mV
		I_{LIM} = VCC, V_{SENSE+} = 3.3V		17		
		I_{LIM} = float, V_{SENSE+} = 3.3V		24		
Valley current limit	V_{VALLEY_ILIMIT}	I_{LIM} = SGND, V_{SENSE+} = 3.3V		22.5		mV
		I_{LIM} = VCC, V_{SENSE+} = 3.3V		47.5		
		I_{LIM} = float, V_{SENSE+} = 3.3V		72.5		
Sense input current	I_{SENSE}	$V_{SENSE±_CM}$ = 0V		-45		µA
		$V_{SENSE±_CM}$ = 3.3V		115		µA
		$V_{SENSE±_CM}$ > 5V		150		µA
Soft Start (SS)						
Soft-start source current	I_{SS}	V_{SS} = 0.5V	2	4	6	µA
Error Amplifier (EA)						
Error amplifier (EA) transconductance	G_M	ΔV_{EA} = 5mV		500		µA/V
EA open-loop DC gain (6)	A_O			70		dB
EA sink/source current	I_{EA}	V_{FB} = 0.7V / 0.9V		±30		µA
Gate Driver						
DRVL low output voltage	V_{OLL}	Sink 100mA		0.15		V
DRVL high output voltage to rail	V_{OHL}	Source 100mA		0.45		V
DRVH low output voltage	V_{OLH}	Sink 100mA		0.15		V
DRVH high output voltage to rail	V_{OHH}	Source 100mA		0.45		V
DRVL peak pull-down current (6)	I_{OLL}	V_{DRVL} = VDRV = 12V		2.5		A
		V_{DRVL} = VDRV = 16V		3.5		A
DRVL peak pull-up current (6)	I_{OHL}	V_{DRVL} = 0V, VDRV = 12V		1.5		A
		V_{DRVL} = 0V, VDRV = 16V		2.5		A
DRVH peak pull-down current (6)	I_{OLH}	V_{DRVH} = VDRV = 12V		2.5		A
		V_{DRVH} = VDRV = 16V		3.5		A
DRVH peak pull-up current (6)	I_{OHH}	V_{DRVH} = 0V, VDRV = 12V		1.5		A
		V_{DRVH} = 0V, VDRV = 16V		2.5		A
Dead time from DRVH off to DRVL on	$t_{DEAD_FALLING}$	C_{LOAD} = 3.3nF, trigger level 3V (DRVH) to 3V (DRVL)		50		ns
Dead time from DRVL off to DRVH on	t_{DEAD_RISING}	C_{LOAD} = 3.3nF, trigger level 3V (DRVL) to 3V(DRVH)		50		ns
DRVH maximum duty cycle	D_{MAX}	V_{FB} = 0.7V	98	99.5		%
DRVH minimum on time (7)	$t_{ON_MIN_DRVH}$			92		ns

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ELECTRICAL CHARACTERISTICS *(continued)*

VDRV = 12V, EN = 2V, T_J = -40°C to +125°C (5), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
DRVL minimum on time (7)	$t_{ON_MIN_DRVL}$			140		ns
Protections						
Over-voltage (OV) threshold	V_{OV}		110	115	120	% of V_{REF}
OV hysteresis	V_{OV_HYS}			10		% of V_{REF}
Thermal shutdown (7)				150		°C
Thermal shutdown hysteresis (7)				20		°C
Power Good (PG)						
PG low	V_{PG_LOW}	I_{SINK} = 4mA		0.1	0.3	V
PG rising threshold	$V_{PG_VTH_RSING}$	V_{OUT} rising	85	90	96.5	% of V_{REF}
		V_{OUT} falling	101	107	112.5	
PG falling threshold	$V_{PG_VTH_FALLING}$	V_{OUT} falling	81	87	92.5	% of V_{REF}
		V_{OUT} rising	105	110	116.5	
PG threshold hysteresis	$V_{PG_VTH_HYS}$			3		% of V_{REF}
PG leakage current	I_{PG_LK}	V_{PG} = 5V			2	µA
PG delay time	t_{PG_DELAY}	PG rising and falling		25		µs
Advanced Asynchronous Modulation (AAM) Mode or Continuous Conduction Mode (CCM)						
AAM mode output current	I_{AAM}	R_{FREQ} = 65kΩ		9.2		µA
Rising AAM mode threshold required for CCM	V_{CCM_RISING}		2.3			V
Falling AAM mode threshold required for CCM	$V_{CCM_FALLING}$		2.1			V

Notes:

5) Not tested in production. Guaranteed by over-temperature correlation.
6) Not tested in production. Derived by design.
7) Not tested in production. Derived by sample characterization.

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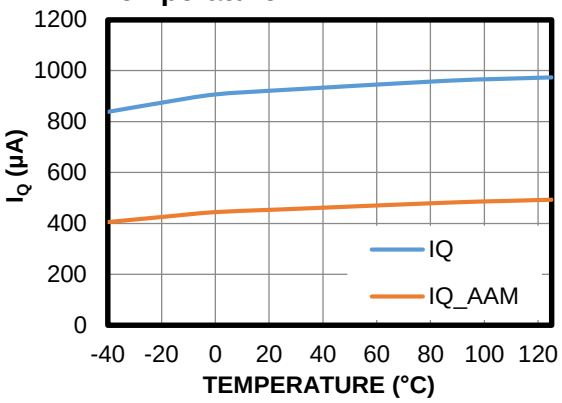
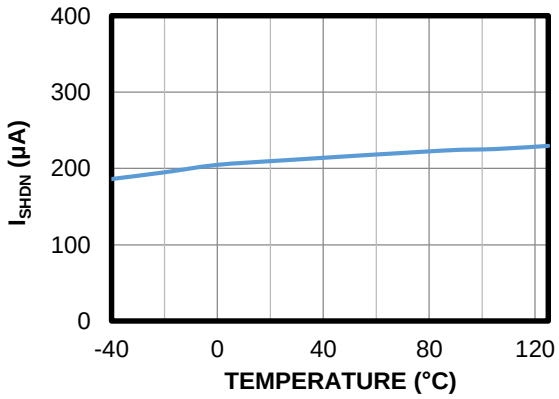
TYPICAL CHARACTERISTICS

V_{IN} = 56V, V_{DRV} = 12V, V_{OUT} = 12V, T_A = 25°C, unless otherwise noted.

Quiescent Supply Current vs. Temperature

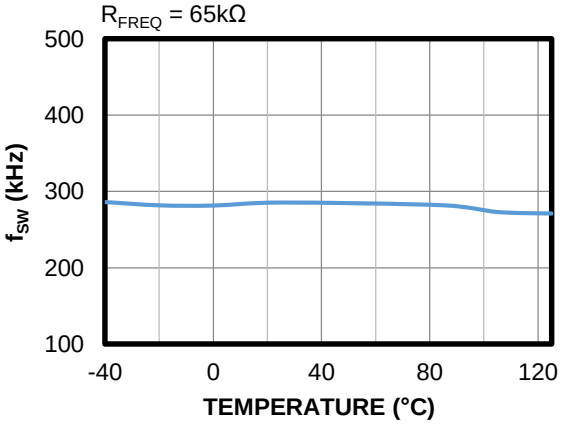


Shutdown Current vs. Temperature

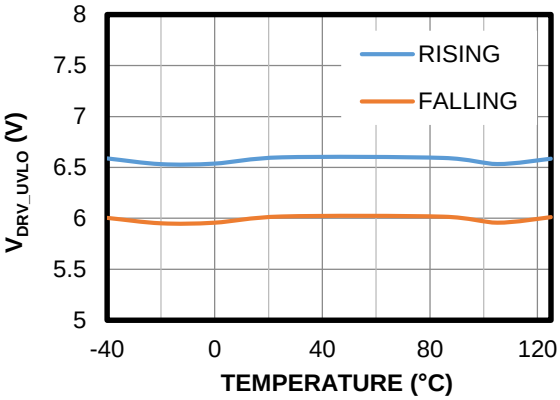


Switching Frequency vs. Temperature

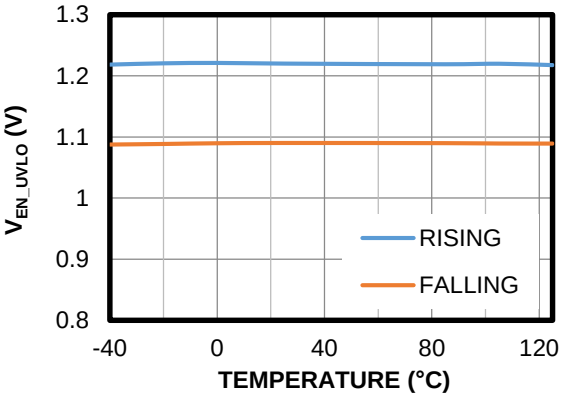
R_{FREQ} = 65kΩ



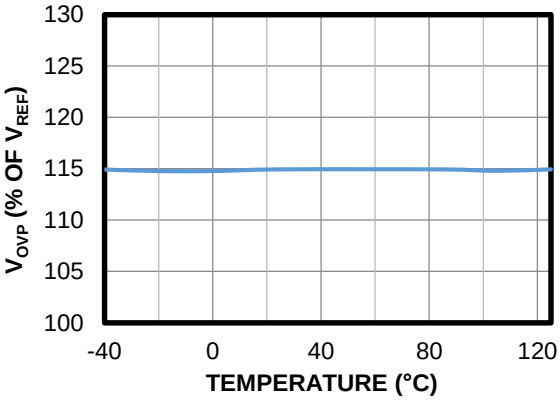
V_{DRV} UVLO Threshold vs. Temperature



EN UVLO Threshold vs. Temperature



OVP Threshold vs. Temperature



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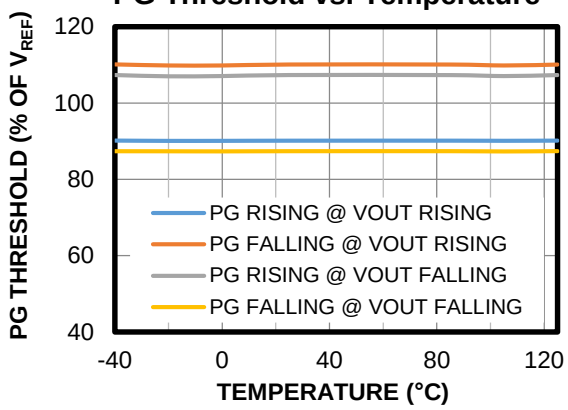
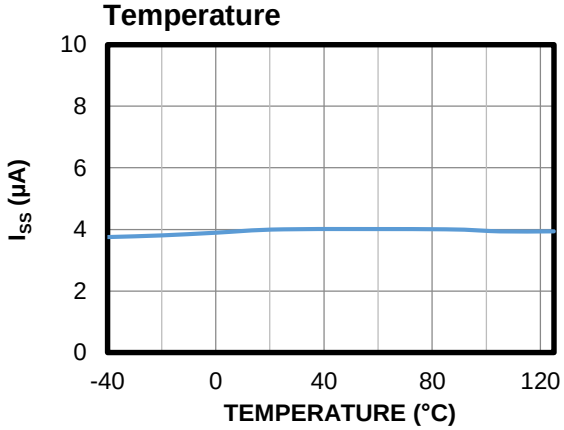
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 56V, V_{DRV} = 12V, V_{OUT} = 12V, T_A = 25°C, unless otherwise noted.

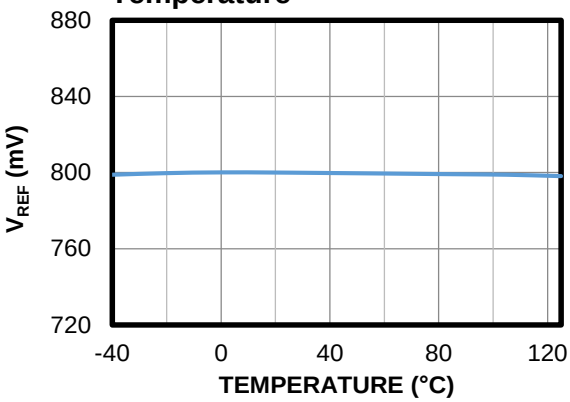
PG Threshold vs. Temperature



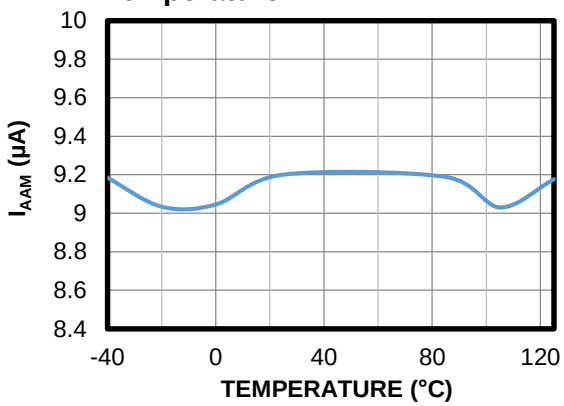
Soft-Start Source Current vs. Temperature



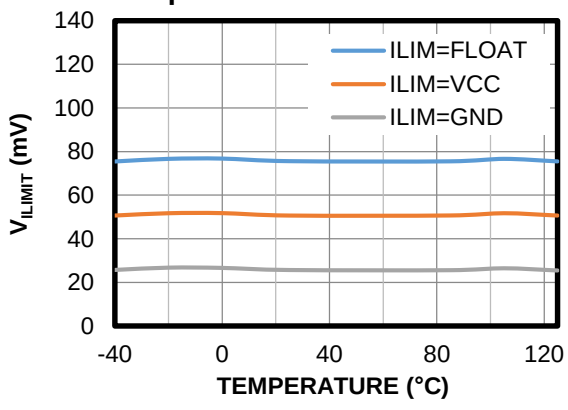
Reference Voltage vs. Temperature



AAM Mode Output Current vs. Temperature

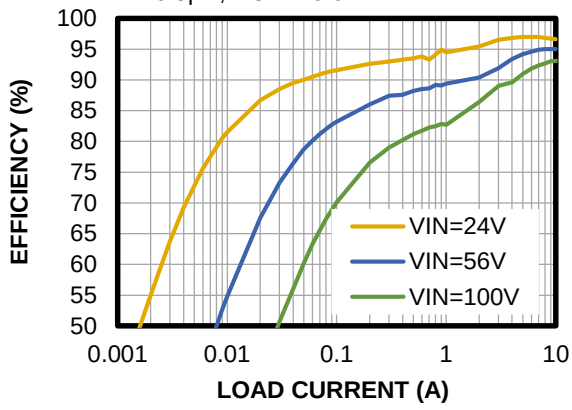


Current Limit Sense Voltage vs. Temperature



Efficiency vs. Load Current

L = 6.8µH, DCR = 9.9mΩ



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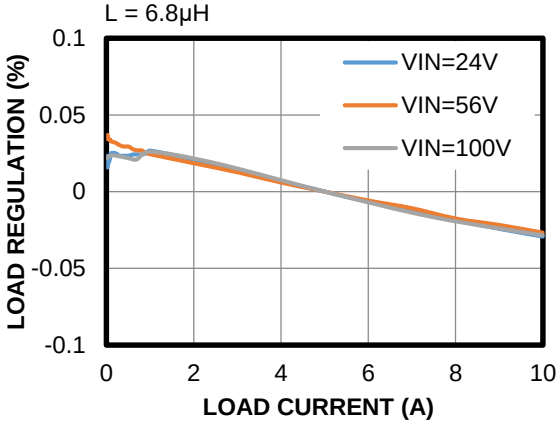
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 56V, V_{DRV} = 12V, V_{OUT} = 12V, T_A = 25°C, unless otherwise noted.

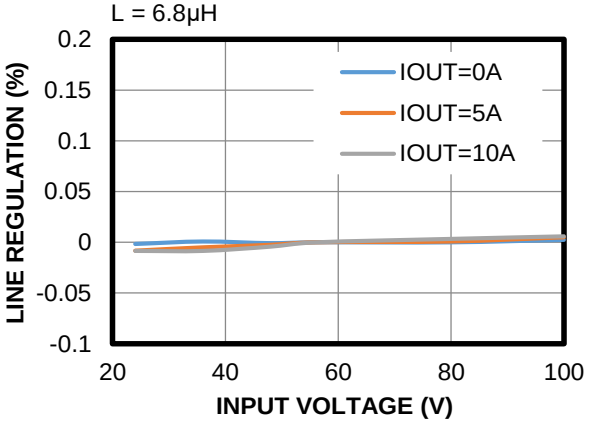
Load Regulation

L = 6.8µH



Line Regulation

L = 6.8µH



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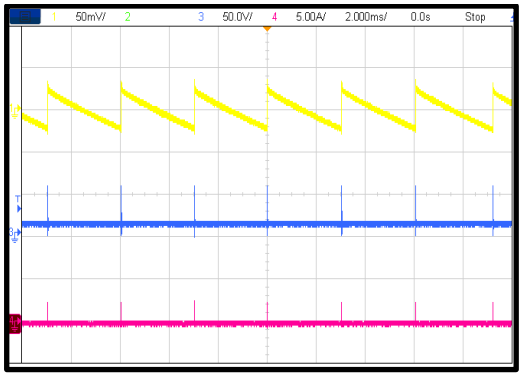
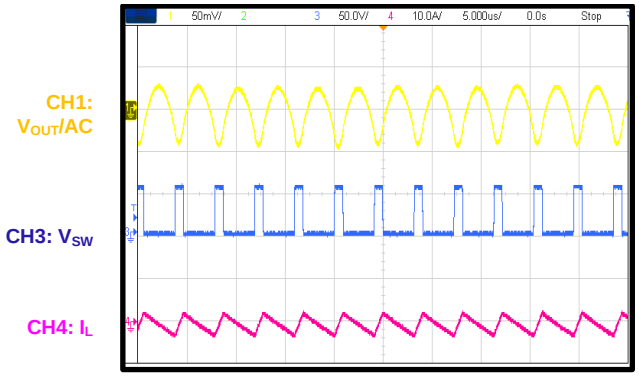
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board in the Design Example section on page 24. V_{IN} = 56V, V_{DRV} = 12V, V_{OUT} = 12V, T_A = 25°C, unless otherwise noted.

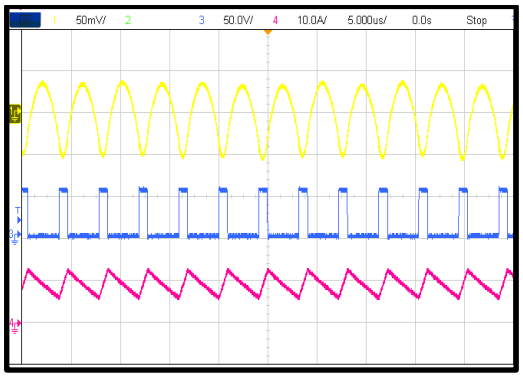
Steady State
I_{OUT} = 0A, AAM mode



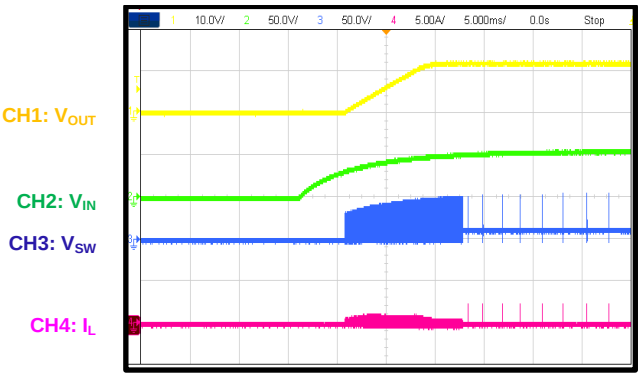
Steady State
I_{OUT} = 0A, FCCM



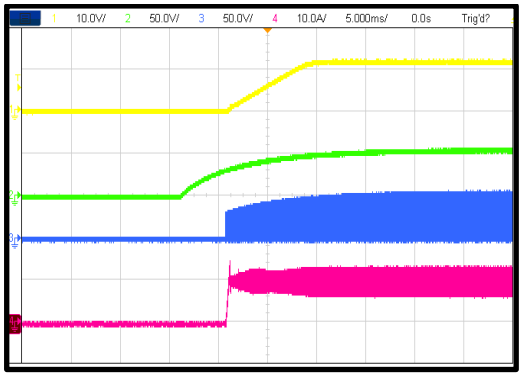
Steady State
I_{OUT} = 10A



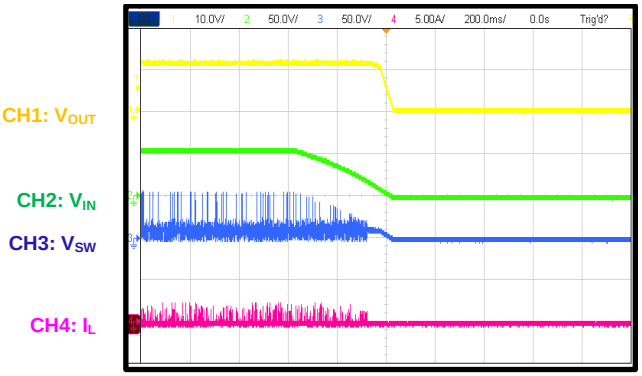
Start-Up through VIN
I_{OUT} = 0A



Start-Up through VIN
I_{OUT} = 10A



Shutdown through VIN
I_{OUT} = 0A



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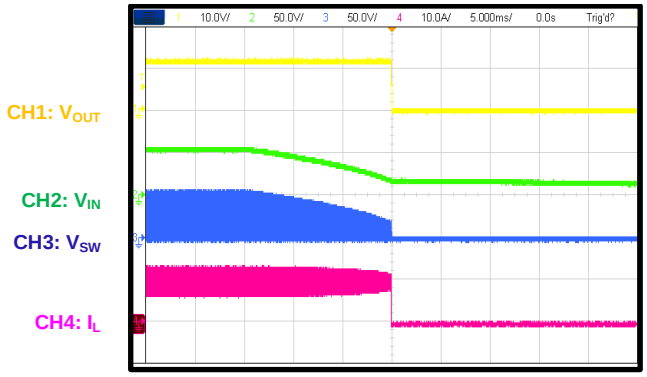
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section on page 24. V_{IN} = 56V, V_{DRV} = 12V, V_{OUT} = 12V, T_A = 25°C, unless otherwise noted.

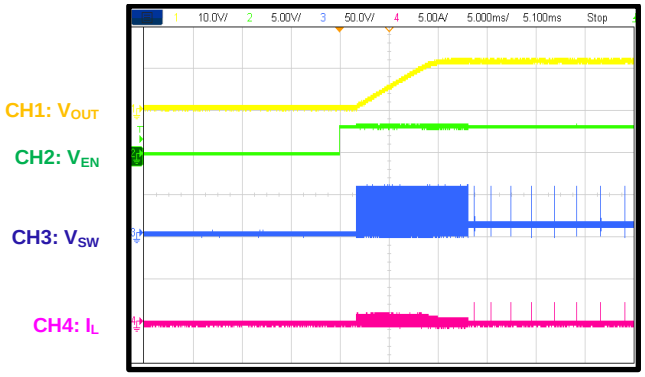
Shutdown through VIN

I_{OUT} = 10A



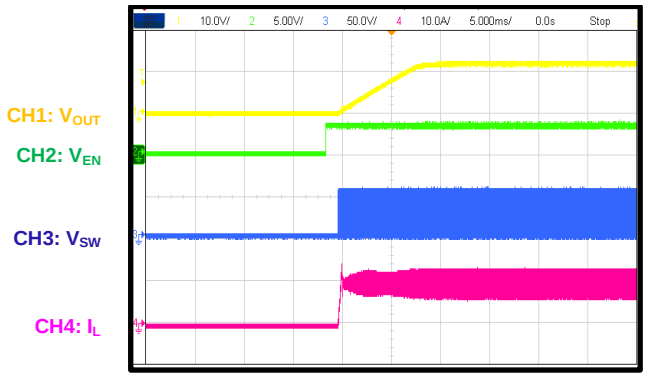
Start-Up through EN

I_{OUT} = 0A



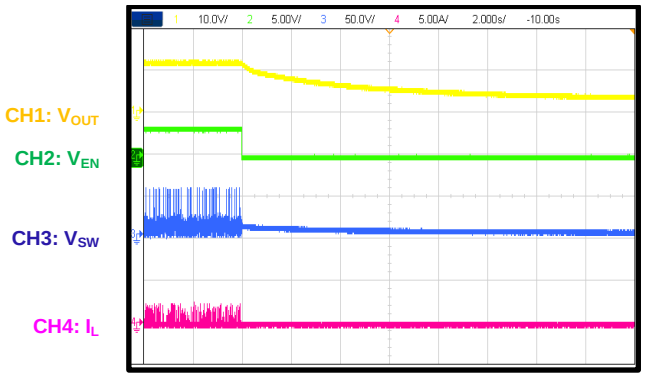
Start-Up through EN

I_{OUT} = 10A



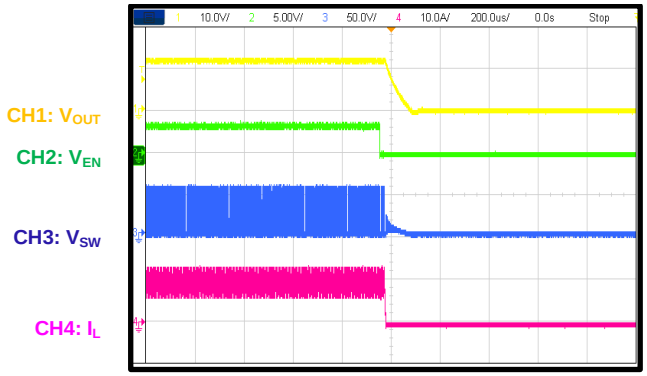
Shutdown through EN

I_{OUT} = 0A



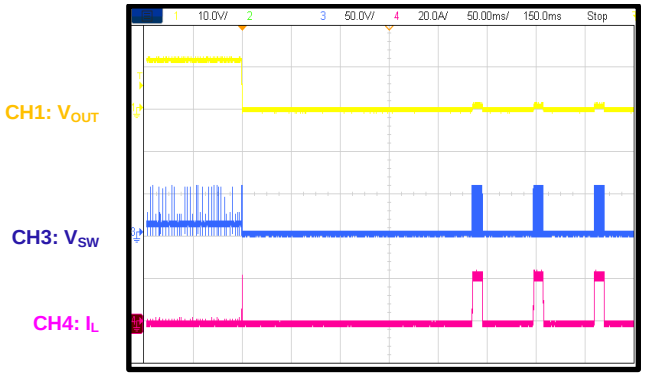
Shutdown through EN

I_{OUT} = 10A



Short-Circuit Protection Entry

I_{OUT} = 0A to short circuit



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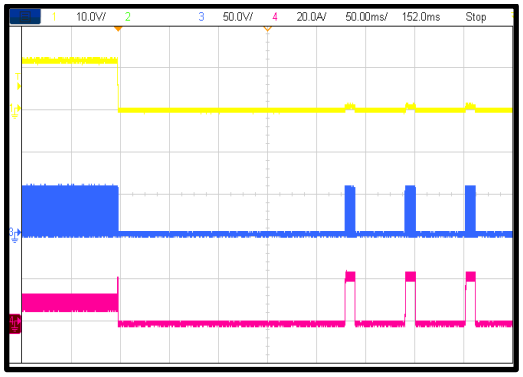
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

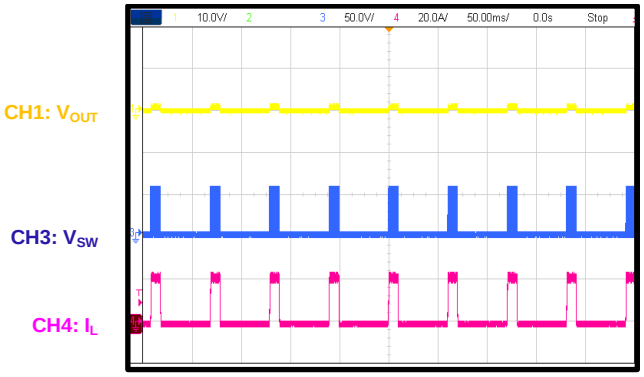
Performance waveforms are tested on the evaluation board in the Design Example section on page 24. V_{IN} = 56V, V_{DRV} = 12V, V_{OUT} = 12V, T_A = 25°C, unless otherwise noted.

Short-Circuit Protection Entry

I_{OUT} = 10A to short circuit

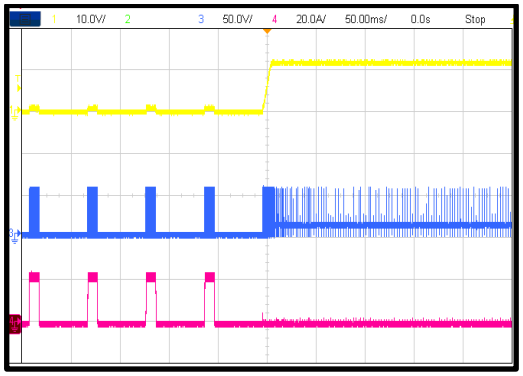


Short-Circuit Protection Steady State



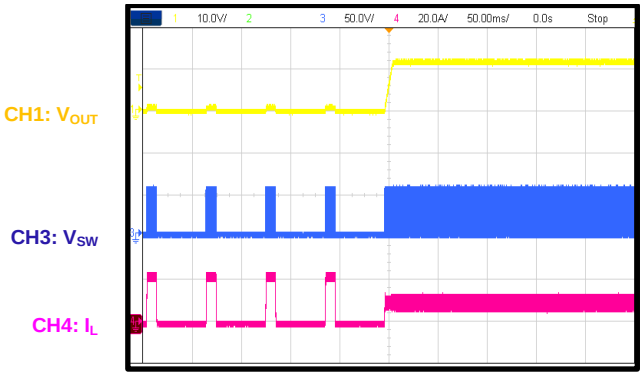
Short-Circuit Protection Recovery

Short circuit to I_{OUT} = 0A



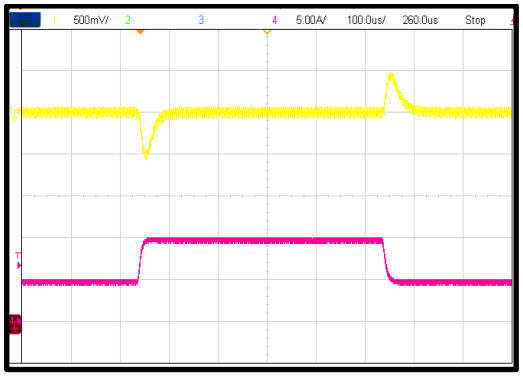
Short-Circuit Protection Recovery

Short circuit to I_{OUT} = 10A



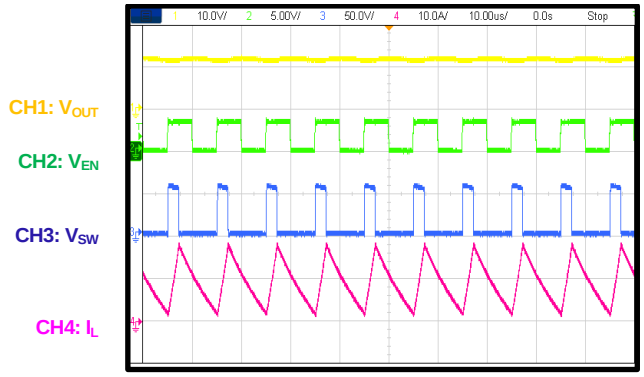
Load Transient

I_{OUT} = 5A to 10A, 500mA/µs



SYNC Function

f_{SYNC} = 100kHz, I_{OUT} = 10A



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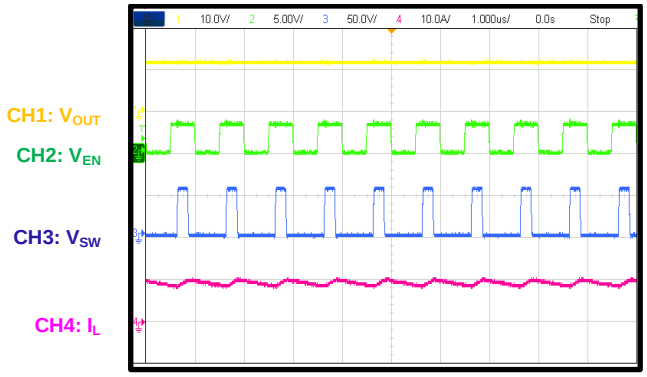
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section on page 24. V_{IN} = 56V, V_{DRV} = 12V, V_{OUT} = 12V, T_A = 25°C, unless otherwise noted.

SYNC Function

f_{SYNC} = 1000kHz, I_{OUT} = 10A



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FUNCTIONAL BLOCK DIAGRAM

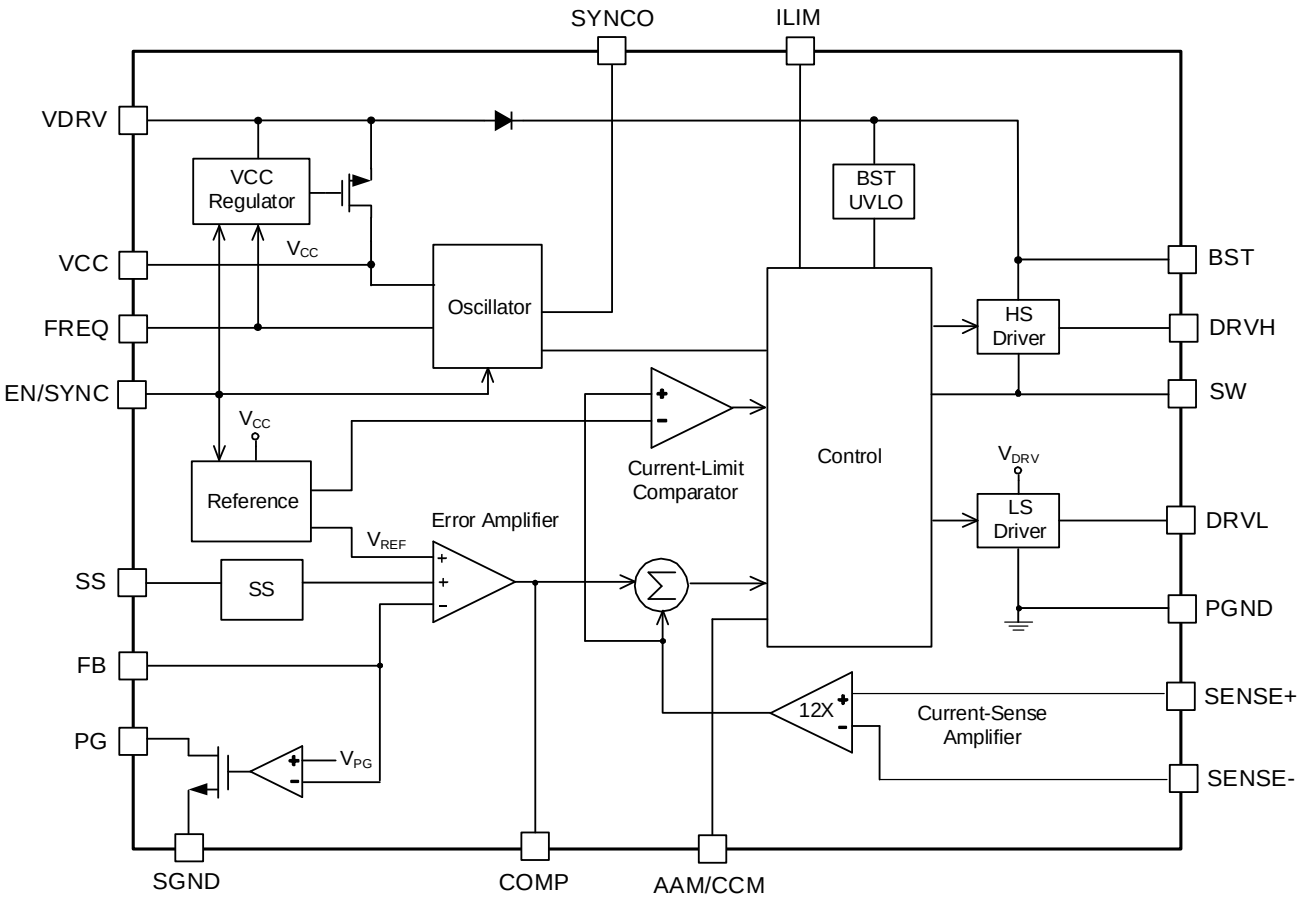

Figure 1: Functional Block Diagram

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OPERATION

Overview

The MP9929 is a high-performance, step-down, synchronous, DC/DC converter controller IC with a wide input voltage (V_{IN}) range. It implements a current-mode, switching frequency (f_{SW}), configurable control architecture to regulate the output voltage (V_{OUT}) with external N-channel MOSFET switches.

The MP9929 senses the voltage at the FB pin (V_{FB}). The difference between V_{FB} and an internal 0.8V reference voltage (V_{REF}) is amplified to generate an error voltage on the COMP pin. This error voltage is used as a threshold for the current-sense comparator with a slope compensation ramp.

Under normal load conditions, the controller operates in full pulse-width modulation (PWM) mode. At the beginning of each oscillator cycle, the top gate driver is enabled. The top gate turns on for a period determined by the duty cycle. When the top gate turns off, the bottom gate turns on after a dead time (DT) and remains on until the beginning of the next clock cycle.

There is an optional power-save mode for light-load or no-load conditions, which is described in further detail below.

Advanced Asynchronous Modulation (AAM) Mode

The MP9929 employs advanced asynchronous modulation (AAM) mode functionality to optimize efficiency during light-load or no-load conditions. AAM mode can be optionally enabled when the AAM/CCM pin is set to a low level by connecting a suitable resistor to SGND. Selecting a suitable resistor ensures that the AAM mode voltage (V_{AAM}) does not drop below 480mV. V_{AAM} can be calculated with Equation (1):

$$V_{AAM}(mV) = I_{AAM}(\mu A) \times R_{AAM}(k\Omega) \quad (1)$$

The AAM mode output current (I_{AAM}) can be calculated with Equation (2):

$$I_{AAM}(\mu A) = 600mV / R_{FREQ}(k\Omega) \quad (2)$$

R_{FREQ} is the resistor connected between the FREQ and SGND pins for a given operating frequency. This frequency can be determined according to the Configurable Switching Frequency section on page 21.

AAM mode is disabled when the AAM/CCM pin is floated or connected to VCC.

If AAM mode is enabled under light-load conditions, and the DC value of the internal COMP voltage ($V_{IN_COMP} = V_{COMP} - V_{OFFSET_COMP}$, where V_{OFFSET_COMP} is about 720mV) is below V_{AAM}, then the MP9929 enters AAM mode. In this mode, the high-side MOSFET (HS-FET) turns on when V_{IN_COMP} exceeds V_{AAM}, then turns off when the inductor current (I_L) reaches the value determined by V_{IN_COMP} and the slope compensation ramp.

The low-side MOSFET (LS-FET) turns on after the HS-FET turns off, then remains on until I_L drops to 0A. When the LS-FET turns off, V_{IN_COMP} remains low for a long period before V_{IN_COMP} exceeds V_{AAM} again due to the slow V_{OUT} drop. During this long period, the no-pulse condition improves efficiency but increases the V_{OUT} ripple. Typically, V_{AAM} is set to ensure that the peak inductor current in AAM mode (I_{PEAK_AAM}) is between hundreds of mA and 2A.

When the load increases and the DC value of V_{IN_COMP} exceeds V_{AAM}, operation changes to discontinuous conduction mode (DCM) or continuous conduction mode (CCM), with a constant f_{SW}. Figure 2 shows the difference in I_L in AAM mode and CCM.

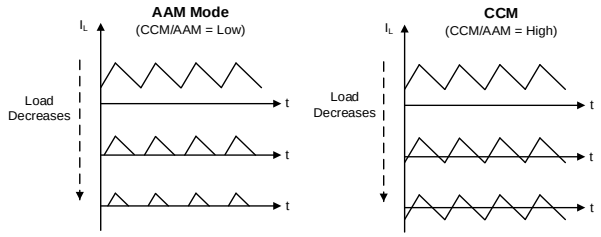

Figure 2: AAM Mode and CCM

Floating Driver and Bootstrap (BST) Charging

The floating top gate driver is powered by an external bootstrap (BST) capacitor (C_{BST}), which is typically refreshed when the HS-FET turns off. This floating driver provides its own under-voltage lockout (UVLO) protection, with a 5V rising threshold and a hysteresis of 500mV.

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VDRV Power Supply and VCC Regulator

The HS-FET and LS-FET drivers are powered from VDRV. Typically, a 1µF to 4.7µF ceramic capacitor is required at each VDRV pin to prevent large voltage spikes at the input.

An internal low-dropout (LDO) linear regulator supplies VCC power from VDRV, where most of the internal circuitries are powered from the VCC regulator. A 1µF ceramic capacitor is recommended between the VCC and SGND pins.

Error Amplifier (EA)

The error amplifier (EA) compares V_{FB} with the internal 0.8V V_{REF} and outputs a current proportional to the difference between these two voltages. This output current (I_{OUT}) is then used to charge or discharge the external compensation network to form the COMP voltage (V_{COMP}), which controls the power MOSFET's current. Adjusting the compensation network between COMP and SGND can optimize the control loop to achieve good stability or fast transient response.

Current Limit

There are three fixed options for setting the current limit. If the ILIM pin is connected to SGND, the current limit sense voltage (V_{ILIMIT}) is set to 25mV. If ILIM is connected to VCC, V_{ILIMIT} is set to 50mV. If ILIM is floated, V_{ILIMIT} is set to 75mV.

When the peak inductor current (I_{PEAK}) exceeds the set current limit threshold, and V_{OUT} starts to drop until V_{FB} is 30% of V_{REF}, the MP9929 enters hiccup mode to periodically restart the part. Meanwhile, the frequency decreases when V_{FB} is below 0.5V. This protection mode is especially useful when the output is dead-shorted to ground. The average short-circuit current is greatly reduced to alleviate the thermal issues. The MP9929 exits hiccup mode once the over-current (OC) condition is removed.

Low-Dropout (LDO) Operation

LDO mode is designed to improve dropout when V_{IN} is close to V_{OUT} by further increasing the HS-FET's on time after the minimum off time is reached. When the current in the HS-FET does not reach the value set by COMP within one PWM cycle, the HS-FET remains on. The MP9929 also monitors the BST-to-SW voltage (V_{BST-SW}). If V_{BST-SW} is below the BST UVLO threshold, then the HS-FET turns off, regardless of whether the current reaches the value set by COMP. Since the BST regulation voltage significantly exceeds the BST UVLO threshold, the HS-FET can remain on for a long time without being required to refresh C_{BST}. As a result, the effective duty cycle of the switching regulator increases. The MP9929 can support up to a 99.5% maximum duty cycle.

Power Good (PG) Function

The MP9929 includes an open-drain power good (PG) output that indicates whether the regulator's output is within about ±10% of its nominal value. When V_{OUT} is outside this range, the PG output is pulled low. The PG output must be connected to a voltage source below 6V via a resistor (e.g. 100kΩ).

The PG pin provides self-driving capabilities. If the input supply fails to power the MP9929, then PG is clamped low even though PG is connected to an external DC source via a pull-up resistor. Figure 3 shows the relationship between the PG clamped voltage and the pull-up current.

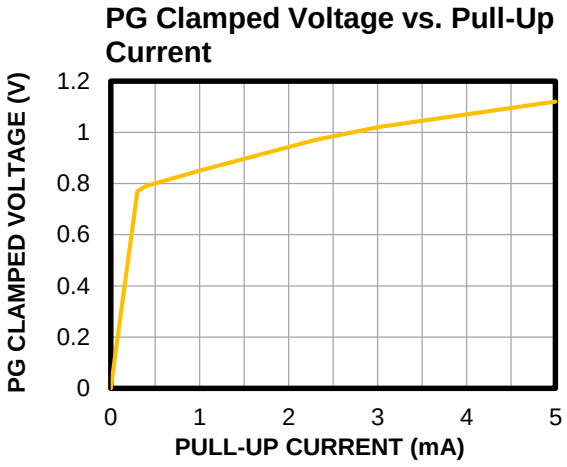

Figure 3: PG Clamped Voltage vs. Pull-Up Current

Soft Start (SS)

Soft start (SS) is implemented to prevent the converter's V_{OUT} from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage (V_{SS}) ramping up from 0V to 0.8V. If V_{SS} is below the internal V_{REF}, then V_{SS} overrides V_{REF}, meaning the EA uses

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V_{SS} as the reference. If V_{SS} exceeds V_{REF}, then V_{REF} regains control.

An external capacitor connected between the SS and SGND pins is charged from an internal current source, which produces a ramped voltage. The soft-start time (t_{SS}) is set by the external SS capacitor (C_{SS}) and can be calculated with Equation (3):

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}(V)}{I_{SS}(\mu A)} \quad (3)$$

Where I_{SS} is the SS charge current. There is no internal SS capacitor.

V_{SS} resets if a fault protection occurs, except for output over-voltage protection (OVP).

Output Over-Voltage Protection (OVP)

The MP9929's V_{OUT} is monitored by V_{FB}. If V_{FB} is typically 115% of V_{REF}, then this triggers OVP. Once OVP is triggered, the MP9929 enters discharge mode, the HS-FET turns off, and the LS-FET turns on until the reverse current limit is triggered. When the LS-FET turns off, I_L increases, and current passes through the HS-FET body diode from V_{OUT} to V_{IN}. The LS-FET turns on again during the next clock cycle. The MP9929 works in discharge mode until V_{FB} drops below 105% of V_{REF}.

Enable (EN)

The MP9929 provides a dedicated enable (EN) control pin, using a bandgap-generated precision threshold. The IC can be enabled or disabled by pulling the EN pin high or low, respectively. To disable the part, the EN/SYNC pin must be pulled low for a minimum of 15µs.

Connect EN to VDRV or VIN via a resistor divider (R_{EN_UP} or R_{EN_DOWN}) to configure the VDRV or VIN start-up threshold (see Figure 4).

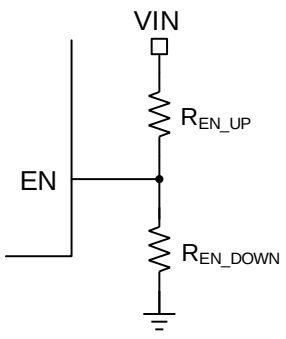

Figure 4: EN Resistor Divider

The V_{DRV} or V_{IN} UVLO threshold is $V_{EN_THRESHOLD}$ x (1+ R_{EN_UP} / R_{EN_DOWN}).

In high input designs, the EN pin voltage (V_{EN}) should not exceed 50V.

Synchronize

The MP9929 can be synchronized to an external clock range between 100kHz and 1000kHz via the EN/SYNC pin. The internal clock's rising edge is synchronized to the external clock's rising edge. The external clock signal's pulse width (both on and off) should be a minimum of 100ns. The MP9929 starts to synchronize about 140µs after adding the external clock signal, and it takes hundreds of ms to accomplish synchronization.

SYNCO Function

The SYNCO pin outputs a default 180° phase-shifted clock when the MP9929 works in CCM or DCM. This function allows two devices to operate at the same frequency while 180° out-of-phase to reduce the total input current ripple. This means a smaller input bypass capacitor can be used.

V_{DRV} Under-Voltage Lockout (UVLO)

V_{DRV} UVLO is implemented to protect the chip from operating at insufficient gate drive supply voltages. The MP9929's V_{DRV} UVLO rising threshold is about 6.5V, and the V_{DRV} UVLO falling threshold is about 6V.

Thermal Protection

The MP9929 provides thermal protection by monitoring the IC's temperature internally. This prevents the chip from operating at exceedingly high temperatures. If the junction temperature (T_J) exceeds the over-temperature protection (OTP) rising threshold, then the whole chip shuts down. It is a non-latch protection, and once T_J drops below with the hysteresis threshold, the device resumes operation by initiating a soft start.

Start-Up and Shutdown

If both V_{DRV} and V_{EN} exceed their respective thresholds, then the chip starts up. The reference block starts first, generating stable reference voltages and currents. Then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitry.

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Three events can shut down the chip: EN going low, VDRV going low, and thermal shutdown. During shutdown, the signal path is blocked first to avoid triggering any faults. V_{COMP} and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets V_{OUT} (see Figure 5).

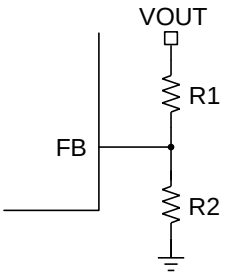

Figure 5: V_{OUT} Setting Resistor

If R1 is determined, then R2 can be calculated with Equation (4):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.8V} - 1} \quad (4)$$

Table 1 shows the resistor selection for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
3.3	160 (1%)	51.2 (1%)
5	160 (1%)	30.5 (1%)
12	160 (1%)	11.5 (1%)

Setting the Current Sense

The current-sense resistor (R_{SENSE}) monitors I_L. R_{SENSE} is selected based on the current limit. The relationship between I_{PEAK} and R_{SENSE} can be calculated with Equation (5):

$$R_{SENSE} = \frac{V_{ILIMIT}}{I_{PEAK}} \quad (5)$$

The SENSE pins (SENSE+ and SENSE-) can draw a positive voltage up to 28V. When R_{SENSE} is connected to V_{OUT} (see Figure 9 on page 26), V_{OUT} is recommended to not exceed 24V. For applications that require a higher V_{OUT}, place R_{SENSE} near PGND (see Figure 10 on page 26). In this scenario, V_{OUT} can be as high as V_{IN} x D_{MAX} in theory.

SENSE+ and SENSE- can only draw a small negative voltage. When R_{SENSE} is connected to V_{OUT}, place an additional protective circuit in case a large negative voltage appears on V_{OUT} (see Figure 6).

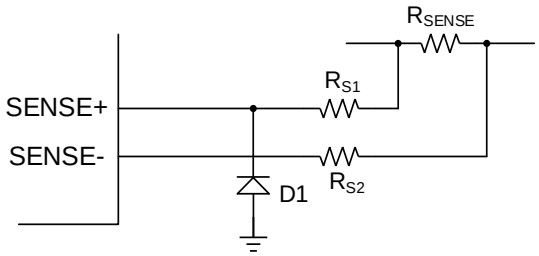

Figure 6: Negative Voltage Protection on SENSE+ and SENSE-

D1's leakage current should be below 100μA across the entire operating temperature range. The serial resistors (R_{S1} and R_{S2}) are also important and are recommended to not exceed 100Ω. A resistance that is too large may cause an offset to the current sense. Otherwise, the MP9929 cannot sufficiently limit I_{PEAK}.

Configurable Switching Frequency

A number of variables must be considered when selecting f_{SW}. A high frequency increases switching losses and gate charge losses, while a lower frequency requires more inductance and capacitance, which results in a larger PCB layout and higher costs. There is a tradeoff between power loss and passive component size. Additionally, in noise-sensitive applications, f_{SW} must be outside of the sensitive frequency band.

The MP9929's frequency can be configured between 100kHz and 1000kHz with a resistor connected between the FREQ and SGND pins. R_{FREQ} for a given operating frequency can be calculated with Equation (6):

$$R_{FREQ}(k\Omega) = \frac{20000}{f_{SW}(kHz)} - 1 \quad (6)$$

Set R_{FREQ} to 39kΩ to obtain a f_{SW} of 500kHz.

Table 2 shows the relationship between R_{FREQ} and frequency.

Table 2: R_{FREQ} vs. Frequency

R_{FREQ} (kΩ)	Frequency (kHz)
65	300
39	500
19	1000

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Selecting the Inductor

MPL Optimized Performance with MPS Inductor MPL-AY1265 Series

An inductor with a DC current rating exceeding the maximum load current by at least 25% is recommended for most applications. A larger-value inductor results in less ripple current and a lower output ripple voltage (ΔV_{IN}). However, the larger-value inductor has a larger physical size, higher series resistance, and lower saturation current. Generally, it is recommended to choose the inductor ripple current to be about 20% to 50% of the maximum load current. Then the inductance (L) can be calculated with Equation (7):

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}} \quad (7)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The maximum inductor peak current (I_{L_MAX}) can be calculated with Equation (8):

$$I_{L_MAX} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (8)$$

Where I_{LOAD} is the load current.

MPS inductors are optimized and tested for use with a complete line of integrated circuits. Table 3 lists the recommended power inductors. Select a part number based on the design requirements.

Table 3: Power Inductor Selection

Part Number	Inductance	Manufacturer
MPL-AY1265-6R8	6.8µH	MPS

Visit MonolithicPower.com under Products > Inductors for more information.

Selecting the Input Capacitor

Since the input capacitor (C_{IN}) absorbs the input switching current, it requires an adequate ripple current rating. C_{IN} selection is mainly based on its maximum ripple current capability.

The RMS ripple current flowing through C_{IN} (I_{RMS}) can calculated with Equation (9):

$$I_{RMS} = I_{LOAD} \sqrt{\frac{V_{OUT}}{V_{IN}} (1 - \frac{V_{OUT}}{V_{IN}})} \quad (9)$$

The worst-case condition occurs at $V_{IN} = 2 \times V_{OUT}$, where $I_{RMS} = I_{LOAD} / 2$. Thus, C_{IN} must be able to handle I_{RMS}.

Selecting the Output Capacitor

The output capacitor (C_{OUT}) keeps the output voltage ripple (ΔV_{OUT}) small and ensures regulation loop stability. C_{OUT} impedance must be low at f_{SW}. ΔV_{OUT} can be calculated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \quad (10)$$

Where R_{ESR} is the equivalent series resistance (ESR) of C_{OUT}.

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. In this scenario, ΔV_{OUT} can be calculated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (11)$$

Compensation Components

The MP9929 employs current-mode control for easy compensation and fast transient response. The COMP pin controls system stability and transient response. COMP is the internal EA's output. A series capacitor-resistor combination sets a pole-zero combination to manage the control system's characteristics. The DC gain of the voltage feedback loop (A_{VDC}) can be calculated with Equation (12):

$$A_{VDC} = R_{LOAD} \times G_{CS} \times A_O \times \frac{V_{FB}}{V_{OUT}} \quad (12)$$

Where A_O is the EA's voltage gain (3000V/V); G_{CS} is the current-sense transconductance, which is equal to 1 / (12 x R_{SENSE}) (in A/V); and R_{LOAD} is the load resistance.

Figure 7 shows the COMP external compensation.

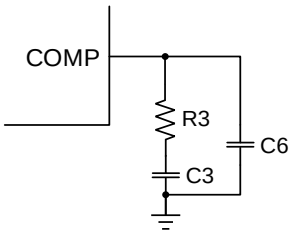

Figure 7: COMP External Compensation

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The system provides two important poles. One pole is from the compensation capacitor (C3) and the EA's output resistor. Its frequency (f_{P1}) can be calculated with Equation (13):

$$f_{P1} = \frac{G_M}{2\pi \times C3 \times A_O} \quad (13)$$

Where G_M is the EA's transconductance (500μA/V).

The second pole is from C_{OUT} and R_{LOAD}. Its frequency (f_{P2}) can be calculated with Equation (14):

$$f_{P2} = \frac{1}{2\pi \times C_{OUT} \times R_{LOAD}} \quad (14)$$

The system has an important zero due to the compensation capacitor (C3) and the compensation resistor (R3). This zero's frequency (f_{Z1}) can be calculated with Equation (15):

$$f_{Z1} = \frac{1}{2\pi \times C3 \times R3} \quad (15)$$

The system may have another significant zero if C_{OUT} has a large capacitance or a high ESR. This zero's frequency (f_{ESR}) can be calculated with Equation (16):

$$f_{ESR} = \frac{1}{2\pi \times C_{OUT} \times R_{ESR}} \quad (16)$$

In this scenario, a third pole set by the compensation capacitor (C6) and the compensation resistor (R3) can compensate for the ESR zero effect.

This pole's frequency (f_{P3}) can be calculated with Equation (17):

$$f_{P3} = \frac{1}{2\pi \times C6 \times R3} \quad (17)$$

The goal of the compensation design is to shape the converter transfer function for a desired loop gain. The system crossover frequency where the feedback loop has unity gain is important, since lower crossover frequencies result in slower line and load transient responses, and higher crossover frequencies lead to system instability. Set the crossover frequency to about 0.1 x f_{SW}. Follow the steps below to design the compensation:

1. Choose R3 to set the desired crossover frequency. R3 can be calculated with Equation (18):

$$R3 = \frac{2\pi \times C_{OUT} \times f_C}{G_M \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}} \quad (18)$$

   Where f_C is the desired crossover frequency.

2. Choose C3 to achieve the desired phase margin. For applications with typical inductances, set the compensation zero frequency (f_{Z1}) to be below 0.25 x f_C to provide a sufficient phase margin. C3 can be calculated with Equation (19):

$$C3 > \frac{4}{2\pi \times R3 \times f_C} \quad (19)$$

3. C6 is required if the C_{OUT} ESR zero is set to be below 0.5 x f_{SW}. Equation (20) shows the relationship between C_{OUT} and f_{SW}:

$$\frac{1}{2\pi \times C_{OUT} \times R_{ESR}} < \frac{f_{SW}}{2} \quad (20)$$

   In this scenario, use C6 to set f_{P3} at ESR zero. C6 can be calculated with Equation (21):

$$C6 = \frac{C_{OUT} \times R_{ESR}}{R3} \quad (21)$$

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Design Example

Table 4 shows a design example following the application guidelines for the given specifications.

Table 4: Design Example

V_{IN}	V_{OUT}	I_{OUT}
13V to 100V	12V	0A to 10A

Figure 9 on page 26 shows the detailed application schematic for V_{OUT} = 12V, which is the basis for the typical performance waveforms. This circuit can work down to 7V after start-up, but V_{OUT} may drop when V_{IN} is low due to the maximum duty cycle limit. For more detailed device applications, refer to the related evaluation board datasheets.

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PCB Layout Guidelines

Efficient layout is crucial for stable operation. Poor layout may result in reduced performance, EMI issues, resistive loss, and even system instability. For the best results, refer to Figure 8 and follow the guidelines below:

1. The input power loop between C_{IN}, the HS-FET, and the LS-FET should be as small as possible.
2. Ensure that the SW trace is as short and wide as possible.
3. Place a small decoupling capacitor close to each of the IC's VDRV and PGND pins.
4. Ensure that the FB loop is far away from noise sources, such as the SW trace.
5. Place the FB divider resistor as close as possible to the FB pin.
6. Route the paired sensing traces (SENSE+ and SENSE-) using the smallest enclosed area.
7. Avoid placing the sensing traces (SENSE+ and SENSE-) in noisy areas, such as SW or the high-side (HS) gate drive traces.
8. Place the filter capacitor for the current-sense signal as close to the IC pins as possible.
9. A short and wide resistor is recommended for current sense.
10. VCC capacitors (C_{VCC}) should be placed as close as possible to the VCC pin.
11. Connect the gate drive traces as directly as possible. Place the forward and return traces close together, either side by side or on top of each other on adjacent layers, to minimize the inductance of the gate drive path.
12. Place the ground return of C_{IN} or C_{OUT} close to the large PGND copper area, then connect the ground return to the IC's PGND pin through a single point.
13. For heavy loads, it is recommended to use wide copper traces as well as additional layers and vias for the heatsink.

Figure 8 shows the recommended placement of the components for the MP9929 in a QFN-26 (4mmx6mm) package. Figure 9 on page 26 shows the corresponding schematic of the layout.

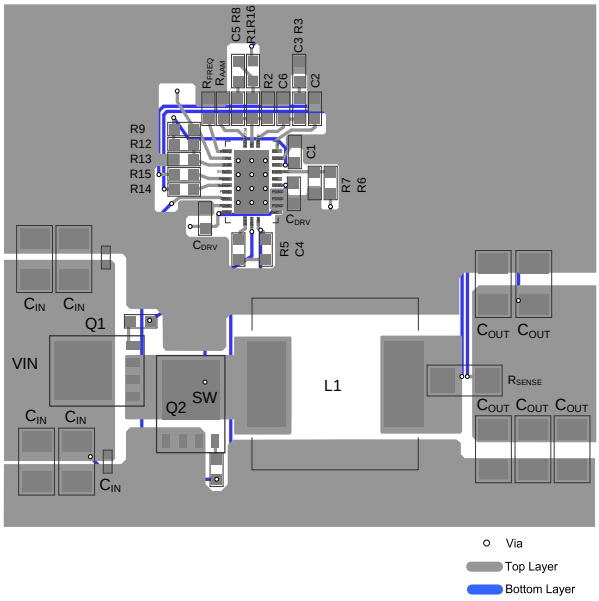

Figure 8: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

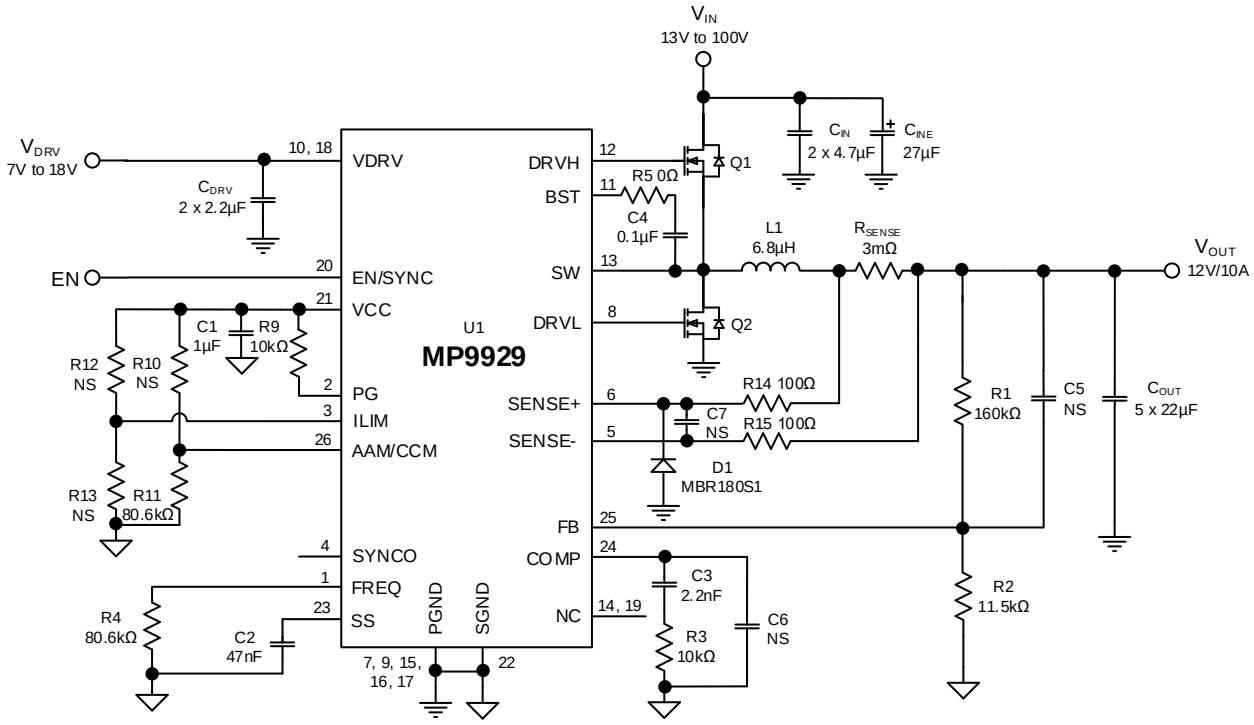

Figure 9: Typical Application Circuit (12V Output) (8)

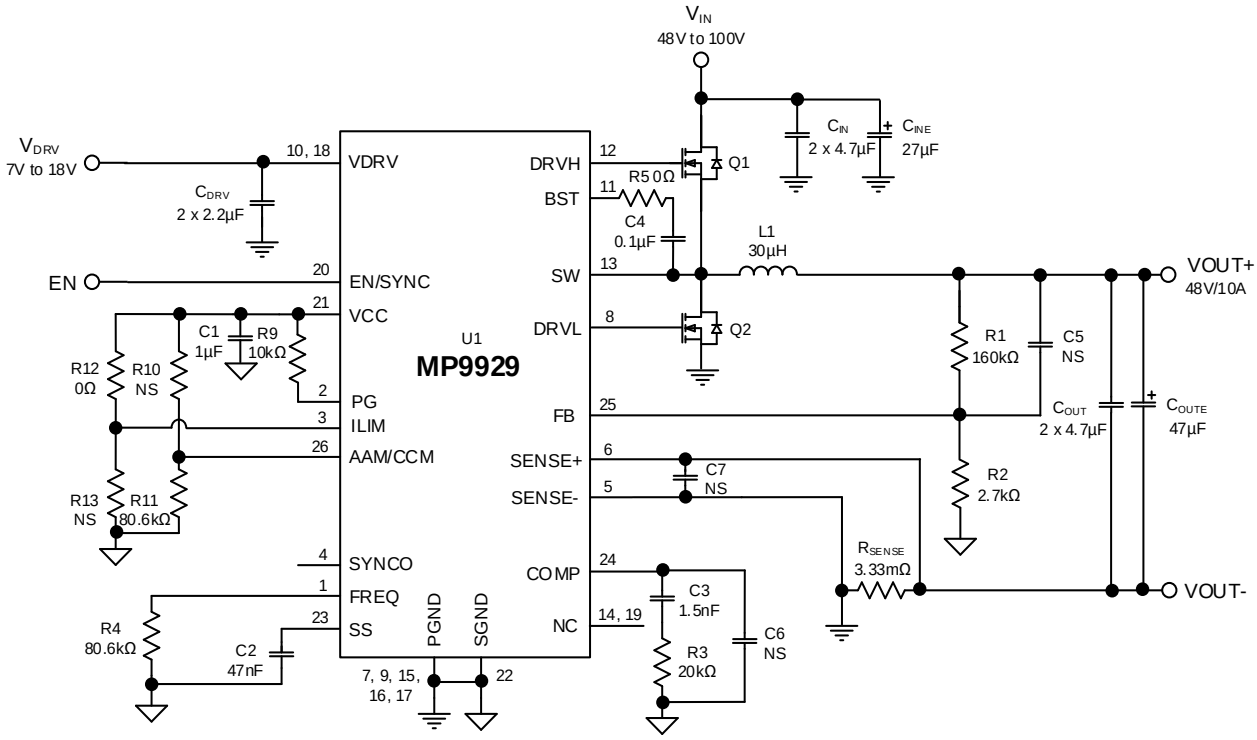

Figure 10: Typical Application Circuit (48V Output) (8)

Note:

8) For 100V input applications, a lower V_{DRV} is required to ensure V_{BST} does not exceed the absolute maximum ratings voltage of 110V.

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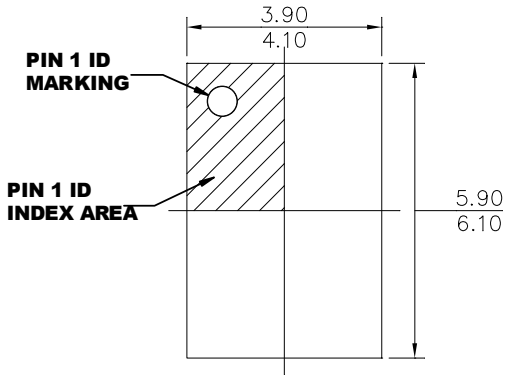
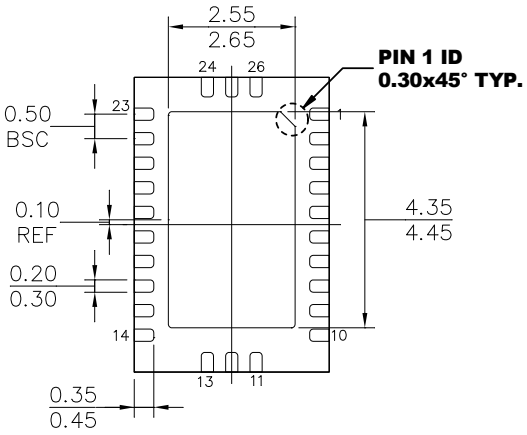
PACKAGE INFORMATION

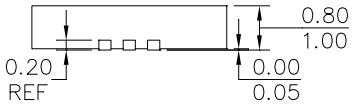
QFN-26 (4mmx6mm)



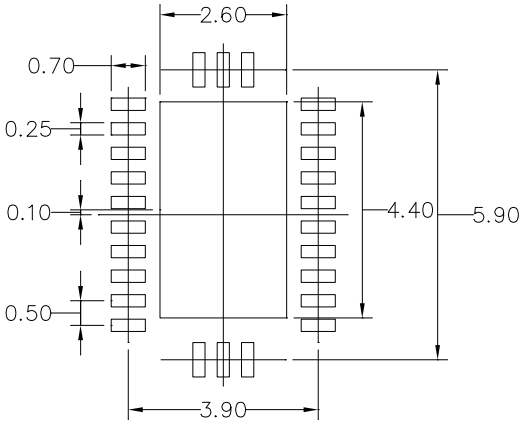
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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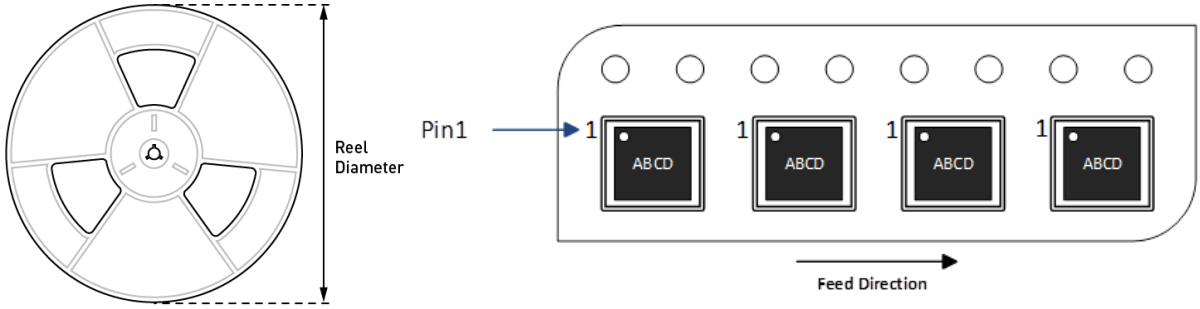
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP9929GQW-Z	QFN-26 (4mmx6mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/24/2024	Initial Release	-

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