MP9473

High-Efficiency, Fast-Transient, 3.5A, 36V Synchronous, Step-Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP9473 is a fully integrated, high-frequency, synchronous, rectified, step-down, switch-mode converter. It offers a compact solution to achieve a 3.5A, continuous-output current over a wide input-supply range with excellent load and line regulation. It provides fast, transient response and good stability for wide input-supply and load range. The MP9473 operates at high efficiency over a wide-output-current load range.

MP9473 has full protection features including, short-circuit protection (SCP), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown (TSD).

The MP9473 requires minimal, readily available, standard, external components, and is available in a compact 3mmx4mm, 20-pin, QFN package.

FEATURES

- Wide 4.5V-to-36V Operating Input Range
- Guaranteed 3.5A, Continuous Output Current
- Internal 40mΩ High-Side, 20mΩ Low-Side Power MOSFETs
- Proprietary Switching-Loss-Reduction Technology
- 1% Reference Voltage
- Programmable Soft-Start Time
- Low Drop-Out Mode
- 200kHz-to-1MHz Switching Frequency
- SCP, OCP, UVP, and Thermal Shutdown
- Output Adjustable from 0.8V to 0.9×V_{IN}
- Available in a 3mmx4mm, 20-pin, QFN Package

APPLICATIONS

- Notebook Systems and I/O Power
- Automotive Systems
- Networking Systems
- Industrial Supplies
- Optical Communications Systems
- Distributed Power and POL Systems

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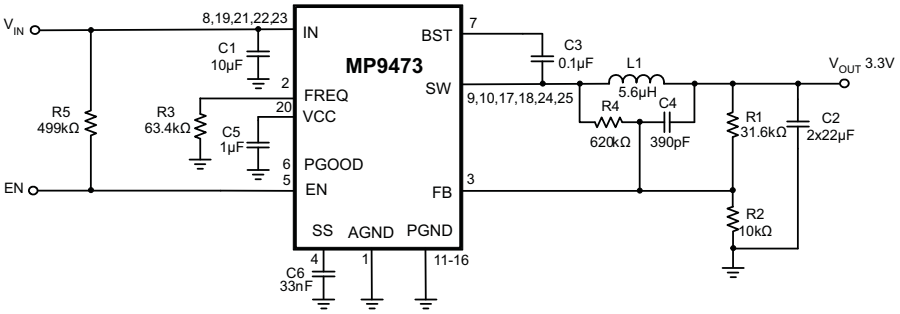
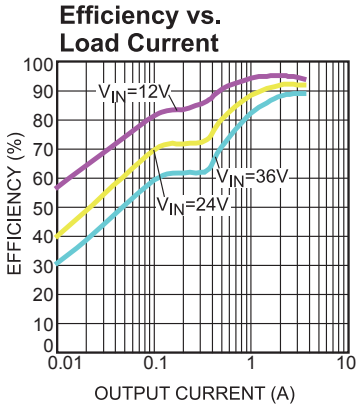
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP9473GL	QFN-20 (3mmx4mm)	*See below*

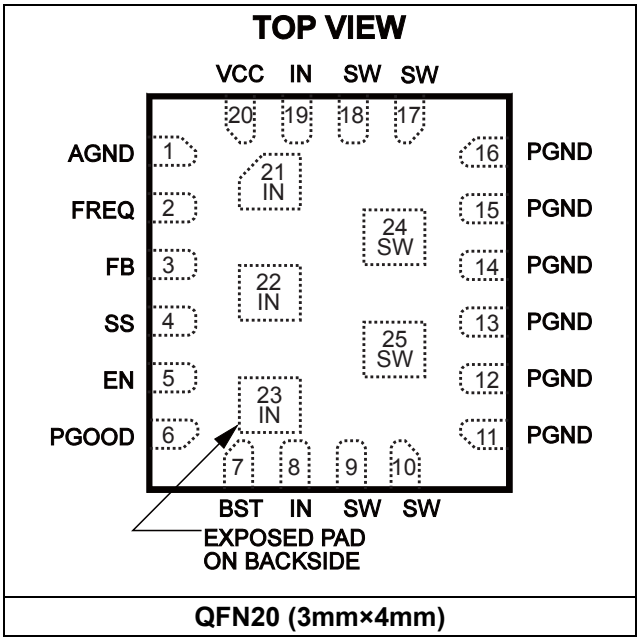
* For Tape & Reel, add suffix –Z (e.g. MP9473GL–Z);

TOP MARKING

MPYW
9473
LLL

MP: MPS prefix:
Y: year code;
W: week code:
9473: first four digits of the part number;
LLL: lot number;

PACKAGE REFERENCE



QFN20 (3mm×4mm)

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ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} 40V
V_{SW} ..... -0.3V(-5V <10ns) to V_{IN} + 0.3V
V_{BST} ..... V_{SW} + 6.5V
V_{PGOOD} ..... -0.3V to V_{CC}+0.6V
All Other Pins ..... -0.3V to +6V
Continuous Power Dissipation (T_A = +25°C) (2)
…… ……2.6W
Operating Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 4.5V to 36V
Output Voltage V_{OUT} ..... 0.8V to 0.9×V_{IN}
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-20 (3mm×4mm)	48	10 °C/W

Notes:

1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, V_{EN} = 2V, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Shutdown)	I_{IN}	V_{EN} = 0V		10	200	nA
Supply Current (Quiescent)	I_{IN}	V_{FB} = 0.95V		500	600	μA
HS Switch On Resistance	HS_{RDS-ON}			40	55	mΩ
LS Switch On Resistance (5)	LS_{RDS-ON}			20		mΩ
Switch Leakage	SW_{LKG}	V_{EN} = 0V V_{SW} = 0V or 36V		10	200	nA
Current Limit	I_{LIMIT}		4.2	6.6	9	A
One-Shot On Time	t_{ON}	V_{IN}=12V, R_{FREQ}=30kΩ	230	280	330	ns
Minimum Off Time(5)	t_{OFF}			100		ns
Fold-Back Off Time(5)	t_{FB}	I_{LIM}=1(HIGH), FB>50%V_{REF}		4.8		μs
Fold-Back Off Time(5)	t_{FB}	I_{LIM}=1(HIGH), FB<50%V_{REF}		16.8		μs
OCP Hold-Off time(5)	t_{OC}	I_{LIM}=1(HIGH)		100		μs
Feedback Voltage	V_{FB}	T_J = 25°C	807	815	823	mV
Feedback Current	I_{FB}	V_{FB} = 815mV		10	50	nA
Soft-Start Charging Current	I_{SS}	V_{SS}=0V	6	8.5	11	μA
Power Good Rising Threshold	$PGOOD_{Vth-Hi}$		0.87	0.9	0.93	V_{FB}
Power Good Falling Threshold	$PGOOD_{Vth-Lo}$		0.82	0.85	0.88	V_{FB}
Power Good Threshold Hysteresis	$PGOOD_{Vth-Hys}$			0.05		V_{FB}
Power Good Rising Delay	t_{PGOOD}		500	700	900	μs
EN Rising Threshold	EN_{Vth-Hi}		1.0	1.2	1.4	V
EN Falling Threshold	EN_{Vth-Lo}		0.7	0.85	0.99	V
EN Threshold Hysteresis	$EN_{Vth-Hys}$			390		mV
EN Input Current	I_{EN}	V_{EN} = 2V		1.5	2	μA
V_{IN} Under-Voltage Lockout Threshold Rising	$INUV_{Vth_R}$		3.7	4.0	4.3	V
V_{IN} Under-Voltage Lockout Threshold Falling	$INUV_{Vth_F}$		2.8	3.1	3.4	V
V_{IN} Under-Voltage Lockout Threshold Hysteresis	$INUV_{HYS}$			900		mV
V_{CC} Regulator	V_{CC}	I_{CC}=0	4.5	4.85	5.2	V
V_{CC} Load Regulation		I_{CC}=10mA		1	2	%
Thermal Shutdown(5)	T_{SD}			175		°C
Thermal Shutdown Hysteresis(5)	T_{SD-HYS}			45		°C

Note:

5) Derived from bench characterization, not tested in production.

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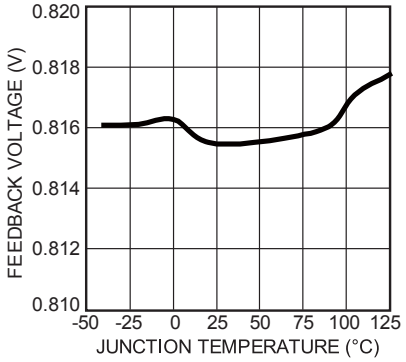
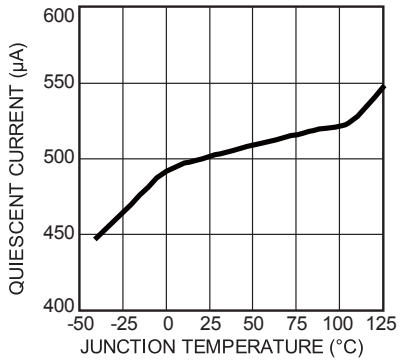
TYPICAL CHARACTERISTICS

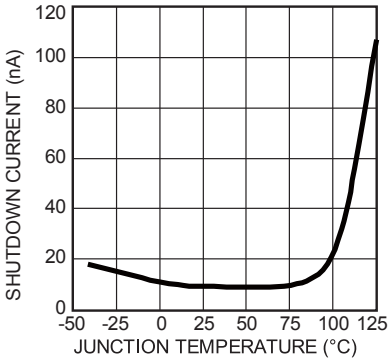
Feedback Voltage vs. Junction Temperature
VIN=24V



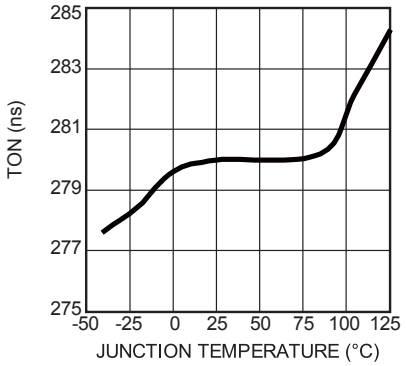
Quiescent Current vs. Junction Temperature
VIN=24V



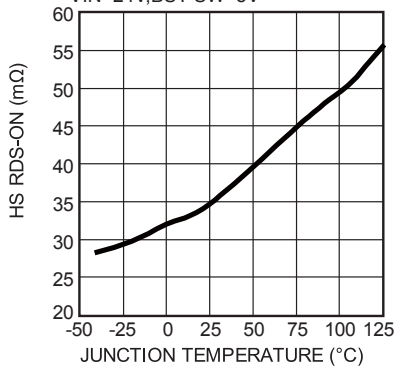
Shutdown Current vs. Junction Temperature
VIN=24V



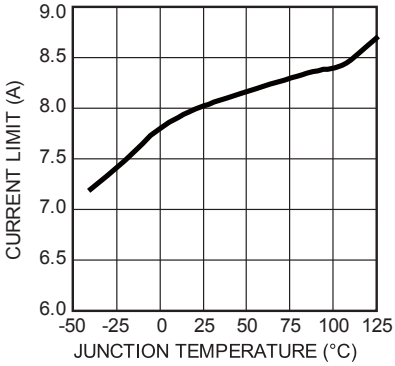
Ton vs. Junction Temperature
VIN=12V



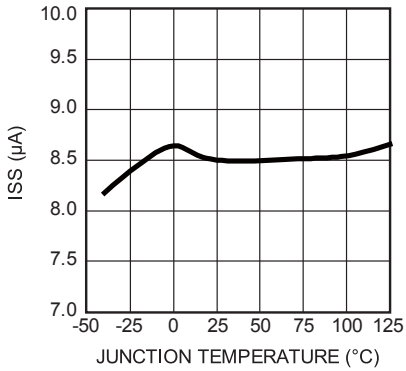
HS R_{DS-ON} vs. Junction Temperature
VIN=24V,BST-SW=5V



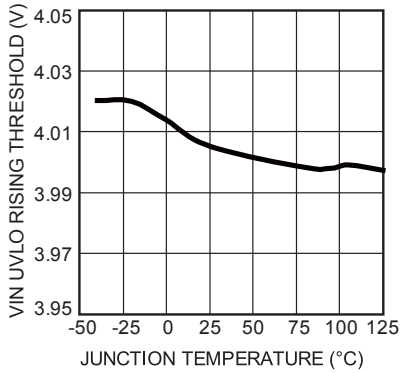
Current Limit vs. Junction Temperature
VIN=24V



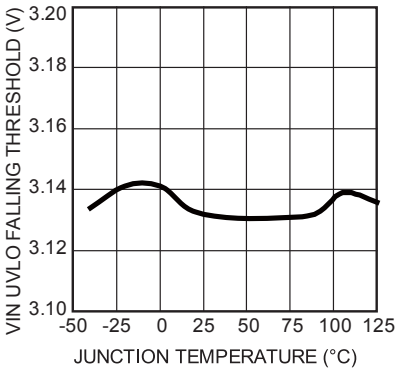
I_{SS} vs. Junction Temperature
VIN=24V



VIN UVLO Rising Threshold vs. Junction Temperature



VIN UVLO Falling Threshold vs. Junction Temperature
VIN=24V



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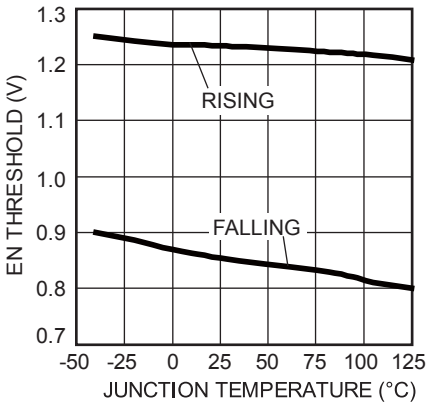
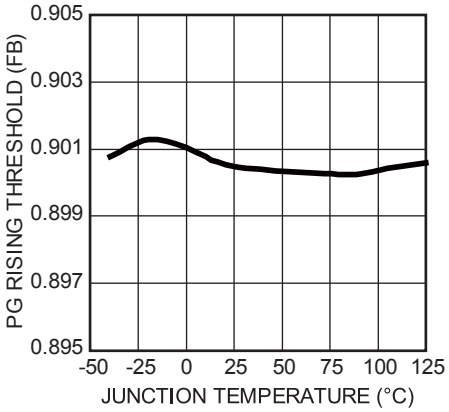
TYPICAL CHARACTERISTICS

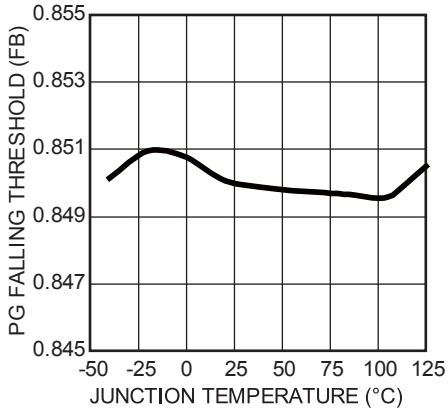
EN Threshold vs. Junction Temperature



PG Rising Threshold vs. Junction Temperature



PG Falling Threshold vs. Junction Temperature



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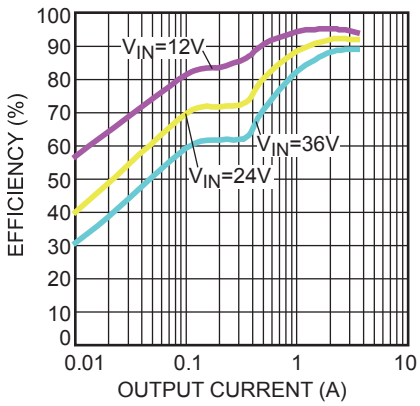
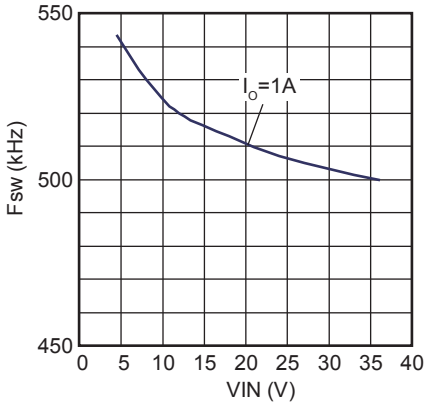
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 24V, V_{OUT} = 3.3V, L = 10µH, R_{FREQ} = 63.4k, T_A = +25°C, unless otherwise noted.

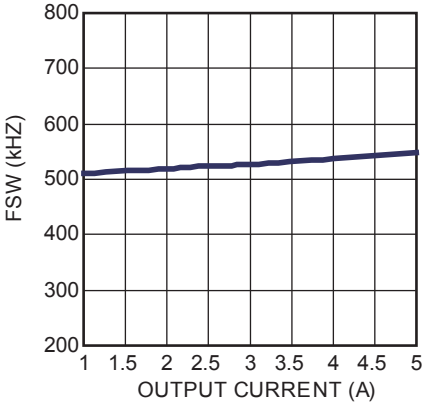
Efficiency vs. Load Current



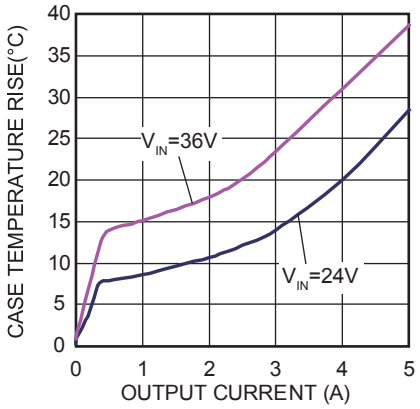
Fsw vs. VIN



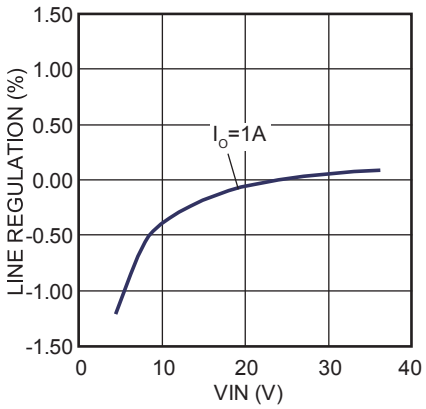
Fsw vs. Output Current



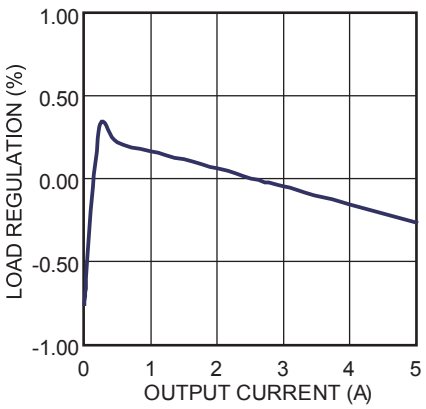
Case Temperature Rise vs. Output Current



Line Regulation



Load Regulation



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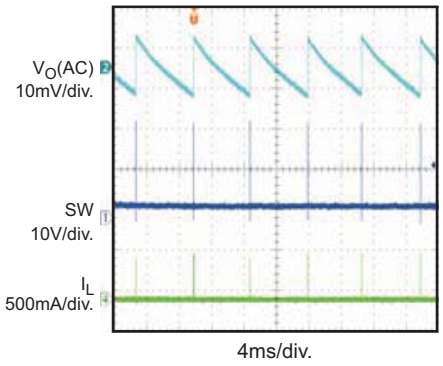
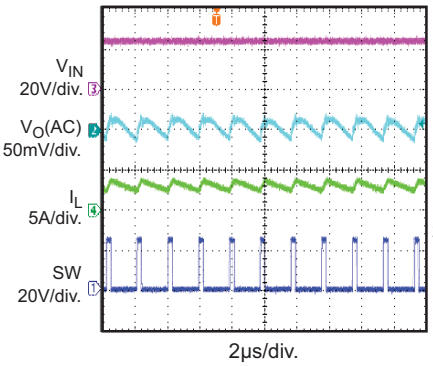
TYPICAL PERFORMANCE CHARACTERISTICS *(CONTINUED)*

V_{IN} = 24V, V_{OUT} = 3.3V, L = 10µH, R_{FREQ} = 63.4k, T_A = +25°C, unless otherwise noted.

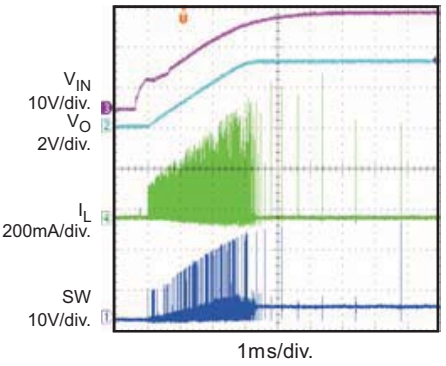
Output-Voltage Ripple
I_O = 0A



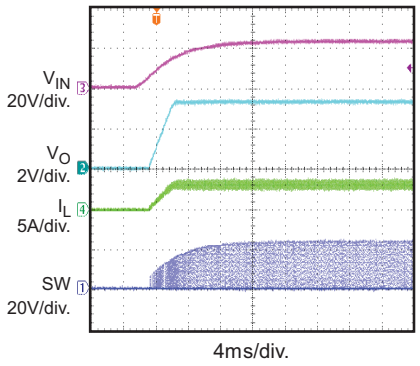
Output-Voltage Ripple
I_O = 3A



Start-up Through VIN
I_O = 0A



Start-up Through VIN
I_O = 3A



Shutdown Through VIN
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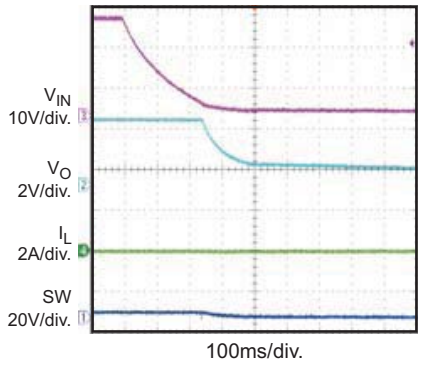
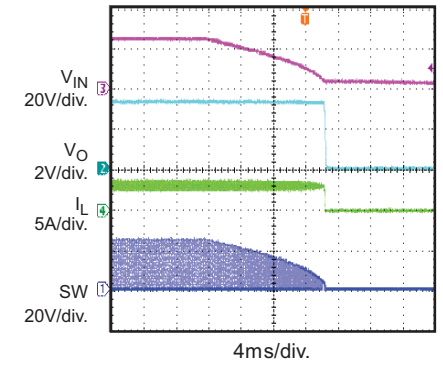


Shutdown Through VIN
I_O = 3A



Start-up Through EN
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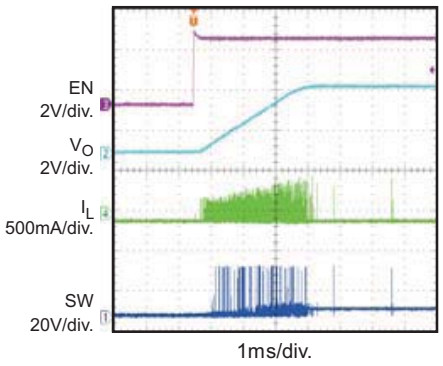

Start-up Through EN
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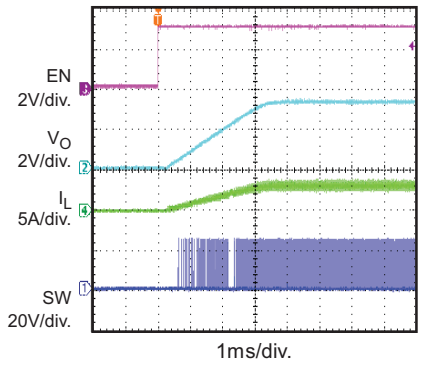

Shutdown Through EN
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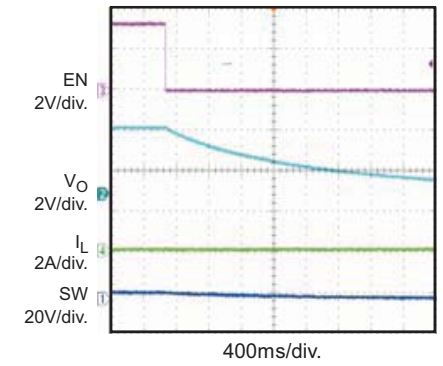

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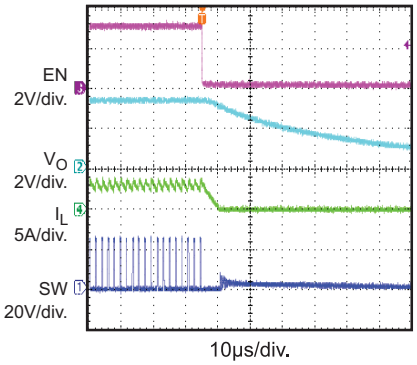
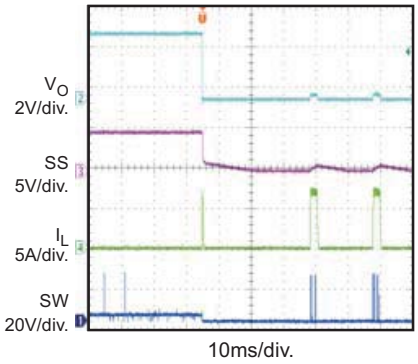
TYPICAL PERFORMANCE CHARACTERISTICS *(CONTINUED)*

V_{IN} = 24V, V_{OUT} = 3.3V, L = 10µH, R_{FREQ} = 63.4k, T_A = +25°C, unless otherwise noted.

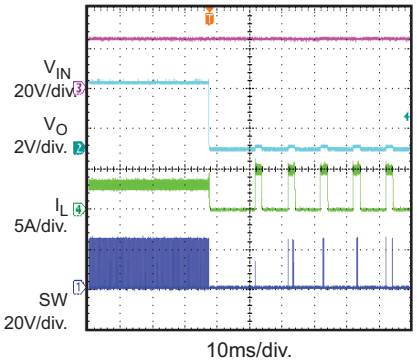
Shutdown Through EN
I_O = 3A



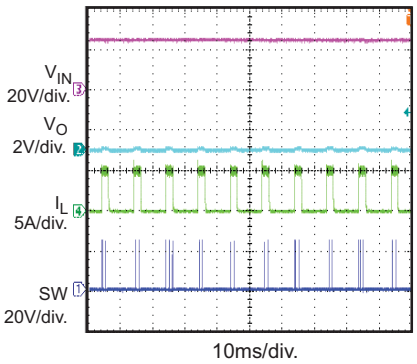
Short-Circuit Entry
I_O = 0A



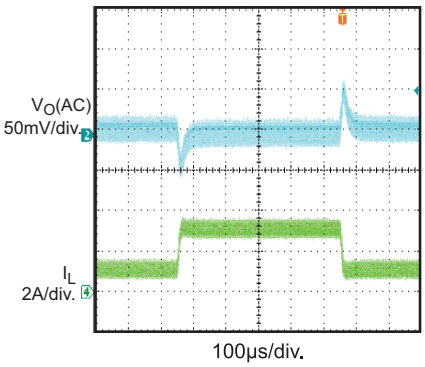
Short-Circuit Entry
I_O = 3A



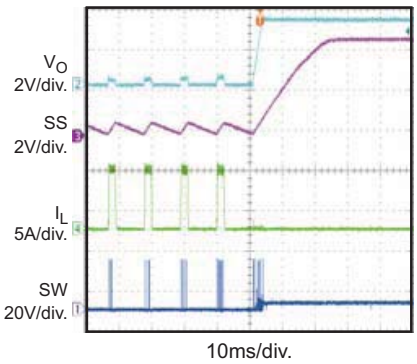
Short-Circuit Steady State



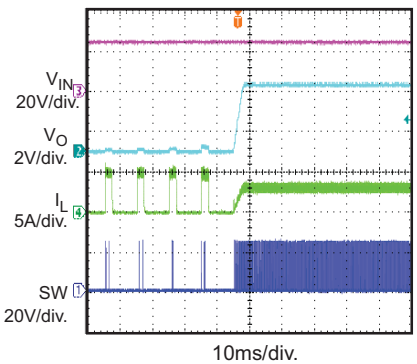
Load Transient
IO= 1A-3A



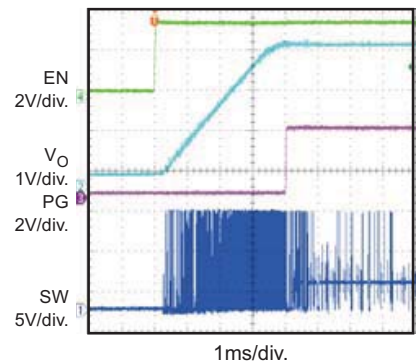
Short-Circuit Recovery
I_O = 0A



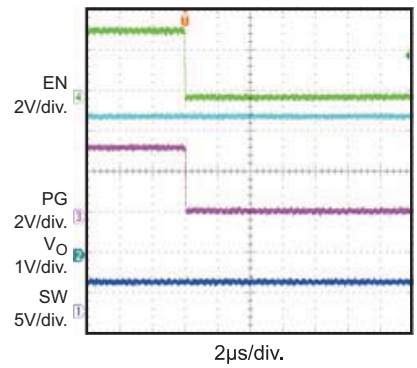
Short-Circuit Recovery
I_O = 3A



Power Good Through EN Start-up



Power Good Through EN Shutdown



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PIN FUNCTIONS

Pin #	Name	Description
1	AGND	Analog Ground.
2	FREQ	Frequency Set (for CCM). The input voltage and the frequency-set resistor are connected to GND to determine the ON period. Decouple with a 1nF capacitor.
3	FB	Feedback. The tap of the external resistor divider from the output to GND sets the output voltage.
4	SS	Soft-Start. Connect an external capacitor to program the soft-start time for the switch-mode regulator. When the EN pin goes HIGH, an internal-current source (8.5μA) charges the capacitor, and the SS voltage slowly and smoothly ramps up from 0 to V_{FB}. When the EN pin goes LOW, the internal-current source discharges the capacitor, and the SS voltage slowly ramps down.
5	EN	Enable. EN=1 to enable the MP9473. For automatic start-up, connect EN pin to IN with a 100kΩ resistor. It includes an internal 1MΩ pull-down resistor.
6	PGOOD	Power Good Output. The output of this pin is an open drain and goes HIGH if the output voltage exceeds 90% of the nominal voltage. There is delay of ~700μs from FB ≥ 90% to PGOOD HIGH.
7	BST	Bootstrap. Requires a 0.1μF to 1μF capacitor connected between the SW and BS pins to form a floating supply across the high-side switch driver.
8, 19, Exposed pads 21, 22, 23	IN	Supply Voltage. The MP9473 operates from a 4.5V to 36V input rail. It requires C_{IN} to decouple the input rail. Connect using wide PCB traces and multiple vias.
9, 10, 17, 18, Exposed pads 24, 25	SW	Switch Output. Connect using wide PCB traces and multiple vias.
11-16	PGND	System Ground. This pin is the reference ground of the regulated output voltage. *Care must be taken in PCB layout.
20	Vcc	Internal Bias Supply. Decouple with a 1μF capacitor as close to the pin as possible.

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BLOCK DIAGRAM

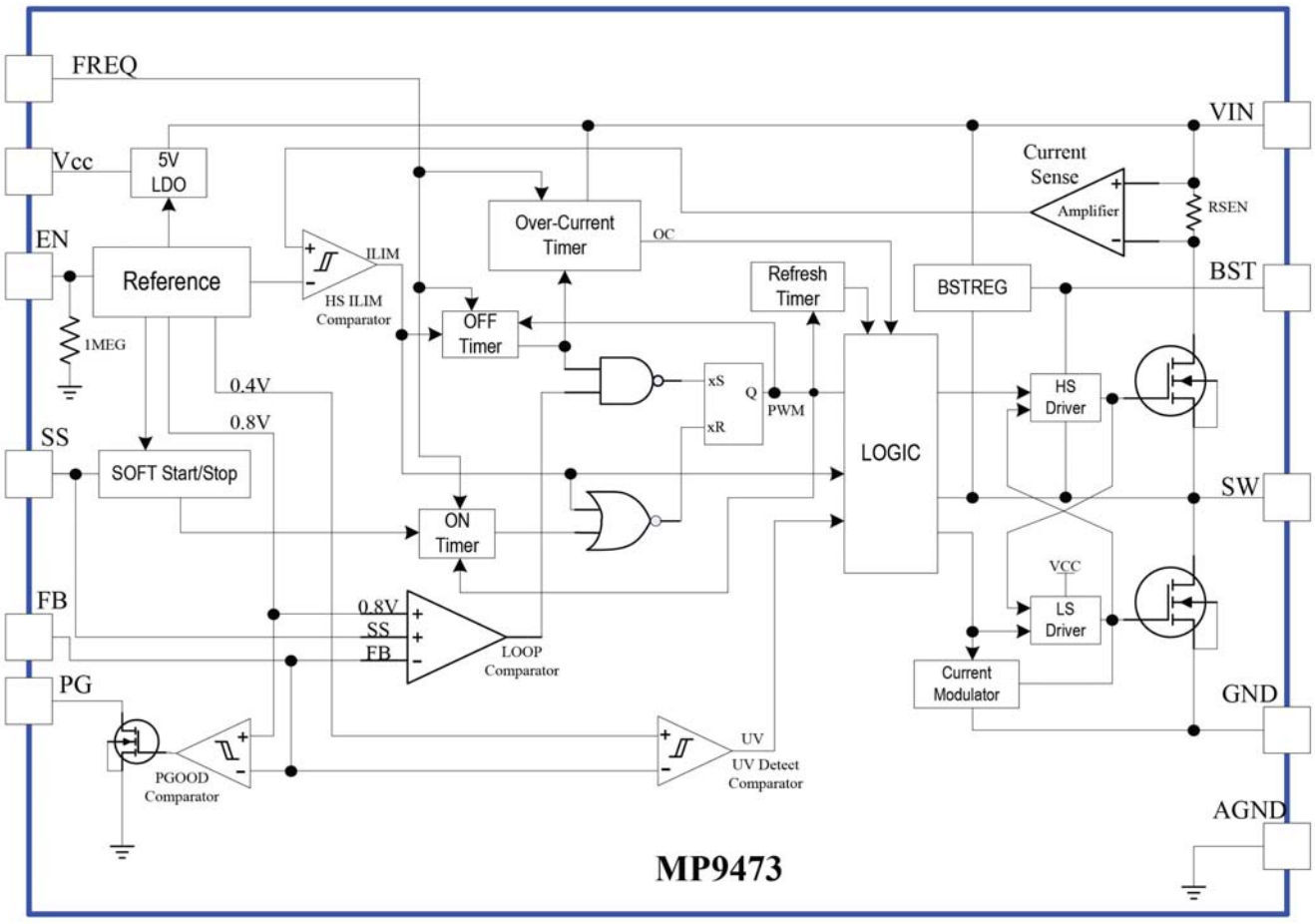

Figure 1: Functional Block Diagram

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OPERATION

PWM Operation

The MP9473 is a fully integrated, synchronous, rectified, step-down, switch-mode converter. At the beginning of each cycle, the high-side MOSFET (HS-FET) turns ON when the feedback voltage (V_{FB}) drops below the reference voltage (V_{REF}). This indicates an insufficient output voltage. The ON period is determined by the input voltage and the frequency-set resistor, which can be calculated as follows:

$$t_{ON}(ns) = \frac{96 \times R_{FREQ}(k\Omega)}{V_{IN}} + t_{DELAY}(ns) \quad (1)$$

After the ON period elapses, the HS-FET turns OFF. It turns ON again when V_{FB} drops below V_{REF}. By repeating this operation, the converter regulates the output voltage. To minimize conduction loss, the integrated, low-side MOSFET (LS-FET) turns ON when the HS-FET is OFF. A dead short occurs between the input and GND if both the HS-FET and the LS-FET turn on simultaneously (shoot through). An internal dead-time (DT), generated between HS-FET OFF and LS-FET ON or LS-FET OFF and HS-FET ON, prevents shoot through.

Heavy-Load Operation

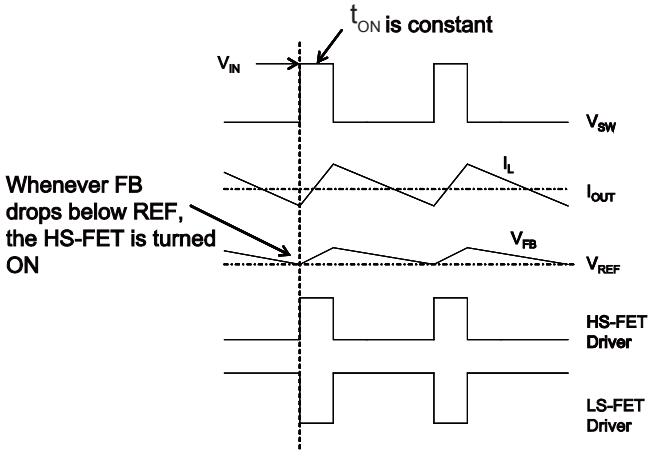

Figure 1: Heavy-Load Operation

In continuous-conduction mode (CCM), when the output current is HIGH, the HS-FET and LS-FET repeatedly turn ON/OFF (see MPS. All Rights Reserved. The inductor current never reaches zero. In CCM, the switching frequency (f_{SW}) is fairly constant.

Light-Load Operation

At light-load or no-load conditions, the output drops very slowly; the MP9473 reduces the switching frequency automatically to maintain high efficiency. Figure 2 shows light-load operation. V_{FB} does not reach V_{REF} as the inductor current approaches zero. The LS-FET driver enters a tri-state (high Z) whenever the inductor current reaches zero. A current modulator takes control of the LS-FET and limits the inductor current to less than -1mA. This causes the output capacitors to discharge slowly to GND through the LS-FET to improve light-load efficiency. At light loads, the HS-FET does not turn ON as frequently as with heavy loads. This is called skip mode.

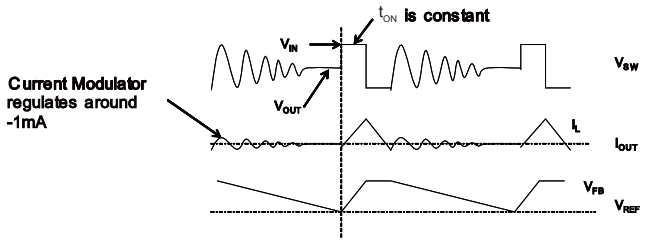

Figure 2: Light-Load Operation

As the output current increases from the light-load conditions, the current modulator's regulatory time period becomes shorter. The HS-FET turns ON more frequently, thus increasing the switching frequency. The output current reaches a critical level when the current modulator time is zero. The critical output-current level can be calculated as follows:

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (2)$$

It enters PWM mode once the output current exceeds the critical level; then the switching frequency stays fairly constant over the output-current range.

Switching Frequency

The input voltage is feed-forwarded to the on-time one-shot timer through the resistor (R_{FREQ}). The duty ratio remains at V_{OUT}/V_{IN}, allowing the switching frequency to remain fairly constant over the input-voltage range. The switching frequency can be calculated as follows:

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$$F_{SW}(kHz) = \frac{10^6}{[\frac{96 \times R_{FREQ}(k\Omega)}{V_{IN}} + t_{DELAY}(ns)] \times \frac{V_{IN}}{V_{OUT}}} \quad (3)$$

where,

t_{DELAY}—The comparator delay (~20ns).

The MP9473 is optimized for 200kHz-to-1MHz applications; this enables applications to operate at high-switching frequencies with high efficiency. The high-switching frequency allows for smaller LC-filter components that reduce PCB space requirements.

Ramp Compensation

Figure 3 and Figure 4 show jitter occurring in both PWM mode and skip mode. Noise on V_{FB}'s downward slope causes the HS-FET ON time to deviate from its intended position and produce jitter. The relationship between system stability and the height of the V_{FB} ripple is significant: the steep slope of the V_{FB} ripple dominates noise immunity. The magnitude of the V_{FB} ripple doesn't affect the noise immunity directly.

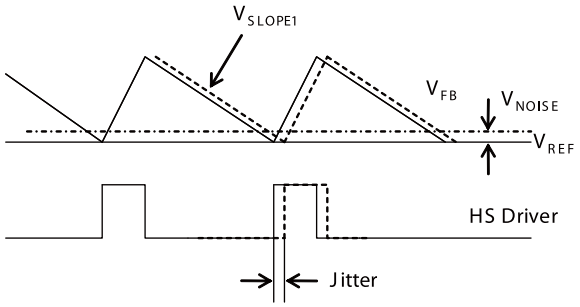

Figure 3: Jitter in PWM Mode

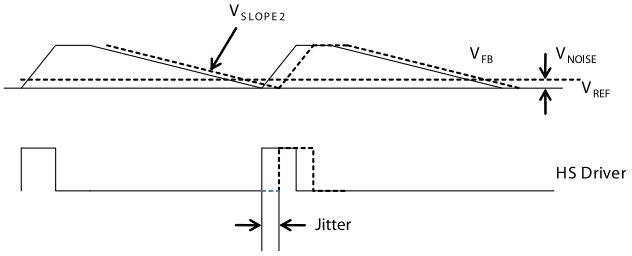

Figure 4: Jitter in Skip Mode

Ceramic output capacitors lack enough ESR ripple to stabilize the system, and require an external compensation ramp.

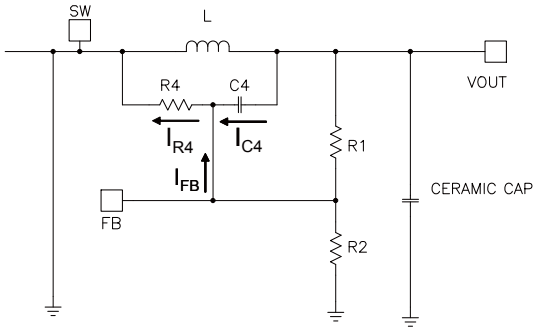

Figure 5: Simplified Circuit in PWM Mode with External Ramp Compensation

In PWM mode, MP9473 has an equivalent circuit with HS-FET OFF and uses an external ramp compensation circuit (R_4, C_4), shown as a simplified circuit in Figure 5. Derive the external ramp from the inductor-ripple current. Choose C_4, R_1, and R_2 to meet the following condition:

$$\frac{1}{2\pi \times F_{SW} \times C_4} < \frac{1}{5} \times \left(\frac{R_1 \times R_2}{R_1 + R_2} \right) \quad (4)$$

then:

$$I_{R4} = I_{C4} + I_{FB} \approx I_{C4} \quad (5)$$

The V_{FB} downward slope ripple is then calculated as follows:

$$V_{SLOPE1} = \frac{-V_{OUT}}{R_4 \times C_4} \quad (6)$$

Using equation 6, reduce R_4 or C_4 to decrease instability in PWM mode. If C4 cannot be reduced further (due to the limitations of equation 4), then only reduce R_4. Based on bench experiments, V_{SLOPE1} is around 20V/ms-40V/ms.

When using POSCAP or types of capacitors with higher ESR, an external ramp is not necessary.

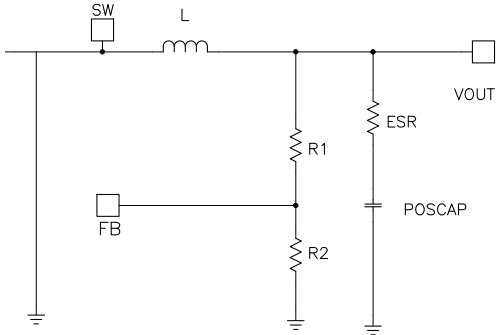

Figure 6: Simplified Circuit in PWM Mode without External Ramp Compensation

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Figure 6 shows an equivalent circuit in PWM mode with the HS-FET OFF and without an external ramp circuit. The ESR ripple dominates the output ripple. The V_{FB} downward slope is calculated as follows:

$$V_{SLOPE1} = \frac{-ESR \times V_{REF}}{L} \quad (7)$$

From equation 7, the V_{FB} downward slope is proportional to ESR/L. Therefore, it's necessary to know the minimum ESR value of the output capacitors without an external ramp. Also, there is an inductance limit: a smaller inductance leads to increased stability. Based on bench experiments, keep V_{SLOPE1} around 15V/ms to 30V/ms.

In skip mode, the external ramp does not affect the downward slope; the downward slope of the V_{FB} ripple remains the same with or without the external ramp. Figure 7 shows an equivalent circuit with the HS-FET OFF and the current modulator regulating the LS-FET.

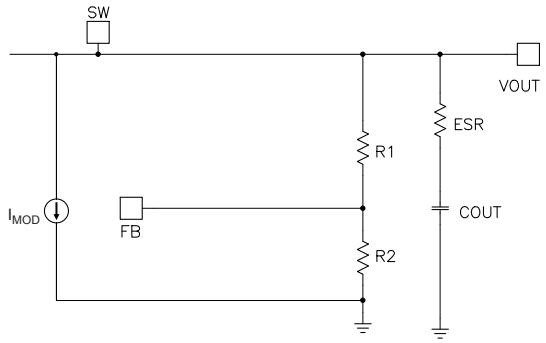

Figure 7: Simplified Circuit in Skip Mode

The downward slope of the V_{FB} ripple is:

$$V_{SLOPE2} = \frac{-V_{REF}}{(R_1 + R_2) \times C_{OUT}} \quad (8)$$

To keep the system stable during light loads, avoid large V_{FB} resistors. Also, keep the V_{SLOPE2} value around 0.4V/ms to 0.8mV/ms. Note that I_{MOD} is excluded from the equation because it does not impact the system's light-load stability.

Soft-Start (SS)

The MP9473 employs soft-start (SS) to ensure smooth output during power-up. When the EN pin goes HIGH, an internal-current source (8.5μA) charges the SS capacitor (C_{SS}). The C_{SS} voltage takes over the REF voltage to the PWM comparator. The output voltage smoothly ramps up with V_{SS}. Once V_{SS} reaches the same level as V_{REF}, it continues ramping up while V_{REF} takes over the PWM comparator. At this point, soft-start finishes and the MP9473 enters steady state.

C_{SS} is then:

$$C_{SS}(nF) = \frac{t_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} \quad (9)$$

If the output capacitors have large capacitance values, avoid setting a short SS or risk hitting the current limit during SS. Select a minimum value of 4.7nF if the output capacitance value exceeds 330μF.

Power Good (PGOOD)

The MP9473 has power-good (PGOOD) output. The PGOOD pin is the open drain of a MOSFET. It connects to V_{CC} (or a different voltage source) through a resistor (e.g. 100kΩ). In the presence of an input voltage, the MOSFET turns ON so that the PGOOD pin is pulled to GND before SS is ready. After V_{FB} reaches 90%xV_{REF}, the PGOOD pin is pulled HIGH (after a delay, typically 700μs).

When the FB voltage drops to 85%xV_{REF}, the PGOOD pin is pulled LOW.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MP9473 has cycle-by-cycle over-current limit control. The inductor current is monitored during the ON state. Once the inductor current exceeds the current limit, the HS-FET turns OFF. Simultaneously, the OCP timer starts. The OCP timer is set at 100μs. Hitting the current limit every cycle during the 100μs time frame will trigger hiccup SCP.

If a short circuit occurs, the MP9473 immediately will hit its current limit and V_{FB} will drop below 50%xV_{REF} (0.815V). The device considers this an output dead short and will trigger hiccup SCP immediately.

Under-Voltage Protection (UVP)

The MP9473 monitors the output voltage through the tap of a resistor divider to the FB pin. This detects output under-voltage conditions.

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A V_{FB} drop below 50%xV_{REF} triggers UVP. Also, it triggers a current limit that initiates SCP.

Under-Voltage Lock-Out Protection (UVLO)

The MP9473 has under-voltage lock-out protection (UVLO). When the input voltage is higher than the UVLO rising threshold voltage, the MP9473 begins to power up. It shuts off when the input voltage is lower than the UVLO falling threshold voltage. This is non-latch protection.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating-power MOSFET driver. A dedicated, internal regulator charges and regulates the bootstrap capacitor voltage to ~5V. When the voltage between the BST and SW nodes drops below regulation, a PMOS pass transistor, connected from VIN to BST, turns on. The charging current path travels from VIN to BST and then to SW. The external circuit should provide enough voltage headroom to facilitate charging.

The bootstrap capacitor remains charged if the V_{IN} is significantly higher than the SW. When the HS-FET is ON, V_{IN}≈V_S. This prevents the bootstrap capacitor from charging.

When the LS-FET is ON, V_{IN}−V_{SW} reaches its maximum for fast charging. When there is no inductor current, V_{SW}=$V_{OUT;}$ the difference between V_{IN} and V_{OUT} can charge the bootstrap capacitor.

At higher duty cycles, the bootstrap-charging time is shorter. Therefore, the bootstrap capacitor may not charge sufficiently. If the internal circuit does not have sufficient time and voltage to charge the bootstrap capacitor, the bootstrap capacitor voltage drops low. When V_{BST}−V_{SW} drops below 2.3V, the HS-FET turns OFF. A UVLO circuit allows the LS-FET to conduct and refresh the charge on the bootstrap capacitor. Once the bootstrap capacitor voltage is charged, the HS-FET turns ON again and the part resumes normal switching. The bootstrap refreshing function allows the MP9473 to work on low drop-out mode.

Thermal Shutdown (TSD)

The MP9473 uses thermal shutdown (TSD). The junction temperature of the IC is internally monitored. If the junction temperature exceeds the threshold value (typically 175°C), the converter shuts off. This is a non-latched protection, with about 45°C hysteresis. Once the junction temperature drops to 130°C, it initiates a SS.

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APPLICATION INFORMATION

Setting the Output Voltage

To set V_{OUT}, connect a resistor divider from the output voltage to the FB pin.

Without an external ramp, the feedback resistors (R_1 and R_2) set the output voltage. To determine the values for the resistors, first choose R_2 (typically 5kΩ-40kΩ). Then R_1 is calculated as follows:

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (10)$$

When using a low-ESR ceramic capacitor on the output, add an external voltage ramp to the FB pin through R_4 and C_4. The ramp voltage (V_{RAMP}) affects output voltage. Calculate V_{RAMP} using equation 19. Choose R_2 between 5kΩ and 40kΩ. Determine R_1 as follows :

$$R_1 = \left(\frac{V_{REF} + \frac{1}{2} V_{RAMP}}{R_2 \times (V_{OUT} - V_{REF} - \frac{1}{2} V_{RAMP})} - \frac{1}{R_4} \right)^{-1} \quad (11)$$

Using equation 11 to calculate the output voltage is complicated. As V_{RAMP} changes (due to changes in V_{OUT} and V_{IN}), V_{FB} also varies. To improve output-voltage accuracy and simplify the R_2 calculation from equation 11, add a DC-blocking capacitor (C_{DC}). Figure 8 shows a simplified circuit with external ramp compensation and a DC-blocking capacitor. (Equation 10 can then estimate R_1.)

Select a C_{DC} value between 1μF and 4.7μF to improve DC-blocking performance.

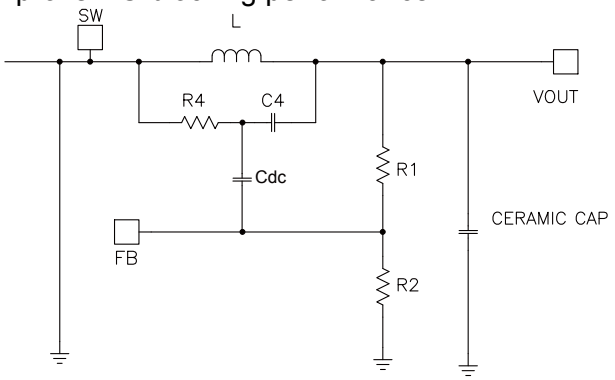

Figure 8: Simplified Circuit with External Ramp Compensation and DC-Blocking Capacitor

Input Capacitor

The input current to the step-down converter is discontinuous, requiring a capacitor to supply the AC current while maintaining the DC-input voltage. Ceramic capacitors are recommended for high performance. Place the input capacitors as close to the IN pin as possible.

The capacitance varies significantly with temperature. Capacitors with X5R and X7R ceramic dielectrics are fairly stable over temperature fluctuations.

The capacitors must have a ripple-current rating greater than the converter's maximum input-ripple current. The input-ripple current can be estimated as follows:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (12)$$

The worst condition occurs at $V_{IN} = 2V_{OUT}$:

Where,

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (13)$$

To simplify calculations, choose an input capacitor whose RMS-current rating is greater than half of the maximum load current. The input-capacitance value determines the input-voltage ripple of the converter. If there is an input-voltage-ripple requirement in the system design, choose an input capacitor that meets the specification

The input-voltage ripple can be estimated as follows:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (14)$$

The worst condition occurs at $V_{IN} = 2V_{OUT}$:

Where,

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (15)$$

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Output Capacitor

The output capacitor maintains the DC-output voltage. Use ceramic or POSCAP capacitors. The output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (16)$$

Where,

R_{ESR}—The equivalent series resistance of the output capacitor.

For ceramic capacitors, capacitance dominates the impedance at the switching frequency. This is the primary cause of the output-voltage ripple. To simplify calculations, estimate the output-voltage ripple as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (17)$$

The output-voltage ripple caused by ESR is very small, requiring an external ramp to stabilize the system. The voltage ramp is ~30mV. The external ramp is generated through R_4 and C_4 using the following equation:

$$V_{RAMP} = \frac{(V_{IN} - V_{OUT}) \times T_{ON}}{R4 \times C4} \quad (18)$$

Select C_4 to meet the following condition:

$$\frac{1}{2\pi \times F_{SW} \times C4} < \frac{1}{5} \times (\frac{R1 \times R2}{R1 + R2}) \quad (19)$$

For POSCAP capacitors, the ESR dominates the impedance at the switching frequency. The ramp voltage generated from the ESR is high enough to stabilize the system. Therefore, an external ramp is not needed. A minimum ESR value of 12mΩ is required to ensure stable operation of the converter. To simplify calculations, the output ripple can be approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (20)$$

Inductor

The inductor is required to supply constant current to the output load while being driven by the switching-input voltage. A larger inductance results in less ripple current and a lower output-ripple voltage. However, a larger inductance results in a larger inductor, which is not only physically larger, but has a higher series resistance and/or lower saturation current. A good rule for determining the inductor value is to allow the peak-to-peak ripple current in the inductor to be approximately 30% to 40% of the maximum switch-current limit. Ensure that the peak-inductor current is below the maximum switch-current limit. The inductance value can be calculated as:

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (21)$$

Where,

ΔI_L—The peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak-inductor current can be calculated as:

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (22)$$

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Typical Design Parameter Tables

The following tables include recommended component values for typical output voltages (3.3V, 5V) and switching frequencies (300kHz, 500kHz, and 700kHz). Refer to tables 1—3 for design cases without external ramp compensation. Refer to tables 4—6 for design cases with external ramp compensation. An external ramp is not needed when using high-ESR capacitors, such as electrolytic or POSCAPs. An external ramp is needed when using low-ESR capacitors, such as ceramic capacitors. To calculate approximate component values for cases not listed, an Excel spreadsheet is available through your local sales representative.

Table 1: 300kHz, 24V_{IN}

V_{OUT} (V)	L (µH)	R1 (kΩ)	R2 (kΩ)	R_{FREQ} (kΩ)
3.3	10	30.1	10	110
5	10	51.1	10	169

Table 2: 500kHz, 24V_{IN}

V_{OUT} (V)	L (µH)	R1 (kΩ)	R2 (kΩ)	R_{FREQ} (kΩ)
3.3	10	30.1	10	63.4
5	10	51.1	10	100

Table 3: 700kHz, 24V_{IN}

V_{OUT} (V)	L (µH)	R1 (kΩ)	R2 (kΩ)	R_{FREQ} (kΩ)
3.3	10	30.1	10	44.2
5	10	51.1	10	69.8

Table 4: 300kHz, 24V_{IN}

V_{OUT} (V)	L (µH)	R1 (kΩ)	R2 (kΩ)	R4 (kΩ)	C4 (pF)	R_{FREQ} (kΩ)
3.3	10	30.9	10	953	390	110
5	10	53.6	10	845	560	169

Table 5: 500kHz, 24V_{IN}

V_{OUT} (V)	L (µH)	R1 (kΩ)	R2 (kΩ)	R4 (kΩ)	C4 (pF)	R_{FREQ} (kΩ)
3.3	10	31.6	10	620	390	63.4
5	10	53.6	10	845	390	100

Table 6: 700kHz, 24V_{IN}

V_{OUT} (V)	L (µH)	R1 (kΩ)	R2 (kΩ)	R4 (kΩ)	C4 (pF)	R_{FREQ} (kΩ)
3.3	10	31.6	10	560	390	44.2
5	10	54.9	10	620	390	69.8

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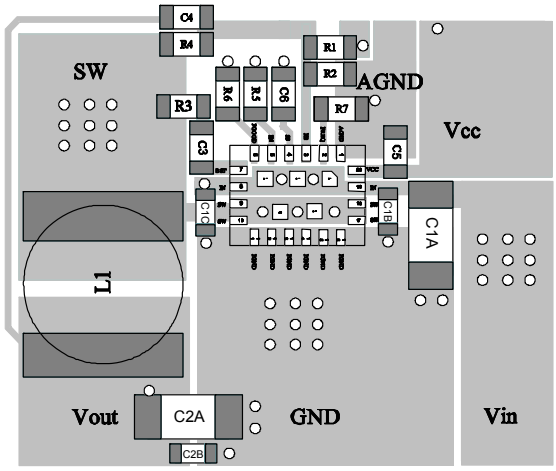
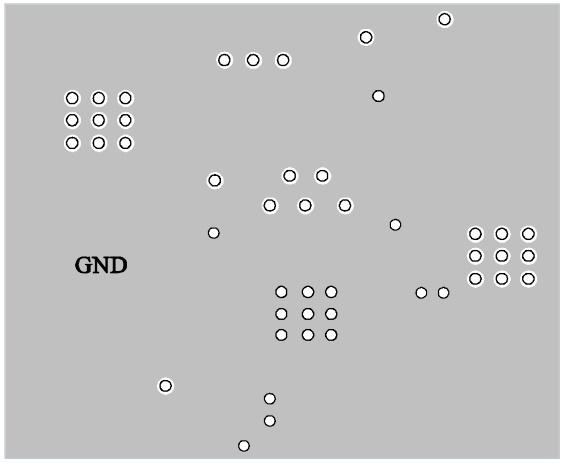
LAYOUT RECOMMENDATION

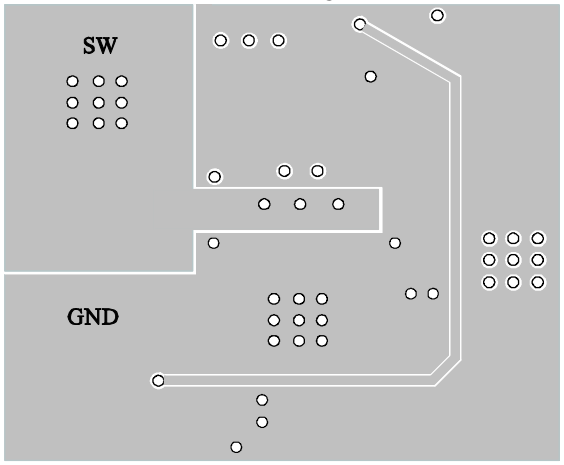
1. Place high-current paths (GND, IN, and SW) very close to the device with short, direct, and wide traces.
2. Place input capacitors on both VIN sides (PIN8 and PIN19) and as close to the IN and GND pins as possible.
3. Place the decoupling capacitor as close to the Vcc and GND pins as possible.
4. Keep the switching node SW short and far away from the feedback network.
5. Place the external feedback resistors next to the FB pin. Do not place vias on the FB trace.
6. Keep the BST voltage path (BST, C3, and SW) as short as possible.
7. Connect the bottom IN and SW pads to a large copper area to achieve optimal thermal performance.
8. A four-layer layout is strongly recommended to achieve optimal thermal performance.



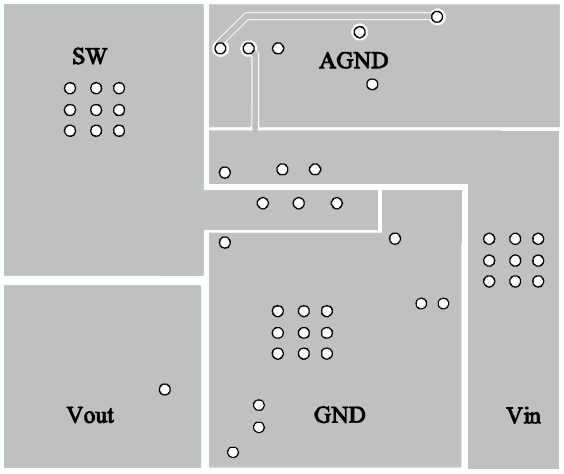
Top Layer



Inner1 Layer



Inner2 Layer



Bottom Layer

Figure 9: PCB Layout

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TYPICAL APPLICATION CIRCUITS

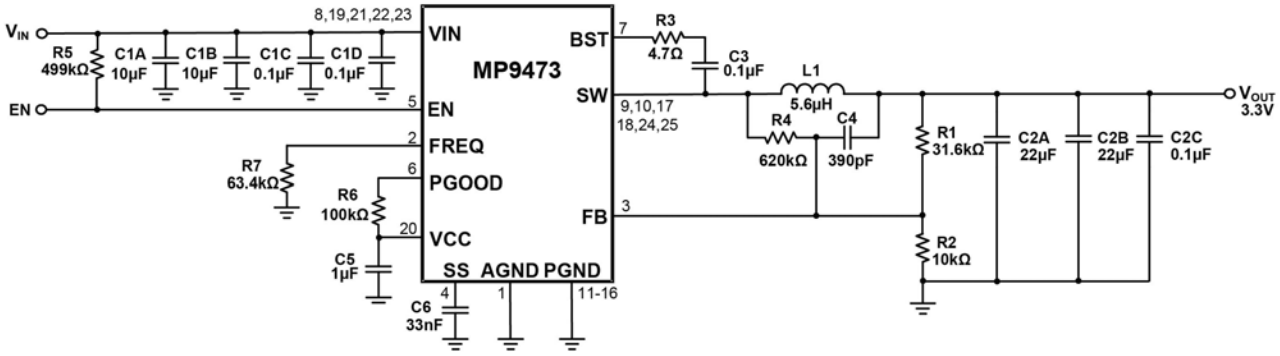

Figure 10: Typical Application Circuit, 3.3V-Output

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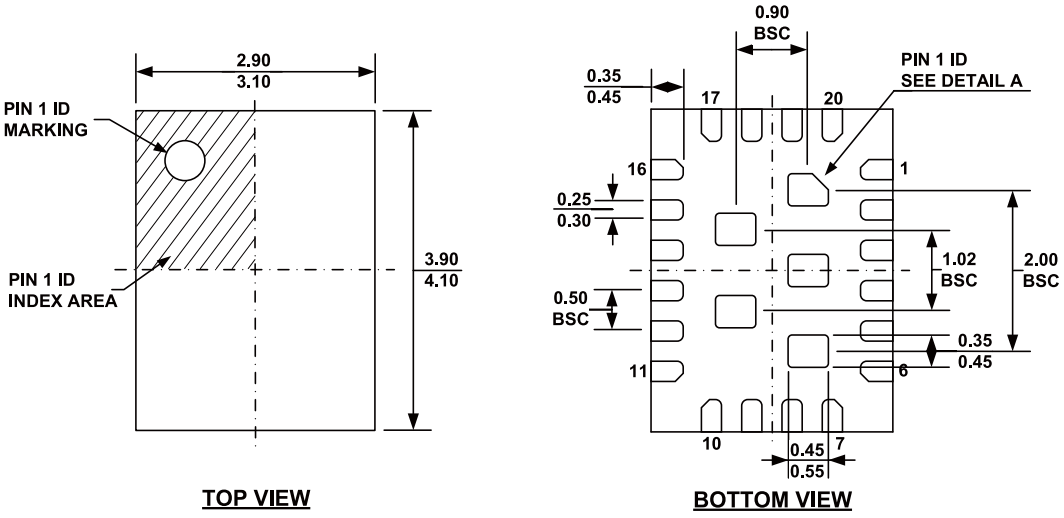
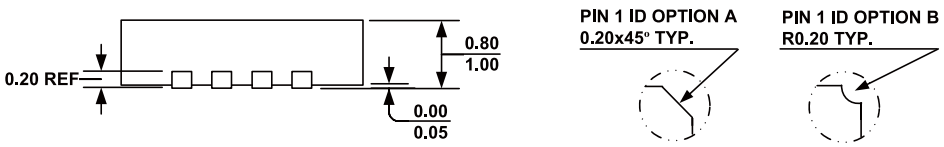
PACKAGE INFORMATION

QFN-20 (3mm × 4mm)



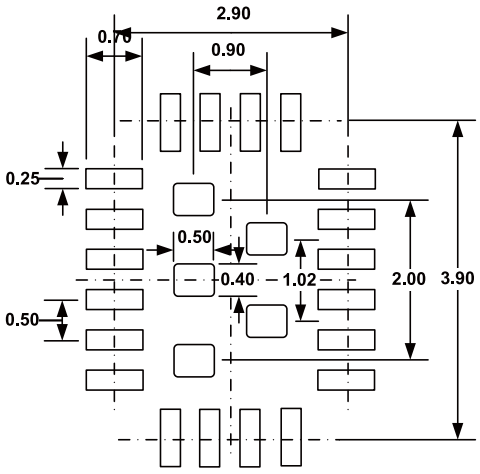
TOP VIEW

BOTTOM VIEW



SIDE VIEW

DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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