DESCRIPTION

The MP9447 is a fully-integrated, high-frequency, synchronous, rectified, step-down, switch-mode converter. It offers a very compact solution to achieve a 5A, continuous-output current over a wide input-supply range with excellent load and line regulation. It also provides fast transient response and good stability for wide input-supply and load range. The MP9447 operates at high efficiency over a wide output current load range.

Full protection features include SCP, OCP, UVP, and thermal shutdown.

The MP9447 requires a minimal number of readily-available, standard, external components, and is available in a space-saving 3mm×4mm, 25-pin, QFN package.

FEATURES

- Wide 4.5V-to-36V Operating Input Range
- Guaranteed 5A, Continuous Output Current
- Internal 65mΩ High-Side, 30mΩ Low-Side Power MOSFETs
- Proprietary Switching-Loss-Reduction Technology
- 1.5% Reference Voltage
- Programmable Soft-Start Time
- Low Drop-out Mode
- 200kHz-to-650kHz Switching Frequency
- SCP, OCP, UVP, and Thermal Shutdown
- Output Adjustable from 0.8V to 0.9×VIN
- Available in a 3×4mm 25-pin QFN Package

APPLICATIONS

- General Consumer
- USB Power Supplies
- Cigarette Lighter Adapters
- Power Supply for Chargers

All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Quality Assurance.

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TYPICAL APPLICATION

![Typical Application Diagram]
ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Part Number*</th>
<th>Package</th>
<th>Top Marking</th>
</tr>
</thead>
<tbody>
<tr>
<td>MP9447GL</td>
<td>QFN-25 (3mm×4mm)</td>
<td>See Below</td>
</tr>
</tbody>
</table>

* For Tape & Reel, add suffix –Z (e.g. MP9447GL–Z)

TOP MARKING

9447: product code of MP9447GL;
MP: MPS prefix;
Y: year code;
W: week code;
LLL: lot number;

PACKAGE REFERENCE

TOP VIEW

VCC IN SW SW

AGND 1
FREQ 2
FB 3
SS 4
EN 5
NC 6
BST IN SW SW
EXPOSED PAD ON BACKSIDE

QFN25 (3×4mm)
ABSOLUTE MAXIMUM RATINGS (1)
Supply Voltage $V_{IN}$ ........................................ 40V
$V_{SW}$ ........................................ $-0.3V(-7V,<10\text{ns})$ to $V_{IN} + 0.3V$
$V_{BST}$ ........................................ $V_{SW} + 6V$
All Other Pins ......................................... -0.3V to +6V
Continuous Power Dissipation ($T_A = +25^\circ\text{C}$) (2)
............................................................................. 2.6W
Operating Junction Temperature .............. 150°C
Lead Temperature ....................................... 260°C
Storage Temperature ...................... -65°C to +150°C

Recommended Operating Conditions (3)
Supply Voltage $V_{IN}$ .............................. 4.5V to 36V
Output Voltage $V_{OUT}$ .................. 0.8V to 0.9×$V_{IN}$
Operating Junction Temp. ($T_J$). -40°C to +125°C

Thermal Resistance (4) $\theta_{JA}$ $\theta_{JC}$
QFN-25 (3mm×4mm) .................. 48 ...... 10... °C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$ (MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX) - $T_A$) $\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.
# ELECTRICAL CHARACTERISTICS

$V_{IN} = 24\text{V}, V_{EN} = 2\text{V}, T_{A} = +25^\circ\text{C}$, unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Current (Shutdown)</td>
<td>$I_{IN}$</td>
<td>$V_{EN} = 0\text{V}$</td>
<td>10</td>
<td></td>
<td>200</td>
<td>nA</td>
</tr>
<tr>
<td>Supply Current (Quiescent)</td>
<td>$I_{IN}$</td>
<td>$V_{FB} = 0.95\text{V}$</td>
<td>500</td>
<td>600</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>HS Switch On Resistance</td>
<td>$R_{DS-ON}$</td>
<td></td>
<td>65</td>
<td>75</td>
<td></td>
<td>mΩ</td>
</tr>
<tr>
<td>LS Switch On Resistance (5)</td>
<td>$R_{DS-ON}$</td>
<td></td>
<td>30</td>
<td></td>
<td></td>
<td>mΩ</td>
</tr>
<tr>
<td>Switch Leakage</td>
<td>$V_{SW} = 0\text{V}$, $V_{SW} = 0\text{V or 36V}$</td>
<td>10</td>
<td>200</td>
<td></td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>Current Limit</td>
<td>$I_{LIMIT}$</td>
<td></td>
<td>6</td>
<td>8</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>One-Shot On Time</td>
<td>$t_{ON}$</td>
<td>$V_{IN}=12\text{V}, R_{FREQ}=30k\Omega$</td>
<td>230</td>
<td>280</td>
<td>330</td>
<td>ns</td>
</tr>
<tr>
<td>Minimum Off Time (5)</td>
<td>$t_{OFF}$</td>
<td></td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Foldback Off Time (5)</td>
<td>$t_{FB}$</td>
<td>$I_{LIMIT}=1\text{(HIGH)}, V_{FB}&gt;50\text{%}V_{REF}$</td>
<td>4.8</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>Foldback Off Time (5)</td>
<td>$t_{FB}$</td>
<td>$I_{LIMIT}=1\text{(HIGH)}, V_{FB}&lt;50\text{%}V_{REF}$</td>
<td>16.8</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>OCP Hold-Off Time (5)</td>
<td>$t_{OC}$</td>
<td>$I_{LIMIT}=1\text{(HIGH)}$</td>
<td>100</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>Feedback Voltage</td>
<td>$V_{FB}$</td>
<td></td>
<td>803</td>
<td>815</td>
<td>827</td>
<td>mV</td>
</tr>
<tr>
<td>Feedback Current</td>
<td>$I_{FB}$</td>
<td>$V_{FB} = 815\text{mV}$</td>
<td>10</td>
<td>50</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>Soft-Start Charging Current</td>
<td>$I_{SS}$</td>
<td>$V_{SS}=0\text{V}$</td>
<td>6</td>
<td>8.5</td>
<td>11</td>
<td>μA</td>
</tr>
<tr>
<td>EN Rising Threshold</td>
<td>$EN_{Vth-Hi}$</td>
<td></td>
<td>1.0</td>
<td>1.25</td>
<td>1.4</td>
<td>V</td>
</tr>
<tr>
<td>EN Falling Threshold</td>
<td>$EN_{Vth-Lo}$</td>
<td></td>
<td>0.7</td>
<td>0.86</td>
<td>0.92</td>
<td>V</td>
</tr>
<tr>
<td>EN Threshold Hysteresis</td>
<td>$EN_{Vth-Hys}$</td>
<td></td>
<td>390</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>EN Input Current</td>
<td>$I_{EN}$</td>
<td>$V_{EN} = 2\text{V}$</td>
<td>1.5</td>
<td>2</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>$V_{IN}$ Under-Voltage Lockout</td>
<td>$INU_{Vth}$</td>
<td></td>
<td>3.7</td>
<td>4.0</td>
<td>4.3</td>
<td>V</td>
</tr>
<tr>
<td>Threshold Rising</td>
<td>$INU_{HY}$</td>
<td></td>
<td>880</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>$V_{CC}$ Regulator</td>
<td>$V_{CC}$</td>
<td>$I_{CC}=0$</td>
<td>4.5</td>
<td>4.85</td>
<td>5.2</td>
<td>V</td>
</tr>
<tr>
<td>$V_{CC}$ Load Regulation</td>
<td>$I_{CC}=10\text{mA}$</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>Thermal Shutdown (5)</td>
<td>$T_{SD}$</td>
<td></td>
<td>165</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Thermal Shutdown Hysteresis (5)</td>
<td>$T_{SD-HYS}$</td>
<td></td>
<td>25</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>

**Note:**

5) Derived from bench characterization, not tested in production.
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 24V, V_{OUT} = 3.3V, L = 10\mu H, T_A = +25^\circ C$, unless otherwise noted.

- **Efficiency vs. Load Current**
- **Fsw vs. VIN**
- **Fsw vs. Output Current**
- **Case Temperature Rise vs. Output Current**
- **Line Regulation**
- **Load Regulation**
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 24V$, $V_{OUT} = 3.3V$, $L = 10\mu H$, $T_A = +25^\circ C$, unless otherwise noted.

### Output Voltage Ripple
- $I_O = 0A$

### Start-up Through VIN
- $I_O = 0A$

### Start-up Through VIN
- $I_O = 5A$

### Shutdown Through VIN
- $I_O = 0A$

### Shutdown Through VIN
- $I_O = 5A$

### Start-up Through EN
- $I_O = 0A$

### Shutdown Through EN
- $I_O = 0A$

### Shutdown Through EN
- $I_O = 5A$
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

VIN = 24V, VOUT = 3.3V, L = 10µH, TA = +25°C, unless otherwise noted.

<table>
<thead>
<tr>
<th>Condition</th>
<th>IO</th>
<th>Chart Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shutdown Through EN</td>
<td>5A</td>
<td><img src="image" alt="Shutdown Chart" /></td>
</tr>
<tr>
<td>Short Circuit Entry</td>
<td>0A</td>
<td><img src="image" alt="Short Circuit Entry Chart" /></td>
</tr>
<tr>
<td>Short Circuit Entry</td>
<td>5A</td>
<td><img src="image" alt="Short Circuit Entry Chart" /></td>
</tr>
<tr>
<td>Short Circuit Steady State</td>
<td></td>
<td><img src="image" alt="Short Circuit Steady State Chart" /></td>
</tr>
<tr>
<td>Load Transient</td>
<td><a href="mailto:2.5A-5A@1.6A">2.5A-5A@1.6A</a>/µs</td>
<td><img src="image" alt="Load Transient Chart" /></td>
</tr>
<tr>
<td>Short Circuit Recovery</td>
<td>0A</td>
<td><img src="image" alt="Short Circuit Recovery Chart" /></td>
</tr>
<tr>
<td>Short Circuit Recovery</td>
<td>5A</td>
<td><img src="image" alt="Short Circuit Recovery Chart" /></td>
</tr>
</tbody>
</table>
### PIN FUNCTIONS

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>AGND</td>
<td>Analog Ground.</td>
</tr>
<tr>
<td>2</td>
<td>FREQ</td>
<td>Frequency Set (for CCM). The input voltage and the frequency-set resistor connected to GND determine the ON period. Decouple with a 1nF capacitor.</td>
</tr>
<tr>
<td>3</td>
<td>FB</td>
<td>Feedback. The tap of external resistor divider from the output to GND sets the output voltage.</td>
</tr>
<tr>
<td>4</td>
<td>SS</td>
<td>Soft-Start. Connect an external capacitor to program the soft-start time for the switch-mode regulator. When the EN pin goes HIGH, an internal current source (8.5µA) charges up the capacitor and the SS voltage slowly and smoothly ramps up from 0 to V_FB. When the EN pin goes LOW, the internal current source discharges the capacitor and the SS voltage slowly ramps down.</td>
</tr>
<tr>
<td>5</td>
<td>EN</td>
<td>Enable. EN=1 to enable the MP9447. For automatic start-up, connect EN pin to IN with a 100kΩ resistor. It includes an internal 1MΩ pull-down resistor.</td>
</tr>
<tr>
<td>6</td>
<td>NC</td>
<td>No Connection. DO NOT CONNECT. The pin must be float.</td>
</tr>
<tr>
<td>7</td>
<td>BST</td>
<td>Bootstrap. Requires a 0.1µF-to-1µF capacitor connected between SW and BS pins to form a floating supply across the high-side switch driver.</td>
</tr>
<tr>
<td>8, 19, Exposed pads 21, 22, 23</td>
<td>IN</td>
<td>Supply Voltage. The MP9447 operates from a 4.5V-to-36V input rail. Requires C_IN to decouple the input rail. Connect using wide PCB traces and multiple vias.</td>
</tr>
<tr>
<td>9, 10, 17, 18, Exposed pads 24, 25</td>
<td>SW</td>
<td>Switch Output. Connect using wide PCB traces and multiple vias.</td>
</tr>
<tr>
<td>11-16</td>
<td>PGND</td>
<td>System Ground. This pin is the reference ground of the regulated output voltage. For this reason care must be taken in PCB layout.</td>
</tr>
<tr>
<td>20</td>
<td>VCC</td>
<td>Internal Bias Supply. Decouple with a 1µF capacitor as close to the pin as possible.</td>
</tr>
</tbody>
</table>
Figure 1—Functional Block Diagram
OPERATION

PWM Operation

The MP9447 is a fully-integrated, synchronous, rectified, step-down, switch-mode converter. At the beginning of each cycle, the high-side MOSFET (HS-FET) turns ON when the feedback voltage (VFB) drops below the reference voltage (VREF), which indicates an insufficient output voltage. The ON period is determined by the input voltage and the frequency-set resistor as:

\[
t_{\text{ON}} \text{(ns)} = \frac{96 \times R_{\text{FREQ}} \times (\kappa \Omega)}{V_{\text{IN}}} + t_{\text{DELAY}} \text{(ns)}
\] (1)

After the ON period elapses, the HS-FET turns OFF. It is turned ON again when VFB drops below VREF. By repeating this operation, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) turns ON when the HS-FET is OFF to minimize conduction loss. A dead short occurs between input and GND if both the HS-FET and the LS-FET turn on at the same time (shoot-through). An internal dead-time (DT) generated between HS-FET OFF and LS-FET ON, or LS-FET OFF and HS-FET ON prevents shoot-through.

Heavy-Load Operation

In continuous-conduction mode (CCM), when the output current is HIGH, the HS-FET and LS-FET repeatedly turn ON/OFF as shown in Figure 2. The inductor current never goes to zero. In CCM, the switching frequency (fSW) is fairly constant.

Light-Load Operation

At light-load or no-load conditions, the output drops very slowly and the MP9447 reduces the switching frequency automatically to maintain high efficiency. Figure 3 shows the light-load operation. VFB does not reach VREF as the inductor current approaches zero. Hence, the output capacitors discharge slowly to GND through the LS-FET to greatly improve the light-load efficiency. At light loads, the HS-FET does not turn ON as frequently as at heavy loads. This is called skip mode.

Switching Frequency

The input voltage is feed-forwarded to the on-time one-shot timer through the resistor, R\text{FREQ}. The duty ratio remains at V\text{OUT}/V\text{IN}. Hence, the switching frequency is fairly constant over the input voltage range. The switching frequency can be set as:

\[
I_{\text{OUT}} = \frac{(V_{\text{IN}} - V_{\text{OUT}}) \times V_{\text{OUT}}}{2 \times L \times f_{\text{SW}} \times V_{\text{IN}}}
\] (2)

It enters PWM mode once the output current exceeds the critical level. After that, the switching frequency stays fairly constant over the output current range.
\[ F_{SW}(kHz) = \left( \frac{96 \times R_{PRED}(k\Omega) + t_{DELAY}(ns)}{V_{IN}} \right) \times \frac{V_{IN}}{V_{OUT}} \]  

(3)

Where \( t_{DELAY} \) is the comparator delay (~20ns).

The MP9447 is optimized for 200kHz-to-650kHz applications to operate at high switching frequencies with high efficiency. The high-switching frequency allows for smaller LC-filter components to reduce PCB space requirements.

Ramp Compensation

Figure 4 and Figure 5 show jitter occurring in both PWM mode and skip mode. Noise on \( V_{FB} \)'s downward slope causes the HS-FET ON time to deviate from its intended position and produces jitter. There is a relationship between system stability and the steepness of the \( V_{FB} \) ripple. The slope steepness of the \( V_{FB} \) ripple dominates noise immunity. The magnitude of the \( V_{FB} \) ripple doesn't affect the noise immunity directly.

In PWM mode has an equivalent circuit with HS-FET OFF and uses a external ramp compensation circuit (R4, C4), shown as a simplified circuit in Figure 6. Derive the external ramp from the inductor-ripple current. Choose C4, R1, and R2 to meet the following condition:

\[ \frac{1}{2\pi \times F_{SW} \times C_4} < \frac{1}{5} \times \frac{R_1 \times R_2}{R_1 + R_2} \]  

(4)

Then:

\[ I_{R4} = \frac{I_{FB}}{C_4} \approx I_{C4} \]  

(5)

The \( V_{FB} \) downward slope ripple is then estimated as:

\[ V_{SLOPE1} = \frac{-V_{OUT}}{R_4 \times C_4} \]  

(6)

From equation 6, reduce \( R_4 \) or \( C_4 \) to reduce instability in PWM mode. If \( C_4 \) cannot be reduced further due to equation 4's limitations, then only reduce \( R_4 \). Based on bench experiments, \( V_{SLOPE1} \) is around 20V/ms-40V/ms.

In the case of POSCAP or other types of capacitors with higher ESR, an external ramp is not necessary.
Figure 7 shows an equivalent circuit in PWM mode with the HS-FET OFF and without an external ramp circuit. The ESR ripple dominates the output ripple. The $V_{FB}$ downward slope is:

$$V_{SLOPE1} = \frac{-ESR \times V_{REF}}{L}$$  \hspace{1em} (7)

From equation 7, the $V_{FB}$ downward slope is proportional to ESR/L. Therefore, it's necessary to know the minimum ESR value of the output capacitors without an external ramp. There is also an inductance limit: A smaller inductance leads to more stability. Based on bench experiments, keep $V_{SLOPE1}$ around 15V/ms to 30V/ms.

In skip mode, the external ramp does not affect the downward slope, and $V_{FB}$ ripple’s downward slope is the same with or without the external ramp. Figure 8 shows an equivalent circuit with the HS-FET off and the current modulator regulating the LS-FET.

![Figure 8: Simplified Circuit in Skip Mode](image)

The $V_{FB}$ ripple’s downward slope is:

$$V_{SLOPE2} = \frac{-V_{REF}}{(R_1 + R_2) \times C_{OUT}}$$  \hspace{1em} (8)

To keep the system stable during light loads, avoid large $V_{FB}$ resistors. Also, keep the $V_{SLOPE2}$ value around 0.4V/ms to 0.8mV/ms. Note that $I_{MOD}$ is excluded from the equation because it does not impact the system’s light-load stability.

**Soft-Start**

The MP9447 employs soft start (SS) to ensure a smooth output during power-up. When the EN pin goes HIGH, an internal current source (8.5μA) charges up the SS capacitor ($C_{SS}$). The $C_{SS}$ voltage takes over the REF voltage to the PWM comparator. The output voltage smoothly ramps up with $V_{SS}$. Once $V_{SS}$ reaches the same level as $V_{REF}$, it continues ramping up while $V_{REF}$ takes over the PWM comparator. At this point, soft-start finishes and the MP9447 enters steady-state.

$C_{SS}$ is then:

$$C_{SS} (\text{nF}) = \frac{t_{ss} (\text{ms}) \times I_{SS} (\text{μA})}{V_{REF} (\text{V})}$$  \hspace{1em} (9)

If the output capacitors have large capacitance values, avoid setting a short SS or risk hitting the current limit during SS. Select a minimum value of 4.7nF if the output capacitance value exceeds 330μF.

**Over-Current Protection (OCP) and Short-Circuit Protection (SCP)**

The MP9447 has cycle-by-cycle over-current limit control. The inductor current is monitored during the ON state. Once the inductor current exceeds the current limit, the HS-FET turns OFF. At the same time, the OCP timer starts. The OCP timer is set at 100μs. Hitting the current limit during each cycle during this 100μs time frame will trigger hiccup SCP.

If a short circuit occurs, the MP9447 will immediately hit its current limit and $V_{FB}$ will drop below 50% × $V_{REF}$ (0.815V). The device considers this an output dead short and will trigger hiccup SCP immediately.

**Under-Voltage Protection (UVP)**

The MP9447 monitors the output voltage through the tap of a resistor divider to the FB pin to detect output under-voltage conditions. A $V_{FB}$ drop below 50% × $V_{REF}$ triggers UVP as well as a current-limit that triggers SCP.
UVLO Protection
The MP9447 has under-voltage lock-out protection (UVLO). When the input voltage is higher than the UVLO rising threshold voltage, the MP9447 will be powered up. It shuts off when the input voltage is lower than the UVLO falling threshold voltage. This is non-latch protection.

Floating Driver and Bootstrap Charging
An external bootstrap capacitor power the floating-power-MOSFET driver. A dedicated internal regulator charges and regulates the bootstrap capacitor voltage to ~5V. When the voltage between the BST and SW nodes drops below regulation, a PMOS pass transistor connected from VIN to BST turns on. The charging current path is from VIN, BST and then to SW. The external circuit should provide enough voltage headroom to facilitate charging.

As long as VIN is significantly higher than SW, the bootstrap capacitor remains charged. When the HS-FET is ON, V_{IN}=V_{SW} so the bootstrap capacitor cannot charge.

When the LS-FET is ON, V_{IN}-V_{SW} reaches its maximum for fast charging. When there is no inductor current, V_{SW}=V_{OUT} so the difference between V_{IN} and V_{OUT} can charge the bootstrap capacitor.

At higher duty cycles, the bootstrap-charging time is shorter so the bootstrap capacitor may not charge sufficiently. In case the internal circuit has insufficient voltage and time to charge the bootstrap capacitor, the bootstrap capacitor voltage will drop low. When V_{BST}-V_{SW} drops below 2.3V, the HS-FET turns OFF. A UVLO circuit allows the LS-FET to conduct and refresh the charge on the bootstrap capacitor. Once bootstrap capacitor voltage is charged, the HS-FET can turn on again and the part resumes normal switching. With this bootstrap refreshing function, MP9447 is able to work on the low dropout mode.

Thermal Shutdown
The MP9447 uses thermal shutdown. The junction temperature of the IC is internally monitored. If the junction temperature exceeds the threshold value (typically 165°C), the converter shuts off. This is a non-latched protection. There is about 25°C hysteresis. Once the junction temperature drops to about 140°C, it initiates a SS.
APPLICATION INFORMATION

Setting the Output Voltage

A resistor divider from the output voltage to the FB pin sets \( V_{OUT} \).

Without an external ramp employed, the feedback resistors (\( R_1 \) and \( R_2 \)) set the output voltage. To determine the values for the resistors, first, choose \( R_2 \) (typically 5k\( \Omega \)-40k\( \Omega \)). Then \( R_1 \) is:

\[
R_1 = \frac{V_{OUT} - V_{REF}}{V_{REF} \times R_2} \tag{10}
\]

When using a low-ESR ceramic capacitor on the output, add an external voltage ramp to the FB pin through \( R_4 \) and \( C_4 \). The ramp voltage (\( V_{RAMP} \)) affects output voltage. Calculate \( V_{RAMP} \) as per equation 19. Choose \( R_2 \) between 5k\( \Omega \) and 40k\( \Omega \). Determine \( R_1 \) as:

\[
R_1 = \left( \frac{V_{REF} + \frac{1}{2}V_{RAMP}}{R_2 \times (V_{OUT} - V_{REF} - \frac{1}{2}V_{RAMP})} \right)^{-1} \tag{11}
\]

Using equation 11 to calculate the output voltage can be complicated. Furthermore, as \( V_{RAMP} \) changes due to changes in \( V_{OUT} \) and \( V_{IN} \), \( V_{FB} \) also varies. To improve the output voltage accuracy and simplify the \( R_2 \) calculation from equation 11, add a DC-blocking capacitor (\( C_{DC} \)). Figure 9 shows a simplified circuit with external ramp compensation and a DC-blocking capacitor. Equation 10 can then estimate \( R_1 \).

Select a \( C_{DC} \) value between 1\( \mu \)F and 4.7\( \mu \)F to improve DC-blocking performance.

Input Capacitor

The input current to the step-down converter is discontinuous, and therefore requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance. Be sure to place the input capacitors as close to the IN pin as possible.

The capacitance varies significantly with temperature. Capacitors with X5R and X7R ceramic dielectrics are fairly stable over temperature fluctuations.

The capacitors must also have a ripple-current rating greater than the converter’s maximum input-ripple current. The input ripple current can be estimated as follows:

\[
I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \tag{12}
\]

The worst-case condition occurs at \( V_{IN} = 2V_{OUT} \), where:

\[
I_{CIN} = \frac{I_{OUT}}{2} \tag{13}
\]

For simplification, choose an input capacitor whose RMS current rating is greater than half of the maximum load current. The input capacitance value determines the input voltage ripple of the converter. If there is an input-voltage-ripple requirement in the system design, choose an input capacitor that meets the specification.

The input voltage ripple can be estimated as follows:

\[
\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{14}
\]

The worst-case condition occurs at \( V_{IN} = 2V_{OUT} \), where:

\[
\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \tag{15}
\]
Output Capacitor
The output capacitor maintains the DC output voltage. Use ceramic or POSCAP capacitors. The output voltage ripple can be estimated as:

\[ \Delta V_{\text{OUT}} = \frac{V_{\text{OUT}}}{F_{\text{SW}} \times L} \times (1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}) \times (\frac{R_{\text{ESR}}}{8 \times F_{\text{SW}} \times C_{\text{OUT}}} + 1) \]  (16)

Where \( R_{\text{ESR}} \) is the equivalent series resistance of the output capacitor.

For ceramic capacitors, capacitance dominates the impedance at the switching frequency, can is the primary cause of the output-voltage ripple. For simplification, estimate the output voltage ripple as:

\[ \Delta V_{\text{OUT}} = \frac{V_{\text{OUT}}}{8 \times F_{\text{SW}} \times L \times C_{\text{OUT}}} \times (1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}) \]  (17)

The output voltage ripple caused by ESR is very small and therefore requires an external ramp to stabilize the system. The voltage ramp is ~30mV. The external ramp can be generated through \( R_4 \) and \( C_4 \) using the following equation:

\[ V_{\text{RAMP}} = \frac{(V_{\text{IN}} - V_{\text{OUT}}) \times T_{\text{ON}}}{R_4 \times C_4} \]  (18)

Select \( C_4 \) to meet the following condition:

\[ \frac{1}{2 \pi \times F_{\text{SW}} \times C_4} < \frac{1}{5} \times \left( \frac{R_1 \times R_2}{R_1 + R_2} \right) \]  (19)

For POSCAP capacitors, the ESR dominates the impedance at the switching frequency. The ramp voltage generated from the ESR is high enough to stabilize the system. Therefore, an external ramp is not needed. A minimum ESR value of 12mΩ is required to ensure stable operation of the converter. For simplification, the output ripple can be approximated as:

\[ \Delta V_{\text{OUT}} = \frac{V_{\text{OUT}}}{F_{\text{SW}} \times L} \times (1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}) \times R_{\text{ESR}} \]  (20)

Inductor
The inductor is required to supply constant current to the output load while being driven by the switching input voltage. A larger inductance will result in less ripple current and a lower output ripple voltage. However, a larger inductance results in a larger inductor, which will physically larger, and have a higher series resistance and/or lower saturation current. A good rule for determining the inductor value is to allow the peak-to-peak ripple current in the inductor to be approximately 30% to 40% of the maximum switch current limit. Ensure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated as:

\[ L = \frac{V_{\text{OUT}}}{F_{\text{SW}} \times \Delta I_L} \times (1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}) \]  (21)

Where \( \Delta I_L \) is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated as:

\[ I_{\text{LP}} = I_{\text{OUT}} + \frac{V_{\text{OUT}}}{2F_{\text{SW}} \times L} \times (1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}) \]  (22)

Typical Design Parameter Tables
The following tables include recommended component values for typical output voltages (3.3V, 5V) and switching frequencies (300kHz, 500kHz). Refer to Tables 1 through 2 for design cases without external ramp compensation, and Tables 3 through 4 for design cases with external ramp compensation. An external ramp is not needed when using high-ESR capacitors, such as electrolytic or POSCAPs. An external ramp is needed when using low-ESR capacitors, such as ceramic capacitors. For cases not listed in this datasheet, an Excel spreadsheet available through your local sales representative can calculate approximate component values.

Table 1—300kHz, 24V IN

<table>
<thead>
<tr>
<th>V_{\text{OUT}} (V)</th>
<th>L (μH)</th>
<th>R1 (kΩ)</th>
<th>R2 (kΩ)</th>
<th>R_{\text{FREQ}} (kΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3</td>
<td>10</td>
<td>30.1</td>
<td>10</td>
<td>110</td>
</tr>
<tr>
<td>5</td>
<td>10</td>
<td>51.1</td>
<td>10</td>
<td>169</td>
</tr>
</tbody>
</table>

Table 2—500kHz, 24V IN

<table>
<thead>
<tr>
<th>V_{\text{OUT}} (V)</th>
<th>L (μH)</th>
<th>R1 (kΩ)</th>
<th>R2 (kΩ)</th>
<th>R_{\text{FREQ}} (kΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3</td>
<td>10</td>
<td>30.1</td>
<td>10</td>
<td>63.4</td>
</tr>
<tr>
<td>5</td>
<td>10</td>
<td>51.1</td>
<td>10</td>
<td>100</td>
</tr>
</tbody>
</table>
### Table 3—300kHz, 24V\textsubscript{IN}

<table>
<thead>
<tr>
<th>V\textsubscript{OUT} (V)</th>
<th>L (\textmu H)</th>
<th>R\textsubscript{1} (k\Omega)</th>
<th>R\textsubscript{2} (k\Omega)</th>
<th>R\textsubscript{4} (k\Omega)</th>
<th>C\textsubscript{4} (pF)</th>
<th>R\textsubscript{FREQ} (k\Omega)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3</td>
<td>10</td>
<td>30.9</td>
<td>10</td>
<td>953</td>
<td>390</td>
<td>110</td>
</tr>
<tr>
<td>5</td>
<td>10</td>
<td>53.6</td>
<td>10</td>
<td>845</td>
<td>560</td>
<td>169</td>
</tr>
</tbody>
</table>

### Table 4—500kHz, 24V\textsubscript{IN}

<table>
<thead>
<tr>
<th>V\textsubscript{OUT} (V)</th>
<th>L (\textmu H)</th>
<th>R\textsubscript{1} (k\Omega)</th>
<th>R\textsubscript{2} (k\Omega)</th>
<th>R\textsubscript{4} (k\Omega)</th>
<th>C\textsubscript{4} (pF)</th>
<th>R\textsubscript{FREQ} (k\Omega)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3</td>
<td>10</td>
<td>31.6</td>
<td>10</td>
<td>620</td>
<td>390</td>
<td>63.4</td>
</tr>
<tr>
<td>5</td>
<td>10</td>
<td>53.6</td>
<td>10</td>
<td>845</td>
<td>390</td>
<td>100</td>
</tr>
</tbody>
</table>
LAYOUT RECOMMENDATION

1. Place high-current paths (GND, IN, and SW) very close to the device with short, direct, and wide traces.
2. Place input capacitors on both VIN sides (PIN8 and PIN19) and as close to the IN and GND pins as possible.
3. Place the decoupling capacitor as close to the VCC and GND pins as possible.
4. Keep the switching node SW short and away from the feedback network.
5. Place the external feedback resistors next to the FB pin. Do not place vias on the FB trace.
6. Keep the BST voltage path (BST, C3, and SW) as short as possible.
7. Connect the bottom IN and SW pads to a large copper area to achieve better thermal performance.
8. A Four-layer layout is strongly recommended to achieve better thermal performance.

Figure 10: PCB Layout
TYPICAL APPLICATION CIRCUITS

![Typical Application Circuit, 5V-Output](image)

**Figure 11:** Typical Application Circuit, 5V-Output
PACKAGE INFORMATION

QFN-25 (3mm × 4mm)

TOPOGRAPHIC MAP

DETAIL A

RECOMMENDED LAND PATTERN

NOTE:
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.