MP8883

45V, 3A, High-Efficiency, Digital, Configurable, Synchronous Step-Down Converter with I^{2}C Interface

DESCRIPTION

The MP8883 is a high-frequency, synchronous, rectified step-down converter with an I^{2}C control interface and multiple-page one-time programmable (OTP) memory. It can achieve up to 3A of continuous output current (I_{OUT}) across a wide input voltage (V_{IN}) range, with excellent load and line regulation.

The MP8883 is designed to be very versatile. The output voltage (V_{OUT}) can be set between 0.8V and 12V via the I^{2}C serial interface. The switching slew rate, switching frequency (f_{SW}), enable (EN) control, and power-save mode can also be configured via the I^{2}C. This allows users to optimize each output for the specific application requirements.

During bench evaluations, different configurations can be evaluated via the I^{2}C interface instead of reworking external components. The OTP can permanently store the optimal settings.

The integrated, internal high-side and low-side power MOSFETs (HS-FETs and LS-FETs, respectively) provide high efficiency without the use of an external Schottky diode.

Current mode provides fast transient response and eases loop stabilization. Full protection features include under-voltage lockout (UVLO) protection, over-voltage protection (OVP), over-current protection (OCP), and thermal shutdown.

With an internal feedback (FB) divider and compensation, the MP8883 offers a very compact solution with a minimal number of readily available, standard external components. It is available in a QFN-16 (3mmx3mm) package.

FEATURES

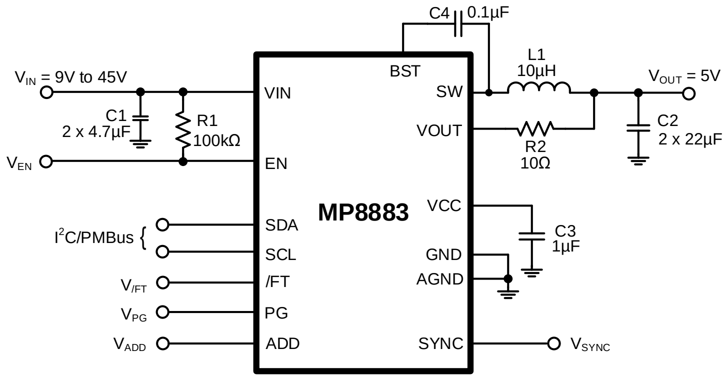
- Wide 3.5V to 45V Input Voltage (V_{IN}) Range
- 3A Continuous Output Current (I_{OUT})
- High-Efficiency Synchronous Mode Control
- Internal 95mΩ/50mΩ Low $R_{DS(ON)}$ MOSFETs
- Power Good (PG) and Fault Indication
- OVP, OCP, and Thermal Shutdown
- Internal Soft Start (SS)
- Configurable Address via a Resistor
- Configurable via the I^{2}C Interface:
    - 0.8V to 12V Output Voltage (V_{OUT})
    - Switching Frequency (f_{SW})
    - Compensation Network
    - Slope Compensation
    - EN Threshold
    - PG Threshold
    - Selectable Advanced Asynchronous Modulation (AAM) Mode and Continuous Conduction Mode (CCM)
    - Light-Load Mode Threshold
    - Selectable Short-Circuit Protection (SCP) Mode
    - Current-Limit Threshold
    - Selectable OVP Mode
    - Input UVLO and OVP Thresholds
    - Output OVP Threshold
    - Thermal Shutdown Threshold
    - Switching Slew Rate
    - Soft-Start Time (t_{SS})
    - Selectable SYNC Input/Output
    - Phase Shift
    - Frequency Dithering for Low EMI
- Multi-Page One-Time Programmable (OTP) Memory for Permanent Storage
- Available in a QFN-16 (3mmx3mm) Package

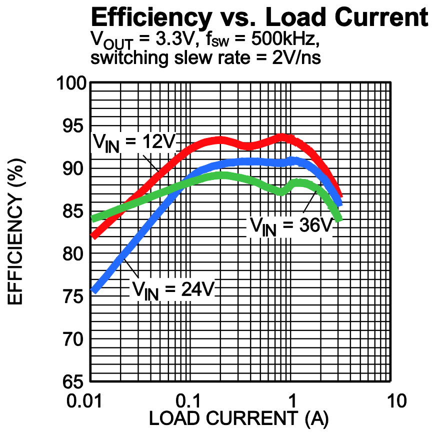
MPL Optimized Performance with MPS MPL-AY1050 Inductor Series

APPLICATIONS

- Industrial Power Systems
- Telecommunication Power Systems

TYPICAL APPLICATION




Efficiency vs. Load Current

V_{OUT} = 3.3V, f_{SW} = 500kHz, switching slew rate = 2V/ns

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP8883GQ-xxxx**	QFN-16 (3mmx3mm)	*See Below*	1
MP8883GQ-0001	QFN-16 (3mmx3mm)	*See Below*	
MP8883GQ-0002	QFN-16 (3mmx3mm)	*See Below*	
EVKT-MP8883	Evaluation kit	-	

* For Tape & Reel, add suffix -Z (e.g. MP8883GQ-xxxx-Z).

****** “xxxx” is the configuration identifier for the register settings stored in the one-time programmable (OTP) memory. Each “x” can be a hexadecimal value between 0 and F. The MP8883GQ-0001 is the default code for internal feedback (FB) divider mode (see Table 3 and Table 4 on page 28). The MP8883GQ-0002 is the default code for external FB divider mode (see Table 5 and Table 6 on page 29). For customized configurations, contact an MPS FAE to create a unique code.

TOP MARKING

BFHY
LLL

BFH: Product code
Y: Year code
LLL: Lot number

EVALUATION KIT EVKT-MP8883

EVKT-MP8883 kit contents (items below can be ordered separately): (1)

#	Part Number	Item	Quantity
1	EVL8883-Q-00A	MP8883 evaluation board for single-phase operation	1
2	EVKT-USBI2C-02	Includes one USB to I^2C communication interface device, one USB cable, and one ribbon cable	1
3	MP8883GQ-0001	The MP8883, which can be configured via the OTP	2
4	Online resources	Include MPS’s Virtual Bench Pro 4.0	-

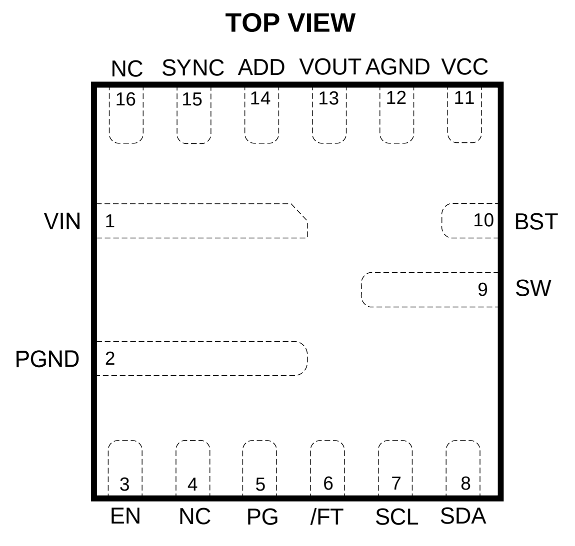
Order directly from MonolithicPower.com or our distributors.

Figure 1: Evaluation Kit Set-Up

Note:

1) Ensure that the input voltage (V_{IN}) is between 8V and 36V when writing to the RAM or ROM. To use the evaluation kit, download the GUI from the MPS website or contact an MPS FAE.

PACKAGE REFERENCE



QFN-16 (3mmx3mm)

PIN FUNCTIONS

Pin #	Name	Description
1	VIN	**Input voltage.** The VIN pin supplies power to the converter. Connect a decoupling capacitor between the VIN and PGND pins. Place this capacitor as close to the IC as possible to reduce switching spikes. Use a wide PCB trace to make the VIN connection.
2	PGND	**Power ground.** The PGND pin is the reference ground of the regulated output voltage (V_{OUT}). Connect PGND to a large copper area to improve thermal dissipation.
3	EN	**Enable.** Pull the EN pin high to turn the converter on; pull EN low to turn it off. Do not float EN.
4	NC	**Not connected.** Float the NC pin, or connect NC to ground.
5	PG	**Power good indicator.** The PG pin is an open-drain output that requires an external pull-up resistor.
6	/FT	**Fault indication.** The /FT pin is puled low if a fault or fault warning occurs. /FT is an open-drain output that requires an external pull-up resistor.
7	SCL	**I²C serial clock.**
8	SDA	**I²C serial data.**
9	SW	**Switch output.** Connect the SW pin and the inductor using a wide PCB trace.
10	BST	**Bootstrap.** Connect a capacitor between the SW and BST pins to form a floating supply across the high-side MOSFET (HS-FET) driver.
11	VCC	**Internal 5V LDO output.** Decouple the VCC pin using a 1µF decoupling capacitor.
12	AGND	**Signal ground.** The AGND pin is the ground for the internal logic and signal circuitry. AGND is not connected to PGND internally. Ensure that AGND is connected to PGND when designing the PCB layout.
13	VOUT	**Output voltage sense input.**
14	ADD	**I²C address setting.**
15	SYNC	**Synchronized external clock signal.** The SYNC pin can be configured for synchronous input or output via the I²C.
16	NC	**Not connected.** Float the NC pin, or connect NC to ground.

ABSOLUTE MAXIMUM RATINGS (2)

Input voltage (V_{IN}) ....-0.3V to +48V
V_{SW}................................ -0.3V (-10V for <3ns) to
V_{IN} + 0.3V (+50V for <3ns)
V_{EN} ....-0.3V to +48V
V_{BST} .... V_{SW} + 5.5V
V_{CC} ....-0.3V to +5.5V
V_{OUT} ....-0.3V to +15V
All other pins ....-0.3V to 5V
Continuous power dissipation (T_A = 25°C) (3) (7)
QFN-16 (3mmx3mm)............................ 3.149W
Junction temperature ....150°C
Lead temperature ....260°C
Storage temperature .... -65°C to +150°C

ESD Ratings

Human body model (HBM) (4)..................... ±2kV
Charged device model (CDM) (5).............. ±750V

Recommended Operating Conditions (6)

Input voltage (V_{IN}) ....3.5V to 45V
Output voltage (V_{OUT}).......................0.8V to 12V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance

	θ_{JA}	θ_{JC}	
EVL8883-Q-00A (7)	31.75	7.25	°C/W
JESD51-7 (8)	55	13	°C/W

Notes:

2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the converter may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The human body model (HBM) is per JEDEC specification JESD22-A114. JEDEC document JEP155 states that a 500V HBM allows for safe manufacturing with a standard ESD control process.
5) The charged device model is per JEDEC specification JESD22-C101. JEDEC document JEP157 states that a 250V CDM allows for safe manufacturing with a standard ESD control process.
6) The device is not guaranteed to function outside of its operating conditions. For the typical application circuit, see page 33.
7) Measured on the EVL8883-Q-00A (64mmx64mm), 4-layer PCB.
8) Measured on JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C (9), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input voltage (V_{IN}) under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_RISING}$	Register 05h, bits[3:1] = 0b000	2.9	3.2	3.4	V
V_{IN} UVLO threshold hysteresis	$V_{IN\_UVLO\_HYS}$	Register 05h, bit[0] = 0b1		4		%
DAC V_{IN} UVLO threshold	$V_{IN\_UVLO\_DAC}$		3.2		7.4	V
Quiescent current	I_Q	T_J = 25°C; register 00h = 0x64; register 01h, bits[1:0] = 0b01; V_{OUT} = 5V		600	1000	μA
Shutdown current	I_{SD}	V_{EN} = 0V, T_J = 25°C			1	μA
Default output voltage	V_{OUT}	T_J = 25°C; register 00h = 0x64; register 01h, bits[1:0] = 0b01	4.95	5	5.05	V
		T_J = -40°C to +125°C	4.925	5	5.075	V
Operating V_{OUT} range			0.8		12	V
Default switching frequency	f_{SW}	T_J = 25°C; register 02h, bits[5:0] = 0b001010	450	500	550	kHz
Configurable frequency range	f_{PROG}		250		2500	kHz
Synchronous frequency range	f_{SYNC}		250		2500	kHz
Synchronous V_{IN} high threshold	V_{SYNC_HIGH}		2			V
Synchronous V_{IN} low threshold	V_{SYNC_LOW}				0.4	V
Minimum on time (10)	t_{ON_MIN}	Peak current control mode		80		ns
Minimum off time (10)	t_{OFF_MIN}			380		ns
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$	V_{BST} - V_{SW} = 5V		95	180	mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$			50	100	mΩ
Default rising switching slew rate (10)	SR_{RISING}	Register 09h, bits[2:1] = 0b00		1		V/ns
SR_{RISING} range (10)			1		4	V/ns
Default falling switching slew rate (10)	$SR_{FALLING}$	Register 09h, bits[4:3] = 0b00		1		V/ns
$SR_{FALLING}$ range (10)			1		4	V/ns
BST to SW refresh UVLO threshold	V_{BST_UVLO}			2.4	2.8	V
BST to SW refresh UVLO hysteresis	$V_{BST\_UVLO\_HYS}$			0.2		V
Default soft-start time	t_{SS}	Register 04h, bits[7:6] = 0b01		1		ms
t_{SS} range			0.5		4	ms
Default EN voltage	V_{EN}	Register 05h, bits[6:5] = 0b01	1.2	1.4	1.6	V
V_{EN} range			1.2		2	V
Default V_{EN} hysteresis	V_{EN_HYS}	Register 05h, bit[4] = 0b0		220		mV
V_{EN_HYS} range			220		420	mV

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C (9), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Default power good (PG) upper rising threshold	V_{PG_UP}		108	110	112	% of V_{OUT}
V_{PG_UP} range			110		115	% of V_{OUT}
Default PG lower rising threshold	V_{PG_LOW}		86	89	92	% of V_{OUT}
V_{PG_LOW} range			84		89	% of V_{OUT}
Default PG threshold hysteresis	V_{PG_HYS}			5.5		% of V_{OUT}
V_{PG_HYS} range			3		5.5	% of V_{OUT}
PG low voltage	V_{PG_LOW}	I_{SINK} = 1mA		0.1	0.3	V
PG rising deglitch timer	$t_{PG\_DELAY\_RISING}$			30		µs
PG falling deglitch timer	$t_{PG\_DELAY\_FALLING}$			30		µs
VCC regulator voltage	V_{CC}	I_{CC} = 5mA	4.7	5	5.2	V
Default peak current limit (10)	I_{LIMIT_PEAK}	Register 06h, bits[5:3] = 0b000	4.2	5	5.8	A
I_{LIMIT_PEAK} range			2		8	A
Default valley current limit (10)	I_{LIMIT_VALLEY}	Register 06h, bits[2:1] = 0b10	3	4	5.2	A
I_{LIMIT_VALLEY} range			2		4	A
Default output OVP threshold	V_{OUT_OVP}	Register 07h, bits[2:1] = 0b01	115	120	125	% of V_{OUT}
V_{OUT_OVP} range			110		130	% of V_{OUT}
Default V_{OUT_OVP} hysteresis	$V_{OUT\_OVP\_HYS}$	Register 07h, bit[0] = 0b0		5.7		% of V_{OUT}
$V_{OUT\_OVP\_HYS}$ range		I^2C-configurable	3.2		5.7	% of V_{OUT}
Input OVP threshold	V_{IN_OVP}	Register 01h, bits[3:2] = 0b10	31	34	36	V
V_{IN_OVP} range			28		40	V
Default V_{IN_OVP} hysteresis	$V_{IN\_OVP\_HYS}$	Register 01h, bit[4] = 0b1		3.5		% of V_{IN_OVP}
$V_{IN\_OVP\_HYS}$ range			3.5		5.5	% of V_{IN_OVP}
Default thermal shutdown (10)	T_{SD}	Register 07h, bits[7:6] = 0b10		175		°C
T_{SD} range (10)			125		175	°C
Default T_{SD} hysteresis (10)	T_{SD_HYS}	Register 07h, bit[5] = 0b0		25		°C
T_{SD_HYS} range (10)			25		50	°C

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C (9), typical values are tested at T_J = 25°C, unless otherwise noted.

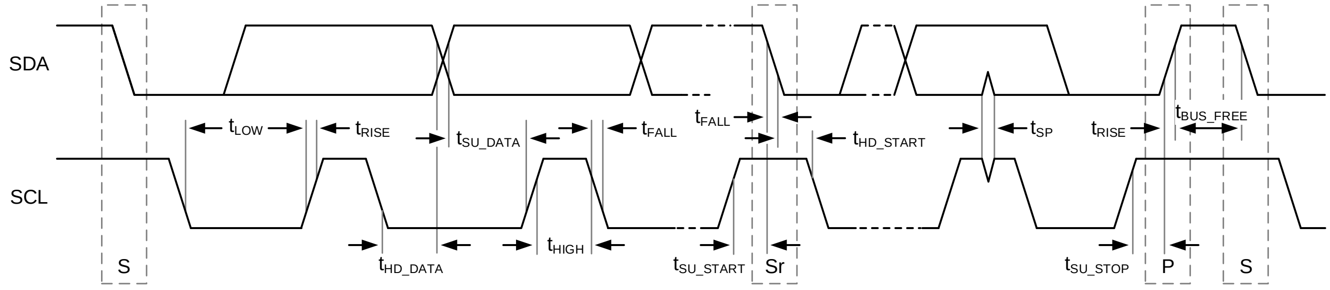
Parameters	Symbol	Condition	Min	Typ	Max	Units
I^2C Interface Specifications (10)						
Input logic low	V_{IN_LOW}				0.4	V
Input logic high	V_{IN_HIGH}		1.3			V
Output logic low	V_{OUT_LOW}	I_{LOAD} = 3mA			0.4	V
SCL clock frequency	f_{SCL}				400	kHz
SCL high time	t_{HIGH}		0.6			µs
SCL low time	t_{LOW}		1.3			µs
Data set-up time	t_{SU_DATA}		100			ns
Data hold time	t_{HD_DATA}		0		0.9	µs
Set-up time for repeated start condition	t_{SU_START}		0.6			µs
Hold time for start condition	t_{HD_START}		0.6			µs
Bus free time between a start and stop condition	t_{BUS_FREE}		1.3			µs
Set-up time for stop condition	t_{SU_STOP}		0.6			µs
SCL/SDA rise time	t_{RISE}		20 + 0.1 x C_B		120	ns
SCL/SDA fall time	t_{FALL}		20 + 0.1 x C_B		120	ns
Suppressed spike pulse width	t_{SPIKE}		0		50	ns
Bus capacitance per bus line	C_{BUS}				400	pF

Note:

9) Guaranteed by over-temperature correlation. Not tested in production.

10) Guaranteed by characterization. Not tested in production.

TIMING DIAGRAM



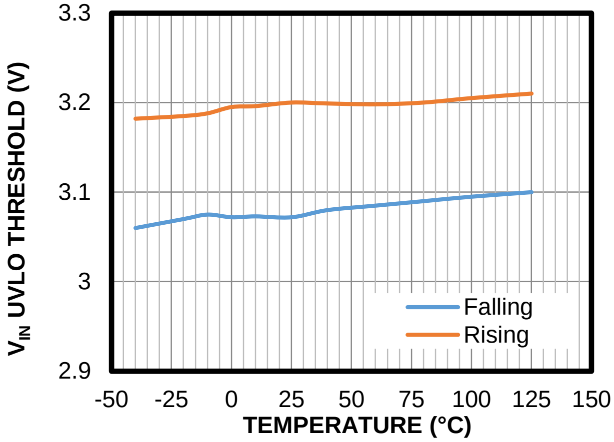
S = Start
Sr = Repeated Start
P = Stop

Figure 1: Timing Diagram

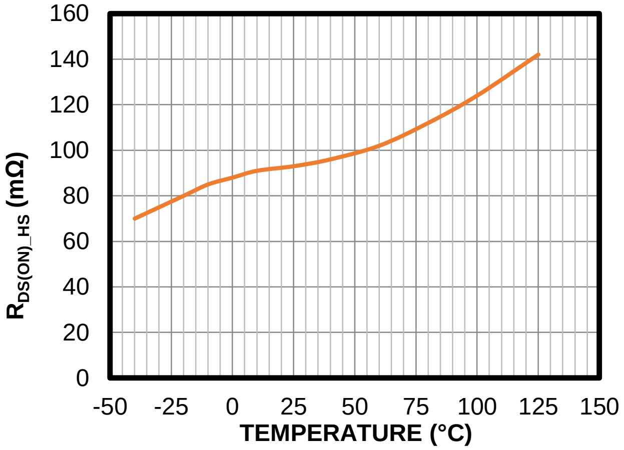
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C, unless otherwise noted.

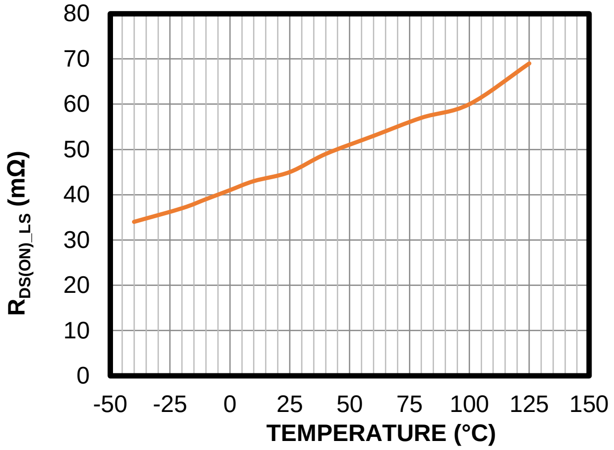
V_{IN} UVLO Threshold vs. Temperature



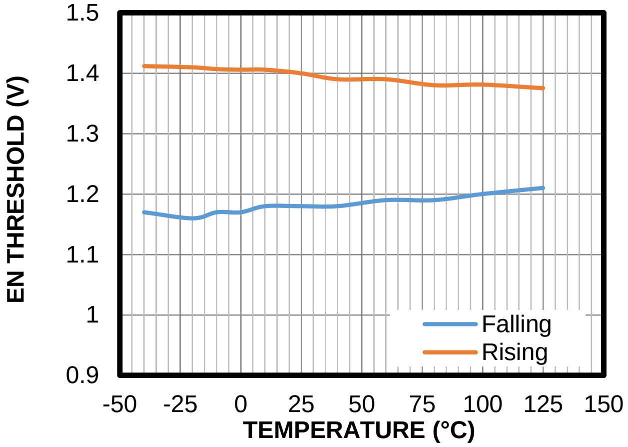
HS-FET On Resistance vs. Temperature



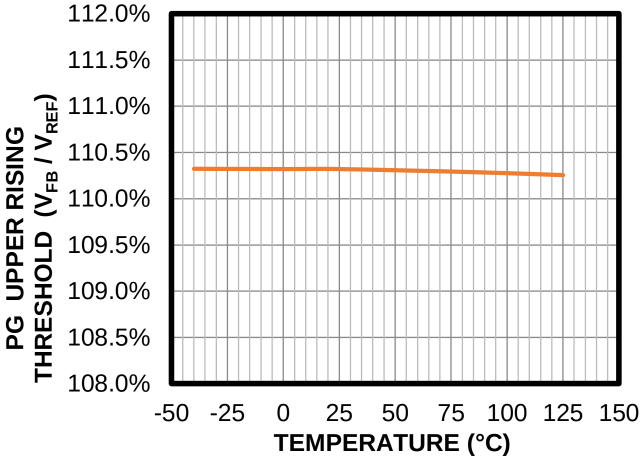
LS-FET On Resistance vs. Temperature



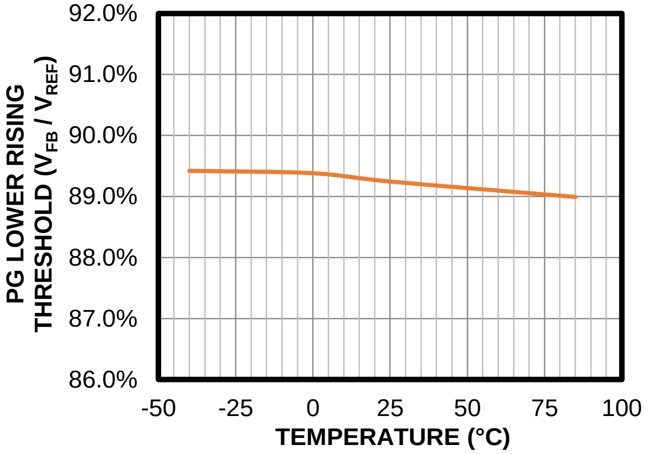
EN Threshold vs. Temperature



PG Upper Rising Threshold vs. Temperature



PG Lower Rising Threshold vs. Temperature

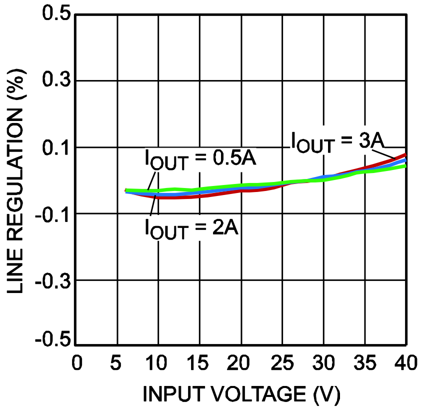


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, L = 10µH, f_{SW} = 500kHz, AAM mode, T_A = 25°C, unless otherwise noted.

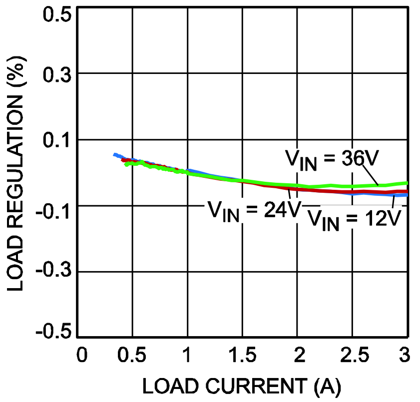
Line Regulation

V_{OUT} = 5V



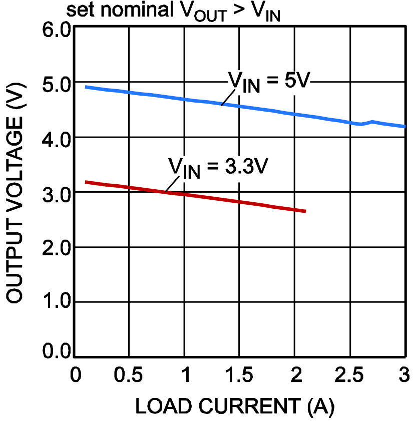
Load Regulation

V_{OUT} = 5V



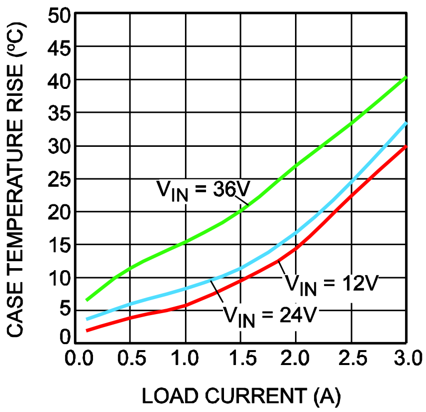
Output Voltage vs. Load Current

Dropout performance
set nominal $V_{OUT} > V_{IN}$



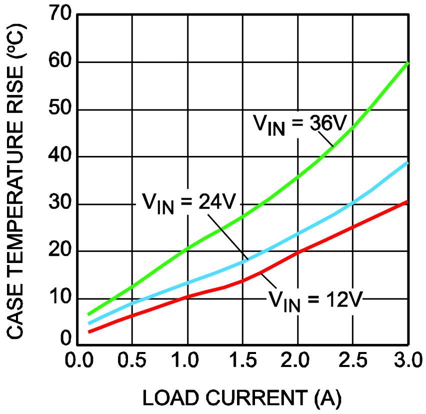
Case Temperature Rise

V_{OUT} = 3.3V, f_{SW} = 500kHz,
switching slew rate = 2V/ns



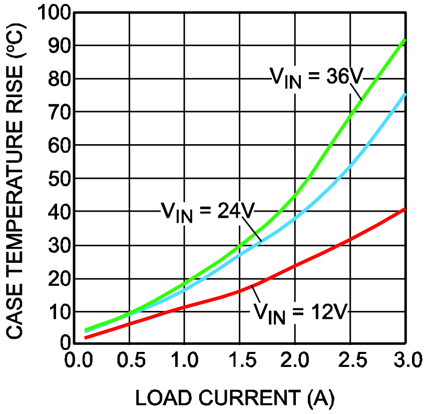
Case Temperature Rise

V_{OUT} = 3.3V, f_{SW} = 1MHz,
switching slew rate = 2V/ns



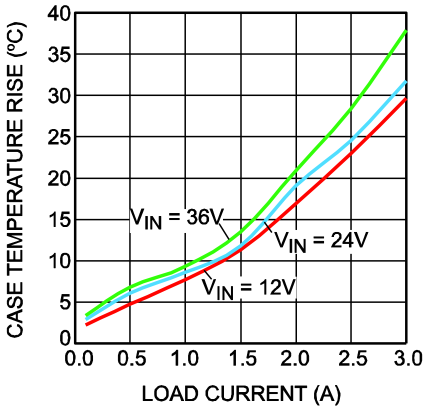
Case Temperature Rise

V_{OUT} = 3.3V, f_{SW} = 2MHz,
switching slew rate = 2V/ns



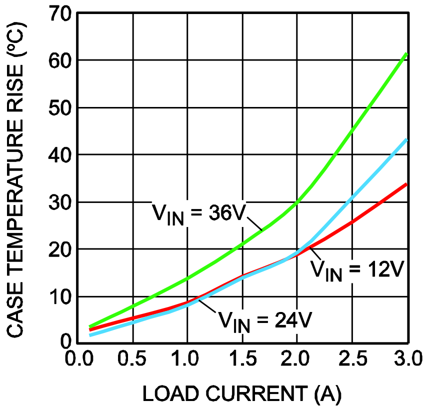
Case Temperature Rise

V_{OUT} = 5V, f_{SW} = 500kHz,
switching slew rate = 2V/ns



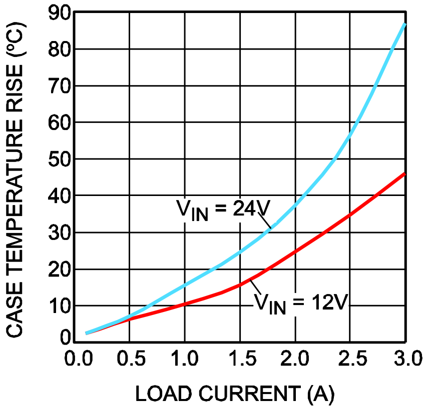
Case Temperature Rise

V_{OUT} = 5V, f_{SW} = 1MHz,
switching slew rate = 2V/ns



Case Temperature Rise

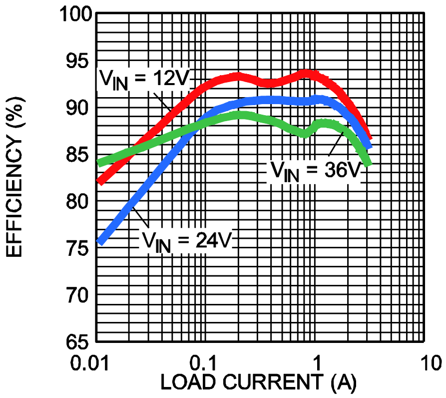
V_{OUT} = 5V, f_{SW} = 2MHz,
switching slew rate = 2V/ns



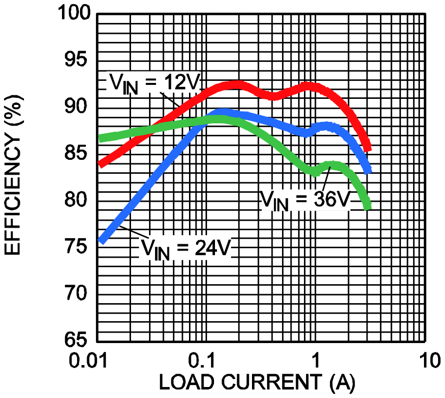
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, L = 10µH, f_{SW} = 500kHz, AAM mode, T_A = 25°C, unless otherwise noted.

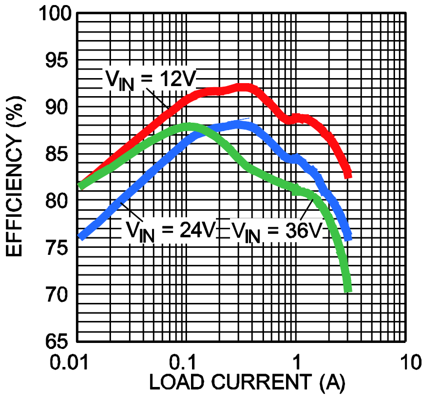
Efficiency vs. Load Current
V_{OUT} = 3.3V, f_{SW} = 500kHz,
switching slew rate = 2V/ns



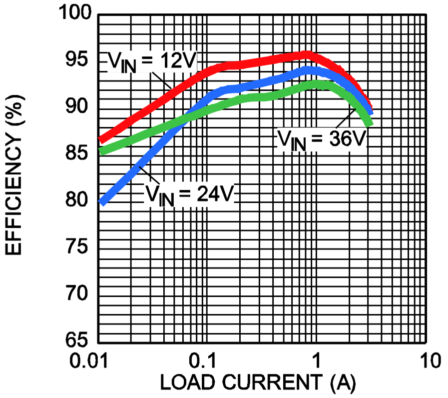
Efficiency vs. Load Current
V_{OUT} = 3.3V, f_{SW} = 1MHz,
switching slew rate = 2V/ns



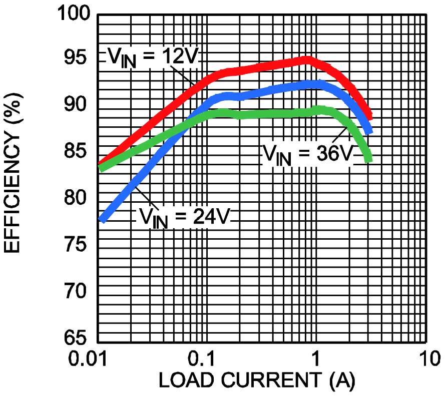
Efficiency vs. Load Current
V_{OUT} = 3.3V, f_{SW} = 2.2MHz,
switching slew rate = 2V/ns



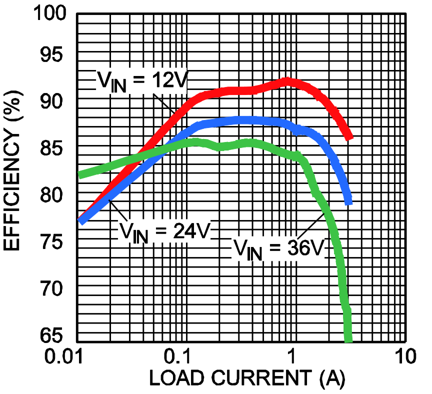
Efficiency vs. Load Current
V_{OUT} = 5V, f_{SW} = 500kHz,
switching slew rate = 2V/ns



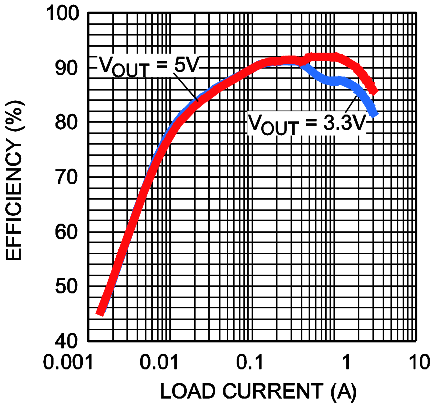
Efficiency vs. Load Current
V_{OUT} = 5V, f_{SW} = 1MHz,
switching slew rate = 2V/ns



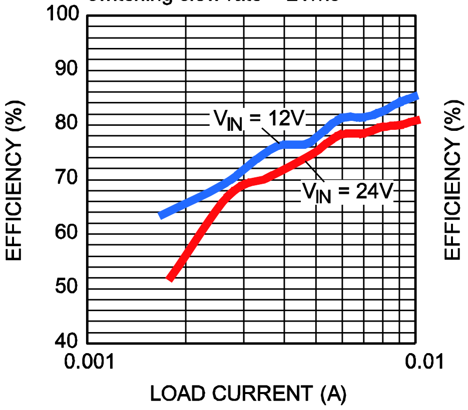
Efficiency vs. Load Current
V_{OUT} = 5V, f_{SW} = 2.2MHz,
switching slew rate = 2V/ns



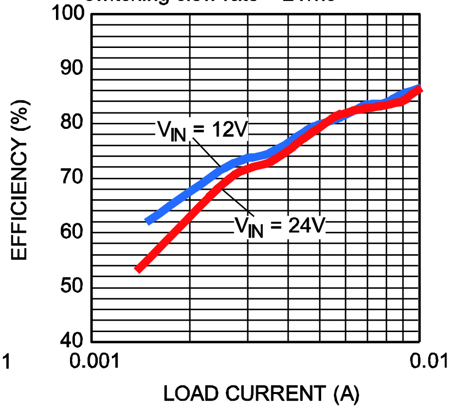
Efficiency vs. Load Current
V_{IN} = 14V, f_{SW} = 2.2MHz,
switching slew rate = 2V/ns



Efficiency vs. Load Current
At extremely light loads,
V_{OUT} = 3.3V, f_{SW} = 2.2MHz,
switching slew rate = 2V/ns



Efficiency vs. Load Current
At extremely light loads,
V_{OUT} = 5V, f_{SW} = 2.2MHz,
switching slew rate = 2V/ns

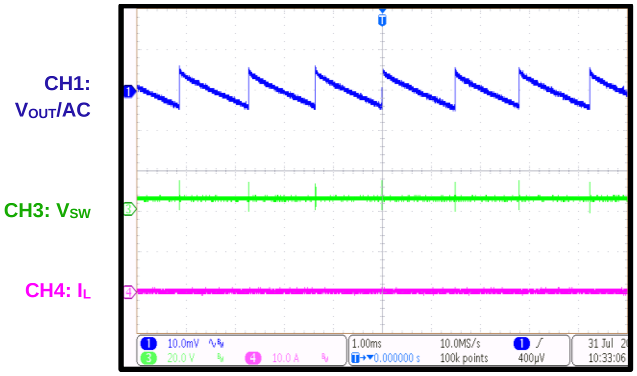


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 10µH, f_{SW} = 500kHz, AAM mode, T_A = 25°C, unless otherwise noted.

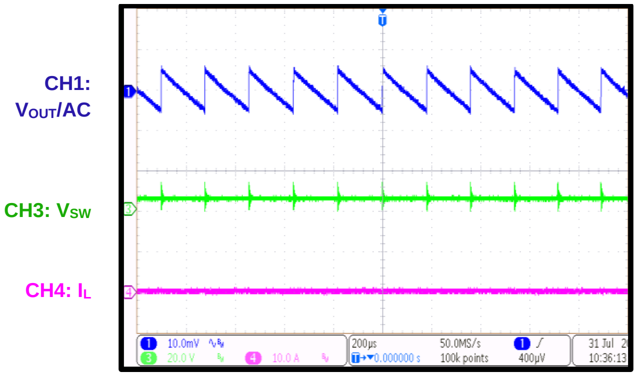
Steady State

I_{OUT} = 0A



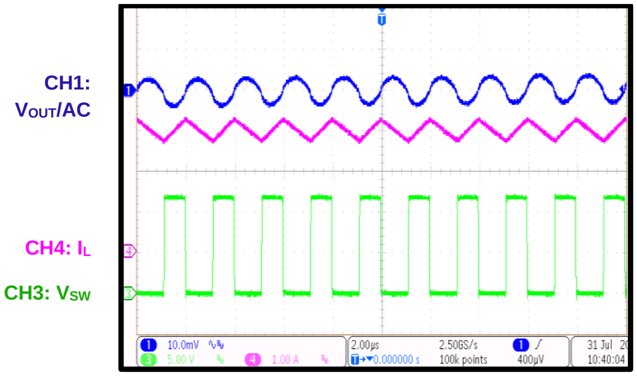
Steady State

I_{OUT} = 1mA



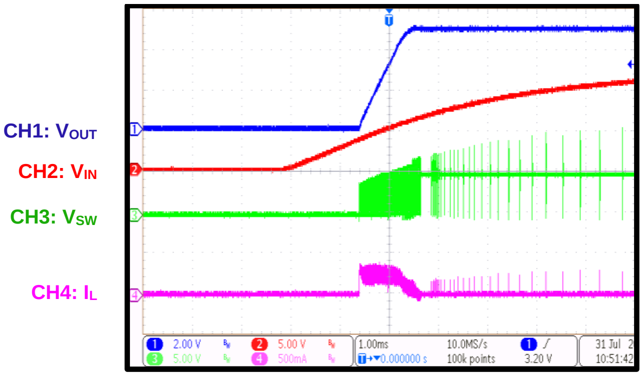
Steady State

I_{OUT} = 3A



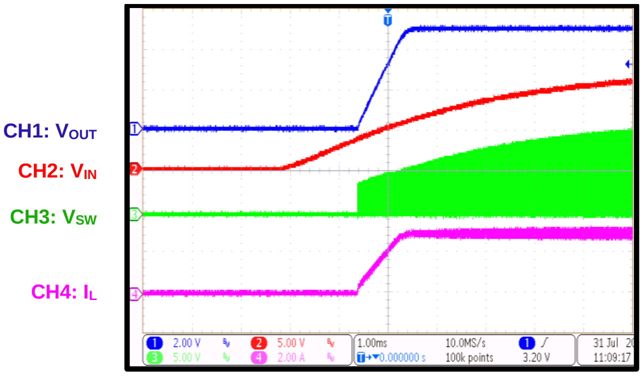
Start-Up through VIN

I_{OUT} = 0A



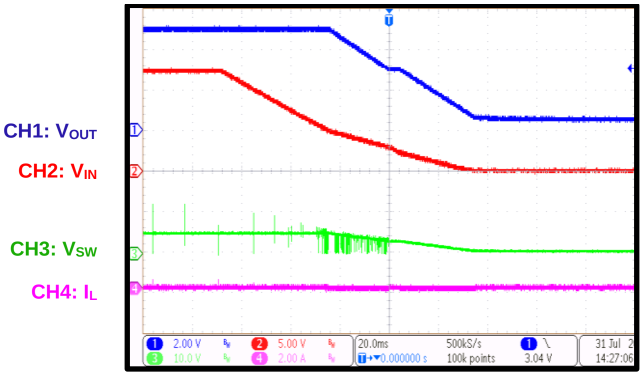
Start-Up through VIN

I_{OUT} = 3A



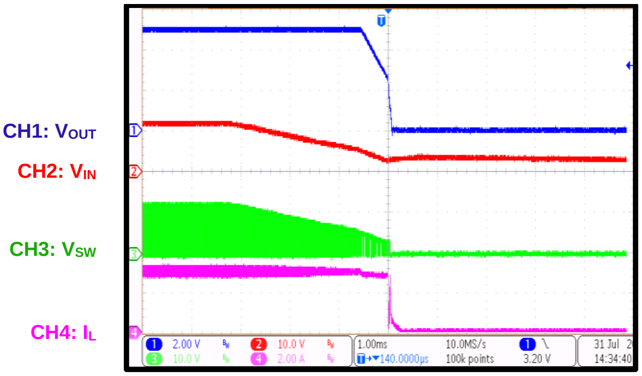
Shutdown through VIN

I_{OUT} = 0A



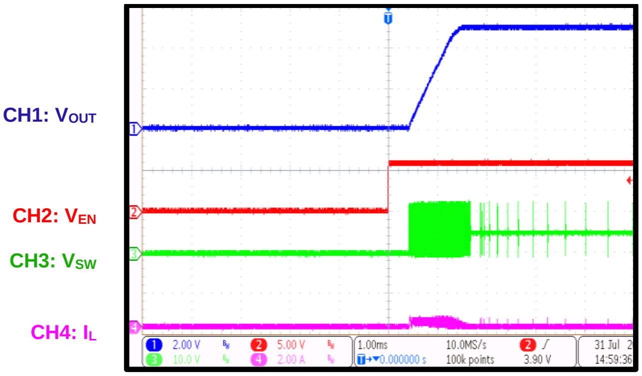
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 10µH, f_{SW} = 500kHz, AAM mode, T_A = 25°C, unless otherwise noted.



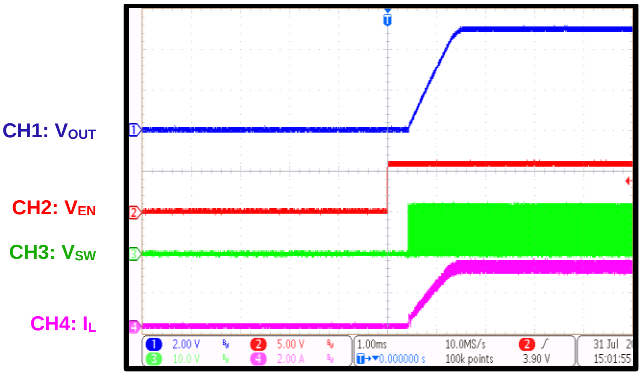
Shutdown through VIN

I_{OUT} = 3A



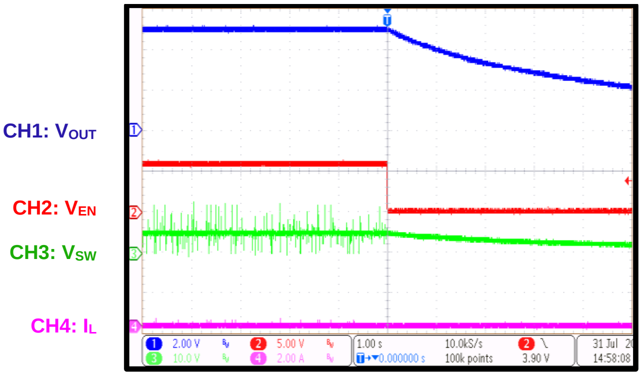
Start-Up through EN

I_{OUT} = 0A



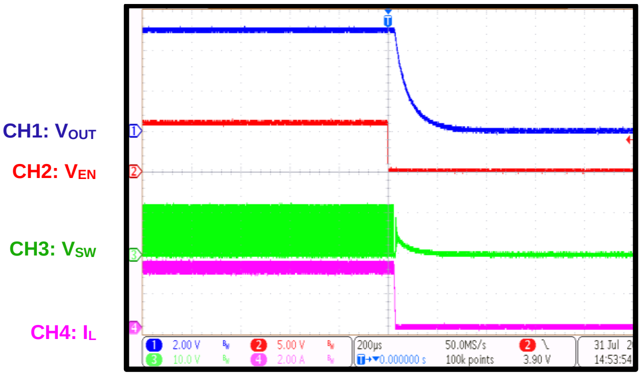
Start-Up through EN

I_{OUT} = 3A



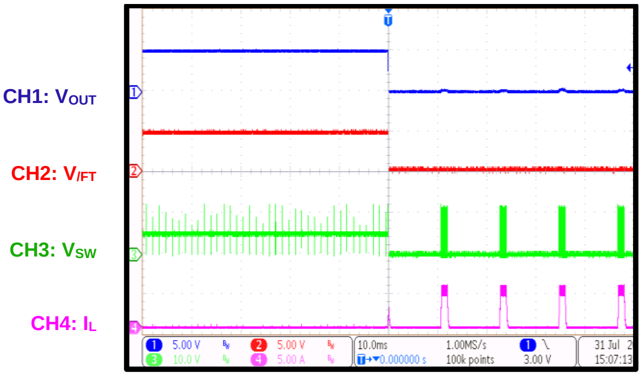
Shutdown through EN

I_{OUT} = 0A



Shutdown through EN

I_{OUT} = 3A



SCP Entry

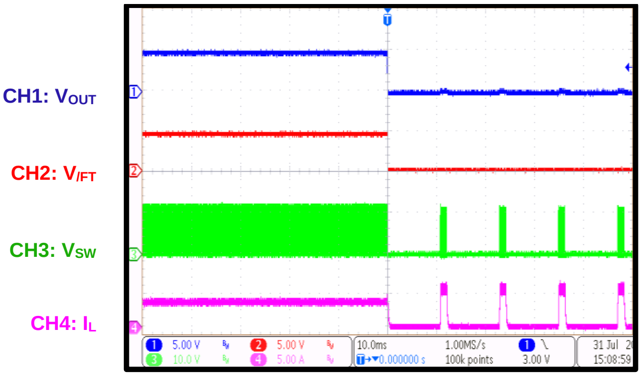
I_{OUT} = 0A

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

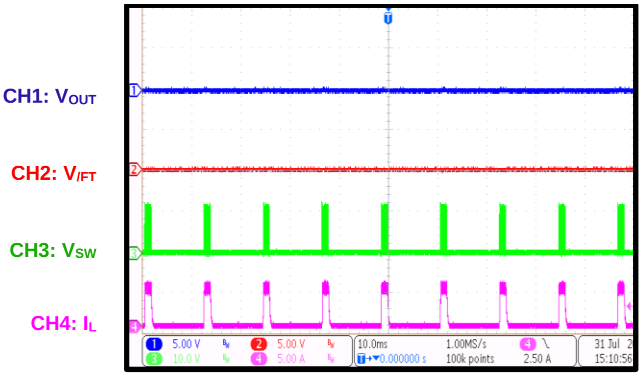
V_{IN} = 12V, V_{OUT} = 5V, L = 10µH, f_{SW} = 500kHz, AAM mode, T_A = 25°C, unless otherwise noted.

SCP Entry

I_{OUT} = 3A

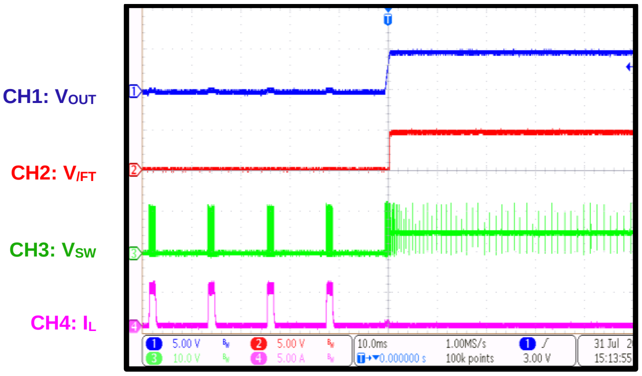


SCP Steady State



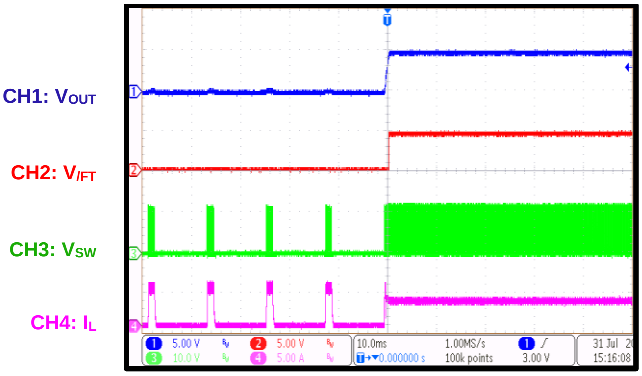
SCP Recovery

I_{OUT} = 0A



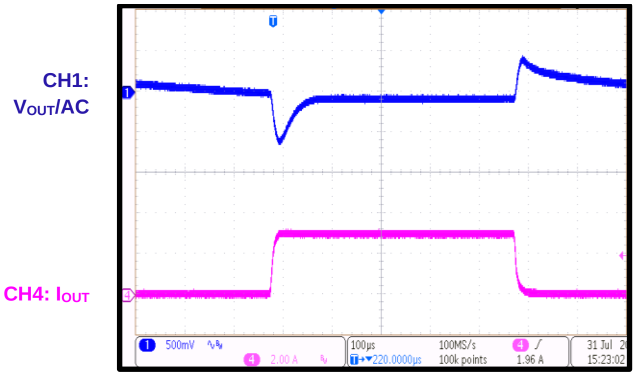
SCP Recovery

I_{OUT} = 3A



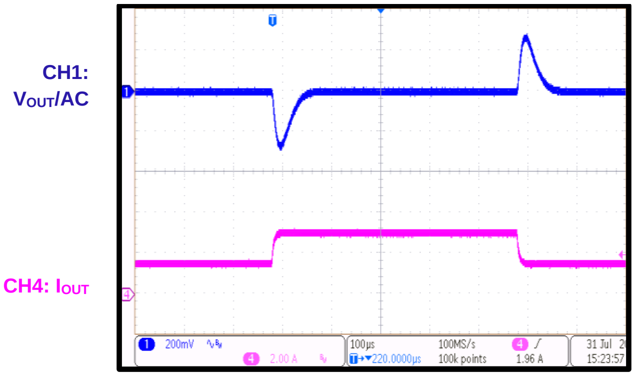
Load Transient

I_{OUT} = 0A to 3A, 0.8A/µs slew rate



Load Transient

I_{OUT} = 1.5 to 3A, 0.8A/µs slew rate

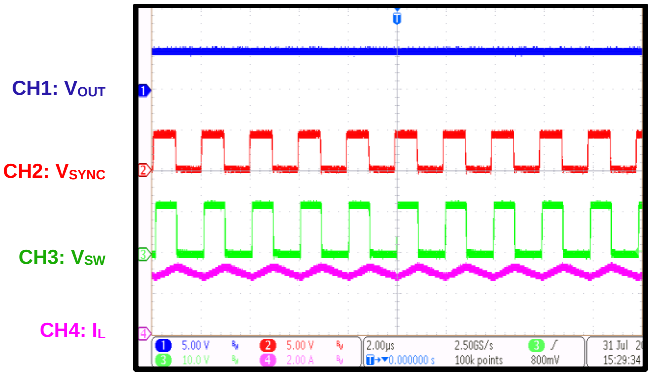


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 10µH, f_{SW} = 500kHz, AAM mode, T_A = 25°C, unless otherwise noted.

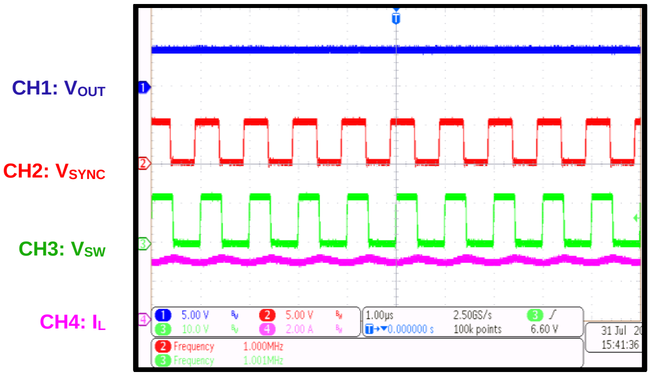
SYNC Output

I_{OUT} = 3A



SYNC Input

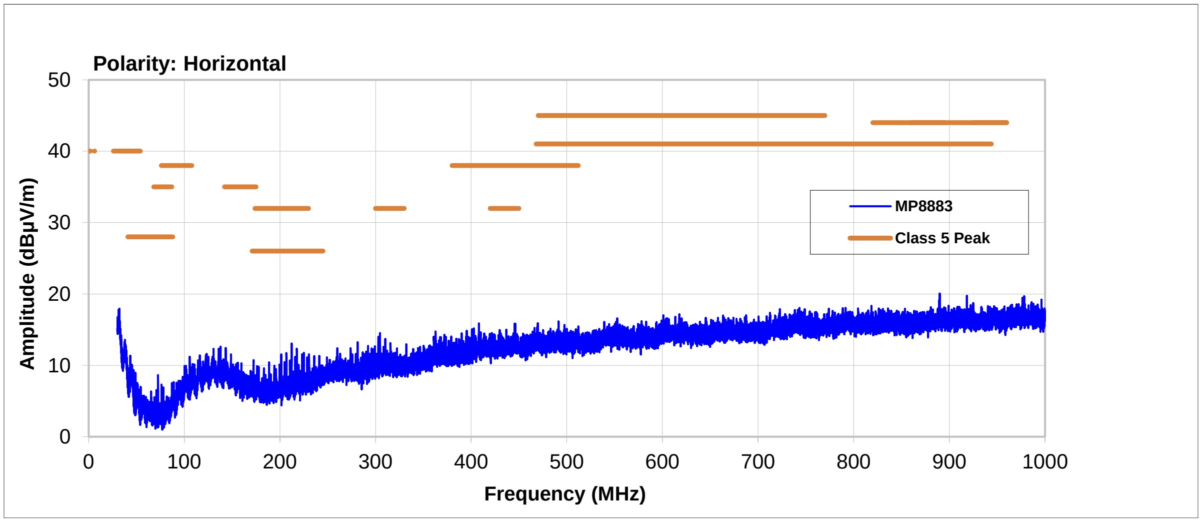
SYNC clock input = 1000kHz



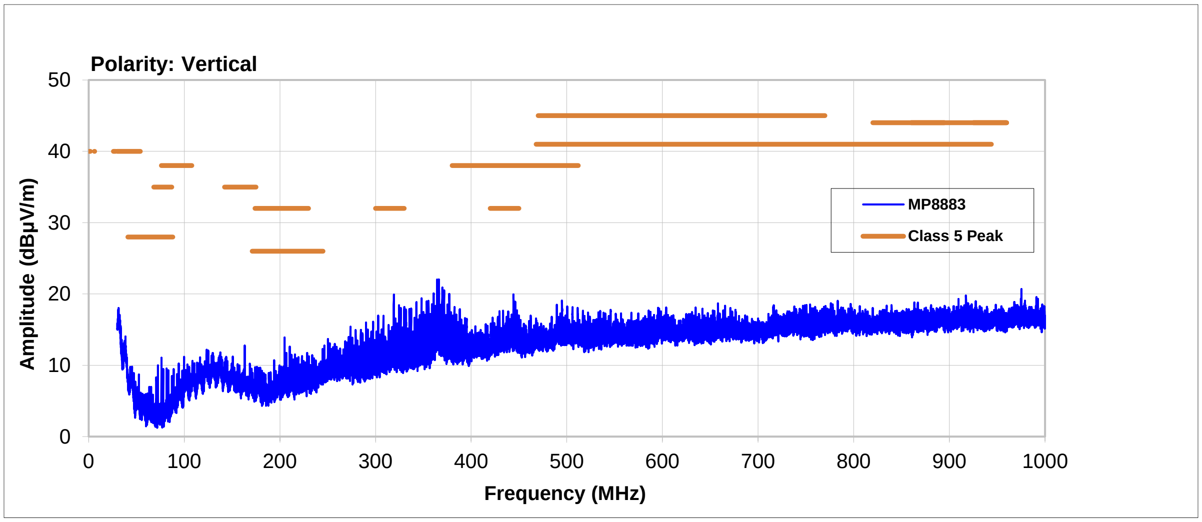
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 10µH, I_{OUT} = 2.5A, f_{SW} = 2MHz, with the EMI filters, unless otherwise noted.

CISPR25 Radiated Emission Test with Class 5 Peak Limits



CISPR25 Radiated Emission Test with Class 5 Peak Limits



FUNCTIONAL BLOCK DIAGRAM

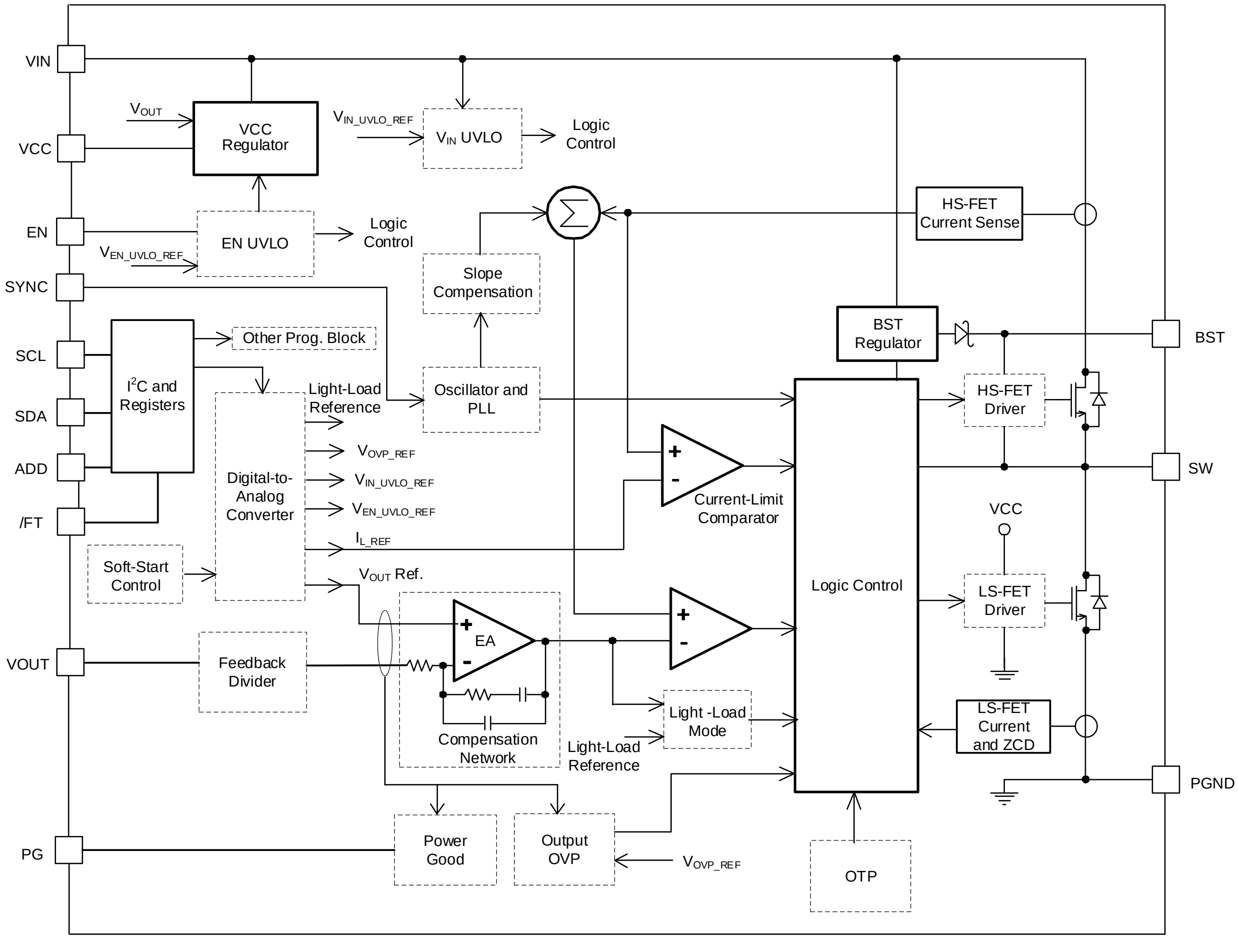


Figure 2: Functional Block Diagram

OPERATION

The MP8883 is a high-frequency, synchronous step-down converter with built-in power MOSFETs. Figure 2 on page 18 shows the device's functional block diagram. The MP8883 can achieve up to 3A of continuous output current (I_{OUT}) across a wide 3.5V to 45V input voltage (V_{IN}) range, with excellent load and line regulation.

Pulse-Width Modulation (PWM) Control

At moderate to high output currents, the MP8883 operates in fixed frequency, peak current control mode to regulate the output voltage (V_{OUT}). An internal clock initiates a PWM cycle. At the rising edge of the clock, the high-side MOSFET (HS-FET) turns on, and the inductor current (I_L) increases linearly to provide energy to the load.

The HS-FET remains on until its current (I_{HS}) reaches the comparator voltage (V_{COMP}), which is the output of the internal error amplifier (EA). The V_{COMP} is determined by the difference between the feedback (FB) voltage (V_{FB}) and the internal high-precision reference voltage (V_{REF}). This value determines how much energy should be transferred to the load. A higher load current (I_{LOAD}) corresponds to a V_{COMP}. Both the FB divider ratio (D_{FB}) and V_{REF} can be adjusted via the I^{2}C. This makes it easy to adjust V_{OUT}.

If the HS-FET is off, then the low-side MOSFET (LS-FET) turns on and remains on until the next clock starts. During this time, I_L flows through the LS-FET. To avoid shoot-through, a dead time (DT) is inserted to prevent the HS-FET and LS-FET from turning on simultaneously.

If I_{HS} does not reach the value set by the comparator within one PWM cycle, then the HS-FET remains on to save a shutdown operation.

Mode Selection

The MP8883 can operate in advanced asynchronous modulation (AAM) mode or forced continuous conduction mode (FCCM). The operation mode (AAM or FCCM) can be selected via the I^{2}C. AAM mode optimizes the efficiency under light-load or no-load conditions. FCCM maintains a constant switching frequency (f_{SW}) and smaller output voltage ripple (ΔV_{OUT}); however, it has a lower efficiency at light loads.

If AAM mode is enabled while the load decreases, the MP8883 operates in discontinuous conduction mode (DCM). In DCM, the part operates with a fixed frequency as I_L approaches 0A. If the load drops further or there is no load, then the peak I_L (I_{L_PEAK}) drops below the AAM peak current threshold set via the I^{2}C. Then the MP8883 enters sleep mode, and consumes a very low quiescent current (I_Q) to further improve light-load efficiency.

In sleep mode, the internal clock is blocked, and the MP8883 skips some pulses. V_{FB} drops below V_{REF}, and V_{COMP} ramps up until I_{L_PEAK} exceeds the AAM threshold. The internal clock is reset, and the crossover time is used as a benchmark for the next clock. This control scheme improves efficiency by scaling down the switching frequency (f_{SW}) to reduce switching and gate driver losses.

Under light-load conditions, V_{COMP} increases as I_{OUT} increases, and f_{SW} also increases. If I_{OUT} exceeds the critical level set by V_{COMP}, then the MP8883 resumes fixed-frequency PWM control (see Figure 3).

During FCCM, the MP8883 operates at a fixed f_{SW} in peak current control mode to regulate V_{OUT}, regardless of I_{OUT}.

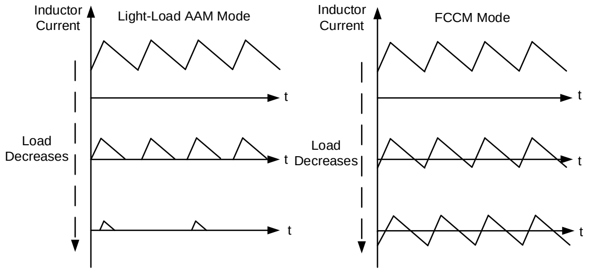


Figure 3: AAM Mode and FCCM

Internal Regulator

A 5V internal regulator powers most of the internal circuitries. This regulator takes V_{IN} and operates in the full V_{IN} range. If V_{IN} exceeds 5V, then the regulator's output is in full regulation. A lower V_{IN} results in lower a V_{OUT}.

The regulator is enabled once V_{IN} exceeds its under-voltage lockout (UVLO) threshold and EN is pulled high. During a shutdown through EN, the internal VCC regulator is disabled to reduce power dissipation.

To improve thermal performance, the V_{OUT} bias function can be enabled via the I^2C. If V_{OUT} exceeds 5V, then VCC and the internal circuit are powered by V_{OUT}. The bias function only works in AAM mode. It does not work in CCM, even if the V_{OUT} bias is enabled. Do not enable the bias function while using the external FB divider. To improve output regulation, do not enable the bias function if V_{OUT} exceeds 9V.

Enable (EN) Control

The enable (EN) pin is a digital control pin that turns the converter (including the I^2C block) on and off. Pull EN high to turn the converter on; pull EN low to turn it off. The EN voltage (V_{EN}) threshold can be configured via the I^2C. Do not float EN. V_{EN} should exceed 2V if the I^2C is used. If EN is pulled low, then the I^2C interface is blocked to reduce current consumption, and the RAM registers are reset to their default values.

Switching Frequency (f_{SW})

f_{SW} can be set between 250kHz and 2.5MHz via the I^2C. The default f_{SW} is 500kHz.

Synchronous Input and Output (SYNC Pin)

The SYNC pin can be configured via the I^2C to work as a synchronous input or output. While operating as a synchronous output, the SYNC pin outputs a SYNC signal in phase with the internal switching clock. While operating as a synchronous input, the internal f_{SW} can be synchronized via an external clock, and the phase shift can be set to 0° or 180° (according to the register 0x02 phase-shift bit).

At start-up, the MP8883 operates at an internal set f_{SW}. Then it synchronizes to the external clock once soft start (SS) is ready. The high amplitude of the SYNC clock should exceed 2V, and the low amplitude should be below 0.4V to drive the internal logic. Set the external SYNC frequency (f_{SYNC}) between 250kHz and 2.5MHz.

Under-Voltage Lockout (UVLO) Protection

The MP8883 provides V_{IN} under-voltage lockout (UVLO) protection to ensure there is reliable output power. If EN is active, then the MP8883 turns on once V_{IN} exceeds the UVLO rising threshold. It shuts down once V_{IN} drops below the UVLO falling threshold. The UVLO rising threshold can be set between 3.2V and 7.4V via the I^2C. This function prevents the device from operating at an insufficient voltage. UVLO is a non-latch protection.

Soft Start (SS)

The MP8883 has built-in soft start (SS), which ramps up V_{OUT} at a controlled slew rate to avoid overshoot during start-up. Once the chip starts up, the internal circuitry generates a soft-start voltage (V_{SS}) that ramps up slowly. If V_{SS} drops below the internal V_{REF}, then V_{SS} overrides V_{REF} as the EA's reference. If V_{SS} exceeds V_{REF}, then V_{REF} acts as the reference. Once SS is complete, the MP8883 enters steady state operation.

The soft-start time (t_{SS}) is set to 1ms internally by default. t_{SS} can also be set to 0.5ms, 2ms, or 4ms via the I^2C. If V_{OUT} is shorted to PGND, then V_{FB} is pulled low, and V_{SS} is discharged. The MP8883 initiates another SS once it returns to a normal state.

Pre-Biased Start-Up

If V_{FB} exceeds V_{SS} during start-up, then the output has a pre-biased voltage. Neither the HS-FET or LS-FET turn on until V_{SS} exceeds V_{FB}.

Power Good (PG) Indication

The MP8883 has power good (PG) indication. The PG pin is an open-drain output that should be pulled up to a voltage source via a resistor (e.g. 100kΩ). In the presence of V_{IN}, PG is pulled to AGND before SS is ready. If V_{OUT} is within the default rated voltage window (±10%), then the PG pin is pulled high after a delay (typically 30µs). If V_{OUT} is outside the default ±10% range with a hysteresis, then PG is pulled low to indicate a failure output status. Both the PG threshold and hysteresis can be configured via the I^2C.

Fault Indication

The /FT pin is open-drain output that should be pulled up to a voltage source via a resistor (e.g. 100kΩ). The /FT pin is pulled high during normal operation. If a fault or warning occurs (e.g. V_{IN} OVP, output OVP, SCP, and thermal shutdown), then the /FT pin is pulled low to indicate a fault status.

Over-Current Protection (OCP)

The MP8883 has a cycle-by-cycle over-current limit. I_L is monitored while the HS-FET is on.

Once I_{L_PEAK} exceeds the peak current limit (I_{LIMIT_PEAK}), the HS-FET turns off, and the LS-FET turns on to discharge the energy and I_L decreases. The HS-FET does not turn on again until I_L drops below the valley current limit (I_{LIMIT_VALLEY}). This prevents I_L runaway and damage to the components. Both I_{LIMIT_PEAK} and I_{LIMIT_VALLEY} can be configured via the I^{2}C.

If I_{LIMIT_PEAK} is triggered, then the over-current protection (OCP) timer starts. If the current exceeds I_{LIMIT_PEAK} during the OCP timer, then short-circuit protection (SCP) is triggered, and the part enters hiccup mode by default.

Short-Circuit Protection (SCP)

If a short circuit occurs, the MP8883 reaches the I_{LIMIT_PEAK} immediately, and V_{OUT} drops to the UVLO threshold. The UV threshold is set to 50% of V_{OUT} by default. The device considers this an output dead short, and SCP is triggered. There are three response modes for SCP that can be selected via the I^{2}C: hiccup mode, switching with non-hiccup mode, and latch-off mode.

In hiccup mode, the MP8883 disables its output power stage and resets V_{SS}. Then a new SS is initiated. The hiccup off time (t_{OFF}) is determined by t_{SS} and the hiccup on time (t_{ON}). Both t_{SS} and the hiccup t_{ON} can be set via the I^{2}C. If the short-circuit condition remains after SS is complete, then the device repeats this operation until the short circuit is removed and the output returns to its regulation level. SCP with hiccup mode greatly reduces the average short-circuit current and protects the regulator by periodically restarting the part to alleviate thermal issues.

In switching with non-hiccup mode, the MP8883 continues switching while I_L is limited by I_{LIMIT_PEAK} and I_{LIMIT_VALLEY}. In latch-off mode, the MP8883 shuts down once SCP is triggered. Cycle the power on VIN or EN to restart the part.

Output Over-Voltage Protection (V_{OUT} OVP)

The MP8883 monitors V_{OUT} via the VOUT pin. If V_{OUT} exceeds the over-voltage protection (OVP) threshold (120% of the set voltage), then OVP is triggered. There are three response modes for OVP that can be selected via the I^{2}C: discharge mode (default), stop switching mode, and latch-off mode.

Once an OC fault is detected in discharge mode, the LS-FET turns on to discharge V_{OUT}. The LS-FET remains on until its current (I_{LS}) reaches the negative I_{LIMIT}. In stop switching mode, the MP8883 stops switching, and recovers once the OV fault is removed. In latch-off mode, the MP8883 shuts down. Cycle the power on VIN or EN to restart the part.

Input Over-Voltage Protection (V_{IN} OVP)

The MP8883 also has optional V_{IN} OVP. The V_{IN} OVP threshold can be set to 28V, 34V, or 40V. If V_{IN} exceeds the threshold, then the MP8883 stops switching (non-latch protection). The device resumes normal operation once the input OV fault is removed. Both the V_{IN} OVP threshold and hysteresis can be configured via the I^{2}C.

Thermal Shutdown

The MP8883 provides over-temperature protection by monitoring the IC temperature internally. This function prevents the chip from operating at exceedingly high temperatures. If the junction temperature (T_J) exceeds this thermal shutdown, the part shuts down. Thermal shutdown is a non-latch protection. Once the T_J to drops below the threshold, the device initiates a SS to resume normal operation. There is a hysteresis of about 25°C. Both the thermal shutdown threshold and hysteresis can be configured via the I^{2}C interface.

Floating Driver and Bootstrap (BST) Charging

An external bootstrap capacitor supplies the floating power MOSFET driver. The floating driver has its own UVLO protection, with a rising threshold of 2.4V and a hysteresis of 200mV. The bootstrap capacitor voltage is charged to about 5V from VCC through a P-channel MOSFET pass transistor when the LS-FET is on.

When the voltage from BST to SW drops below the UVLO threshold, the HS-FET turns off and the LS-FET turns on with a minimum t_{OFF} (t_{OFF_MIN}) to conduct and refresh the charge on the BST capacitor. At higher duty cycles, the internal charging circuit may not have sufficient voltage or time to charge the bootstrap capacitor. External circuitry can be added to ensure that the bootstrap voltage stays in the normal operation region.

Low-Dropout Mode

To improve dropout, the MP8883 is designed to operate at close to 100% duty cycle (so long as the BST to SW voltage exceeds its UVLO threshold).

If V_{IN} drops, the HS-FET remains on and close to 100% duty cycle to maintain output regulation. The HS-FET remains on until the BST-to-SW voltage falls below the UVLO threshold. Since the supply current sourced from the BST capacitor is low, the BST charge refreshes infrequently, and the HS-FET can remain on for more switching cycles. This keeps the switching regulator's effective duty cycle high.

The effective duty cycle during regulator dropout is mainly influenced by the voltage drops across the power MOSFET, inductor resistance, low-side diode, and PCB resistance

I^{2}C Control and the Default Output Voltage

When the MP8883 is enabled (EN is high and V_{IN} exceeds its UVLO threshold), the chip starts up to a default V_{OUT}. Then the I^{2}C bus can communicate with the master, and the internal configuration can be set via a valid I^{2}C command.

V_{OUT} can be set by adjusting the internal V_{REF} and D_{FB}. Before adjusting V_{OUT} or changing any other register value, the master controller should send the operation off command to disable the output by writing "0x00" to register D0h. Then commands can be sent to update the parameters.

The MP8883 starts up once it receives an operation on command. The internal RAM parameters (e.g. V_{OUT}) cannot be adjusted on-the-fly. See Figure 7 on page 24 for more details.

It is recommended to only use MPS's communication interface and GUI to access the part. Contact an MPS FAE for more application information if the device does not need to be accessed via a local microcontroller (MCU).

Frequency Dithering for Low EMI

Frequency dithering is used to reduce EMI, especially for EMI-sensitive applications. This spread spectrum modulation technique spreads the converter's frequency spectrum, which spreads the energy of the switching harmonics across a wider band while reducing their amplitudes. This helps devices meet stringent EMI standards. Both the frequency dithering range and cycle can be set via the I^{2}C interface.

Multi-Page One-Time Programmable (OTP) Memory

The MP8883 features 3 pages of one-time programmable (OTP) memory to permanently store system settings.

Instead of a single-end cell, a differential OTP cell is used for long-term reliability. Data is stored on two floating gate avalanche injection metal oxide semiconductors (FAMOSs), and output comparators are used for differential reading.

The first page of the OTP is configured with manufactured default values. The two remaining pages can be configured using MPS's GUI. Once the device is enabled, the default values on the first page set the register's control parameters. If there is data on the other pages, the newest setting is loaded into the I^{2}C registers automatically. The MPS GUI can check if the part is completely configured, or if there are blank pages.

For more information about the I^{2}C register configuration, see the I^{2}C Interface section on page 23.

When configuring the MP8883's pages, the V_{OUT} biased function must be disabled first.

I^{2}C INTERFACE

I^{2}C Serial Interface Description

The I^{2}C is a two-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. Connecting to the line, a master device generates the SCL signal and device address, then arranges the communication sequence. The MP8883 interface is an I^{2}C slave that supports fast mode (400kHz), which adds flexibility to the power supply solution. The MP8883's SDA and SCL can be pulled up to voltage levels between 1.8V and 5V for different systems. The output voltage and transition slew rate can be instantaneously controlled by the I^{2}C interface.

Data Validity

One clock pulse is generated for each data bit that is transferred. The data on SDA must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on SCL is low (see Figure 4).

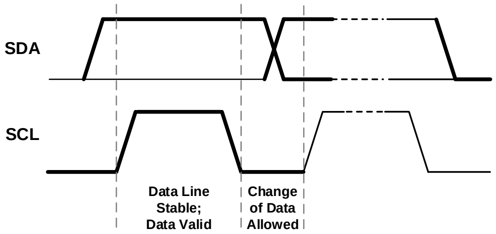


Figure 4: Bit Transfer on the I^{2}C Bus

Start and Stop Commands

Start and stop commands are signaled by the master device, which signifies the beginning and the end of the I^{2}C transfer. A start (S) command is defined as the SDA signal transitioning from high to low while SCL is high. A stop (P) command is defined as the SDA signal transitioning from low to high while SCL is high (see Figure 5).

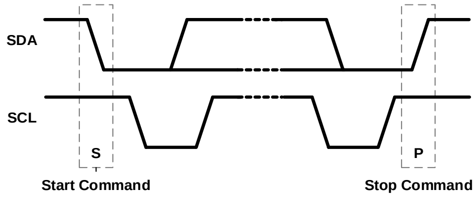


Figure 5: Start and Stop Commands

Start and stop commands are always generated by the master. The bus is considered busy after the start command. The bus is considered free a minimum of 4.7μs after the stop command. The bus stays busy if a repeated start (Sr) command is generated instead of a stop command. The start and repeated start commands are functionally identical.

Transfer Data

Every byte on the SDA line must be 8 bits long. Each byte must be followed by an acknowledge (ACK) bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases SDA (high) during the acknowledge clock pulse. The receiver must pull down SDA during the acknowledge clock pulse, so that it remains stable and low during the high period of the clock pulse.

Figure 10 shows the data transfer. After the start condition, a slave address is sent. This address is 7 bits long, followed by an eighth data direction bit (R/W). A 0 indicates a transmission (write), while a 1 indicates a request for data (read). A data transfer is always terminated by a stop command, which is generated by the master. If a master must continue communicating on the bus, the device can generate a repeated start command and address another slave without first generating a stop command (see Figure 6).

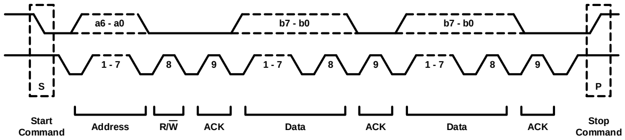


Figure 6: A Complete Data Transfer

I^{2}C Update Sequence

The MP8883 requires a start command, a valid I^{2}C address, a register address byte, and a data byte for a single data update. After receiving each byte, the MP8883 acknowledges by pulling SDA low during the high period of a single clock pulse. A valid I^{2}C address selects the MP8883. The MP8883 performs an update on the falling edge of the LSB.

I^{2}C Chip Address

The ADD pin can configure the I^{2}C address. The MP8883 supports 8 addresses, for up to 8 voltage rails. These addresses can be configured via the resistor connected to the ADD pin and ground. When the master sends the address as an 8-bit value, the 7-bit address should be followed by 0/1 to indicate a write/read operation.

Table 2 shows the resistor values for different I^{2}C addresses.

Table 2: 7-Bit I^{2}C Address

Resistor (kΩ) 1%	Address
0 to 20	21h
23 to 45	22h
49 to 71.5	23h
73.5 to 97.3	24h
100 to 124	25h
127 to 147	26h
150 to 174	27h
>178	28h

I^{2}C Interface Diagram Block

The MPS GUI can send I^{2}C commands to the MP8883 to generate the OTP interface timing, which controls the OTP to process RAM/ROM operation.

Note that the registers described on page 26 and page 27 are not directly addressed through the I^{2}C. The MP8883 uses an internal command module to access user registers. These commands are supported by MPS's GUI and are not fully described in this document.

Contact MPS or visit the MPS website to obtain the GUI program. In addition, the user can access the RAM and ROM with a customized controller. Contact MPS for more application information if the local MCU is used to write, read, or configure the device. Figure 7 shows the I^{2}C interface diagram block.

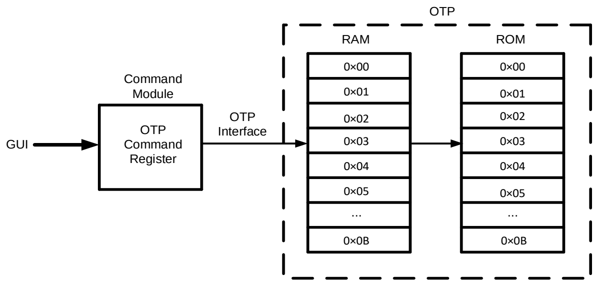


Figure 7: I^{2}C Interface Diagram Block

Figure 8 and Figure 9 on page 25 show the write and read processes for the RAM registers.

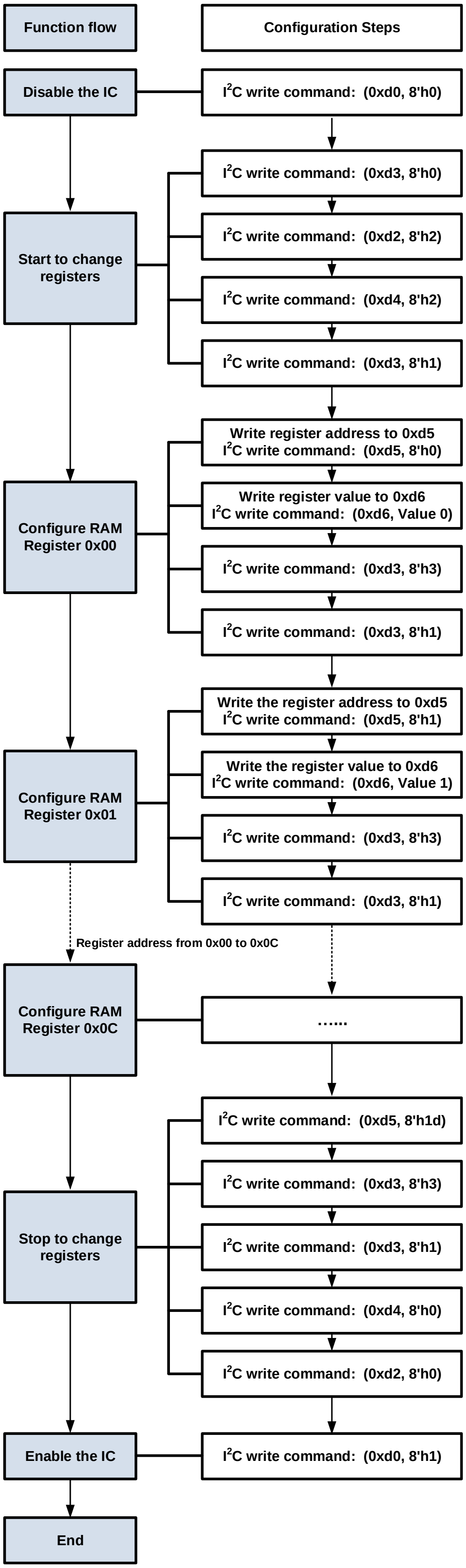


Figure 8: RAM Registers Write Operating Process

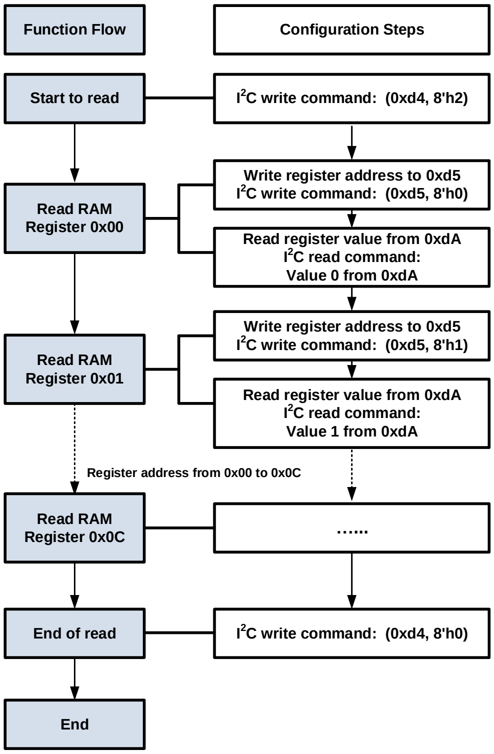


Figure 9: RAM Registers Read Operating Process

REGISTER MAP

Add	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0x00	R/W	Reference Voltage (DAC)							
0x01	R/W	Frequency Dithering (Enable/ Disable)	Frequency Dithering (Dithering Cycle)	Frequency Dithering (Dithering Range)	Input OVP Hysteresis	Input OVP Threshold		FB Divider Ratio	
0x02	R/W	N/A	Phase Shift	Switching Frequency (f_{SW})					
0x03	R/W	Compensation (C_{COMP2})		Compensation (R_T)			Compensation (R_{COMP})		
0x04	R/W	Soft-Start Time		Slope Compensation			Compensation (C_{COMP1})		
0x05	R/W	N/A	EN Rising Threshold		EN Rising Hysteresis	V_{IN} UVLO Rising Threshold			V_{IN} UVLO Hysteresis
0x06	R/W	SCP Mode		Peak Current Limit Threshold			Valley Current Limit Threshold		N/A
0x07	R/W	OTP Rising Threshold		OTP Hysteresis	Output OVP Mode		Output OVP Rising Threshold		Output OVP Hysteresis
0x08	R/W	PG Lower Hysteresis	PG Lower Rising Threshold	PG Upper Hysteresis	PG Upper Rising Threshold	SCP Detecting Time		SCP Triggered FB Voltage	N/A
0x09	R/W	/FT Setting	SYNC In/Out	Hiccup Duty	Switching Slew Rate (Falling)		Switching Slew Rate (Rising)		N/A
0x0A	R/W	N/A							AAM/CCM
0x0B	R/W	AAM Threshold				PKC	V_{OUT} Bias		N/A

REGISTER DESCRIPTION

Description	Address	Bits	Default Code	Default Value	Values	Min Value	Max Value	Resolution / LSB	Units
Reference voltage (DAC)	0x00	D[7:0]	01100100	1	0.6V to 2.55V	0.60	2.55	0.01	V
FB divider ratio (D_{FB})	0x01	D[1:0]	01	1/5	1/2, 1/5, 1/5, 1	1/5	1	N/A	N/A
Input OVP threshold	0x01	D[3:2]	00	No OVP	No OVP, 28V, 34V, 40V	28	40	N/A	V
Input OVP hysteresis	0x01	D[4]	1	3.5%	5.5%, 3.5%	3.5%	5.5%	N/A	V_{IN}
Frequency dithering range	0x01	D[5]	1	3/48	3/28, 3/48	3/48	3/28	N/A	f_{SW}
Frequency dithering cycle	0x01	D[6]	1	150	120, 150	120	150	N/A	µs
Frequency dithering	0x01	D[7]	0	Disabled	Disabled, enabled	N/A	N/A	N/A	N/A
Switching frequency (f_{SW})	0x02	D[5:0]	001010	500	250 to 2500	250	2500	50	kHz
Phase shift	0x02	D[6]	0	0	0, 180 degree	0	180	N/A	°
Reserved	0x02	D[7]	0	N/A	N/A	N/A	N/A	N/A	N/A
Compensation (R_{COMP})	0x03	D[2:0]	011	700	400, 500, 600, 700, 800, 900, 1000, 1100	400	1100	N/A	kΩ
Compensation (R_T)	0x03	D[5:3]	011	60	0, 20, 40, 60, 80, 100, 120, 140	0	140	N/A	kΩ
Compensation (C_{COMP2})	0x03	D[7:6]	00	0.5	0.5	N/A	N/A	N/A	pF
Compensation (C_{COMP1})	0x04	D[2:0]	000	40	40, 45	40	45	N/A	pF
Slope compensation	0x04	D[5:3]	000	750	750, 600, 450, 300, 750, 900, 1050, 1200	300	1200	N/A	mV
Soft-start time (t_{SS})	0x04	D[7:6]	01	1	0.5, 1, 2, 4	0.5	4	N/A	ms
V_{IN} UVLO hysteresis	0x05	D[0]	1	4%	2%, 4%	2%	4%	N/A	V_{UVLO_TH}
V_{IN} UVLO rising threshold	0x05	D[3:1]	000	3.2	3.2, 3.8, 4.4, 5.0, 5.6, 6.2, 6.8, 7.4	3.2	7.4	N/A	V
EN UVLO rising hysteresis	0x05	D[4]	0	220	220, 420	220	420	N/A	mV

REGISTER DESCRIPTION *(continued)*

Description	Address	Bits	Default Code	Default Value	Range/Values	Min Value	Max Value	Resolution/ LSB	Units
EN Rising Threshold	0x05	D[6:5]	01	1.4	1.2, 1.4, 1.6, 2	1.2	2	N/A	V
RESERVED	0x05	D[7]	0	N/A	N/A	N/A	N/A	N/A	N/A
RESERVED	0x06	D[0]	0	N/A	N/A	N/A	N/A	N/A	N/A
Valley Current Limit Threshold	0x06	D[2:1]	10	4	2, 3, 4	2	4	N/A	A
Peak Current Limit Threshold	0x06	D[5:3]	000	5	5, 6, 7, 8, 4, 3, 2	2	8	N/A	A
SCP Mode	0x06	D[7:6]	00	Hiccup	Hiccup mode, latch-off mode, switching with non-hiccup mode	N/A	N/A	N/A	N/A
Output OVP Hysteresis	0x07	D[0]	0	5.7%	5.7%, 3.2%	3.2%	5.7%	N/A	V_{OUT_SET}
Output OVP Rising Threshold	0x07	D[2:1]	01	120%	110%, 120%, 130%	110%	130%	N/A	V_{OUT_SET}
Output OVP Mode	0x07	D[4:3]	01	Stop switching mode	Discharge mode, stop switching mode, latch-off mode	N/A	N/A	N/A	N/A
OTP Hysteresis	0x07	D[5]	0	25	25, 50	25	50	N/A	°C
OTP Rising Threshold	0x07	D[7:6]	10	175	125, 150, 175	125	175	N/A	°C
Reserved	0x08	D[0]	0	N/A	N/A	N/A	N/A	N/A	N/A
SCP Triggered FB Voltage	0x08	D[1]	0	50%	50%, 75%	50%	75%	N/A	V_{REF}
SCP Detecting Time	0x08	D[3:2]	01	128	256, 128, 64, 32	32	256	N/A	t_{SW}
PG Upper Rising Threshold	0x08	D[4]	0	110%	110%, 115%	110%	115%	N/A	V_{OUT_SET}
PG Upper Hysteresis	0x08	D[5]	0	5.5%	5.5%, 3%	3%	5.5%	N/A	V_{OUT_SET}
PG Lower Rising Threshold	0x08	D[6]	0	89%	89%, 84%	84%	89%	N/A	V_{OUT_SET}
PG Lower Hysteresis	0x08	D[7]	0	5.5%	5.5%, 3%	3%	5.5%	N/A	V_{OUT_SET}
RESERVED	0x09	D[0]	0	N/A	N/A	N/A	N/A	N/A	N/A
Switching Slew Rate (Rising) (11)	0x09	D[2:1]	00	1	1, 2, 3, 4	1	4	N/A	V/ns
Switching Slew Rate (Falling) (11)	0x09	D[4:3]	00	1	1, 2, 3, 4	1	4	N/A	V/ns
Hiccup Duty (On Time)	0x09	D[5]	0	10%	10%, 20%	10%	20%	N/A	N/A
SYNC In/Out	0x09	D[6]	1	SYNC In	SYNC out, SYNC in	N/A	N/A	N/A	N/A
/FT Setting	0x09	D[7]	1	Auto-reset	Need EN restart to reset the fault status, auto-reset when the fault is removed	N/A	N/A	N/A	N/A
AAM/CCM control	0x0A	D[0]	0	AAM	AAM, CCM	N/A	N/A	N/A	N/A
RESERVED	0x0A	D[7:1]	0101000	N/A	N/A	N/A	N/A	N/A	N/A
RESERVED	0x0B	D[0]	0	N/A	N/A	N/A	N/A	N/A	N/A
V_{OUT} Bias	0x0B	D[2:1]	00	Bias	No bias, bias, bias in sleep mode only	N/A	N/A	N/A	N/A
PKC	0x0B	D[3]	1	PKC	PKC	N/A	N/A	N/A	N/A
AAM Threshold (PKC)	0x0B	D[7:4]	1000	530	Disabled, 605, 680, 755, 830, 905, 980,1055, 530, 455, 380, 305, 225, 150, 75, 0	0	1055	N/A	mA

Note:

11) To limit the SW spike, do not use a switching slew rate faster than 2V/ns when the input exceeds 30V.

DEFAULT OTP CONFIGURATIONS

Table 3: MP8883GQ-0001 Suffix Code Configuration

OTP Items	Values
Reference voltage (DAC)	1V
FB divider ratio	1/5
Output voltage	5V
Mode	AAM
SCP mode	Hiccup mode
Soft-start time	1ms
Switching slew rate (rising)	1V/ns
Switching slew rate (falling)	1V/ns
Valley current limit	4A
Peak current limit	5A
Switching frequency	500kHz
OTP rising threshold	175°C
OTP configuration code	0x0001

Table 4: MP8883GQ-0001 Suffix Code Register Value

Suffix Code	Register	Hex Value
0001	0x00	64h
0001	0x01	71h
0001	0x02	0Ah
0001	0x03	1Bh
0001	0x04	40h
0001	0x05	21h
0001	0x06	04h
0001	0X07	8Ah
0001	0x08	04h
0001	0x09	C0h
0001	0x0A	50h
0001	0x0B	88h
0001	0x0C	FFh

DEFAULT OTP CONFIGURATIONS *(continued)*

Table 5: MP8883GQ-0002 Suffix Code Configuration

OTP Items	Values
Reference voltage (DAC)	0.8V
FB divider ratio	Using external divider
Mode	AAM
SCP mode	Hiccup mode
Soft-start time	1ms
Switching slew rate (rising)	1V/ns
Switching slew rate (falling)	1V/ns
Valley current limit	4A
Peak current limit	5A
Switching frequency	500kHz
OTP rising threshold	175°C
OTP configuration code	0x0002

Table 6: MP8883GQ-0002 Suffix Code Register Value

Suffix Code	Register	Hex Value
0002	0x00	50h
0002	0x01	73h
0002	0x02	0Ah
0002	0x03	1Bh
0002	0x04	40h
0002	0x05	21h
0002	0x06	04h
0002	0X07	8Ah
0002	0x08	04h
0002	0x09	C0h
0002	0x0A	50h
0002	0x0B	88h
0002	0x0C	FFh

APPLICATION INFORMATION

Setting the Output Voltage

The MP8883's V_{OUT} can be set with two methods: internal divider mode and external divider mode.

Internal divider mode adjusts the internal V_{REF} and D_{FB} via the I²C. Register 0x00, bits[7:0] adjust the internal V_{REF} between 0.6V and 2.55V with a 10mV/LSB. Register 0x01, bits[1:0] D_{FB} to 1/5, 1/2, or 1. V_{OUT} depends on the internal V_{REF} and D_{FB}. V_{OUT} can be calculated with Equation (1):

$$V_{OUT} = \frac{V_{REF}}{D_{FB}} \tag{1}$$

For example, if V_{REF} is 1V, and D_{FB} is 1/5, then V_{OUT} is 5V.

For external divider mode, the FB divider ratio should be set to 1, and V_{REF} can be set between 0.6V and 2.55V. Adjust the values of the external divider resistors connected to VOUT to adjust V_{OUT} (see Figure 10).

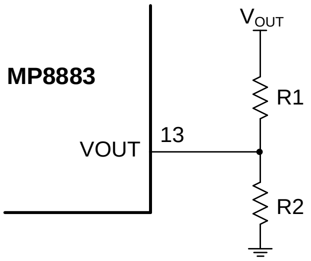


Figure 10: External Divider Mode

In external divider mode, V_{OUT} can be estimated with Equation (2):

$$V_{OUT} = \frac{R1 + R2}{R2} \times V_{FB} \tag{2}$$

It is recommended that the external divider resistor values range between 10kΩ and 100kΩ.

Selecting the Input Capacitor (C_{IN})

The step-down converter has a discontinuous input current (I_{IN}), and requires a capacitor to supply AC current to the converter while maintaining the DC V_{IN}. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their low ESR and small temperature coefficients.

For most applications, choose a 4.7µF to 10µF input capacitor (C_{IN}). In addition, it is strongly recommended to use a second, smaller-value capacitor (e.g. 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place C_{IN} as close to the VIN and PGND pins as possible.

Since C_{IN} absorbs the input switching current, it requires an adequate ripple current rating. The input capacitor's RMS current (I_{CIN}) can be calculated with Equation (3):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \tag{3}$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be estimated with Equation (4):

$$I_{CIN} = \frac{I_{LOAD}}{2} \tag{4}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum I_{LOAD} (I_{LOAD_MAX}).

C_{IN} can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC as possible.

When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple (ΔV_{IN}) caused by the capacitance can be calculated with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{5}$$

Selecting the Output Capacitor (C_{OUT})

The output capacitor (C_{OUT}) maintains the DC V_{OUT}. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to reduce the output voltage ripple (ΔV_{OUT}). ΔV_{OUT} can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \tag{6}$$

Where L is the inductance, and R_{ESR} is the ESR value of C_{OUT}.

For ceramic capacitors, the capacitance dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (8)$$

The characteristics of C_{OUT} also affect the stability of the regulation system. The MP8883 can be optimized for a wide range of capacitances and ESR values.

Selecting the Inductor

It is recommended that the inductor have a DC current rating of at least ≥25% I_{LOAD_MAX}. To improve efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage; however, a larger-value inductor also has a larger physical size, higher series resistance, and lower saturation current. A good rule to determine the inductance is to allow the inductor ripple current to be approximately 30% to 50% of I_{LOAD_MAX}.

The inductance (L) can be calculated with Equation (9):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose the inductor ripple current to be approximately 30% of I_{LOAD_MAX}. The maximum peak I_L (I_{L_PEAK}) can be calculated with Equation (10):

$$I_{L\_PEAK} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

In CCM, the inductance should be large enough to avoid dropping below the negative current limit during normal operation. The inductance's worst-case condition can be calculated with Equation (11):

$$L \geq \frac{V_{OUT}}{2 \times f_{SW}} \quad (11)$$

Table 7 shows the recommend inductances for different applications.

Table 7: Inductor Values for Different Applications (V_{IN} = 24V to 45V)

V_{OUT}	f_{SW}	L
5V	500kHz	10µH
5V	1MHz	4.7µH
9V	500kHz	15µH
9V	1MHz	8.2µH
12V	500kHz	22µH
12V	1MHz	10µH

MPS's MPL-AY1050 family series are recommended for optimized performance. Visit MonolithicPower.com under Products > Inductors for more information.

PCB Layout Guidelines (12)

An efficient PCB layout is critical for stable operation. A 4-layer layout is recommended to improve thermal performance. For the best results, refer to Figure 11 and follow the guidelines below:

1. Keep the input capacitor, HS-FET, and LS-FET power loop as small as possible.
2. Connect PGND directly to a large ground plane.
3. If the bottom layer is a ground plane, place multiple vias near PGND.
4. Connect the PGND and VIN high-current paths using short, direct, and wide traces.
5. Place the ceramic input capacitor, especially the small package size (0603) input bypass capacitors, as close to the VIN and PGND pins as possible to reduce high-frequency noise.
6. Route the path between the input capacitor and VIN pin using short and wide traces.
7. Place the VCC capacitor as close to the VCC and AGND pins as possible.
8. Route the SW and BST paths away from sensitive analog areas.
9. Connect the VIN, SW, VOUT, and PGND pins to a large copper area to improve thermal performance and long-term reliability.
10. Separate the input PGND from the other ground areas on the top layer.
11. Connect these ground areas to the middle layers and the bottom layer using multiple vias.
12. Ensure that there is an integrated PGND on a middle layer or on the bottom layer.
13. Connect the power planes to the middle layers using multiple vias.

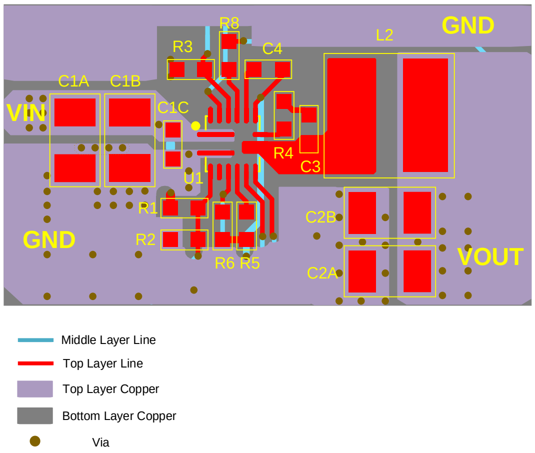


Figure 11: Recommended PCB Layout

Note:

12) This layout can be used in a wide range of application specifications. A smaller layout size can be achieved for specific applications (e.g. a higher f_{SW}, lower V_{IN}, or lower I_{OUT}) by selecting smaller package sizes for the inductors and capacitors.

TYPICAL APPLICATION CIRCUITS (13)

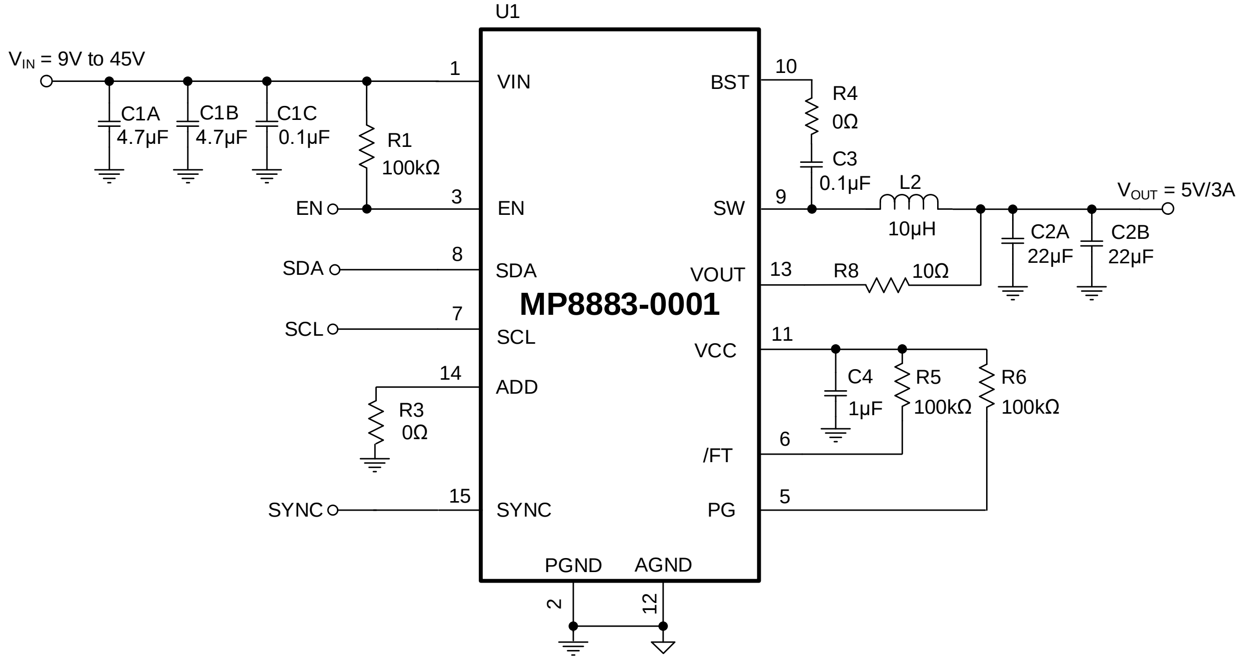


Figure 12: Typical Application Circuit (V_{OUT} = 5V, I_{OUT} = 3A)

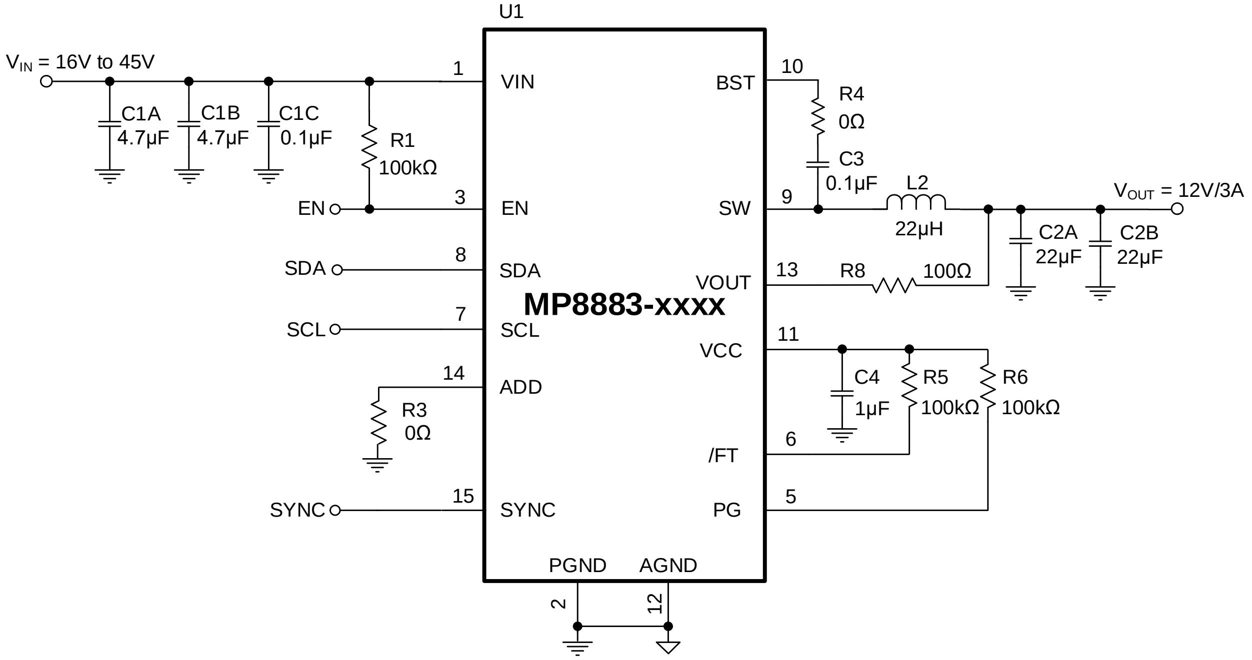


Figure 13: Typical Application Circuit (V_{OUT} = 12V, I_{OUT} = 3A)

TYPICAL APPLICATION CIRCUITS *(continued)* (13)

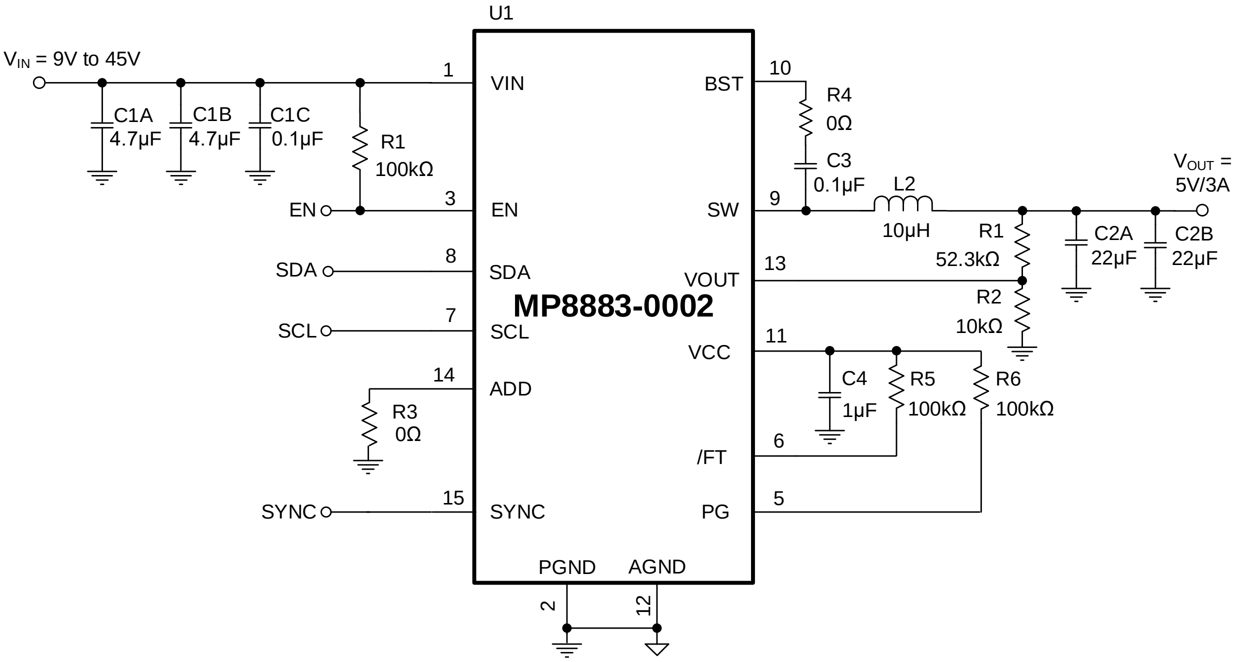


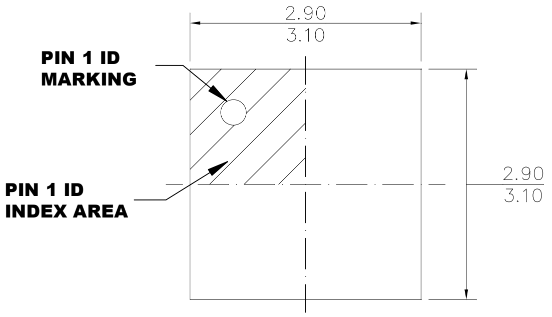
Figure 14: Typical Application Circuit (V_{OUT} = 5V, I_{OUT} = 3A with External Divider)

Note:

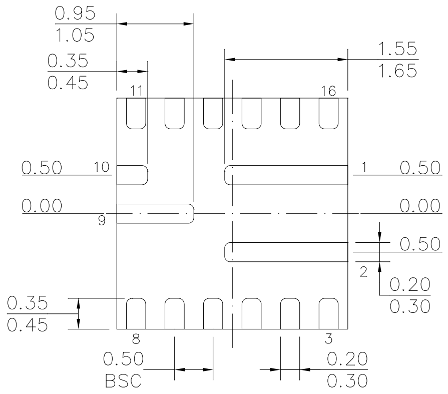
13) If V_{OUT} exceeds 9V, choose R8 to be 100Ω, and disable the V_{OUT} bias function.

PACKAGE INFORMATION

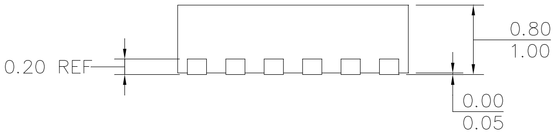
QFN-16 (3mmx3mm)



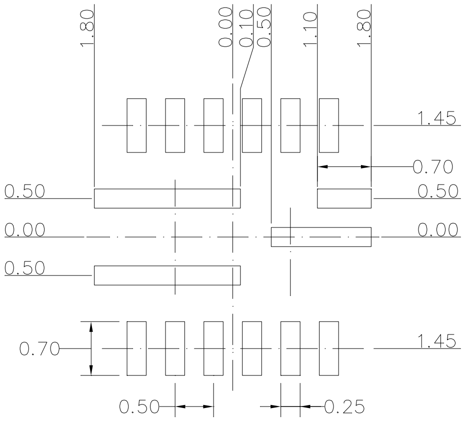
TOP VIEW



BOTTOM VIEW



SIDE VIEW

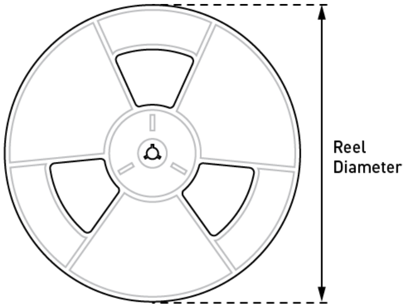


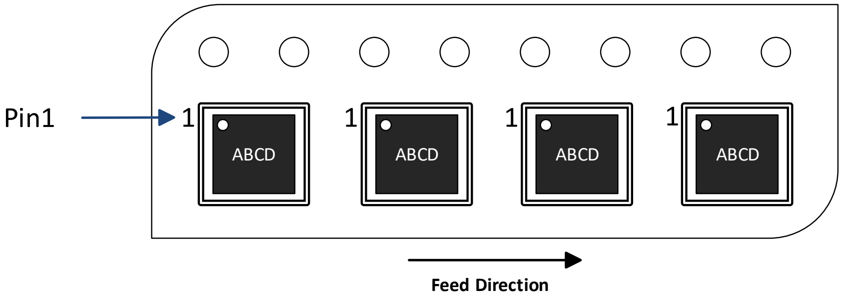
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITIES SHALL BE 0.1 MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION





Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP8883GQ-xxxx-Z	QFN-16 (3mmx3mm)	5000	N/A	N/A	13in	12mm	8mm
MP8883GQ-0001-Z							
MP8883GQ-0002-Z							

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	8/8/2022	Initial Release	-