DESCRIPTION
The MP8859 is a synchronous, 4-switch, integrated buck-boost converter capable of regulating the output voltage from a 2.8V to 22V wide input voltage range with high efficiency. The integrated output voltage scaling and adjustable output current limit functions meet the USB power delivery (PD) requirement.

The MP8859 uses constant-on-time (COT) control in buck mode and constant-off-time control in boost mode, providing fast load transient response and smooth buck-boost mode transient. The MP8859 provides auto PFM/PWM or forced PWM switching modes, programmable output constant current (CC) current limit, which supports flexible design for different applications.

Full protection features include over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), programmable soft start, and thermal shutdown. The MP8859 is available in a 16-pin QFN (3mmx3mm) package.

FEATURES
• Wide 2.8V to 22V Operating Input Voltage Range
• 1V (1) to 20.47V Output Voltage Range (5V Default) with 10mV Resolution through I²C
• 3A Output Current or 4A Input Current
• Four Low R_DS(ON) Internal Buck Power MOSFETs
• Adjustable Accurate CC Output Current Limit with Internal Sensing MOSFET via I²C
• 500kHz Switching Frequency
• Output Over-Voltage Protection (OVP) Hiccup
• Output Short-Circuit Protection (SCP) with Hiccup
• Over-Temperature Warning and Shutdown
• I²C Interface with ALT Pin
• Four Programmable I²C Addresses
• One-Time Programmable (OTP) Non-Volatile Memory
• I²C Programmable Line Drop Compensation, PFM/PWM Mode, Soft Start, OCP, etc.
• EN Shutdown Discharge Programmable
• Available in a QFN-16 (3mmx3mm) Package
• UL Certified, UL2367: E322138
  UL60950-1/ UL60950-1-07: E500002-A1-CB-1

APPLICATIONS
• USB PD Sourcing Ports
• Buck-Boost Bus Supplies

NOTE:
1) For V_OUT < 3V applications, the switching frequency decreases.
TYPICAL APPLICATION

Efficiency vs. Output Current

*V_IN = 12V, V_OUT = 5 - 20V, Forced PWM Mode*

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**MP8859**

- 22V **V_IN**, 3A **I_OUT**, INTEGRATED BUCK-BOOST WITH **I^2C** INTERFACE

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**TYPICAL APPLICATION**

![Circuit Diagram](image-url)

**Efficiency vs. Output Current**

- V_IN = 12V, V_OUT = 5 - 20V, Forced PWM Mode

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**MP8859**

- MP8859 Rev 1.0
- www.MonolithicPower.com

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### ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Part Number*</th>
<th>Package</th>
<th>Top Marking</th>
</tr>
</thead>
<tbody>
<tr>
<td>MP8859GQ-xxxx**</td>
<td>QFN-16 (3mmx3mm)</td>
<td>See Below</td>
</tr>
<tr>
<td>MP8859GQ-0000</td>
<td>QFN-16 (3mmx3mm)</td>
<td>See Below</td>
</tr>
<tr>
<td>EVKT-8859</td>
<td>Evaluation Kit</td>
<td></td>
</tr>
</tbody>
</table>

* For Tape & Reel, add suffix –Z (e.g.: MP8859GQ-XXXX-Z).

** "xxxx" is the configuration code identifier for the register setting stored in the OTP. The default number is "0000". Each "x" can be a hexadecimal value between 0 and F. Please work with an MPS FAE to create this unique number, even if ordering the "0000" code. MP8859GQ-0000 is the default version.

### TOP MARKING

BGRY

LLL

BGR: Product code of MP8859GQ
Y: Year code
LLL: Lot number

### EVALUATION KIT EVKT-8859

EVKT-8859 Kit contents: (Items below can be ordered separately).

<table>
<thead>
<tr>
<th>#</th>
<th>Part Number</th>
<th>Item</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>EV8859-Q-00B</td>
<td>MP8859GQ-0000 evaluation board</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>EVKT-USB2C-02</td>
<td>Includes one USB to I2C communication interface device, one USB cable, and one ribbon cable</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>Tdrive-8859</td>
<td>USB thumb drive that stores the GUI installation file and supplemental documents</td>
<td>1</td>
</tr>
</tbody>
</table>

Order direct from MonolithicPower.com or our distributors.

![Figure 1: EVKT-8859 Evaluation Kit Set-Up](image-url)
**ABSOLUTE MAXIMUM RATINGS**

Supply voltage ($V_{IN}$, $V_{OUT}$)......................... 24V

$V_{SW1, SW2}$ ........................................ -0.3V (-7V for <10ns) to $V_{IN} + 0.3V$ (26V for <10ns)

$V_{BST1, BST2}$ .......................................... $V_{SW} + 4V$

$V_{EN}$ .................................................. -0.3V to 24V

$V_{ALT}$ .................................................. -0.3V to +5.5V

All other pins .......................................... -0.3V to +4V

Continuous power dissipation ($T_J = +25°C$) (3)(5)

...................................................... 4.8W

Junction temperature .................................... 150°C

Lead temperature .................................... 260°C

Storage temperature .................................. -65°C to +150°C

**Recommended Operating Conditions**

Operation input voltage range .......... 2.8V to 22V

Output voltage range ...................... 1V to 20.47V

Output current .................. 3A continuous current or 4A input current

Operating junction temp. ($T_J$) ...... -40°C to +125°C

**Thermal Resistance**

$\theta_{JA}$  $\theta_{JC}$

QFN-16 (3mmx3mm)

EV8859-Q-00B (5) ...................... 26........ 3.... °C/W

JESD51-7 (6) ...................... 50...... 12... °C/W

**NOTES:**

2) Exceeding these ratings may damage the device.

3) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$ (MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX) - $T_A$)$\theta_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, and the regulator goes into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

4) The device is not guaranteed to function outside of its operating conditions.

5) Measured on EV8859-Q-00B, 4-layer PCB, 64mmx64mm.

6) Measured on JESD51-7, 4-layer PCB.
## OTP E-Fuse Selection Table by Default (MP8859GQ-0000)

<table>
<thead>
<tr>
<th>OTP Items</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output voltage</td>
<td>5V</td>
</tr>
<tr>
<td>IOUT_LIMIT</td>
<td>3.5A (For 21.5kΩ OC resistor)</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>500kHz</td>
</tr>
<tr>
<td>Mode</td>
<td>Forced PWM mode</td>
</tr>
<tr>
<td>Soft start time</td>
<td>900μs</td>
</tr>
<tr>
<td>Line drop compensation</td>
<td>V\textsubscript{OUT} compensates 150mV@3A \textsubscript{I\textsubscript{OUT}}</td>
</tr>
<tr>
<td>Output voltage discharge mode</td>
<td>Enabled</td>
</tr>
<tr>
<td>OCP_OVP protection mode</td>
<td>Hiccup</td>
</tr>
<tr>
<td>OTP configure code (ID1)</td>
<td>0x00</td>
</tr>
</tbody>
</table>
### ELECTRICAL CHARACTERISTICS

$V_{IN} = 12\, V$, $V_{EN} = 5\, V$, $T_J = -40^\circ C$ to $+125^\circ C$ \(^7\), typical value is tested at $T_J = +25^\circ C$, unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply current (shutdown)</td>
<td>$I_N$</td>
<td>$V_{EN} = 0, V$</td>
<td>0</td>
<td>3</td>
<td></td>
<td>$\mu A$</td>
</tr>
<tr>
<td>Supply current (quiescent)</td>
<td>$I_Q$</td>
<td>Non-switching, I$^2$C sets PFM mode</td>
<td>1</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>EN rising threshold</td>
<td>$V_{EN,, Rising}$</td>
<td></td>
<td>1.04</td>
<td>1.10</td>
<td>1.16</td>
<td>V</td>
</tr>
<tr>
<td>EN hysteresis</td>
<td>$V_{EN,, Falling}$</td>
<td></td>
<td>65</td>
<td>110</td>
<td>160</td>
<td>mV</td>
</tr>
<tr>
<td>EN to ground resistance</td>
<td>$R_{EN}$</td>
<td>$V_{EN} = 2, V$</td>
<td>2</td>
<td></td>
<td></td>
<td>M$\Omega$</td>
</tr>
<tr>
<td>EN on to $V_{OUT} &gt; 90%$ delay</td>
<td>$T_{Delay}$</td>
<td>See Figure 8.</td>
<td>900</td>
<td></td>
<td></td>
<td>$\mu s$</td>
</tr>
<tr>
<td>VCC regulator</td>
<td>$V_{CC}$</td>
<td></td>
<td>3.4</td>
<td>3.6</td>
<td>3.8</td>
<td>V</td>
</tr>
<tr>
<td>VCC load regulation</td>
<td>$V_{CC,, LOG}$</td>
<td>$I_{CC} = 10, mA$</td>
<td>1</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>$V_{IN}$ under-voltage lockout threshold rising</td>
<td>$V_{IN,, UVLO}$</td>
<td></td>
<td>2.50</td>
<td>2.65</td>
<td>2.79</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IN}$ under-voltage lockout threshold hysteresis</td>
<td>$V_{UVLO,, HYS}$</td>
<td></td>
<td>115</td>
<td>160</td>
<td>205</td>
<td>mV</td>
</tr>
</tbody>
</table>

### Power Converter

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>HS switch on resistance</td>
<td>$R_{DS,, ON,, HS}$</td>
<td>Switch A, D</td>
<td>25</td>
<td>40</td>
<td></td>
</tr>
<tr>
<td>LS switch on resistance</td>
<td>$R_{DS,, ON,, LSB}$</td>
<td>Switch B, C</td>
<td>21</td>
<td>35</td>
<td></td>
</tr>
<tr>
<td>Output voltage</td>
<td>$V_{OUT}$</td>
<td></td>
<td>-1.5$%$</td>
<td>5.0</td>
<td>+1.5$%$</td>
</tr>
<tr>
<td>Output discharge resistance</td>
<td>$R_{DIS}$</td>
<td></td>
<td>60</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>Switch leakage</td>
<td>$SW_{LKG}$</td>
<td>$V_{EN} = 0, V$, $V_{SW1,, SW2} = 22, V$, $T_J = +25^\circ C$</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{EN} = 0, V$, $V_{SW1,, SW2} = 22, V$, $T_J = -40^\circ C$ to $+125^\circ C$</td>
<td>5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Oscillator frequency</td>
<td>$F_s$</td>
<td></td>
<td>-20$%$</td>
<td>500</td>
<td>20$%$</td>
</tr>
<tr>
<td>Minimum on time ((^8))</td>
<td>$T_{ON,, MIN}$</td>
<td>Switch A, B, C, D</td>
<td>160</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maximum duty cycle</td>
<td>$D_{MAX}$</td>
<td>Buck mode, FREQ $= 500kHz$</td>
<td>85</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Minimum duty cycle</td>
<td>$D_{MIN}$</td>
<td>Boost mode, FREQ $= 500kHz$</td>
<td>15</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Protection

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output over-voltage protection</td>
<td>$V_{OVP,, R}$</td>
<td></td>
<td>150</td>
<td>160</td>
<td>170</td>
</tr>
<tr>
<td>Output OVP recovery</td>
<td>$V_{OVP,, F}$</td>
<td></td>
<td>130</td>
<td>140</td>
<td>150</td>
</tr>
<tr>
<td>Low-side B valley limit</td>
<td>$I_{LIMIT2}$</td>
<td>Switch B</td>
<td>6</td>
<td>8</td>
<td>10</td>
</tr>
<tr>
<td>Low-side C peak current limit</td>
<td>$I_{LIMIT3}$</td>
<td>Switch C</td>
<td>10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output average current</td>
<td>$I_{OUT,, LIMIT1}$</td>
<td>$V_{OUT} = 5, V$, over $0 - 125^\circ C$ temp range</td>
<td>0.85</td>
<td>1</td>
<td>1.15</td>
</tr>
<tr>
<td></td>
<td>$I_{OUT,, LIMIT2}$</td>
<td>$V_{OUT} = 5, V$, over $0 - 125^\circ C$ temp range</td>
<td>-5%</td>
<td>3.5</td>
<td>+5%</td>
</tr>
<tr>
<td>Output UV threshold</td>
<td>$V_{UV}$</td>
<td>$20\mu s$ deglitch, UV falling</td>
<td>45%</td>
<td>50%</td>
<td>55%</td>
</tr>
</tbody>
</table>
### ELECTRICAL CHARACTERISTICS (continued)

$V_{IN} = 12\text{V}, \ V_{EN} = 5\text{V}, \ T_J = -40^\circ \text{C} \text{ to } +125^\circ \text{C}$ (7), typical value is tested at $T_J = +25^\circ \text{C}$, unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>ALT sink current capability</td>
<td>ALT_LOW</td>
<td>Sink 4mA</td>
<td>0.2</td>
<td>0.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>ALT leakage</td>
<td>ALT_LKG</td>
<td>$V_{\text{PULL}} = 5\text{V}$</td>
<td></td>
<td></td>
<td>1</td>
<td>μA</td>
</tr>
<tr>
<td>Thermal shutdown rising threshold</td>
<td>$T_{\text{STD}}$</td>
<td></td>
<td>150</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Thermal hysteresis</td>
<td>$T_{\text{STD, HYS}}$</td>
<td></td>
<td>20</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>

#### I2C Specification

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADD voltage threshold 1</td>
<td>$V_{\text{ADD}, 1}$</td>
<td>ADD pin float</td>
<td>60H</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADD voltage threshold 2</td>
<td>$V_{\text{ADD}, 2}$</td>
<td>$R_4 = 499k\Omega, \ R_5 = 301k\Omega$</td>
<td>62H</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADD voltage threshold 3</td>
<td>$V_{\text{ADD}, 3}$</td>
<td>$R_4 = 301k\Omega, \ R_5 = 499k\Omega$</td>
<td>64H</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADD voltage threshold 4</td>
<td>$V_{\text{ADD}, 4}$</td>
<td>$R_4 = 100k\Omega$</td>
<td>66H</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADD to GND pull-down resistor</td>
<td>$R_{\text{ADD}}$</td>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td>MΩ</td>
</tr>
<tr>
<td>Input logic high</td>
<td>$V_{\text{IH}}$</td>
<td>$I^2C$ pull-up VDD can be 1.8V to 5V</td>
<td>1.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Input logic low</td>
<td>$V_{\text{IL}}$</td>
<td></td>
<td>0.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Output voltage logic low</td>
<td>$V_{\text{OUT, L}}$</td>
<td></td>
<td></td>
<td>0.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>SCL clock frequency</td>
<td>$f_{\text{SCL}}$</td>
<td></td>
<td>400</td>
<td></td>
<td>3400</td>
<td>kHz</td>
</tr>
<tr>
<td>SCL high time</td>
<td>$t_{\text{HIGH}}$</td>
<td></td>
<td>60</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>SCL low time</td>
<td>$t_{\text{LOW}}$</td>
<td></td>
<td>160</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Data set-up time</td>
<td>$t_{\text{SU, DAT}}$</td>
<td></td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Data hold time</td>
<td>$t_{\text{HD, DAT}}$</td>
<td></td>
<td>0</td>
<td>60</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Set-up time for (repeated) start condition</td>
<td>$t_{\text{SU, STA}}$</td>
<td></td>
<td>160</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Hold time for (repeated) start condition</td>
<td>$t_{\text{HD, STA}}$</td>
<td></td>
<td>160</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Bus free time between a start and a stop condition</td>
<td>$t_{\text{BUF}}$</td>
<td></td>
<td>160</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Set-up time for stop condition</td>
<td>$T_{\text{SU, STO}}$</td>
<td></td>
<td>160</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Rise time of SCL and SDA</td>
<td>$t_{\text{R}}$</td>
<td></td>
<td>10</td>
<td></td>
<td>300</td>
<td>ns</td>
</tr>
<tr>
<td>Fall time of SCL and SDA</td>
<td>$t_{\text{F}}$</td>
<td></td>
<td>10</td>
<td></td>
<td>300</td>
<td>ns</td>
</tr>
<tr>
<td>Pulse width of suppressed spike</td>
<td>$t_{\text{SP}}$</td>
<td></td>
<td>0</td>
<td></td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>Capacitance for each bus line</td>
<td>$C_B$</td>
<td></td>
<td>400</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
</tbody>
</table>

#### NOTES:

7) All min/max parameters are tested at $T_J = 25^\circ \text{C}$. Limits over temperature are guaranteed by design, characterization, and correlation.

8) Guaranteed by engineering sample characterization.
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 12V$, $V_{OUT} = 5V$, $T_A = 25^\circ C$, unless otherwise noted.

**Load Regulation vs. Output Current**

$V_{IN} = 12V$, $V_{OUT} = 5V/9V/12V/20V$, $I_{OUT} = 0A$ to $3A$, no line drop compensation

**Line Regulation vs. Input Voltage**

$V_{OUT} = 5V$

$V_{OUT} = 9V$

$V_{OUT} = 12V$

$V_{OUT} = 20V$

**Thermal Rising vs. Output Current**

$V_{IN} = 12V$, $V_{OUT} = 5 - 20V$, $I_{OUT} = 0 - 3A$
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

\( \text{V}_{\text{IN}} = 12 \text{V}, \text{V}_{\text{OUT}} = 5 \text{V}, T_{\text{A}} = 25^\circ \text{C}, \) unless otherwise noted.

**Efficiency vs. Output Current**

\( \text{V}_{\text{IN}} = 12 \text{V}, \text{V}_{\text{OUT}} = 5 - 20 \text{V}, \) forced PWM mode

![Efficiency vs. Output Current](image)

**Efficiency vs. Output Current**

\( \text{V}_{\text{IN}} = 12 \text{V}, \text{V}_{\text{OUT}} = 5 - 20 \text{V}, \) auto PFM/PWM mode

![Efficiency vs. Output Current](image)

**Efficiency vs. Output Current**

\( \text{V}_{\text{IN}} = 5 \text{V}, \text{V}_{\text{OUT}} = 5/9 \text{V}, \) forced PWM mode

![Efficiency vs. Output Current](image)

**Efficiency vs. Output Current**

\( \text{V}_{\text{IN}} = 5 \text{V}, \text{V}_{\text{OUT}} = 5/9 \text{V}, \) auto PFM/PWM mode

![Efficiency vs. Output Current](image)

**Recommended Maximum \( \text{I}_{\text{OUT}} \) vs. \( \text{V}_{\text{IN}} \) and \( \text{V}_{\text{OUT}} \) with 120\( \mu \)F Low ESR \( \text{C}_{\text{OUT}} \) Capacitor**

![Recommended Maximum \( \text{I}_{\text{OUT}} \) vs. \( \text{V}_{\text{IN}} \) and \( \text{V}_{\text{OUT}} \) with 120\( \mu \)F Low ESR \( \text{C}_{\text{OUT}} \) Capacitor](image)

**Recommended Maximum \( \text{I}_{\text{OUT}} \) vs. \( \text{V}_{\text{IN}} \) and \( \text{V}_{\text{OUT}} \) with 22\( \mu \)F x5 Ceramic \( \text{C}_{\text{OUT}} \) Capacitor**

![Recommended Maximum \( \text{I}_{\text{OUT}} \) vs. \( \text{V}_{\text{IN}} \) and \( \text{V}_{\text{OUT}} \) with 22\( \mu \)F x5 Ceramic \( \text{C}_{\text{OUT}} \) Capacitor](image)
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{\text{IN}} = 12V$, $V_{\text{OUT}} = 5V$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

- **Output Voltage vs. Temperature**
- **$V_{\text{IN}}$ UVLO Rising and Falling Threshold vs. Temperature**
- **EN Rising and Falling Threshold vs. Temperature**
- **Buck Valley Current Limit vs. Temperature**
- **Output Voltage UVP Threshold vs. Temperature**
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12\,V$, $V_{OUT} = 5\,V$, $T_A = 25\,^\circ C$, test waveform is based on Figure 12, unless otherwise noted.

**EN Bit Enable through I$^2$C Command**

- **Load = 0A**
- **Load = 3A**

**EN Bit Disable through I$^2$C Command**

- **Load = 0A**
- **Load = 3A**

**V$IN$ Start-Up**

- **Load = 0A**
- **Load = 3A**
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

\( V_{\text{IN}} = 12V, \ V_{\text{OUT}} = 5V, \ \theta_A = 25^\circ C, \) test waveform is based on Figure 12, unless otherwise noted.

**VIN Power Off**

- **Load = 0A**

**CH1: VOUT 5V/div.**

**CH2: VSW1 10V/div.**

**CH3: VSW2 10V/div.**

**CH4: IL 1A/div.**

**100ms/div.**

**VIN Power Off**

- **Load = 3A**

**CH1: VOUT 5V/div.**

**CH2: VSW1 10V/div.**

**CH3: VSW2 10V/div.**

**CH4: IL 5A/div.**

**1ms/div.**

**EN Pin Enable**

- **Load = 0A**

**CH1: VOUT 5V/div.**

**CH2: VSW1 10V/div.**

**CH3: VSW2 10V/div.**

**CH4: IL 5A/div.**

**4ms/div.**

**EN Pin Enable**

- **Load = 3A**

**CH1: VOUT 5V/div.**

**CH2: VSW1 10V/div.**

**CH3: VSW2 10V/div.**

**CH4: IL 5A/div.**

**4ms/div.**

**EN Pin Disable**

- **Load = 0A**

**CH1: VOUT 5V/div.**

**CH2: VSW1 10V/div.**

**CH3: VSW2 5V/div.**

**CH4: IL 5A/div.**

**2ms/div.**

**EN Pin Disable**

- **Load = 3A**

**CH1: VOUT 5V/div.**

**CH2: VSW1 10V/div.**

**CH3: VSW2 5V/div.**

**CH4: IL 5A/div.**

**200μs/div.**
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12\text{V}$, $V_{OUT} = 5\text{V}$, $T_A = 25^\circ\text{C}$, test waveform is based on Figure 12, unless otherwise noted.

Steady State

$V_{OUT} = 5\text{V}$, load = 0A

Steady State

$V_{OUT} = 5\text{V}$, load = 3A

Steady State

$V_{OUT} = 9\text{V}$, load = 0A

Steady State

$V_{OUT} = 9\text{V}$, load = 3A

Steady State

$V_{OUT} = 12\text{V}$, load = 0A

Steady State

$V_{OUT} = 12\text{V}$, load = 3A
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 5V$, $T_A = 25^\circ C$, test waveform is based on Figure 12, unless otherwise noted.

Steady State
$V_{OUT} = 20V$, load = 0A

Load Transient
$V_{IN} = 12V$, $V_{OUT} = 5V$, no line drop compensation, 0 - 3A, 150mA/μs

Load Transient
$V_{IN} = 12V$, $V_{OUT} = 5V$, no line drop compensation, 0 - 1.5A, 150mA/μs

Load Transient
$V_{IN} = 12V$, $V_{OUT} = 5V$, no line drop compensation, 1.5 - 3A, 150mA/μs

SCP Entry with Latch-Off Mode

CH1: $V_{OUT}/AC$ 200mV/div.
CH2: $V_{SW1}$ 20V/div.
CH3: $V_{SW2}$ 20V/div.
CH4: $I_{OUT}$ 2A/div.

CH1: $V_{OUT}/AC$ 200mV/div.
CH2: $V_{SW1}$ 20V/div.
CH3: $V_{SW2}$ 20V/div.
CH4: $I_{OUT}$ 1A/div.

CH1: $V_{OUT}/AC$ 200mV/div.
CH2: $V_{SW1}$ 10V/div.
CH3: $V_{SW2}$ 10V/div.
CH4: $L$ 10A/div.
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 5V$, $T_A = 25^\circ C$, test waveform is based on Figure 12, unless otherwise noted.

SCP Entry with Hiccup Mode

SCP Recovery with Hiccup Mode

CC Current Limit Entry (Test with CV Mode of Electronic Load)

CC Current Limit Steady State

$V_{OUT}$ OVP with Hiccup Mode

$V_{OUT}$ OVP with Latch-Off Mode
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V\textsubscript{IN} = 12V, V\textsubscript{OUT} = 5V, T\textsubscript{A} = 25°C, Test waveform is based on Figure 12, unless otherwise noted.

\textbf{I\textsuperscript{2}C VID}

\textbf{V\textsubscript{OUT} = 5-12V, I\textsubscript{OUT} = 0A}

\begin{itemize}
  \item CH1: V\textsubscript{OUT} 5V/div.
  \item CH2: V\textsubscript{SW1} 10V/div.
  \item CH3: V\textsubscript{SW2} 20V/div.
  \item CH4: I\textsubscript{L} 5A/div.
\end{itemize}

\begin{itemize}
  \item 20ms/div.
\end{itemize}

\textbf{I\textsuperscript{2}C VID}

\textbf{V\textsubscript{OUT} = 12-5V, I\textsubscript{OUT} = 0A}

\begin{itemize}
  \item CH1: V\textsubscript{OUT} 5V/div.
  \item CH2: V\textsubscript{SW1} 10V/div.
  \item CH3: V\textsubscript{SW2} 20V/div.
  \item CH4: I\textsubscript{L} 5A/div.
\end{itemize}

\begin{itemize}
  \item 20ms/div.
\end{itemize}

\textbf{I\textsuperscript{2}C VID}

\textbf{V\textsubscript{OUT} = 5-12V, I\textsubscript{OUT} = 3A}

\begin{itemize}
  \item CH1: V\textsubscript{OUT} 5V/div.
  \item CH2: V\textsubscript{SW1} 20V/div.
  \item CH3: V\textsubscript{SW2} 20V/div.
  \item CH4: I\textsubscript{L} 2A/div.
\end{itemize}

\begin{itemize}
  \item 20ms/div.
\end{itemize}

\textbf{I\textsuperscript{2}C VID}

\textbf{V\textsubscript{OUT} = 12-5V, I\textsubscript{OUT} = 3A}

\begin{itemize}
  \item CH1: V\textsubscript{OUT} 5V/div.
  \item CH2: V\textsubscript{SW1} 20V/div.
  \item CH3: V\textsubscript{SW2} 20V/div.
  \item CH4: I\textsubscript{L} 2A/div.
\end{itemize}

\begin{itemize}
  \item 20ms/div.
\end{itemize}
# PIN FUNCTIONS

<table>
<thead>
<tr>
<th>QFN 3x3 Pin #</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>IN</td>
<td><strong>Supply voltage.</strong> IN is the drain of the internal power device and provides power to the entire chip. The MP8859 operates from a 2.8V to 22V input voltage. A capacitor (C&lt;sub&gt;IN&lt;/sub&gt;) is required to prevent large voltage spikes from appearing at the input. Place C&lt;sub&gt;IN&lt;/sub&gt; as close to the IC as possible.</td>
</tr>
<tr>
<td>2, 11</td>
<td>GND</td>
<td><strong>Power ground.</strong> GND is the reference ground of the regulated output voltage. GND requires extra care during PCB layout. Connect GND with copper traces and vias.</td>
</tr>
<tr>
<td>3</td>
<td>EN</td>
<td><strong>On/off control for entire chip.</strong> Drive EN high to turn on the chip. Drive EN low or float EN to turn off the device. EN has internal 2MΩ pull-down resistor to ground.</td>
</tr>
<tr>
<td>4</td>
<td>ADD</td>
<td><strong>I&lt;sup&gt;2&lt;/sup&gt;C slave addresses program pin.</strong> Connect a resistor divider from VCC to ADD to set four different I&lt;sup&gt;2&lt;/sup&gt;C slave addresses.</td>
</tr>
<tr>
<td>5</td>
<td>SCL</td>
<td><strong>Clock pin of the I&lt;sup&gt;2&lt;/sup&gt;C interface.</strong> SCL can support an I&lt;sup&gt;2&lt;/sup&gt;C clock up to 3.4MHz.</td>
</tr>
<tr>
<td>6</td>
<td>SDA</td>
<td><strong>Data pin of the I&lt;sup&gt;2&lt;/sup&gt;C interface.</strong></td>
</tr>
<tr>
<td>7</td>
<td>OC</td>
<td><strong>Output constant current limit set pin.</strong></td>
</tr>
<tr>
<td>8</td>
<td>ALT</td>
<td><strong>Alert output.</strong> ALT pulling to logic low indicates that a fault or warning has occurred.</td>
</tr>
<tr>
<td>9</td>
<td>VCC</td>
<td><strong>Internal 3.6V LDO regulator output.</strong> Decouple VCC with a 1µF capacitor.</td>
</tr>
<tr>
<td>10</td>
<td>AGND</td>
<td><strong>Analog Ground.</strong> Connect AGND to GND.</td>
</tr>
<tr>
<td>12</td>
<td>OUT</td>
<td><strong>Output power pin.</strong> Place the output capacitor close to OUT and GND.</td>
</tr>
<tr>
<td>13</td>
<td>BST2</td>
<td><strong>Bootstrap.</strong> Connect a 0.1µF capacitor between SW2 and BST2 to form a floating supply across the high-side switch driver.</td>
</tr>
<tr>
<td>14</td>
<td>SW2</td>
<td><strong>Switching node of the second half bridge.</strong> Connect one end of the inductor to SW2 for the current to run through the bridge.</td>
</tr>
<tr>
<td>15</td>
<td>SW1</td>
<td><strong>Switching node of the first half bridge.</strong> Connect one end of the inductor to SW1 for the current to run through the bridge.</td>
</tr>
<tr>
<td>16</td>
<td>BST1</td>
<td><strong>Bootstrap.</strong> Connect a 0.1µF capacitor between SW1 and BST1 to form a floating supply across the high-side switch driver.</td>
</tr>
</tbody>
</table>
Figure 2: Functional Block Diagram
OPERATION

The MP8859 is a 4-switch, integrated buck-boost converter that can work in constant-on-time (COT) mode with fixed frequency, which provides fast transient response for the buck, boost, and buck-boost modes. One special buck-boost control strategy provides high efficiency over the full input range and smooth transient between different modes.

Buck-Boost Operation

The MP8859 can regulate the output to be above, equal to, or below the input voltage. Based on the one-inductor, four-switch power structure shown in Figure 3, the MP8859 can operate in buck mode, boost mode, or buck-boost mode with different VIN inputs (see Figure 4).

SWA on, SWB off
SWC and SWD switching

Figure 3: Buck-Boost Topology

Boost Mode (VIN > VOUT)

When the input voltage is significantly higher than the output voltage, the MP8859 works in buck mode. In buck mode, SWA and SWB are switching for the buck regulation. SWC is off, and SWD remains on to conduct the inductor current.

SWA works with COT control logic, and SWB turns on as a complement of SWA. In each cycle, SWB turns on to conduct the inductor current. When the inductor current drops to the COMP voltage (VCOMP), SWB turns off, and SWA turns on. SWA turns on for a fixed on-time period before turning off. Then SWB turns on again, and the operation repeats. The COMP signal is the error amplifier (EA) output from the VOUT feedback and internal FB reference voltage (see Figure 5).

Figure 5: Buck Waveform

Boost Mode (VIN < VOUT)

When the input voltage is significantly lower than the output voltage, the MP8859 works in boost mode. In boost mode, SWC and SWD are switching for the boost regulation. SWB is off, and SWA remains on to conduct the inductor current.

SWC remains off with COT control in each period, while SWD turns on as a complement of SWC to boost the inductor current to the output. In each cycle, SWC turns on to conduct the inductor current. When the inductor current rises and reaches VCOMP, SWC turns off and SWD turns on. SWC turns off with a fixed off-time before turning on again. During this period, SWD turns on for the current freewheel (see Figure 6).

Figure 6: Boost Waveform

Buck-Boost Mode (VIN ≈ VOUT)

When VIN is close to VOUT, the converter cannot provide enough energy to operate in buck mode due to SWA’s minimum off time, or the converter supplies too much power to VOUT in boost mode due to SWC’s minimum on time. The MP8859 uses buck-boost control to regulate the output in these conditions.
In buck mode, if \( V_{IN} \) drops and the SWA off period is close to the buck minimum off time, the buck-boost mode is engaged. When the next cycle starts after the SWA and SWD on-time period (buck high-side MOSFET (HS-FET) on period), the boost starts with SWA and SWC on (boost low-side MOSFET (LS-FET) on). SWA and SWD turn on again for the rest period of the boost period (boost HS-FET on). After the boost period elapses, the buck period starts, and SWB and SWD remain on until the inductor current drops to \( V_{COMP} \). Then SWA and SWD turn on until the next boost period begins. Buck and boost switching work with a one-interval period. This is called buck-boost mode.

In boost mode, if \( V_{IN} \) drops and the SWC on period is close to the boost minimum on time, buck-boost mode engaged. After the boost constant-off time period (SWA and SWD on), SWB and SWD remain on until the inductor current signal drops to \( V_{COMP} \), just like a buck off-time period control. After the inductor current signal triggers \( V_{COMP} \), SWA and SWB turn on for the buck on time, which is followed by a boost switching (SWA and SWC on). Buck and boost switching work with a one-interval period. Figure 7 shows the buck-boost waveform for both \( V_{IN} > V_{OUT} \) and \( V_{IN} < V_{OUT} \).

![Buck to Buck-Boost Transient](image)

Boost to Buck-Boost Transient

Figure 7: Buck-Boost Waveform

In buck-boost mode, if \( V_{IN} \) is higher than 130% of \( V_{OUT} \), the MP8859 switches from buck-boost mode to buck mode. If \( V_{IN} \) is lower than 20% of \( V_{OUT} \), the MP8859 switches from buck-boost mode to boost mode.

**Working Mode Selection**

The MP8859 works with a fixed frequency in heavy-load condition. When the load current decreases, the MP8859 can work in forced continuous conduction mode (FCCM) or pulse-skipping mode (PSM) based on the MODE register setting.

**FCCM (or Forced PWM)**

In FCCM condition, the buck on time and boost off time are determined by the internal circuit to achieve a fixed frequency based on the \( V_{IN}/V_{OUT} \) ratio. When the load decreases, the average input current drops, and the inductor current may go negative from \( V_{OUT} \) to \( V_{IN} \) during the off time (SWD on). This forces the inductor current to work in continuous mode with a fixed frequency, producing a lower \( V_{OUT} \) ripple than in PSM mode.

**PSM (Auto PFM/PWM Mode)**

In PSM condition, once the inductor current drops to 0A, SWD turns off to prevent the current from flowing from \( V_{OUT} \) to \( V_{IN} \), forcing the inductor current to work in discontinuous conduction mode (DCM). Simultaneously, the internal off-time clock stretches once the MP8859 enters DCM mode. The frequency drops when the inductor current conduction period decreases, helping to save power loss and reduce the \( V_{OUT} \) ripple.

If \( V_{COMP} \) drops to the PSM threshold, even if the IC stretches the frequency, the MP8859 stops switching to decrease more switching power loss. The MP8859 recovers switching once \( V_{COMP} \) rises above the PSM threshold. The switching pulse skips based on \( V_{COMP} \) in very light-load condition. PSM has a much higher efficiency than FCCM mode in light load, but the \( V_{OUT} \) ripple may be higher due to the group switching pulse.

**Internal VCC Regulator**

The 3.6V internal regulator powers most of the internal circuitries. This regulator takes \( V_{IN} \) and operates in the full \( V_{IN} \) range. When \( V_{IN} \) exceeds 3.6V, the output of the regulator is in
full regulation. If $V_{IN}$ is less than 3.6V, the output decreases with $V_{IN}$. VCC requires an external 1µF ceramic capacitor for decoupling.

**Enable Control (EN)**

The MP8859 has an enable control pin (EN). Pull EN high to enable the IC. Pull EN low or float EN to disable the IC.

If EN is pulled down when the output discharge function is enabled, the MP8859 truly shuts down after 55ms. The MP8859’s I2C register value is reset to default only after the MP8859 truly shuts down. If EN is pulled high within 55ms, the I2C register is not reset, and the MP8859 enables the output with previous register setting.

If the output discharge function is disabled, the MP8859 truly shuts down once EN is pulled down for more than 100µs, and the MP8859 I2C register is reset after a 100µs delay.

**Under-Voltage Lockout (UVLO)**

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors the input voltage and enables or disables the entire IC.

**Internal Soft Start (SS)**

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a SS voltage that ramps up from 0V to 3.6V. When SS is lower than REF, the error amplifier uses SS as the reference. When SS is higher than REF, the error amplifier uses REF as the reference.

If the output of the MP8859 is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side switches until the voltage on the internal SS capacitor exceeds the internal feedback voltage (see Figure 9).

**Figure 8: EN On/Off Logic for I2C Register Reset**

**Output Constant Current Limit (OCP)**

The MP8859 has a constant-current limit control loop to limit the output average current. The current information is sensed from switch A, B, C, and D. Then an average algorithm is used to calculate the output current.

When the output current exceeds the current-limit threshold, the output voltage starts to drop. If $V_{OUT}$ drops below the under-voltage (UV) threshold (typically 50% below the reference), the MP8859 enters hiccup mode or latch-off mode according to the I2C setting.

In hiccup mode, the MP8859 stops switching and recovers automatically with 12.5% duty cycles. In latch-off mode, the MP8859 stops switching until the IC restarts ($V_{IN}$, EN, or EN bit toggle).

**Over-Voltage Protection (OVP)**

The MP8859 monitors a resistor-divided feedback voltage to detect output over-voltage. When the feedback voltage rises higher than 160% of the target voltage, the over-voltage protection (OVP) comparator output goes high. The output-to-ground discharge resistor turns on.

The OUT pin has an absolute OVP function. Once $V_{OUT}$ is higher than the absolute OVP threshold (23V), the MP8859 stops switching and turns on the OUT-to-ground discharge resistor.

**Start-Up and Shutdown**

If both $V_{IN}$ and EN exceed their respective thresholds, the chip is enabled. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: EN low, $V_{IN}$ low, and thermal shutdown. During shutdown, the signaling path is blocked to avoid any fault triggering. Then $V_{COMP}$ and the internal...
supply rail are pulled down. The floating driver is not subject to this shutdown command.

**Output Discharge**

The MP8859 has an output discharge function that provides a resistive discharge path for the external output capacitor. The function is active when the part is disabled (input voltage is under UVLO or enable off), the discharge path is turned off when \( V_{OUT} < 50 \text{mV} \) or waits for the 50ms maximum timer to pass. This function can also be disabled via the \(^{\text{I}^2\text{C}}\) interface.

**Thermal Warning (TSW) and Shutdown (TSD)**

Thermal warning and thermal shutdown prevent the part from operating at exceedingly high temperatures. When the silicon die temperature exceeds 120°C, the MP8859 sets the OTW bit[D5] to 1. When the temperature falls below its lower threshold (typically 100°C), the OTW bit[D5] is 0.

When the silicon die temperature exceeds 150°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled. This is a non-latch protection.

**\(^{\text{I}^2\text{C}}\) INTERFACE**

**\(^{\text{I}^2\text{C}}\) Serial Interface Description**

The \(^{\text{I}^2\text{C}}\) is a 2-wire, bidirectional, serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle. When connecting to the line, a master device generates the SCL signal and device address and arranges the communication sequence. The MP8859 interface is an \(^{\text{I}^2\text{C}}\) slave, which supports both fast mode (400kHz) and high-speed mode (3.4MHz). The \(^{\text{I}^2\text{C}}\) interface adds flexibility to the power supply solution. The output voltage, transition slew rate, and other parameters can be controlled instantaneously via the \(^{\text{I}^2\text{C}}\) interface. When the master sends the address as an 8-bit value, the 7-bit address should be followed by a 0 or 1 to indicate a write or read operation.

**Start and Stop Conditions**

The start and stop conditions are signaled by the master device, which signifies the beginning and end of an \(^{\text{I}^2\text{C}}\) transfer. The start condition is defined as the SDA signal transitioning from high to low while the SCL is high. The stop condition is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 10).

The master then generates the SCL clocks and transmits the device address and the read/write direction bit (r/w) on the SDA line.

**Transfer Data**

Data is transferred in 8-bit bytes by an SDA line. Each byte of data is to be followed by an acknowledge bit.

**\(^{\text{I}^2\text{C}}\) Update Sequence**

The MP8859 requires a start condition, a valid \(^{\text{I}^2\text{C}}\) address, a register address byte, and a data byte for a single data update. The MP8859 acknowledges the receipt of each byte by pulling the SDA line low during the high period of a single clock pulse. A valid \(^{\text{I}^2\text{C}}\) address selects the MP8859. The MP8859 performs an update on the falling edge of the LSB byte. Examples of an \(^{\text{I}^2\text{C}}\) write and read sequence are shown on page 23.

**\(^{\text{I}^2\text{C}}\) Start-Up Timing**

The \(^{\text{I}^2\text{C}}\) function is enabled once \( V_{IN} > \text{UVLO} \) and EN is active. The \(^{\text{I}^2\text{C}}\) function continues working during OCP, OVP, and thermal shutdown.
Figure 10: Start and Stop Condition

<table>
<thead>
<tr>
<th>Master to Slave</th>
<th>Slave to Master</th>
</tr>
</thead>
<tbody>
<tr>
<td>A = Acknowledge (SDA = LOW)</td>
<td>NA = NOT Acknowledge (SDA = HIGH)</td>
</tr>
<tr>
<td>S = Start Condition</td>
<td>P = Stop Condition</td>
</tr>
</tbody>
</table>

**I2C Write Example – Write Single Register**

<table>
<thead>
<tr>
<th>8 bits</th>
<th>8 bits</th>
<th>8 bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>Slave Address</td>
<td>WR</td>
</tr>
</tbody>
</table>

Multi byte write executed from current register location
(the read only register will be skipped)

**I2C Write Example – Write Multi Register**

<table>
<thead>
<tr>
<th>8 bits</th>
<th>8 bits</th>
<th>8 bits</th>
<th>8 bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>Slave Address</td>
<td>WR</td>
<td>A</td>
</tr>
</tbody>
</table>

Register address to read specified
Read register data from current register location

**I2C Read Example – Read Single Register**

<table>
<thead>
<tr>
<th>8 bits</th>
<th>8 bits</th>
<th>8 bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>Slave Address</td>
<td>WR</td>
</tr>
</tbody>
</table>

Master to Slave
A = Acknowledge (SDA = LOW)  S = Start Condition  Sr = Repeat
Slave to Master
NA = NOT Acknowledge (SDA = HIGH)  P = Stop Condition

WR Write = 0  RD Read = 1
### I²C REGISTER MAP

<table>
<thead>
<tr>
<th>ADD (HEX)</th>
<th>NAME</th>
<th>R/W</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>VOUT_L</td>
<td>r/w</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>RESERV</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>VOUT DATA BIT LOW [2:0]*</td>
</tr>
<tr>
<td>01</td>
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<td>OUTPUT CURRENT LIMIT THRESHOLD (0A-6.35A/50mA STEP FOR 21.5K OC RESISTOR)*</td>
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<td>OTP Configure Code. &quot;0x00&quot; means standard MP8859, &quot;0x01&quot; means MP8859-0001 part number*</td>
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</table>

**NOTE:**

* These items have one-time programmable (OTP) non-volatile memory. The OTP is reloaded to the I²C register during V_IN > UVLO or EN shutdown.
REGISTER DESCRIPTION

I2C Bus Slave Address

A resistor-divider from VCC to GND can achieve an accurate reference voltage. Connect ADD to this reference voltage to set different I2C addresses. The internal circuit changes the I2C address accordingly. Table 1 shows the four voltage thresholds for the four I2C addresses and recommended setting resistors.

Table 1: I2C Address Setting via ADD Voltage

<table>
<thead>
<tr>
<th>ADD Voltage</th>
<th>ADD Upper Resistor R4 (kΩ)</th>
<th>ADD Lower Resistor R5 (kΩ)</th>
<th>I2C Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;25%Vcc</td>
<td>No connection</td>
<td>No connection</td>
<td>1100 000 60H</td>
</tr>
<tr>
<td>25%Vcc-50%Vcc</td>
<td>499</td>
<td>301</td>
<td>1100 010 62H</td>
</tr>
<tr>
<td>50%Vcc-75%Vcc</td>
<td>301</td>
<td>499</td>
<td>1100 100 64H</td>
</tr>
<tr>
<td>&gt;75%Vcc</td>
<td>100</td>
<td>No connection</td>
<td>1100 110 66H</td>
</tr>
</tbody>
</table>

VOUT Setting

The registers VOUT_L and VOUT_H set the output voltage and follow the 11-bit direct format below.

<table>
<thead>
<tr>
<th>Name</th>
<th>Format</th>
<th>VOUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Register Name</td>
<td>Direct, unsigned binary integer</td>
<td>VOUT_H D[7:0]</td>
</tr>
<tr>
<td>Bit</td>
<td>N/A</td>
<td>15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td>
</tr>
<tr>
<td>Access</td>
<td>N/A</td>
<td>r/w r/w r/w r/w r/w r/w r/w r/w r/w r/w r/w r/w</td>
</tr>
<tr>
<td>Function</td>
<td>N/A</td>
<td>Data bit high</td>
</tr>
<tr>
<td>Default value (5V)</td>
<td>N/A</td>
<td></td>
</tr>
</tbody>
</table>

The output voltage can be calculated with Equation (1):

\[ Vout (V) = V/100 \]  

(1)

Where V is an 11-bit unsigned binary integer of VOUT[10:0], and V ranges from 0 to 2047. The VOUT resolution is 10mV/LSB.

Inside the MP8859, there is a feedback resistor network from OUT to the internal FB reference voltage. The feedback resistor ratio is VOUT/V_FB = 12.5. The output voltage change slew rate is fixed at 1mV/µs. Refer to the GO_BIT bit when implementing the output voltage change.

VOUT_GO Register

GO_BIT D[0]

The MP8859 can be controlled when to VOUT begins to change. Set GO_BIT to 1 to start the output change based on the VOUT register. When the VOUT change is complete (internal VREF steps to the goal of VREF), GO_BIT auto-resets to 0. This prevents a false operation of the VOUT scaling.

Write the output voltage (0x00 and 0x01 registers) first, and then write GO_BIT = 1. VOUT changes based on new register setting. GO_BIT resets to 0 when VOUT reaches a new value. The host can read GO_BIT to determine if the VOUT scaling is finished or not.

The VOUT-to-ground discharge function is enabled when GO_BIT is 1. This can help ramp VOUT from high to low in light-load condition.

When GO_BIT is 0, VOUT will not change. When GO_BIT is 1, VOUT changes based on the VOUT register setting. After VOUT scaling finishes, GO_BIT is reset to 0 automatically.
PG_DELAY_EN D[1]
When PG_DELAY_EN D[1] is 0, there is no delay on PG. When PG_DELAY_EN D[1] is 1, PG experiences a 100µs rising delay. The default value is 0.

IOUT_LIM Register
Set the output current limit threshold.

<table>
<thead>
<tr>
<th>Name</th>
<th>IOUT_LIM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Format</td>
<td>Direct, unsigned binary integer</td>
</tr>
<tr>
<td>Bit</td>
<td>7 6 5 4 3 2 1 0</td>
</tr>
<tr>
<td>Access</td>
<td>N/A r/w r/w r/w r/w r/w r/w</td>
</tr>
<tr>
<td>Default value</td>
<td>(3.5A) N/A 70 Integer</td>
</tr>
</tbody>
</table>

IOUT_OC can be calculated with Equation (2):

\[
I_{OUT\_OC} (A) = I_{OUT\_LIM} \times 0.05 \quad (2)
\]

Where IOUT_LIM is a 7-bit unsigned binary integer of IOUT_LIM D[6:0]. The IOUT_OC resolution is 50mA/LSB (maximum value is 6.35A).

The OC pin-to-ground resistor should be 21.5KΩ when using the above IOUT_LIM register. A 22nF (C6) filter capacitor should be added on OC to keep the CC loop stable. The MP8859 supports the I2C setting IOUT_LIM directly. If the CC threshold needs to be changed dynamically after the MP8859 has already entered the CC limit operation state, it is recommended to change the CC threshold step-by-step (e.g.: 50mA per step) instead of changing the current value to the final value directly.

CTL1 Register

<table>
<thead>
<tr>
<th>NAME</th>
<th>BITS</th>
<th>DEFAULT</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN</td>
<td>D[7]</td>
<td>1</td>
<td>I2C controlled turn-on or turn-off of the part. When the external EN pin is low, the converter is off, and the I2C shuts down. When EN is high, the EN bit takes over. 1: part is turned on. Default. 0: part is turned off. I2C register does not reset.</td>
</tr>
<tr>
<td>HICCUP_OCP_OVP</td>
<td>D[6]</td>
<td>1</td>
<td>Over-current and over-voltage protection mode selection. 1: hiccup mode 0: latch-off mode</td>
</tr>
<tr>
<td>DISCHG_EN</td>
<td>D[5]</td>
<td>1</td>
<td>Output discharge enable bit. 1: output discharge function during EN or VIN shutdown 0: no discharge output during shutdown</td>
</tr>
<tr>
<td>MODE</td>
<td>D[4]</td>
<td>1</td>
<td>Default is PWM mode for light load. 0: enables auto PFM/PWM mode 1: sets forced PWM mode</td>
</tr>
<tr>
<td>FREQ</td>
<td>D[3:2]</td>
<td>00</td>
<td>Sets the switching frequency. 00: 500kHz 01, 10, 11: reserved</td>
</tr>
</tbody>
</table>
### CTL2 Register

<table>
<thead>
<tr>
<th>NAME</th>
<th>BITS</th>
<th>DEFAULT</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>LINE DROP COMP</td>
<td>D[7:6]</td>
<td>01</td>
<td>Sets the output voltage compensation vs. the load feature.</td>
</tr>
<tr>
<td></td>
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<td></td>
<td>00: no compensation</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>01: (V_{OUT}) compensates 150mV @ 3A (I_{OUT})</td>
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<td></td>
<td>10: (V_{OUT}) compensates 300mV @ 3A (I_{OUT})</td>
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<td></td>
<td></td>
<td>11: (V_{OUT}) compensates 500mV @ 3A (I_{OUT})</td>
</tr>
<tr>
<td>SS</td>
<td>D[5:4]</td>
<td>11</td>
<td>Sets the output start-up soft-start timer (from 0 to 100%). For 5V output voltage:</td>
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<td></td>
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<td>00: 300µs</td>
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<td></td>
<td></td>
<td></td>
<td>01: 500µs</td>
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<td>10: 700µs</td>
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<td>11: 900µs</td>
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<td>The above compensation amplitude is fixed for any output voltage. Line drop compensation is only enabled for (V_{OUT}) 5V and above.</td>
</tr>
</tbody>
</table>

### Status Register

<table>
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<th>DEFAULT</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: output power is not good</td>
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<td></td>
<td></td>
<td>1: output power is good</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: normal state</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: chip is in over-temperature protection state</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: normal state</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: chip is in-over temperature warning state</td>
</tr>
<tr>
<td>CC_CV</td>
<td>D[4]</td>
<td>X</td>
<td>The chip works in constant-current output mode or constant-voltage output mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: CV mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: CC mode</td>
</tr>
</tbody>
</table>

### Interrupt Register

<table>
<thead>
<tr>
<th>NAME</th>
<th>BITS</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>OTEMPPP_ENTER</td>
<td>D[7]</td>
<td>Over-temperature protection entry indication. When this bit is high, the IC enters thermal shutdown. This bit is not masked, even if setting OTMPSK = 1. OTMPSK = 1 only masks the interrupt pin's output (ALT).</td>
</tr>
<tr>
<td>OTWARNING_ENTER</td>
<td>D[6]</td>
<td>Die temperature early warning entry bit. When this bit is high, the die temperature is higher than 120°C. This bit is not masked, even if setting OTWMSK = 1. OTWMSK = 1 only masks the interrupt pin's output (ALT).</td>
</tr>
<tr>
<td>OC_ENTER</td>
<td>D[5]</td>
<td>Entry of OC or CC current-limit mode. The OC_MSK bit can enable or disable OC.ENTER and OC.RECOVER alert output.</td>
</tr>
<tr>
<td>UVP_FALLING</td>
<td>D[3]</td>
<td>Output voltage is in under-voltage protection.</td>
</tr>
<tr>
<td>OTEMPPP_EXIT</td>
<td>D[2]</td>
<td>Over-temperature protection exit. OTMPSK can mask off the ALT of this bit.</td>
</tr>
<tr>
<td>OTWARNING_EXIT</td>
<td>D[1]</td>
<td>Die temperature early warning exit bit. When the die temperature is lower than 100°C, this bit is set to 1. This bit is not masked, even if setting OTWMSK = 1. OTWMSK = 1 only masks the interrupt pin's output (ALT).</td>
</tr>
<tr>
<td>PG_RISING</td>
<td>D[0]</td>
<td>Output power good rising edge.</td>
</tr>
</tbody>
</table>

These status bits indicate instantaneous value.

This bit is latched once triggered. Write 0xFF to this register to reset the interrupt and ALT pin's state.
### MSK Register

<table>
<thead>
<tr>
<th>NAME</th>
<th>BITS</th>
<th>DEFAULT</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>OTPMSK</td>
<td>D[4]</td>
<td>0</td>
<td>Set OTPMSK = 1 to mask off the OTP alert. OTPMSK = 1 only masks the interrupt pin’s output (ALT). This is not the interrupt register, but is similar for other mask bits.</td>
</tr>
<tr>
<td>OTWMSK</td>
<td>D[3]</td>
<td>0</td>
<td>Masks off the over-temperature warning</td>
</tr>
<tr>
<td>OC_MSK</td>
<td>D[2]</td>
<td>0</td>
<td>Masks off both OC/CC entry and recovery.</td>
</tr>
<tr>
<td>UVP_MSK</td>
<td>D[1]</td>
<td>0</td>
<td>Masks off the output UVP interrupt.</td>
</tr>
<tr>
<td>PG_MSK</td>
<td>D[0]</td>
<td>0</td>
<td>Masks off the PG indication function on ALT.</td>
</tr>
</tbody>
</table>

1: ALT pin does not indicate a PG event
0: ALT indicates a PG rising event.

---

![Figure 11: ALT Behavior of OTP, OT Warning, and OC Recovery](image)

**Figure 11:** ALT Behavior of OTP, OT Warning, and OC Recovery
**APPLICATION INFORMATION**

**Selecting the Inductor**

In a buck-boost topology circuit, the inductor must support buck applications with the maximum input voltage and boost applications with the minimum input voltage. Two critical inductance values can be determined according to the buck mode and boost mode current ripple using Equation (2) and Equation (3):

\[
L_{\text{MIN-BUCK}} = \frac{V_{\text{OUT}} \times (V_{\text{IN(MAX)}} - V_{\text{OUT}})}{V_{\text{IN(MAX)}} \times F_{\text{REQ}} \times \Delta I_L}
\]  
(2)

\[
L_{\text{MIN-BOOST}} = \frac{V_{\text{IN(MIN)}} \times (V_{\text{OUT}} - V_{\text{IN(MIN)}})}{V_{\text{OUT}} \times F_{\text{REQ}} \times \Delta I_L}
\]  
(3)

Where \( F_{\text{REQ}} \) is the switching frequency, and \( \Delta I_L \) is the peak-to-peak inductor current ripple. As a rule of thumb, the peak-to-peak ripple can be set to 10% - 40% of the inductor current. The minimum inductor value for the application is the higher than both the Equation (2) and Equation (3) results.

In addition to the inductance value, the inductor must support the peak current based on Equation (4) and Equation (5) to avoid saturation:

\[
I_{\text{PEAK-BUCK}} = I_{\text{OUT}} + \frac{V_{\text{OUT}} \times (V_{\text{IN(MAX)}} - V_{\text{OUT}})}{2 \times V_{\text{IN(MAX)}} \times F_{\text{REQ}} \times L}
\]  
(4)

\[
I_{\text{PEAK-BOOST}} = \frac{V_{\text{OUT}} \times I_{\text{OUT}}}{\eta \times V_{\text{IN(MIN)}}} + \frac{V_{\text{IN(MIN)}} \times (V_{\text{OUT}} - V_{\text{IN(MIN)}})}{2 \times V_{\text{OUT}} \times F_{\text{REQ}} \times L}
\]  
(5)

Where \( \eta \) is the estimated efficiency of the MP8859.

**Input and Output Capacitor Selection**

It is recommended to use ceramic capacitors plus an electrolytic capacitor for input and output capacitors to filter the input and output ripple current and achieve stable operation.

Since the input capacitor absorbs the input switching current, it requires sufficient capacitance. For most applications, a 100µF electrolytic capacitor and a 22µF ceramic capacitor are sufficient.

The output capacitor stabilizes the DC output voltage. Low ESR capacitors and a sufficient capacitor value are recommended to limit the output voltage ripple. Considering the ceramic DC voltage derating, if the output voltage is less than 12V, the minimum \( C_{\text{OUT}} \) should be 22µFx5 ceramic. If the output voltage is higher than 12V, use a 100µF low ESR (≤80mΩ) aluminum electrolytic or polymer capacitor and two 10µF ceramic capacitors.

The input and output ceramic capacitors must be placed as close as possible to the device.
PCB Layout Guidelines (9)

Efficient PCB layout is critical for stable operation and thermal dissipation. For best results, refer to Figure 12 and follow the guidelines below.

1. Place the ceramic $C_{\text{IN}}$ and $C_{\text{OUT}}$ capacitor close to the IC’s VIN-to-GND and OUT-to-GND pins, respectively.
2. Use a large copper plane for PGND.
3. Add multiple vias to improve thermal dissipation.
4. Connect AGND to PGND.
5. Use short, direct, and wide traces to connect OUT.
6. Add vias under the IC and routing the OUT trace on both PCB layers (highly recommended).
7. Use a large copper plane for SW1 and SW2.
8. Place the VCC decoupling capacitor as close to VCC as possible.

NOTES:

9) The recommended layout is based on the typical application circuits in Figure 13 and Figure 14.
TYPICAL APPLICATION CIRCUITS

Figure 13: Typical Application Circuit for 1 - 20V_{\text{OUT}}
NOTE: Refer to the recommended maximum I_{\text{OUT}} vs. V_{\text{IN}} and V_{\text{OUT}} with 22μF ceramic C_{\text{OUT}} capacitor curve on page 9.

Figure 14: Typical Application Circuit for 1 - 12V_{\text{OUT}}
NOTE: Refer to the recommended maximum I_{\text{OUT}} vs. V_{\text{IN}} and V_{\text{OUT}} with 22μF ceramic C_{\text{OUT}} capacitor curve on page 9.
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MP8859 – 22V \( V_{\text{IN}} \), 3A \( I_{\text{OUT}} \), INTEGRATED BUCK-BOOST WITH I\(^2\)C INTERFACE

PACKAGE INFORMATION

QFN-16 (3mmx3mm)

TOP VIEW

BOTTOM VIEW

SIDE VIEW

NOTE:
1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

RECOMMENDED LAND PATTERN