MP8796

16V, 30A, Scalable, Configurable-Frequency, Synchronous Step-Down Converter with Adjustable Current Limit and Remote Sense

DESCRIPTION

The MP8796 is a fully integrated, high-frequency, synchronous step-down converter. It offers a very compact solution that can achieve up to 30A of output current (I_{OUT}) across a wide 4V to 16V input voltage (V_{IN}) range, with excellent load and line regulation. The MP8796 operates at high efficiency across a wide I_{OUT} load range.

MPS's proprietary multiphase constant-on-time (MCOT) control that provides fast transient response and eases loop stabilization. The MCOT scheme allows for multiple MP8796s to be connected in parallel, with excellent current sharing and phase interleaving for high-current applications.

The switching frequency (f_{SW}) can be set between 400kHz and 1000kHz. This maintains a constant f_{SW}, regardless of V_{IN} and the output voltage (V_{OUT}).

During start-up, V_{OUT} ramps up in a controlled manner using an external capacitor. An open-drain power good (PG) signal indicates whether V_{OUT} is within its nominal voltage range.

Full protection features include over-current protection (OCP), over-voltage protection (OVP), and over-temperature protection (OTP) with selectable hiccup mode or latch-off mode.

The MP8796 requires a minimal number of readily available, standard external components, and is available in a TQFN-25 (4mmx5mm) package.

FEATURES

- Wide 4V to 16V Operating Input Voltage (V_{IN}) Range
- Wide 3V to 16V Operating V_{IN} Range with External 3.3V VCC Bias
- Up to 30A Continuous Output Current (I_{OUT}) per Phase
- Adjustable Current Limit (I_{LIMIT})
- 850µA Quiescent Current (I_Q)
- Low $R_{DS(ON)}$ Integrated Power MOSFETs
- Lossless and Accurate On-Die Current-Sensing
- Adaptive Constant-On-Time (COT) Control for Ultrafast Transient Response
- Stable with Zero-ESR Output Capacitor
- Remote Sense
- Scalable Multiphase Operation
- 400kHz to 1000kHz Selectable Switching Frequency (f_{SW})
- Configurable Soft-Start Time (t_{SS})
- Selectable Pulse-Frequency Modulation (PFM) Mode and Forced Continuous Conduction Mode (FCCM)
- Selectable Internal Ramp Compensation
- Over-Current Protection (OCP), Over-Voltage Protection (OVP), and Over-Temperature with Selectable Hiccup Mode or Latch-Off Mode
- Available in a TQFN-25 (4mmx5mm) Package

APPLICATIONS

- Multifunctional Printers
- Flat-Panel Televisions and Monitors
- Access Points and Routers
- Optical Modules

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TYPICAL APPLICATION

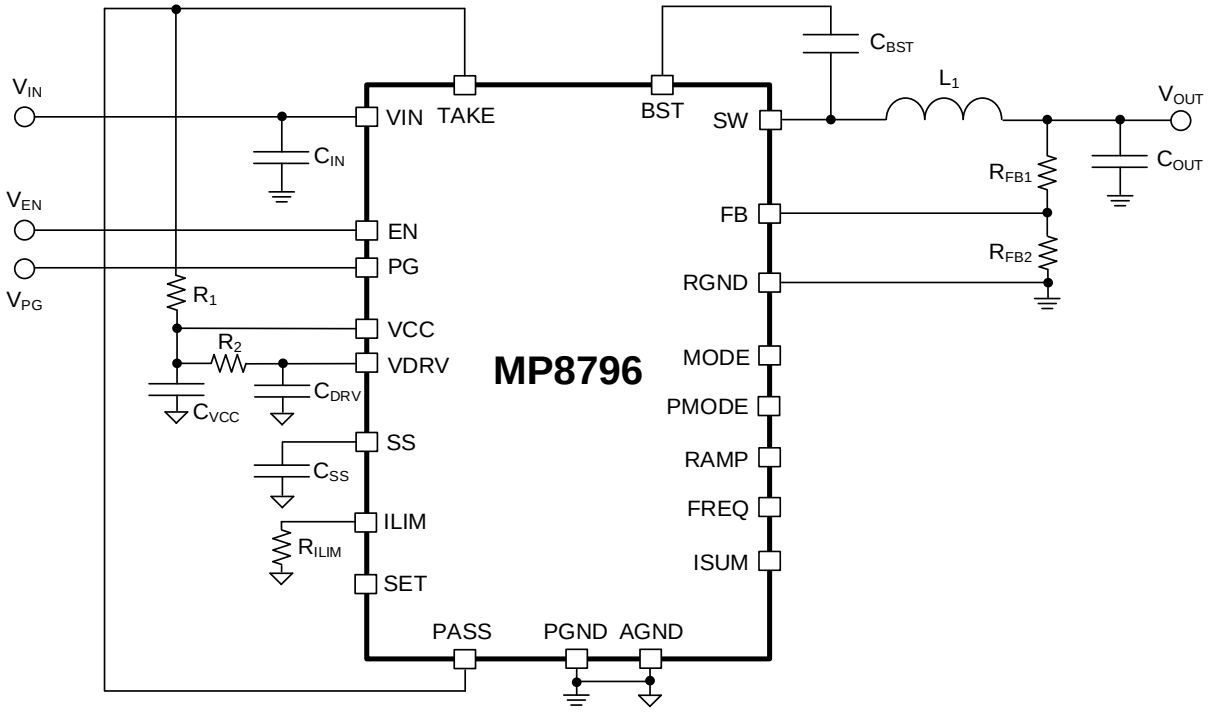

Figure 1: Single-Phase Operation

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TYPICAL APPLICATION *(continued)*

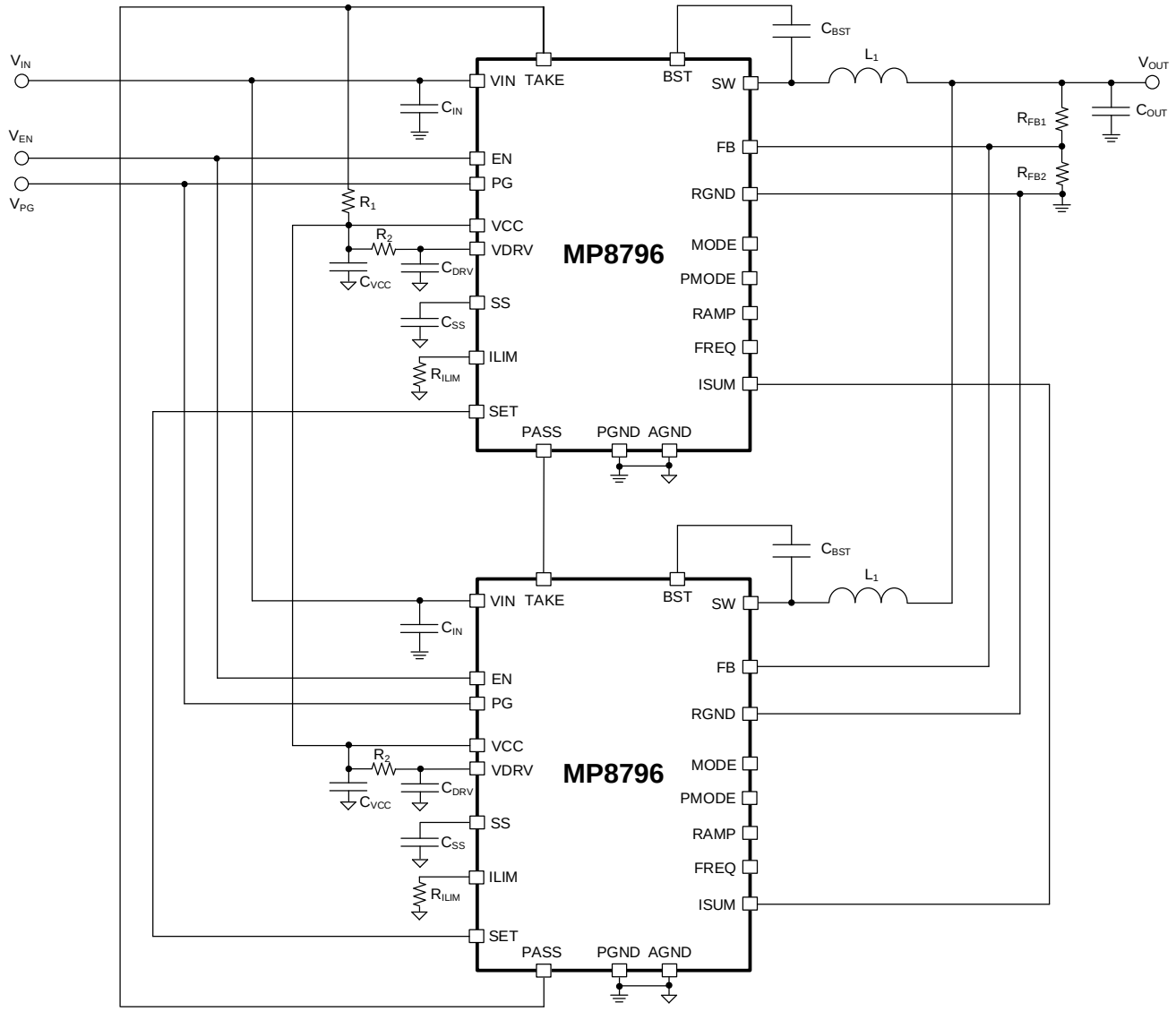

Figure 2: Dual-Phase Operation

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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP8796GVT	TQFN-25 (4mmx5mm)	*See Below*	*1*

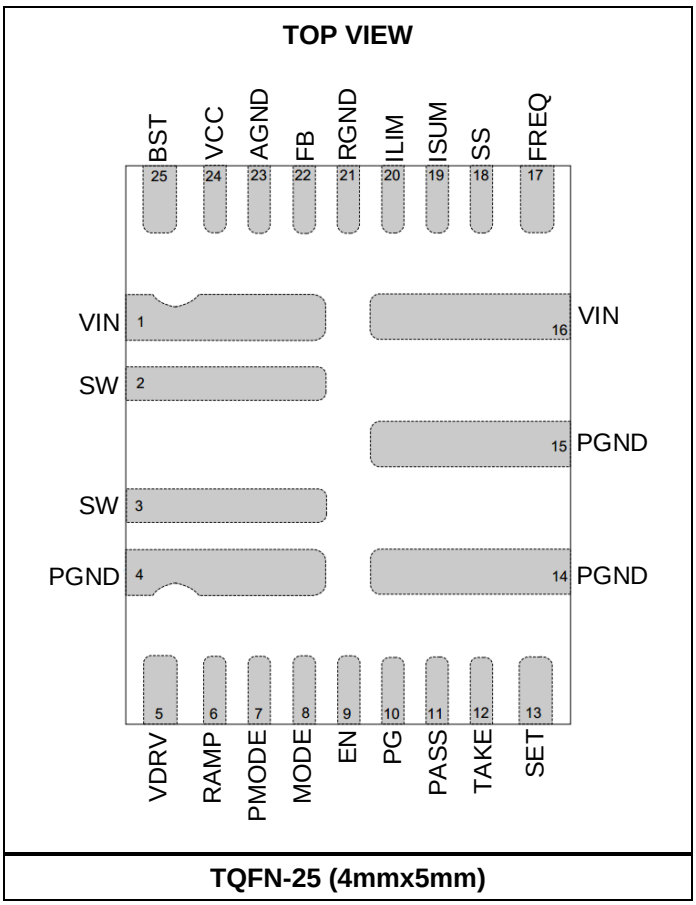
* For Tape & Reel, add suffix -Z (e.g. MP8796GVT-Z).

TOP MARKING

MPSYWW
MP8796
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP8796: Part number
LLLLLL: Lot number

PACKAGE REFERENCE



TQFN-25 (4mmx5mm)

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PIN FUNCTIONS

Pin #	Name	Description
1, 16	VIN	**Supply voltage.** The VIN pin supplies power to internal high-side MOSFET (HS-FET) and converter. An input capacitor (C_{IN}) is required to decouple the input rail. Use wide PCB traces and multiple vias to make the VIN connection. See the PCB Layout Guidelines section on page 26 for more details.
2, 3	SW	**Switch output**. Connect the SW pin to the inductor and bootstrap (BST) capacitor (C_{BST}). The SW voltage (V_{SW}) is pulled up to the VIN voltage (V_{IN}) by the HS-FET during the pulse-width modulation (PWM) duty cycle on time (t_{ON}). V_{SW} is pulled negative by the inductor current (I_L) during the PWM off time (t_{OFF}). Use wide PCB traces to make the SW connection.
4, 14, 15	PGND	**System ground.** The PGND pin is the reference ground of the regulated output voltage (V_{OUT}). PGND requires careful consideration during PCB layout design. Use wide PCB traces to make the PGND connection.
5	VDRV	**3.3V driver power supply decoupling input pin.** Place a ≥1µF ceramic decoupling capacitor as close to the VDRV pin as possible to decouple VDRV. X7R or X5R grade dielectric ceramic capacitors are recommended. VDRV accepts an external 3.3V bias. If there is not an external 3.3V bias, connect the VDRV and VCC pins via a 2.2Ω to 10Ω resistor.
6	RAMP	**Internal ramp compensation selection.** The RAMP pin selects the internal ramp compensation (15mV or 44mV). Pull the RAMP pin low to set the internal ramp compensation to 15mV. Pull RAMP high to set the internal ramp compensation to 44mV. Do not float RAMP.
7	PMODE	**Protection mode selection.** The PMODE pin selects the protection mode (hiccup or latch-off) for over-current protection (OCP), over-voltage protection (OVP), and over-temperature protection (OTP). Pull PMODE high to have the converter operate in hiccup mode if OCP, OVP, or OTP is triggered. Pull PMODE low to have it operate in latch-off mode if OCP, OVP, or OTP is triggered. Do not float PMODE.
8	MODE	**Operation mode selection.** Pull MODE low to have the converter operate in pulse-frequency modulation (PFM) mode at light loads. Pull MODE high to have it operate in PWM mode across the full load range. Do not float MODE.
9	EN	**Enable pin.** Pull the EN pin high to turn the converter on; pull EN low to turn it off. Do not float EN.
10	PG	**Power good output.** The PG pin is an open drain output. A pull-up resistor connected to a DC voltage is required to indicate whether V_{OUT} is within the nominal voltage range. If V_{OUT} exceeds 90% of its nominal voltage, then PG is pulled high. There is a delay between when PG transitions from low to high. PG should be pulled high to ensure proper operation. PG has a slave fault-detection feature. See the Power Good (PG) section on page 24 for more details.
11	PASS	**RUN signal pass.** The PASS pin passes the RUN signal to the next phase.
12	TAKE	**RUN signal receive.** The TAKE pin receives the RUN signal from the previous phase. This is used for master detection during initial start-up. Pull TAKE high via a 10kΩ resistor for master phase. Connect TAKE to the PASS pin of the previous phase for slave phase.
13	SET	**PWM signal.** The SET signal turns the HS-FET on once the RUN signal is present. Tie the SET pins of all phases together for multi-phase operation.
17	FREQ	**Switching frequency.** Connect a resistor between the FREQ and AGND pins to set the switching frequency (f_{SW}) between 400kHz and 1MHz.

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PIN FUNCTIONS *(continued)*

Pin #	Name	Description
18	SS	**Soft-start input.** Place a ceramic decoupling capacitor (C_{SS}) as close to the SS pin as possible to decouple SS. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics. The C_{SS} value determines the soft-start time (t_{SS}).
19	ISUM	**Current-sense output.** Float ISUM for single-phase operation. Tie the ISUM pins of all phases together for current sharing in multi-phase operation.
20	ILIM	**Valley current limit set pin.** Connect a resistor between the ILIM and AGND pins to set the valley current limit (I_{LIMIT_VALLEY}).
21	RGND	**Output voltage sense negative return.** Tie the RGND pin directly to the ground-sense point of the load. Connect RGND to AGND if remote sense is not used.
22	FB	**Feedback (differential remote sense positive input).** To set V_{OUT}, connect an external resistor divider (tapped to the FB pin) between the output and RGND. It is recommended to place this resistor divider as close to FB as possible.
23	AGND	**Analog ground.** Select the AGND pin as the control circuit reference point.
24	VCC	**Internal 3.3V LDO output.** The VCC pin supplies power to the analog and digital control circuitry. Place a ≥1µF ceramic decoupling capacitor as close to VCC as possible to decouple VCC. X7R or X5R grade dielectric ceramic capacitors are recommended. Connect the VCC pins of all phases together for multi-phase operation. For applications with a low V_{IN}, a VCC bias is required.
25	BST	**Bootstrap.** Connect a capacitor between the SW and BS pins to form a floating supply across the HS-FET driver.

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ABSOLUTE MAXIMUM RATINGS (1)

Input voltage (V_{IN}) 18V
V_{SW} (DC) .....-0.3 V to +18.3V
V_{SW} (25ns) (2).....-5V to +25V
V_{BST} ..... V_{SW} + 4V
V_{BST} - V_{SW} (25ns) (2)..... 5V
V_{CC}, V_{DRV} 4.5V
All other pins .....-0.3V to +4.3V
Junction temperature .....170°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +170°C

ESD Ratings

Human body model (HBM) .....±1KV
Charged device model (CDM) .....±2KV

Recommended Operating Conditions 3)

Input voltage (V_{IN}) .....4V to 16V
Output voltage (V_{OUT}).....0.6V to 6V
External V_{DRV} bias.....2.9V to 3.6V
Other signal pins.....-0.3V to +3.6V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance

TQFN-25 (4mmx5mm) (4) (5)
θ_{JA} (6)..... 21.9°C/W
θ_{JC_TOP} (7) (9)..... 0.6°C/W
θ_{JB} (8) (10) ..... 4.5°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Specified by design. Measured by using differential oscilloscope probe.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on the EV8796-VT-01B (7.18cmx7.62cm), 6-layer PCB, 2oz copper thickness, without airflow.
5) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by PD (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause an excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
6) θ_{JA} is the thermal resistance from the junction to the ambient temperature.
7) θ_{JC_TOP} is the thermal characterization parameter from the junction to the top of the package.
8) θ_{JB} is the thermal characterization parameter from the junction to the board.
9) θ_{JC_TOP} estimates the junction temperature (T_J) in the real system when $T_J = \theta_{JC_TOP} \times P_{LOSS} + T_{CASE_TOP}$. Where P_{LOSS} is the chip's entire loss during real application, and T_{CASE_TOP} is the case top's temperature.
10) θ_{JA} estimates T_J in the real system, when $T_J = \theta_{JB} \times P_{LOSS} + T_{BOARD}$. Where P_{LOSS} is the chip's entire loss during real application, and T_{BOARD} is case top's temperature.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to 125°C (11), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VIN Supply Current						
Input current	I_{IN}	V_{EN} = 2V, V_{FB} = 0.65V, R_{TAKE} = 100kΩ, connected to VCC R_{FREQ} = 30kΩ, connected to PGND R_{ILIM} = 60.4kΩ, connected to PGND		0.85		mA
MOSFET						
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)_HS}$			4.4		mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)_LS}$			1.5		mΩ
HS-FET switch leakage	$I_{SW_LKG_HS}$	V_{SW} = 0V, T_J = 25°C		0.1	1	μA
LS-FET switch leakage	$I_{SW_LKG_LS}$	V_{SW} = 12V, T_J = 25°C		1	10	μA
Output Current (I_{OUT}) Limit						
Valley current limit	I_{LIMIT_VALLEY}	R_{ILIM} = 60.4kΩ		30		A
LS-FET negative current limit	I_{LIMIT_NEG}			-13		A
Switching Frequency (f_{SW}) and Timer						
Switching frequency	f_{SW}	R_T = 30kΩ		800		kHz
Minimum on time (12)	t_{ON_MIN}	f_{SW} = 800kHz, V_{OUT} = 0.6V		50		ns
Minimum off time (12)	t_{OFF_MIN}			220		ns
Output Over-Voltage Protection (OVP) and Under-Voltage Protection (UVP)						
OVP threshold	V_{OVP}		116	120	124	% of V_{REF}
UVP Threshold	V_{UVP}		70	74	78	% of V_{REF}
Enable (EN)						
EN input high voltage	V_{EN_HIGH}		2.15			V
EN input low voltage	V_{EN_LOW}				1.2	V
Feedback (FB) Voltage						
FB accuracy			594	600	606	mV
Soft Start (SS)						
Soft-start current	I_{SS}		15	20	25	μA
Error Amplifier (EA)						
FB current	I_{FB}	V_{FB} = 0.65V		50	100	nA
Soft Shutdown						
Soft-shutdown discharge MOSFET on resistance	$R_{DS(ON)_DISCH}$	T_J = 25°C		60	120	Ω

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to 125°C (11), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Under-Voltage Lockout (UVLO) Protection						
VCC UVLO rising threshold	$V_{CC_UVLO_RISING}$		2.6	2.75	2.9	V
VCC UVLO falling threshold	$V_{CC_UVLO_FALLING}$		2.3	2.45	2.6	V
VCC voltage	V_{CC}		3.1	3.25	3.4	V
VDRV UVLO rising threshold	$V_{DRV_UVLO_RISING}$		2.55	2.75	2.95	V
VDRV UVLO falling threshold	$V_{DRV_UVLO_FALLING}$		2.15	2.35	2.55	V
Power Good (PG)						
PG high threshold	V_{PG_HIGH}	V_{FB} rising	88.5	92.5	96.5	% of V_{REF}
PG low threshold	$V_{PG_LOW_RISING}$	V_{FB} rising	116	120	124	% of V_{REF}
	$V_{PG_LOW_FALLING}$	V_{FB} falling	70	74	78	% of V_{REF}
PG sink current capability	V_{PG}	I_{PG} = 10mA			0.3	V
PG leakage current	I_{PG_LEAK}	V_{PG} = 3V, T_J = 25°C		1.5	2.5	µA
PG low-level output voltage	$V_{PG_LOW_100}$	V_{IN} = 0V, T_J = 25°C, V_{PG} is pulled up to 3.3V via a 100kΩ resistor		600	720	mV
	$V_{PG_LOW_10}$	V_{IN} = 0V, T_J = 25°C, V_{PG} is pulled up to 3.3V via a 10kΩ resistor		700	820	mV
Thermal Protection						
Thermal shutdown threshold (12)				145		°C
Thermal shutdown hysteresis (12)				30		°C

Notes:

11) Guaranteed by sample characterization. Tested during parameter characterization. Not tested in production.
12) Guaranteed by sample characterization. Not tested in production.

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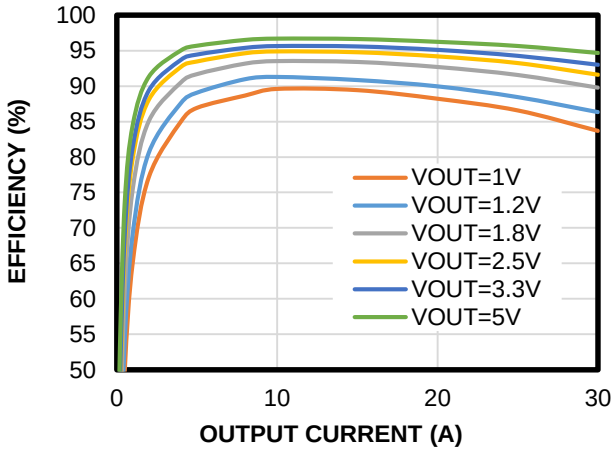
TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1.2V, L = 220nH, T_A = 25°C, unless otherwise noted.

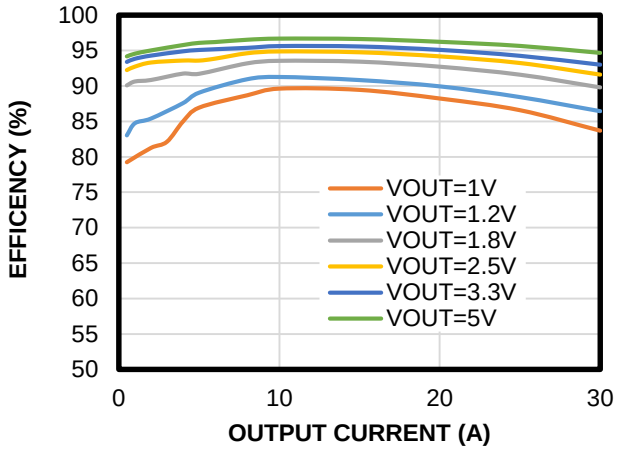
Efficiency vs. Output Current

PWM mode, DCR = 0.17mΩ



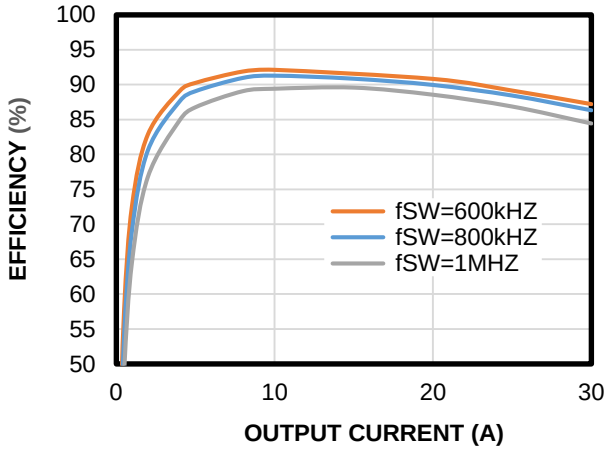
Efficiency vs. Output Current

PFM mode, DCR=0.17mΩ



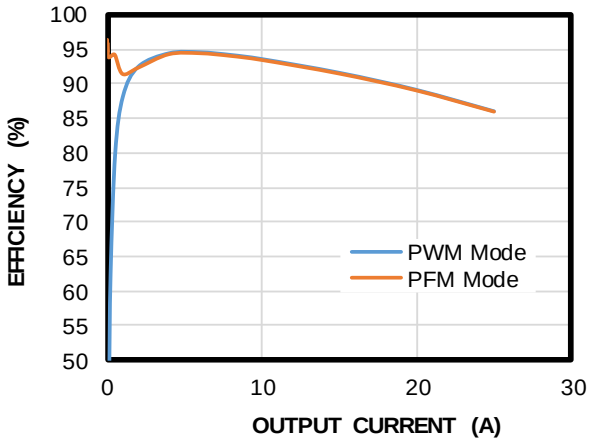
Efficiency vs. Output Current

V_{OUT} = 1.2V, DCR = 0.17mΩ

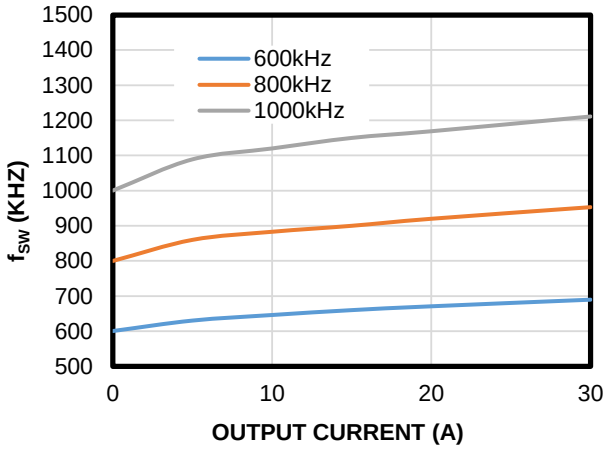


Efficiency Vs. Output Current

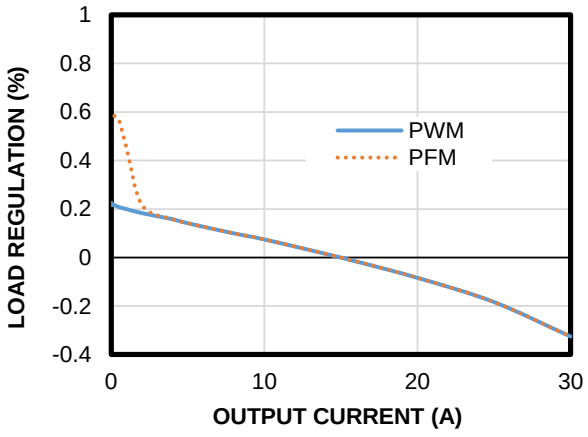
V_{IN} = 3.3V, V_{OUT} = 1.2V, DCR = 0.325mΩ, external 3.3V VCC bias



Switching Frequency vs. Output Current



Load Regulation



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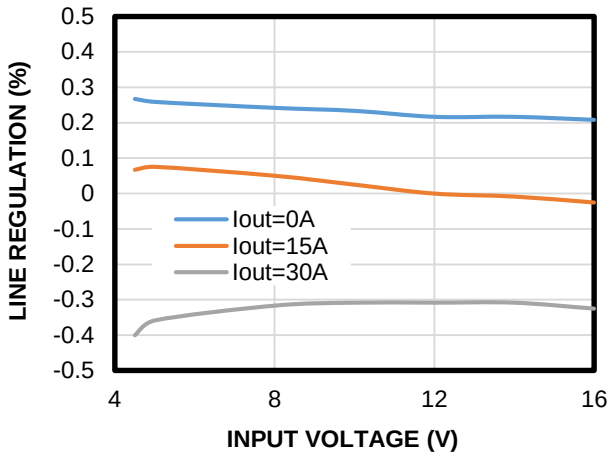
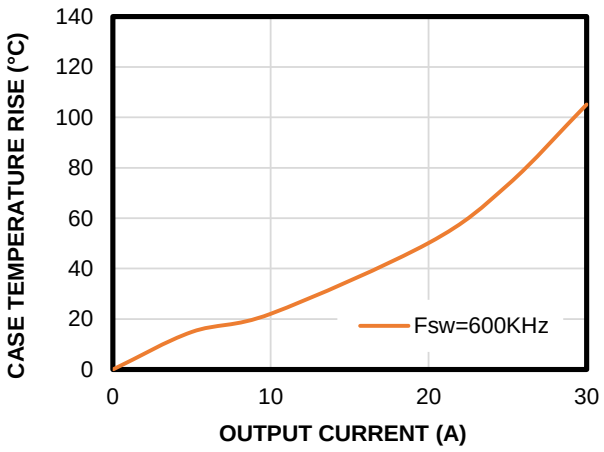
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.2V, L = 220nH, T_A = 25°C, unless otherwise noted.

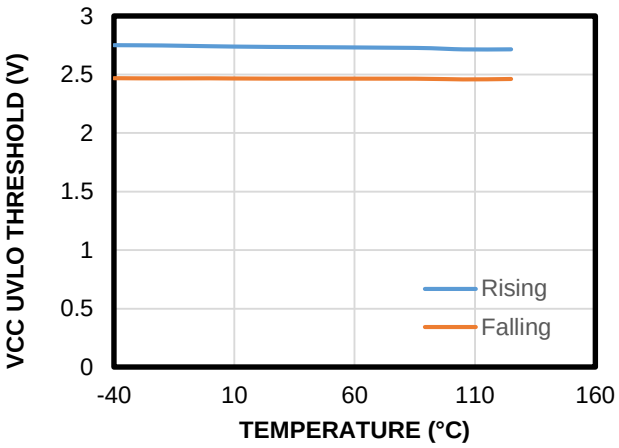
Line Regulation



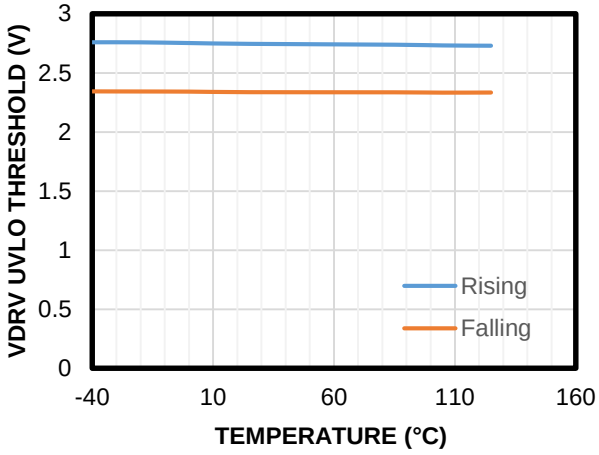
Case Temperature Rise



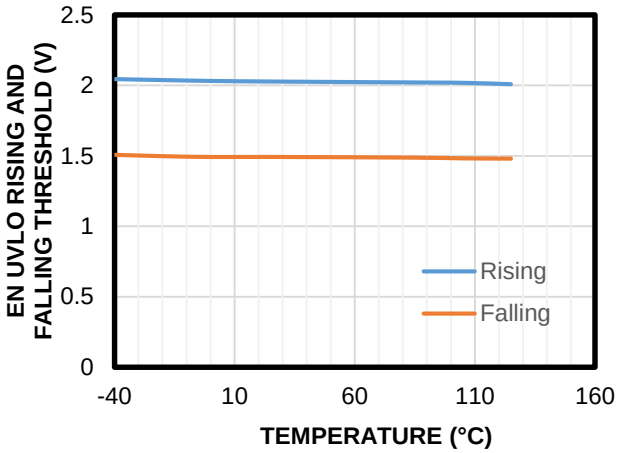
VCC UVLO Threshold vs. Temperature



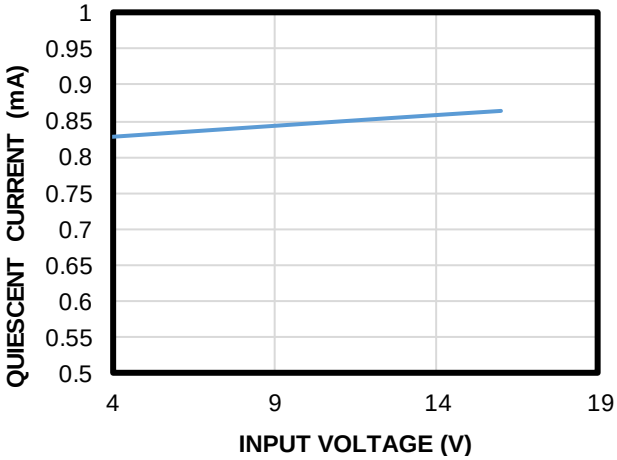
VDRV UVLO Threshold vs. Temperature



EN UVLO Threshold vs. Temperature



Quiescent Current vs. Input Voltage



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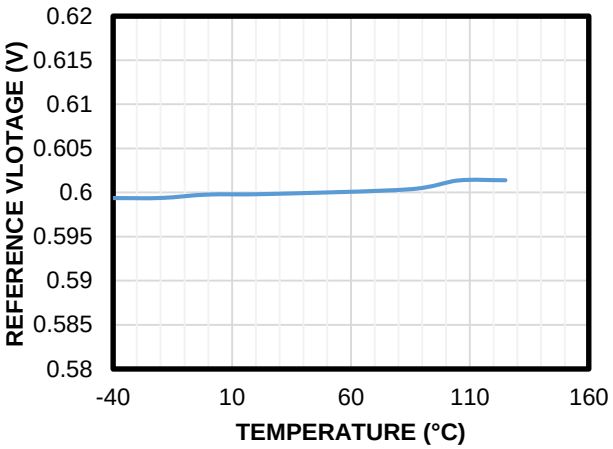
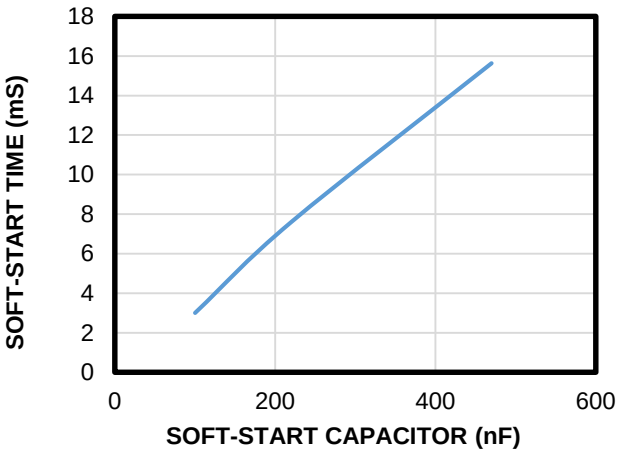
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.2V, L = 220nH, T_A = 25°C, unless otherwise noted.

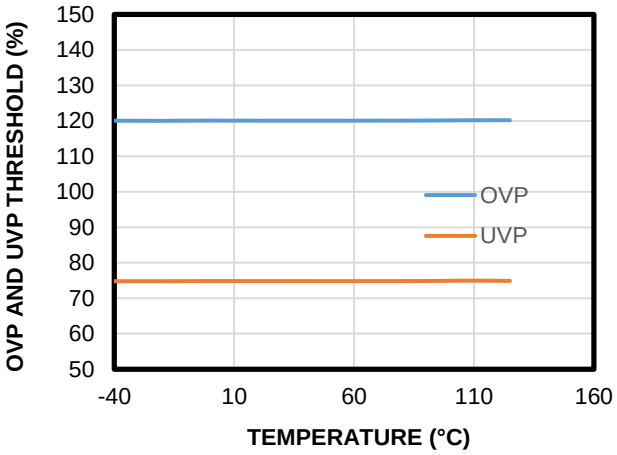
Reference Voltage vs. Temperature



Soft-Start Time vs. Soft-Start Capacitance



OVP and UVP Threshold vs. Temperature



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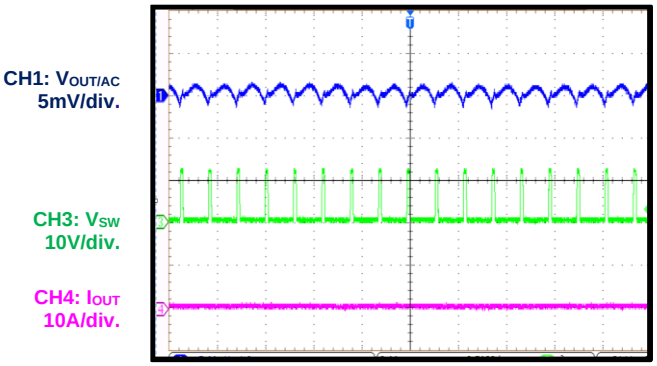
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1.2V, L = 220nH, C_{OUT} = 330µF x 2 POSCAP + 47µF x 5 Ceramic, T_A = 25°C, unless otherwise noted.

Output Voltage Ripple

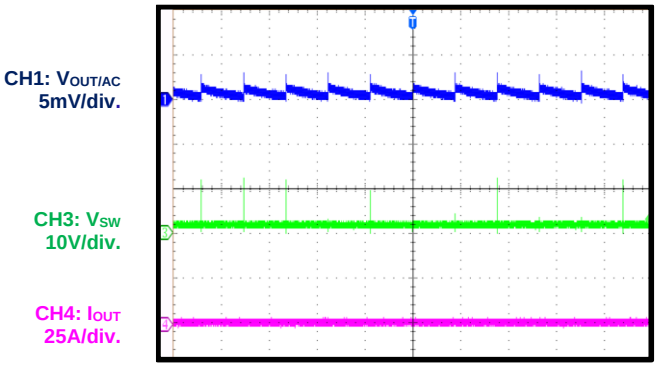
I_{OUT} = 0A, PWM mode



2µs/div.

Output Voltage Ripple

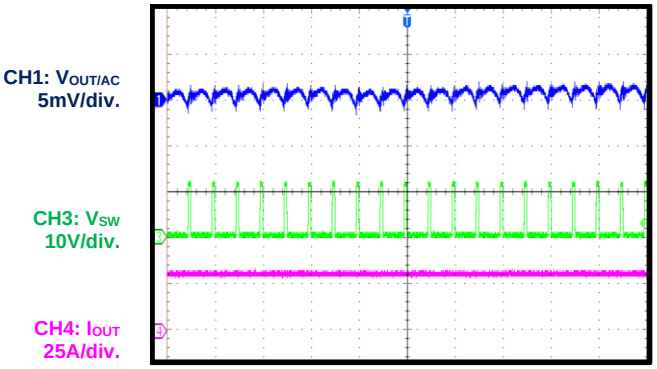
I_{OUT} = 0A, PFM mode



20ms/div.

Output Voltage Ripple

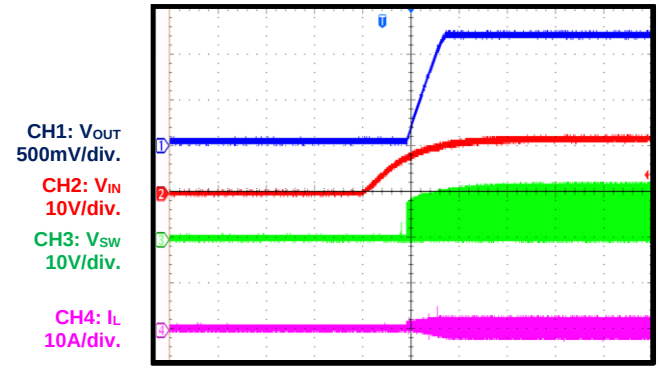
I_{OUT} = 30A



2µs/div.

Start-Up through VIN

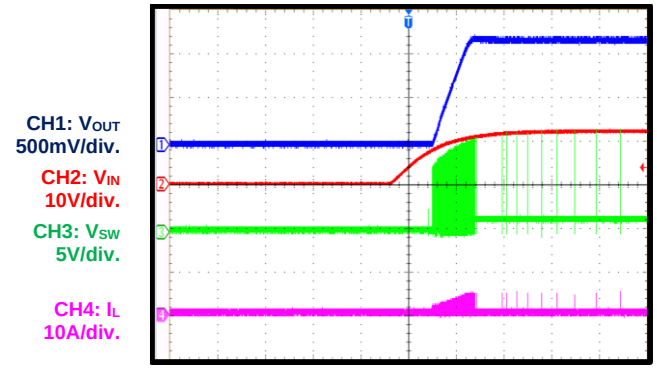
I_{OUT} = 0A, PWM mode



4ms/div.

Start-Up through VIN

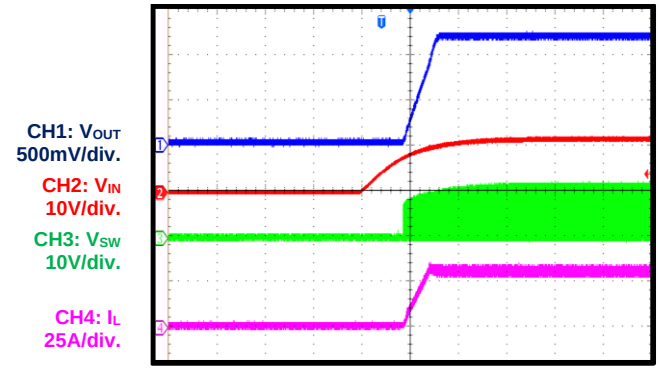
I_{OUT} = 0A, PFM mode



4ms/div.

Start-Up through VIN

I_{OUT} = 30A



4ms/div.

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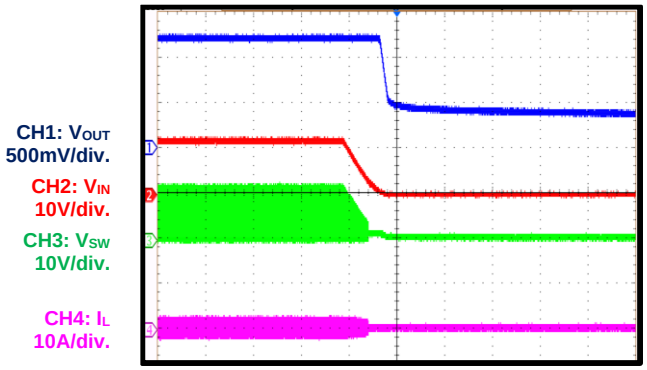
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.2V, L = 220nH, C_{OUT} = 330µF x 2 POSCAP + 47µF x 5 Ceramic, T_A = 25°C, unless otherwise noted.

Shutdown through VIN

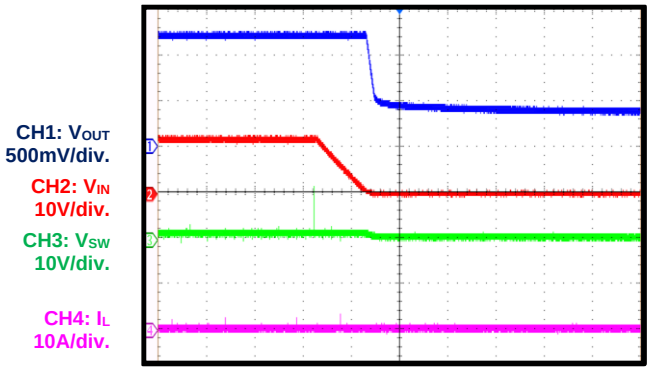
I_{OUT} = 0A, PWM mode



100ms/div.

Shutdown through VIN

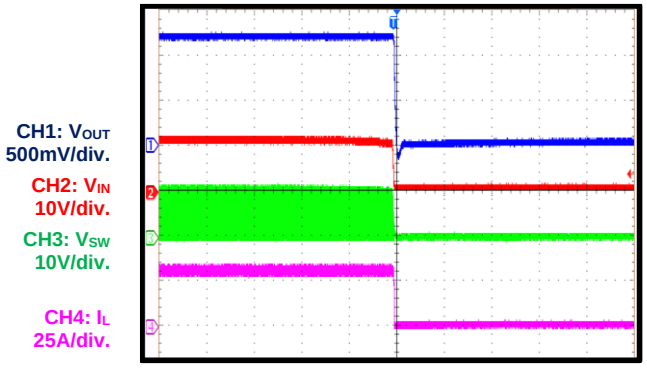
I_{OUT} = 0A, PFM mode



100ms/div.

Shutdown through VIN

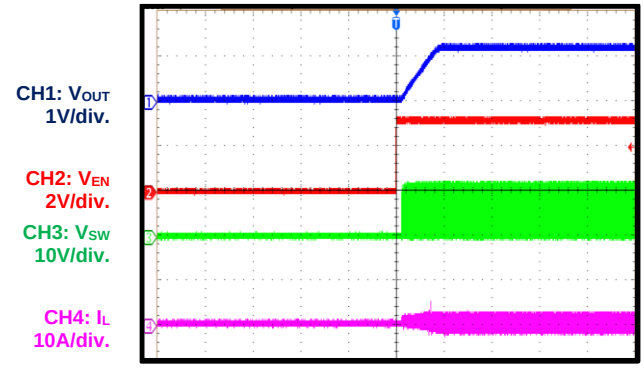
I_{OUT} = 30A



1ms/div.

Start-Up through EN

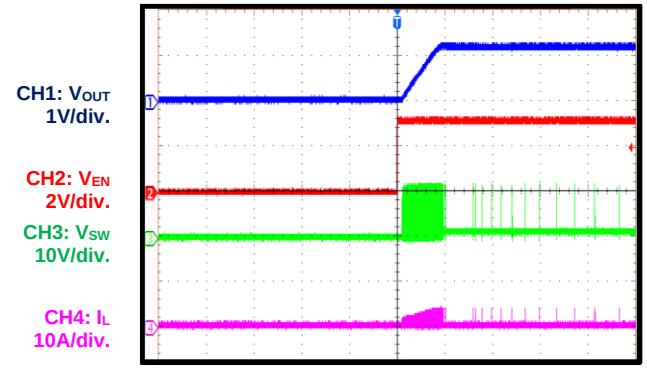
I_{OUT} = 0A, PWM mode



4ms/div.

Start-Up through EN

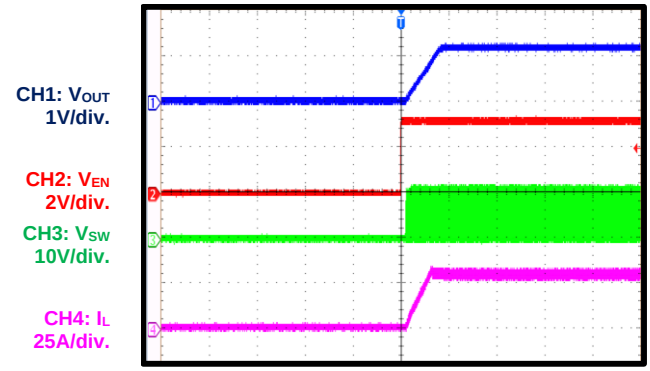
I_{OUT} = 0A, PFM mode



4ms/div.

Start-Up through EN

I_{OUT} = 30A



4ms/div.

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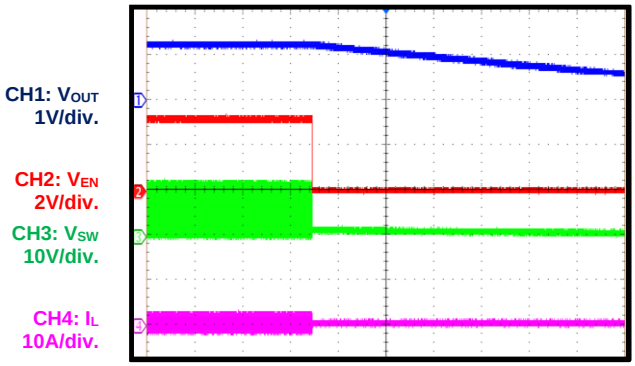
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.2V, L = 220nH, C_{OUT} = 330µF x 2 POSCAP + 47µF x 5 Ceramic, T_A = 25°C, unless otherwise noted.

Shutdown through EN

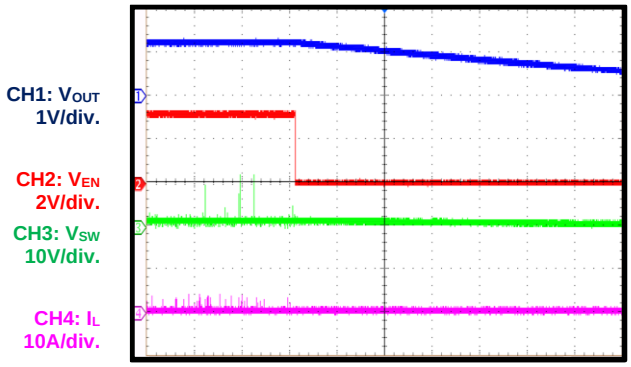
I_{OUT} = 0A, PWM mode



400ms/div.

Shutdown through EN

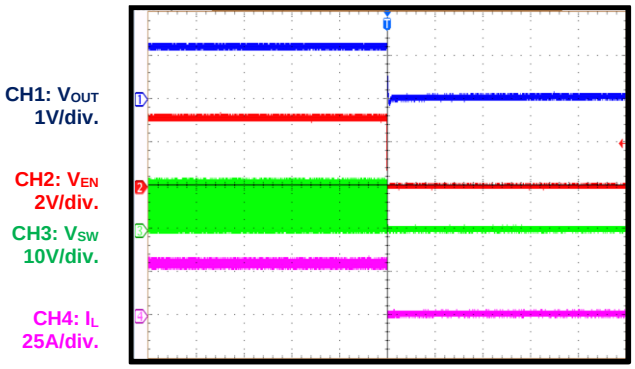
I_{OUT} = 0A, PFM mode



400ms/div.

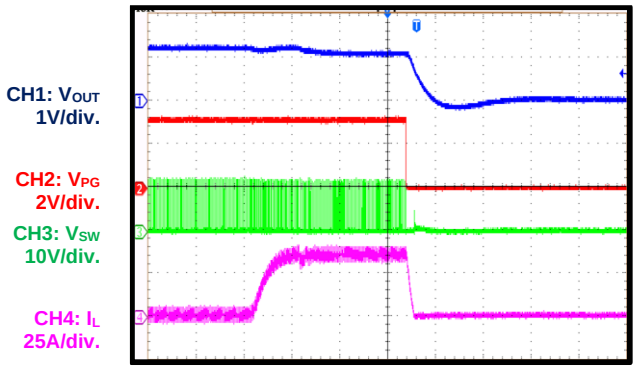
Shutdown through EN

I_{OUT} = 30A



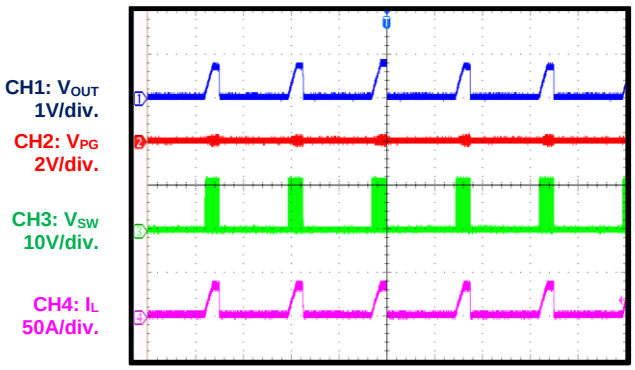
2ms/div.

SCP Entry



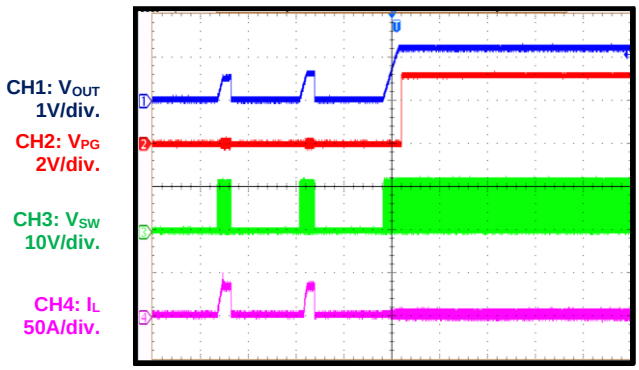
80µs/div.

SCP Steady State



10ms/div.

SCP Recovery



10ms/div.

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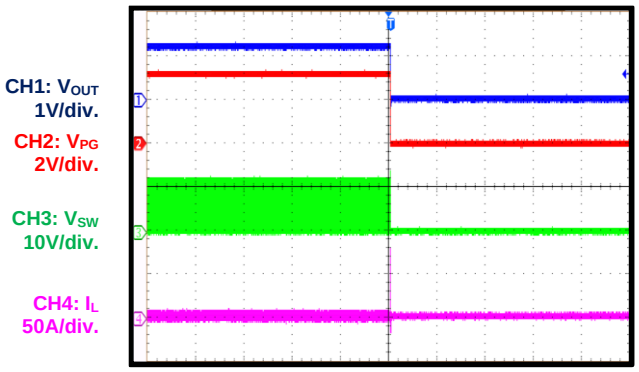
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.2V, L = 220nH, C_{OUT} = 330µF x 2 POSCAP + 47µF x 5 Ceramic, T_A = 25°C, unless otherwise noted.

SCP Entry

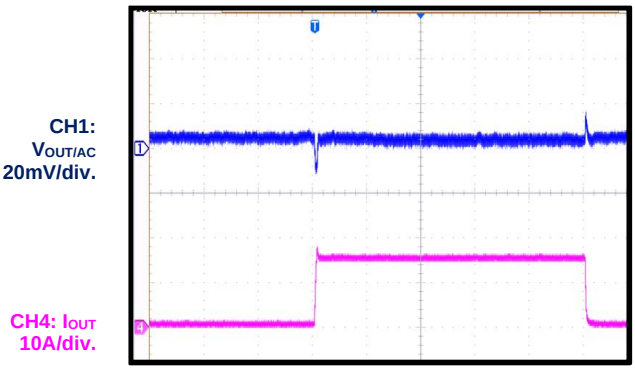
Latch-off mode



20ms/div.

Load Transient

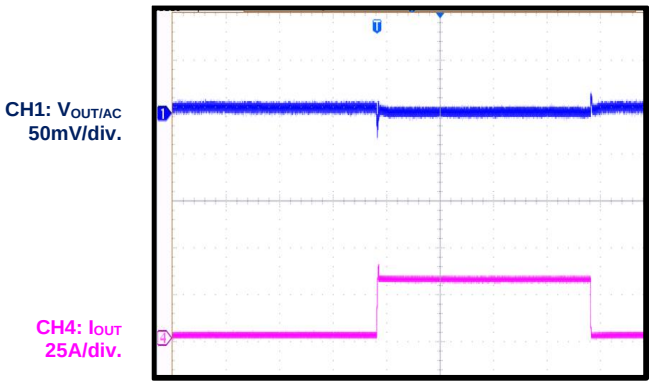
I_{OUT} = 0A to 15A, 2.5A/µs slew rate



400µs/div.

Load Transient

I_{OUT} = 0A to 30A, 2.5A/µs slew rate



2ms/div.

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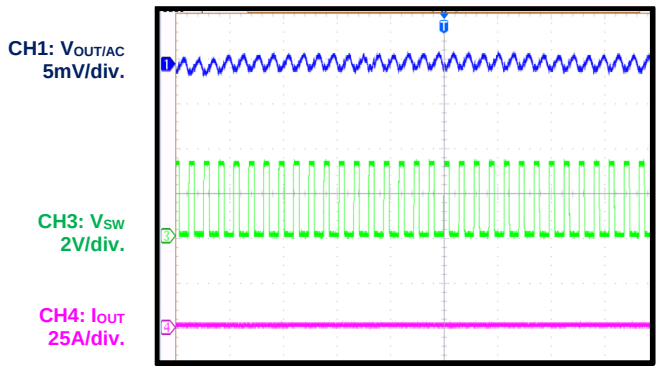
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 1.2V , V_{CC} = 3.3V, L = 220nH, C_{OUT} = 330µF x 2 POSCAP + 47µF x 5 Ceramic, T_A = 25°C, unless otherwise noted.

Output Voltage Ripple

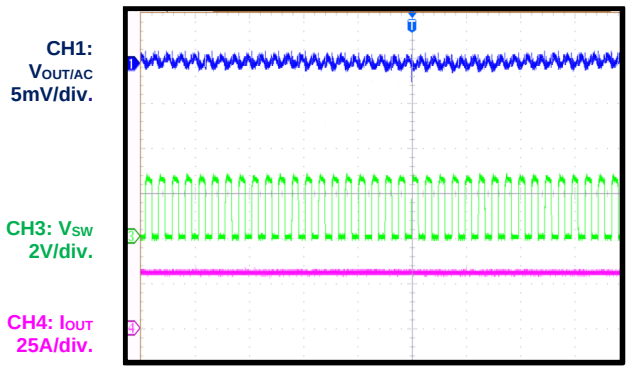
External 3.3V VCC bias, V_{IN} = 3.3V, I_{OUT} = 0A, PWM mode



4µs/div.

Output Voltage Ripple

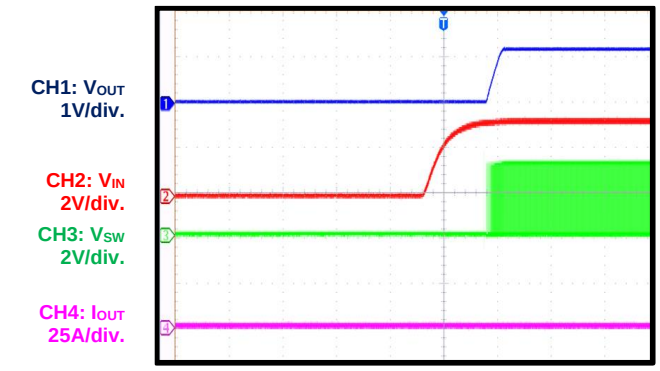
External 3.3V VCC bias, V_{IN} = 3.3V, I_{OUT} = 30A, PWM mode



4µs/div.

Start-Up through VIN

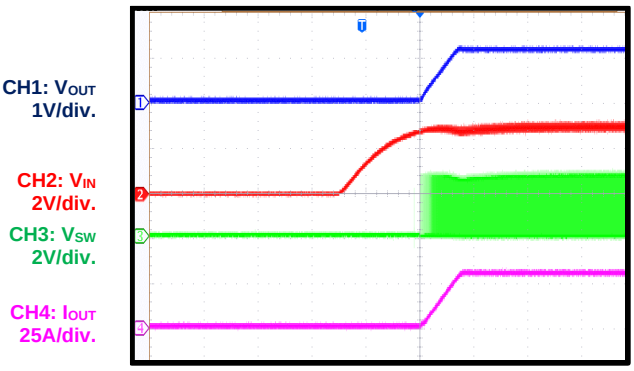
External 3.3V VCC bias, V_{IN} = 3.3V, I_{OUT} = 0A, PWM mode



10ms/div.

Start-Up through VIN

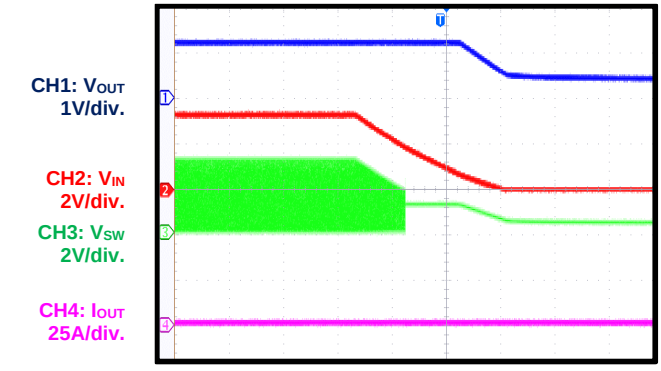
External 3.3V VCC bias, V_{IN} = 3.3V, I_{OUT} = 30A, PWM mode



4ms/div.

Shutdown through VIN

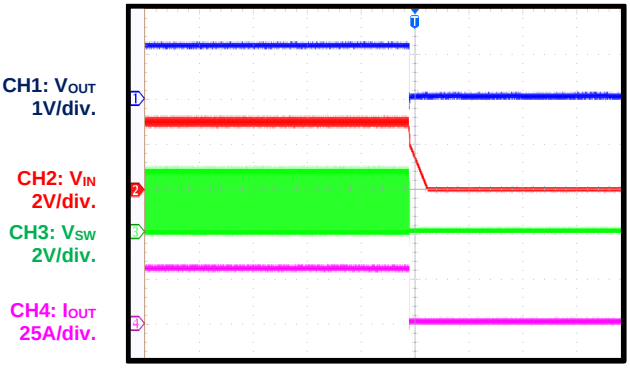
External 3.3V VCC bias, V_{IN} = 3.3V, I_{OUT} = 0A, PWM mode



10ms/div.

Shutdown through VIN

External 3.3V VCC bias, V_{IN} = 3.3V, I_{OUT} = 30A, PWM mode



200ms/div.

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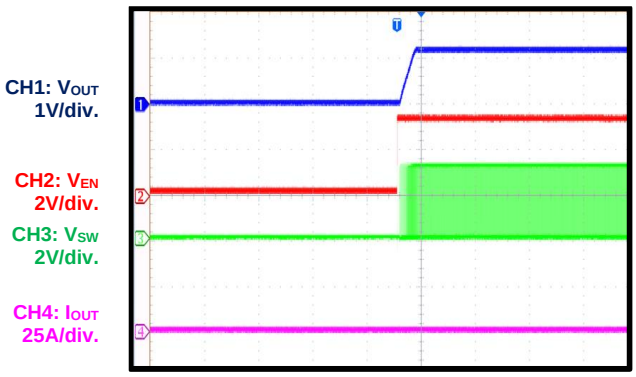
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 1.2V , V_{CC} = 3.3V, L = 220nH, C_{OUT} = 330µF x 2 POSCAP + 47µF x 5 Ceramic, T_A = 25°C, unless otherwise noted.

Start-Up through EN

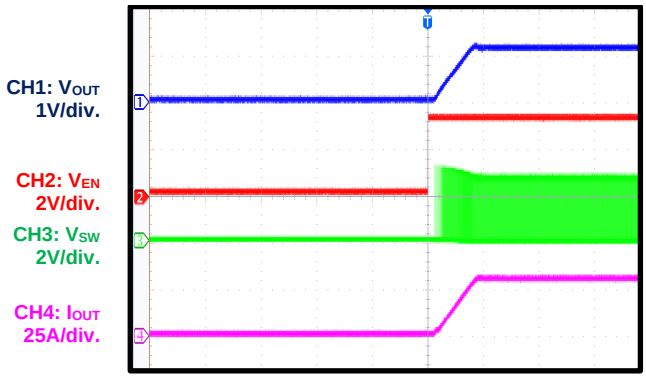
External 3.3V VCC bias, V_{IN} = 3.3V, I_{OUT} = 0A, PWM mode



10ms/div.

Start-Up through EN

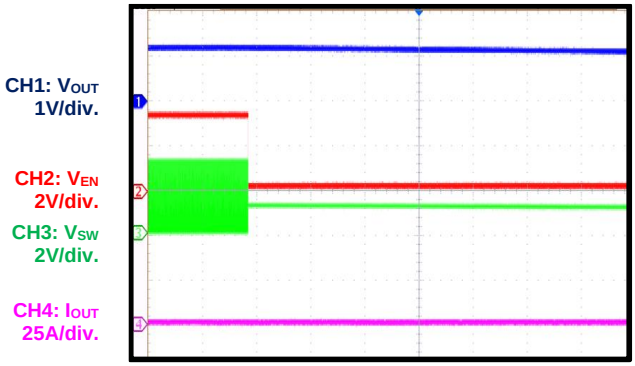
External 3.3V VCC bias, V_{IN} = 3.3V, I_{OUT} = 30A, PWM mode



4ms/div.

Shutdown through EN

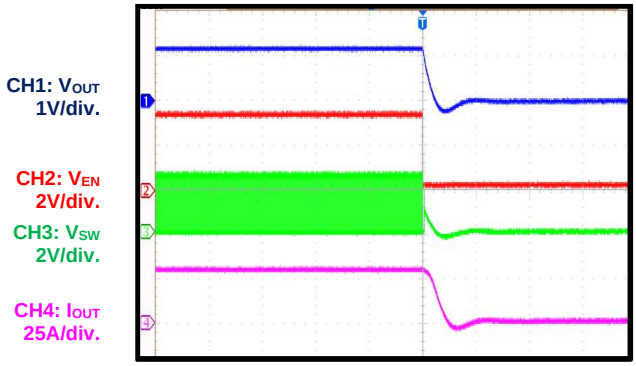
External 3.3V VCC bias, V_{IN} = 3.3V, I_{OUT} = 0A, PWM mode



400ms/div.

Shutdown through EN

External 3.3V VCC bias, V_{IN} = 3.3V, I_{OUT} = 30A, PWM mode



200µs/div.

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FUNCTIONAL BLOCK DIAGRAM

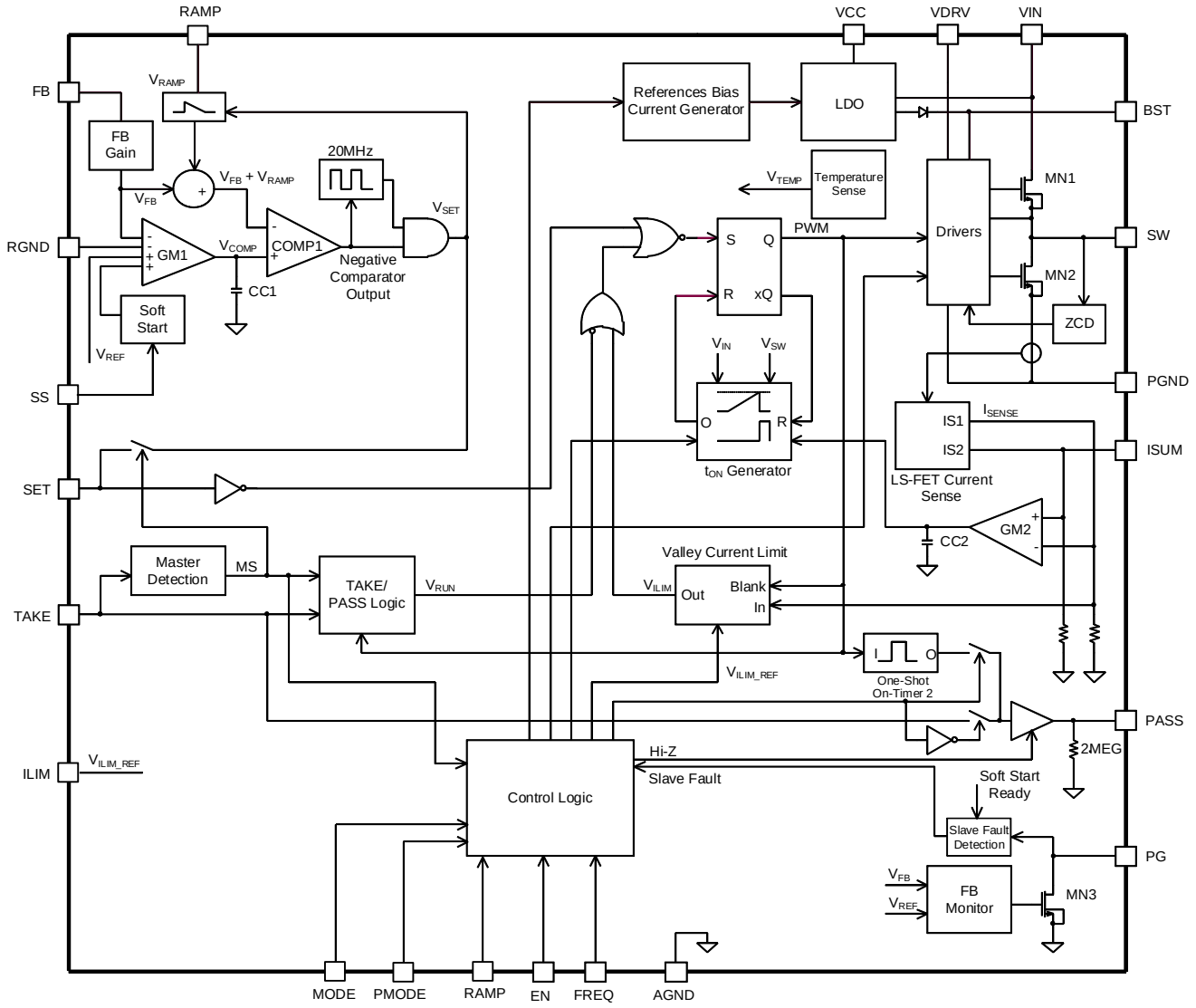

Figure 3: Functional Block Diagram

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MULTI-PHASE OPERATION

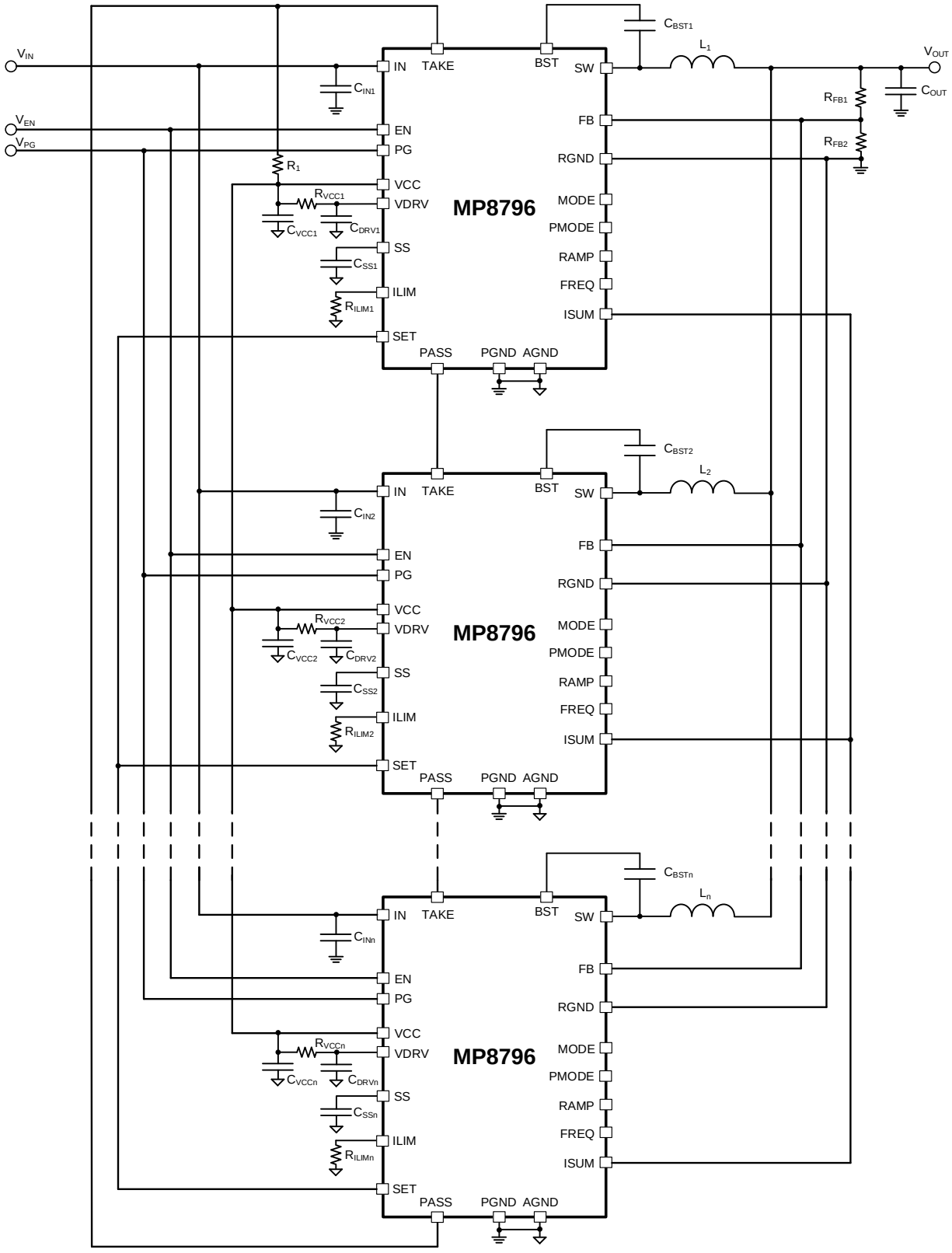

Figure 4: Multi-Phase (n) Configuration

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MULTI-PHASE OPERATION *(continued)*

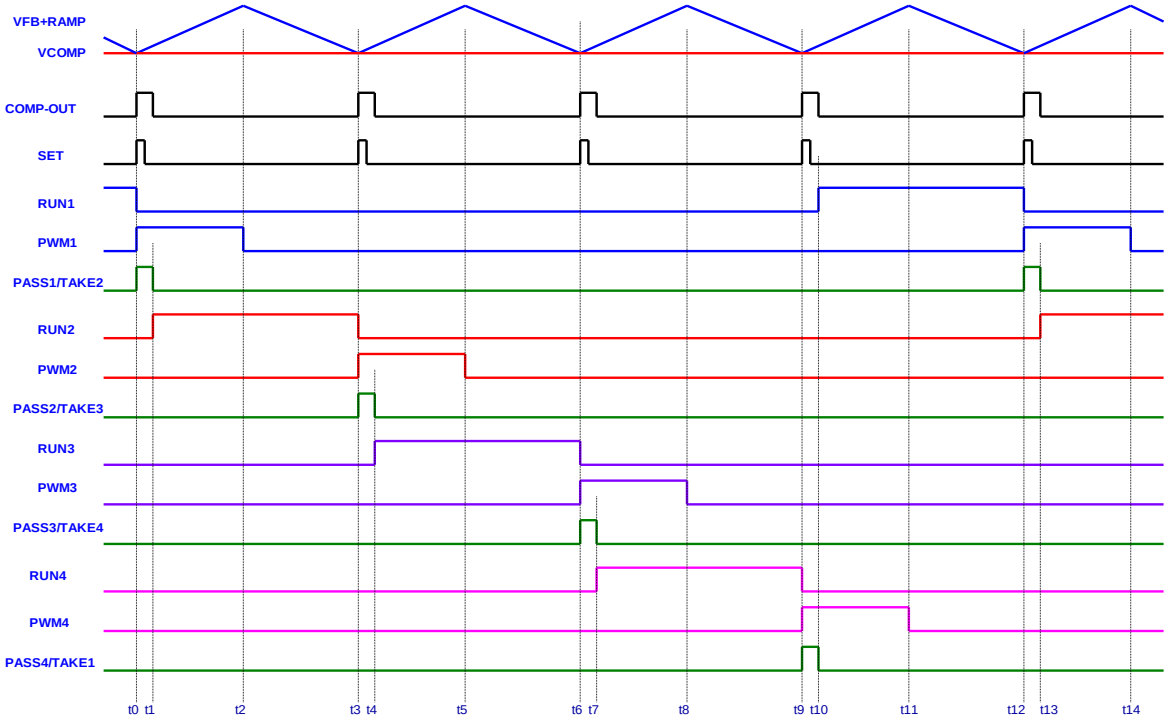

Figure 5: Multi-Phase Interleaved Operation (Steady State)

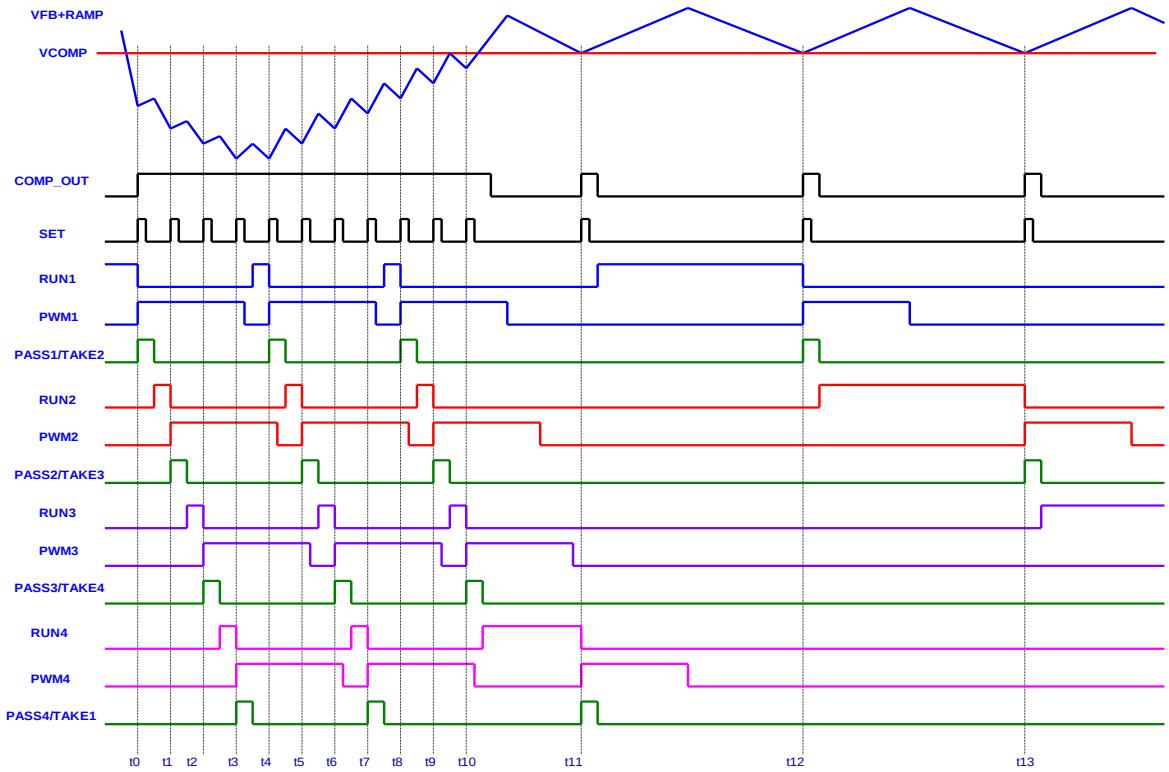

Figure 6: Multi-Phase Interleaved Operation (Load Step-Up Response)

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OPERATION

The MP8796 is a fully integrated, synchronous, rectified, step-down switch-mode converter.

Multi-Phase Constant-On-Time (MCOT) Control

Multi-phase constant-on-time (MCOT) control to provides fast load transient response and eases loop stabilization. The selectable internal ramp compensation stabilizes the system, making it easy to use.

Master and Slave Auto-Detection

A master phase is required for both single-phase and multi-phase operation. To configure a phase as a master phase, pull the TAKE pin of the phase up to a voltage source. The PASS and TAKE pins of all the phases are connected via daisy-chaining. The PASS pin of the last phase is connected to the TAKE pin of the first master phase. For single-phase operation, the PASS and TAKE pins are connected together. The master phase is determined after start-up. The remaining phases of the rail are the slave phases.

Master Phase MCOT Control

The master phase has the following functions:

- Generate the SET signals
- Manage the start-up, shutdown, and protection functions
- Monitor the fault alerts from the slave phases via the PG pin
- Start the first on pulse
- Start the on pulse while receiving the RUN and SET signals
- Dynamically adjusts its on time to ensure equal current sharing
- Carry the PASS and TAKE signals

Slave Phase MCOT Control

The slave phase has the following functions:

- Receive the SET signal from the master
- Send over-voltage (OV), under-voltage (UV), and over-temperature (OT) fault alerts to the master via the PG pin
- Start the on pulse while receiving RUN and SET signals
- Dynamically adjusts its on time to ensure equal current sharing
- Carry the PASS and TAKE signals

Figure 5 on page 21 shows the details of MCOT control.

At t_0, (V_{FB} + V_{RAMP}) drops below the level set by the comparator voltage (V_{COMP}) of the master phase. Then the master phase generates a SET signal. All of the phases receive this SET signal; however, only the phase that receives an active RUN signal should act. At this point, it is the master phase that acts. The master phase turns the high-side MOSFET (HS-FET) on. The master also generates a fixed on pulse on the PASS pin, and passes it to the TAKE pin of first slave phase (SLAVE1).

At t_1, the falling edge of SLAVE1's TAKE pin activates the RUN signal. SLAVE1 waits for the SET signal to turn on the HS-FET.

At t_2, the on pulse of the master phase expires, and the HS-FET turns off. The on pulse width is set by the input voltage (V_{IN}), output voltage (V_{OUT}), and switching frequency (f_{SW}). The on pulse width is determined by its own current and the total current of all phases.

At t_3, (V_{FB} + V_{RAMP}) drops below V_{COMP} of the master phase. At this point, it is SLAVE1 that has the active RUN signal to turn on its HS-FET. All of the other phases ignore this SET signal. SLAVE1 generates a fixed on pulse on the PASS pin, and passes it to the TAKE pin of the second slave phase (SLAVE2).

The following slave phases repeat the above operation, turning on each phase's HS-FET one after another for a fixed on time (t_{ON}). Only the phase that receives the RUN signal can turn on its HS-FET once the SET signal is ready.

The MP8796 utilizes MCOT control to provide ultra-fast load transient response. If a load step-up occurs, then the FB voltage (V_{FB}) drops below than the reference voltage (V_{REF}), and the SET is generated more frequently than during steady-state operation. The SET signal frequency depends on the load transient step size and slew rate. The SET signal can be generated with a minimum 50ns interval (e.g.

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the next phase can be turned on as fast as 50ns after the turn-on of the previous phase). This provides ultra-fast load transient response. Figure 6 on page 21 shows the load step-up response.

Ramp Compensation

The MP8796 includes internal ramp compensation to support all types of output capacitor (C_{OUT}) solutions. The ramp value can be selected via the RAMP pin. Pull RAMP high for slow transient response. Pull RAMP low for fast transient response. The RAMP signal is superimposed on the FB signal. Once the superimposed (V_{FB} + V_{RAMP}) signal reaches V_{REF}, the part generates a new SET signal. A larger V_{RAMP} reduces jitter in the system; however, a larger V_{RAMP} also leads to slower transient response. It is recommended to choose an optimal value based on the particular design if load transient response is a critical design target.

Mode Selection

The MP8796 provides both forced continuous conduction mode (FCCM) and pulse-skip mode (PSM) for light-load operation. The MODE pin sets the operation mode. Pull MODE high for FCCM. Pull MODE low for PSM.

Soft Start (SS)

The soft-start time (t_{SS}) can be configured via a resistor (C_{SS}) connected between the SS and AGND pins. t_{SS} can be calculated with Equation (1):

$$t_{SS}\,(ms) = 30 \times C_{SS}\,(\mu F) \quad (1)$$

Switching Frequency (f_{SW})

The switching frequency (f_{SW}) can be configured via a resistor (R_{FREQ}) connected between the FREQ and AGND pins. f_{SW} can be calculated with Equation (2):

$$f_{SW}\,(MHz) = \frac{24}{R_{FREQ}\,(k\Omega)} \quad (2)$$

Output Voltage Discharge

If the MP8796 shuts down through EN, then V_{OUT} discharge mode is enabled. Both the HS-FET and the LS-FET latch off, and a discharge MOSFET connected between the SW and PGND pins turns on to discharge V_{OUT}. The typical on resistance of this MOSFET is 60Ω. Once V_{FB} drops below 10% of V_{REF}, the discharge MOSFET turns off.

Protection Mode Selection

The MP8796 provides both hiccup mode and latch-off mode for the protection functions. The PMODE pin sets the protection mode. Pull PMODE high to have the part operate in hiccup mode if over-current protection (OCP), over-voltage protection (OVP), or over-temperature protection (OTP) is triggered. Pull PMODE down to PGND to have the part operate in latch-off mode if OCP, OVP, or OTP triggered.

Over-Current Protection (OCP)

The MP8796 features on-die current sense. During the LS-FET t_{ON}, the inductor current (I_L) is sensed and monitored cycle by cycle. If V_{FB} drops below V_{REF}, then the HS-FET turns on once there is no over current (OC) detected. I_L is limited cycle by cycle. If an OC fault is detected for 31 consecutive cycles, then OCP is triggered. If V_{OUT} drops below under-voltage protection (UVP) threshold (V_{UVP}) during an OC fault or an output short-circuit fault, then OCP is triggered.

Once OCP is triggered, the part enters either enters hiccup mode or latch-off mode. Cycle the power on VCC or VIN to reset a fault latch and start-up the part again.

The inductor valley current limit (I_{LIMIT_VALLEY}) can be configured via an external resistor (R_{ILIM}). R_{ILIM} can be calculated with Equation (3):

$$I_{LIMIT_VALLEY} = \frac{1.8(V)}{R_{ILIM}(M\Omega)} \quad (3)$$

The ILIM pin sets the per-phase I_{LIMIT_VALLEY} regardless of whether the part is configured for single-phase or multi-phase operation.

Negative Inductor Current Limit

If the LS-FET detects a negative current (below about -13A), then the LS-FET turns off for 100ns to limit the negative current.

Over-Temperature Protection (OTP)

The IC monitors the junction temperature (T_J) internally. If T_J exceeds the thermal shutdown threshold (typically 160°C), then the converter shuts down.

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Once OTP is triggered, the part enters either hiccup mode or latch-off mode. If the part latches off, cycle the power on VCC or EN to start the part up again.

External Voltage Divider

An external voltage divider is used to set V_{OUT}. Figure 7 shows the configuration of external voltage divider is used. The FB and RGND are connected to the V_{OUT} sense point via a resistor divider (R_{FB1} and R_{FB2}).

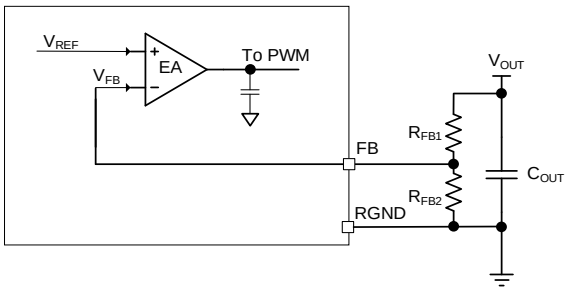

Figure 7: External Voltage Divider

There is not a strict requirement for the feedback resistor (R_{FB}). V_{OUT} can be estimated with Equation (4):

$$V_{OUT} = V_{REF} x (1 + \frac{R_{FB1}}{R_{FB2}}) \quad (4)$$

Power Good (PG)

The PG pin is a power good (PG) output. PG is the open drain of a MOSFET. Connect PG to VDRV or another external voltage source (<3.6V) via a pull-up resistor (e.g. 100kΩ). Once V_{IN} is applied, the MOSFET turns on, and PG is pulled up to PGND before soft start (SS) is ready. Once V_{FB} exceeds its threshold, PG is pulled high after a delay time (about 1ms).

If a fault occurs (e.g. UV fault, OV fault, or OT fault), then PG is latched low. Once PG is latched low, it cannot be pulled high again until a new SS is initiated.

If the MP8796 is configured as the master in either single-phase or multi-phase operation, the PG pin is used for fault indication. Pull PG above 2.2V to ensure proper operation; otherwise, the MP8796 may enter a protection mode. Do not add a long RC delay on the PG pin, as the IC may enter slave fault protection mode. If V_{FB} exceeds 90% of V_{REF} during SS, the MP8796 should detect the PG status within 100µs. If PG is below 2.2V within 100µs, then the IC enters slave fault protection mode.

If V_{IN} fails to power the MP8796, then PG is clamped low regardless of whether it is tied to an external DC source via a pull-up resistor. Figure 8 shows the relationship between the PG voltage (V_{PG}) and the PG pull-up current (I_{PG}).

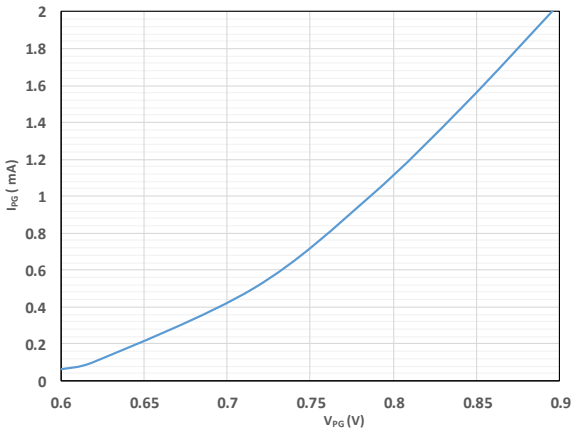

Figure 8: V_{PG} vs. I_{PG}

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APPLICATION INFORMATION

Selecting the Input Capacitor (C_{IN})

The step-down converter has a discontinuous input current (I_{IN}), and requires a capacitor to supply AC current to the step-down converter while maintaining the DC V_{IN}. Use ceramic capacitors for the best performance. Place the input capacitors as close to the VIN pin as possible.

The capacitance can vary significantly with the temperature. Capacitors with X5R and X7R dielectrics are recommended due to their stable temperature characteristics and low ESR.

The input capacitors should have a ripple current rating that exceeds the converter's maximum input ripple current (I_{CIN_MAX}). The input ripple current (I_{CIN}) can be estimated with Equation (5):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (5)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (6):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (6)$$

For simplification, choose an input capacitor (C_{IN}) with an RMS current rating that exceeds half the maximum load current (I_{LOAD_MAX}).

The input capacitance value determines converter's V_{IN} ripple (ΔV_{IN}). If there is a ΔV_{IN} requirement in the system, then select C_{IN} to meet the system's specification.

ΔV_{IN} can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (8):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (8)$$

Selecting the Output Capacitor (C_{OUT})

The output capacitor (C_{OUT}) maintains the DC V_{OUT}. The V_{OUT} ripple (ΔV_{OUT}) can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (9)$$

When using ceramic capacitors, the capacitance dominates the impedance at f_{SW}. The capacitance also dominates ΔV_{OUT}. For simplification, ΔV_{OUT} can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

When using POSCAP capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (11)$$

Selecting the Inductor

The inductor supplies a constant current to the output load while being driven by the switching V_{IN}. A larger-value inductor results in less ripple current and a lower ΔV_{OUT}; however, a larger-value inductor has a larger physical size, a higher series resistance, and a lower saturation current. Choose an inductor so that the peak-to-peak inductor ripple current (ΔI_L) is between 30% and 40% of the maximum output current (I_{OUT_MAX}). The peak inductor current (I_{L_PEAK}) should be below the saturation current. The inductance (L) can be calculated with Equation (12):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (12)$$

Choose an inductor that will not saturate under the maximum I_{L_PEAK}. I_{L_PEAK} can be calculated with Equation (13):

$$L_{LP} = I_{OUT} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (13)$$

Low-Input Voltage Applications

For applications with a low V_{IN} (between 3V and 4V), a >2.9V external VCC biased power supply is required (see Figure 11 on page 27).

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PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best performance, refer to Figure 9 and follow the guidelines below:

1. Place the MLCC input capacitors as close to the VIN and PGND pins as possible.
2. Place the major MLCC capacitors on the same layer as the IC.
3. Maximize the VIN and PGND copper plane to minimize parasitic impedance.
4. Place as many PGND vias as possible close to the PGND pins to minimize both parasitic impedance and thermal resistance.
5. Place VCC decoupling capacitor close to the IC.
6. Connect AGND and PGND at the VCC capacitor's ground connection.
7. Place a 0.1μF to 1μF BST capacitor as close to the BST and SW pins as possible.
8. Route the BST path using ⩾20mils trace width.
9. Place a 0.1μF to 1μF MLCC input capacitor (0402) near the VIN pin.

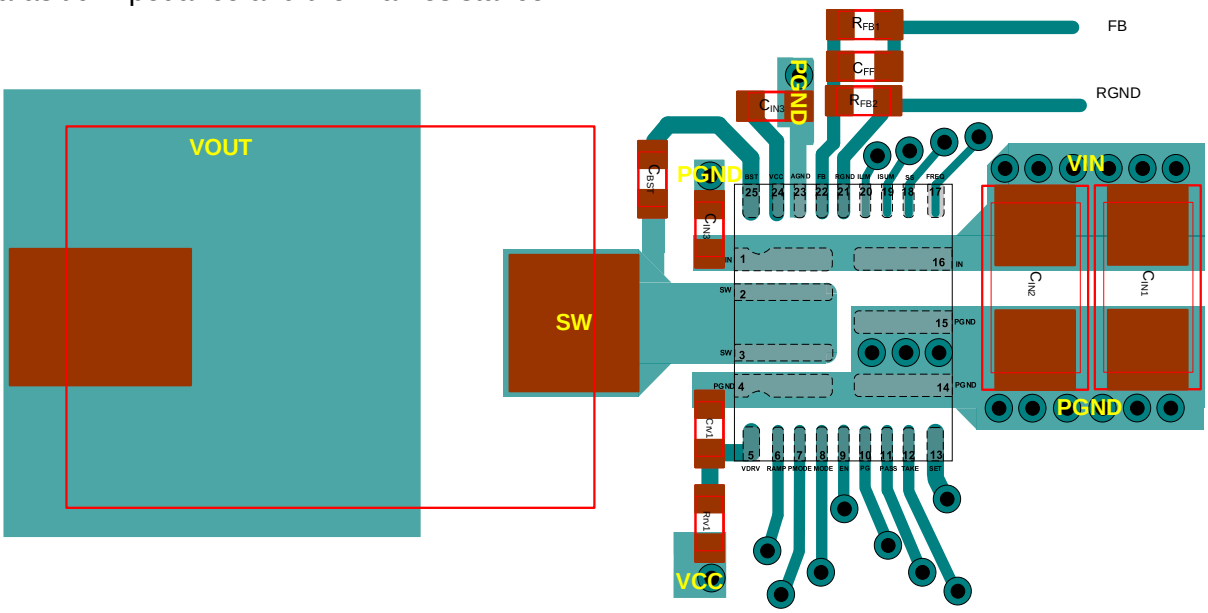

Figure 9: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

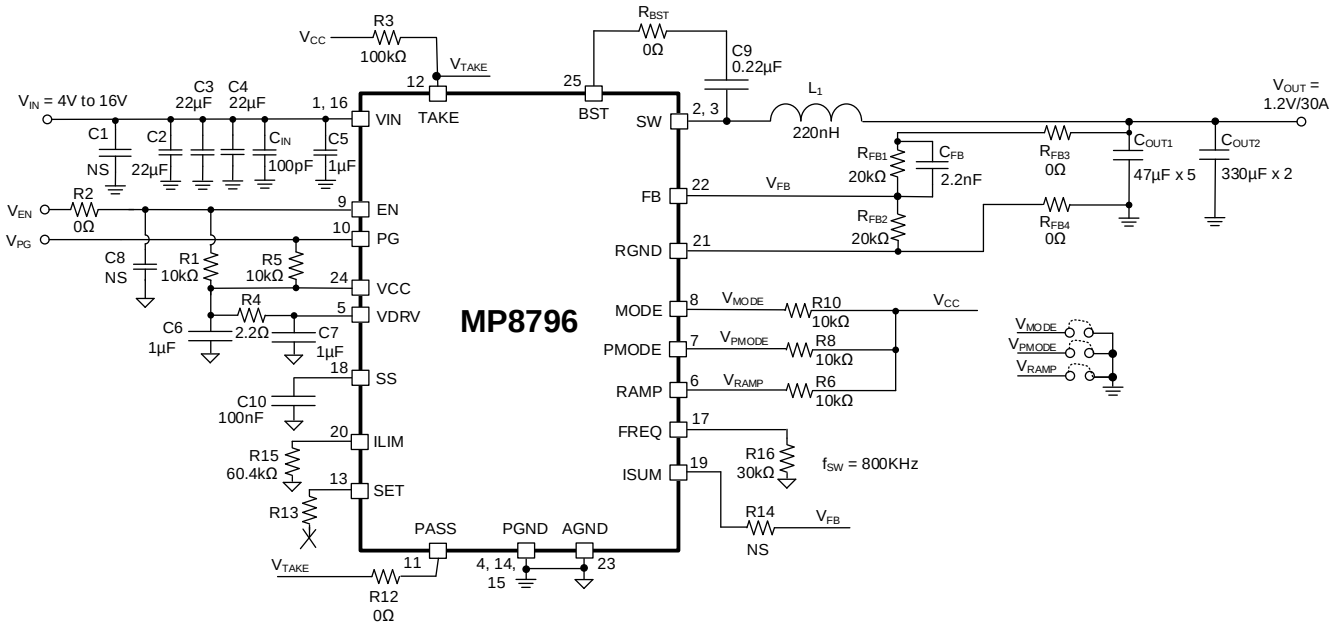

Figure 10: Typical Application Circuit (V_{IN} = 4V to 16V)

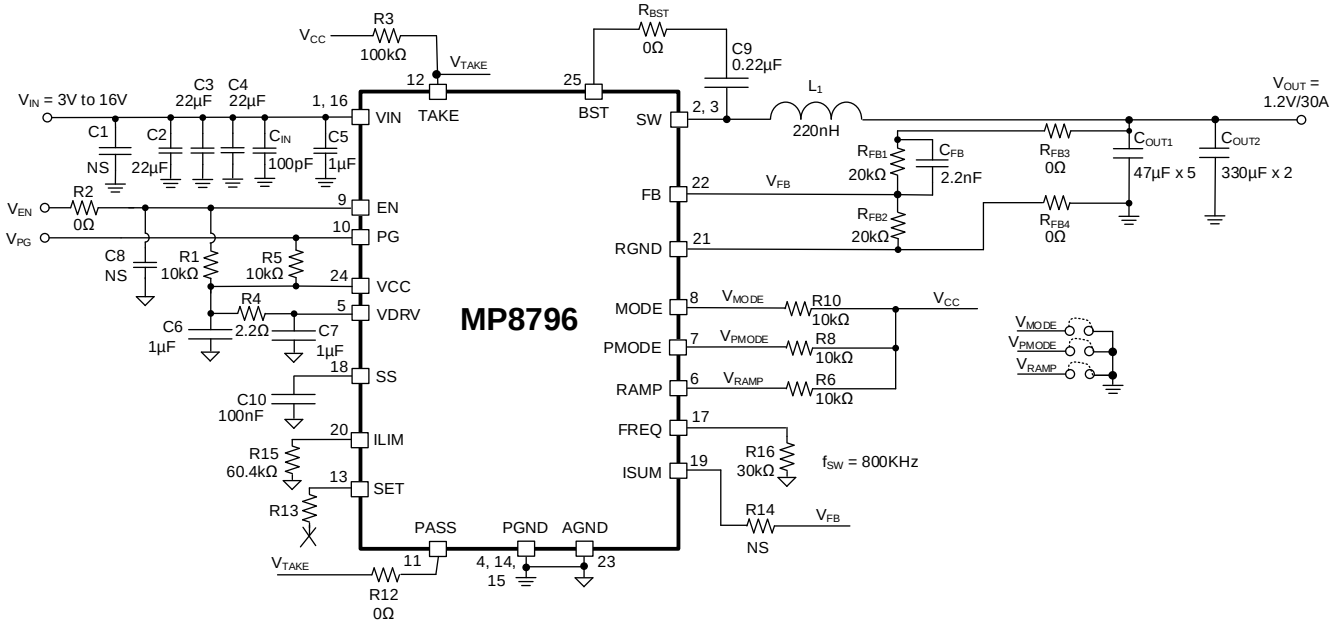

Figure 11: Typical Application Circuit with Low V_{IN} and VCC Bias (V_{IN} = 3V to 16V)

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TYPICAL APPLICATION CIRCUITS *(continued)*

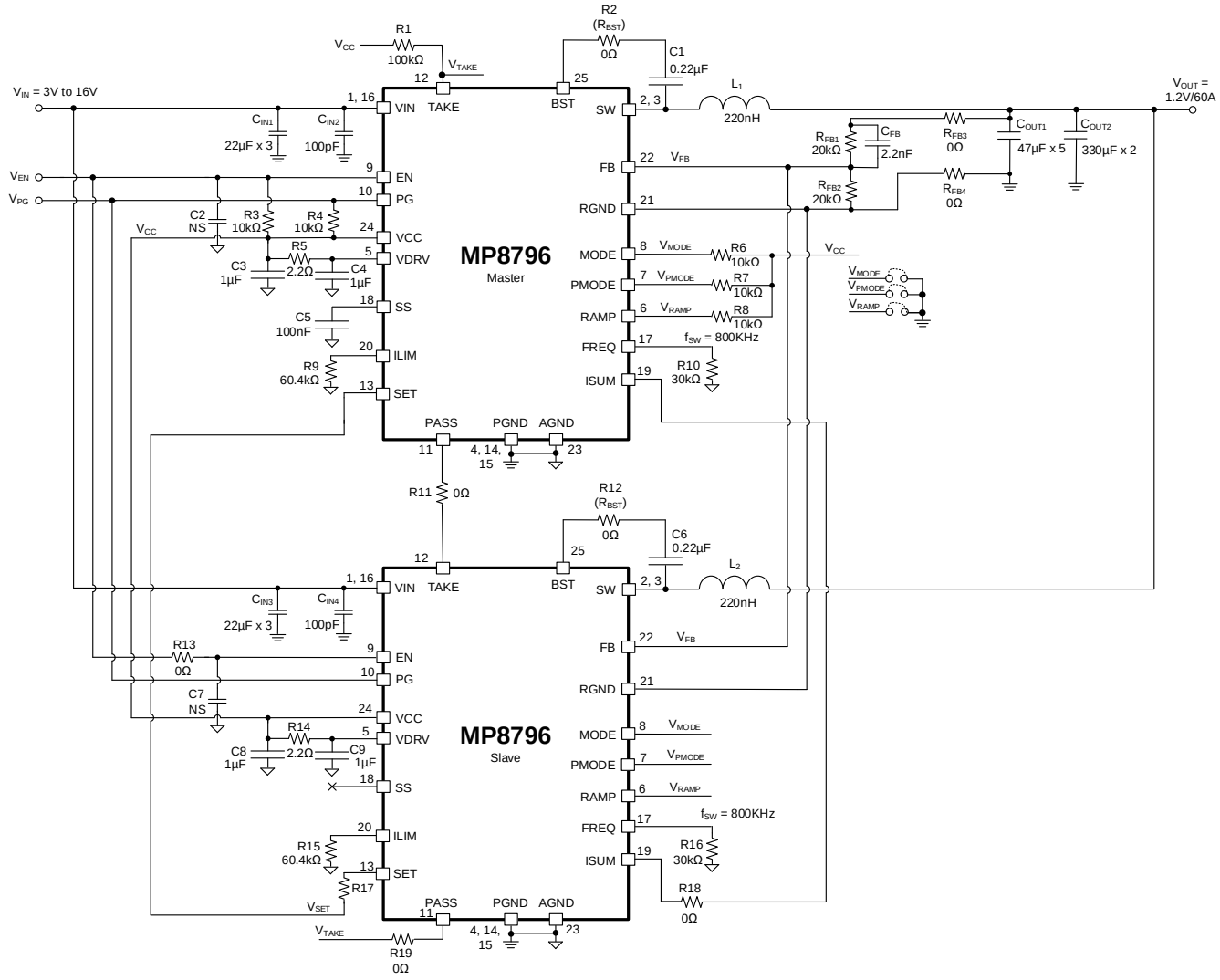

Figure 12: Typical Application Circuit (Dual-Phase Operation)

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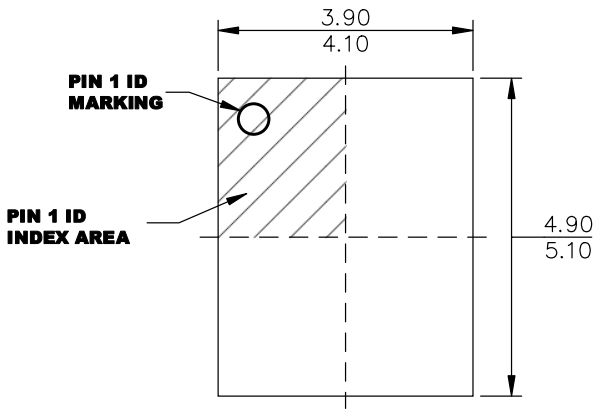
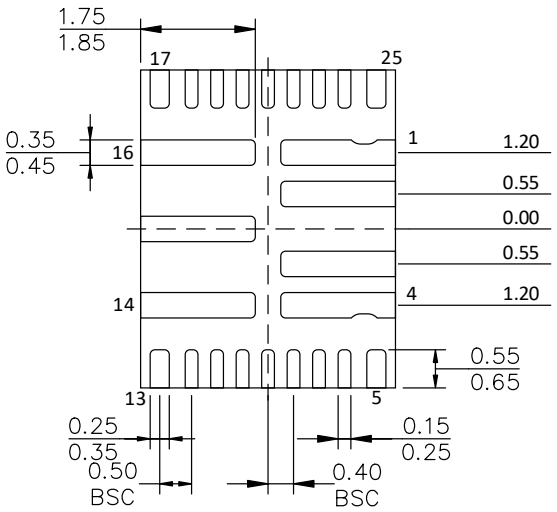
PACKAGE INFORMATION

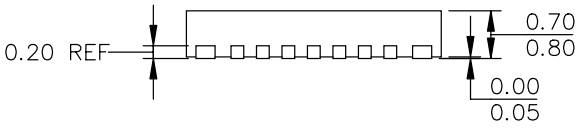
TQFN-25 (4mmx5mm)



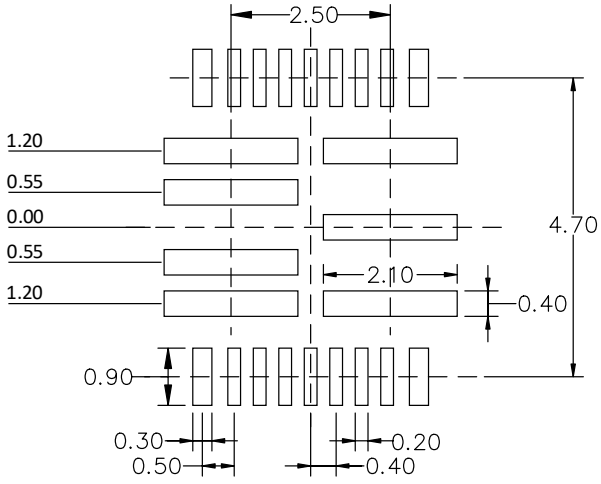
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) THE LAND PATTERNS OF PIN 1, PIN 2, PIN 3, PIN 4, PIN 14, PIN 15, AND PIN 16 HAVE THE SAME LENGTH AND WIDTH.
2) THE LAND PATTERNS OF PIN 5, PIN 13, PIN 17, AND PIN 25 HAVE THE SAME LENGTH AND WIDTH.
3) ALL DIMENSIONS ARE IN MILLIMETERS.
4) LEAD COPLANARITIES SHALL BE 0.08 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.

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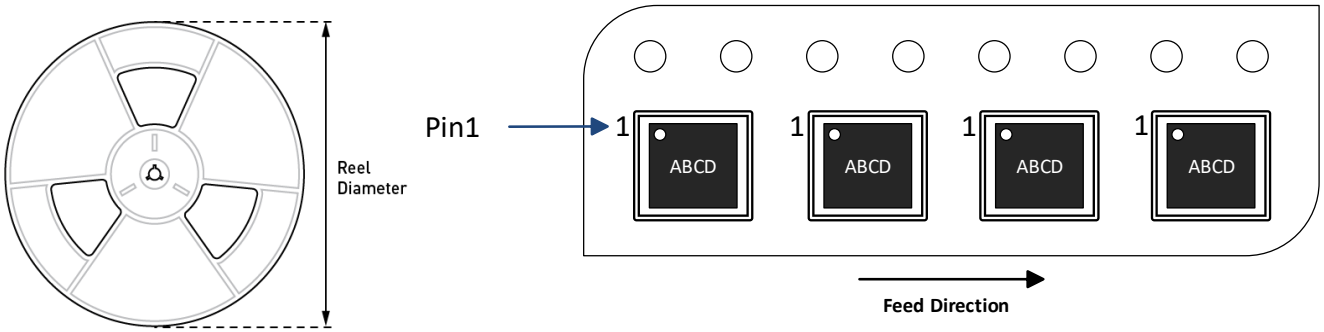
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity /Tube	Quantity /Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP8796GVT-Z	TQFN-25 (4mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	6/1/2022	Initial Release	-

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