MP8774C

12A, Wide 3V to 18V Input, 1.4MHz, Synchonous Step-Down Converter with FCCM in a QFN-16 (3mmx3mm) Package

DESCRIPTION

The MP8774C is a fully integrated, high-frequency, synchronous, rectified, step-down switch-mode converter with internal power MOSFETs. The MP8774C offers a very compact solution that achieves up to 12A of continuous output current (I_{OUT}) across a wide input voltage (V_{IN}) range, with excellent load and line regulation. The MP8774C employs synchronous mode for higher efficiency across the entire I_{OUT} load range.

Constant-on-time (COT) control provides very fast transient response, easy loop design, and very tight output regulation.

Full protection features include short-circuit protection (SCP), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown.

The MP8774C requires a minimal number of readily available, standard external components, and is available in a space-saving QFN-16 (3mmx3mm) package.

FEATURES

- Fixed 1.4MHz Switching Frequency (f_{SW})
- Forced Continuous Conduction Mode (FCCM)
- Output Adjustable from 0.6V
- Wide 3V to 18V Operating Input Voltage (V_{IN}) Range
- 12A Output Current (I_{OUT})
- 16mΩ/5.5mΩ Low On Resistance, Internal Power MOSFETs
- 100μA Quiescent Current (I_Q)
- High-Efficiency Synchronous Mode
- Pre-Biased Start-Up
- Configurable External Soft-Start Time (t_{SS})
- Enable (EN) and Power Good (PG) for Power Sequencing
- Over-Current Protection (OCP) with Hiccup Mode
- Thermal Shutdown
- Available in a QFN-16 (3mmx3mm) Package

APPLICATIONS

- Security Cameras
- AP Routers and xDSL Devices
- Digital Set-Top Boxes
- Flat-Panel Televisions and Monitors
- General-Purpose Power Supplies

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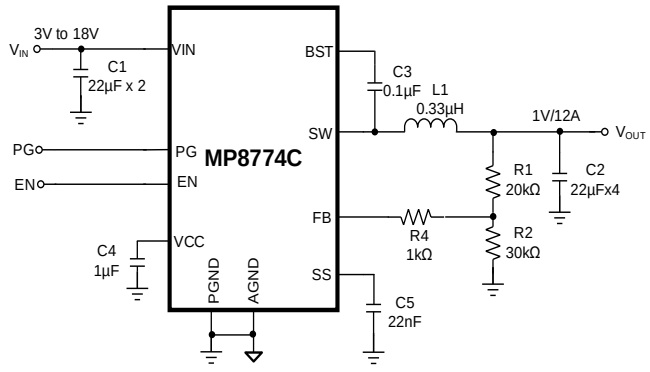
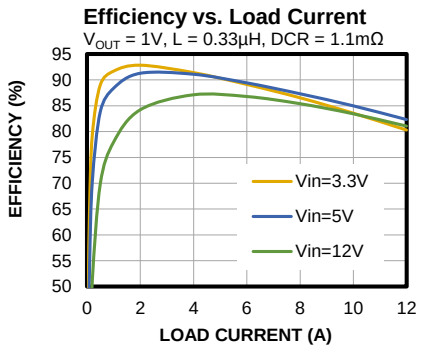
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP8774CGQ	QFN-16 (3mmx3mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP8774CGQ-Z).

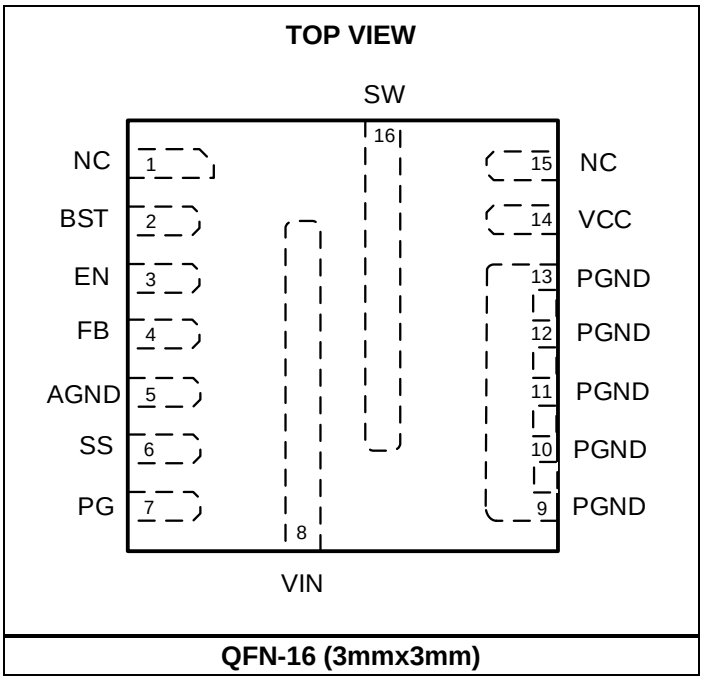
TOP MARKING

CAEY

LLLL

CAE: Product code of MP8774CGQ
Y: Year code
LLLL: Lot number

PACKAGE REFERENCE



QFN-16 (3mmx3mm)

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PIN FUNCTIONS

Pin #	Name	Description
1, 15	NC	**Not connected.**
2	BST	**Bootstrap.** Connect a capacitor between the SW and BST pins to form a floating supply across the high-side MOSFET (HS-FET) driver. A BST resistor <4.7Ω is recommended.
3	EN	**Enable.** Pull the EN pin high to enable the MP8774C. When floating, EN is pulled down to AGND and disabled by an internal 1.2MΩ resistor.
4	FB	**Feedback.** The FB pin sets the output voltage (V_{OUT}) when connected to the tap of an external resistor divider between the output and AGND.
5	AGND	**Signal ground.** AGND is not connected to PGND internally. Ensure that AGND is connected to PGND in the PCB layout.
6	SS	**Soft start.** Connect a capacitor between the SS and AGND pins to set the soft-start time (t_{SS}) and to avoid inrush current during start-up.
7	PG	**Power good output.** The PG pin is an open-drain output. PG changes state if under-voltage protection (UVP), over-current protection (OCP), over-temperature protection (OTP), or over-voltage protection (OVP) occurs.
8	VIN	**Input voltage.** The MP8774C operates from a 3V to 18V input rail. A capacitor is required to decouple the input rail. Use a wide PCB trace to make the VIN connection.
9, 10, 11, 12, 13	PGND	**System ground.** PGND is the reference ground of the regulated V_{OUT}. PGND requires careful consideration during PCB layout. It is recommended to use wide PCB traces and vias to make the PGND connection.
14	VCC	**Internal bias supply output.** Decouple VCC using a 1µF capacitor. Place the VCC capacitor (C_{VCC}) close to VCC and PGND.
16	SW	**Switch output.** Connect the SW pin using a wide PCB trace.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN}, V_{EN} .....-0.3V to +20V
V_{SW}..... -0.3V (-5V < 10ns) to V_{IN} + 0.7V (23V < 10ns)
V_{BST} ..... V_{SW} + 4V
All other pins .....-0.3V to +4V
Continuous power dissipation (T_A = 25°C) (2) (4) 3.2W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +125°C

Recommended Operating Conditions (3)

Input voltage (V_{IN}) .....3V to 18V
Output voltage (V_{OUT})..... . 0.6V to V_{IN} x D_{MAX} or 12V max
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-16 (3mmx3mm)		
EV8774C-Q-00A (4)	38	10 °C/W
JESD51-7 (5)	50	12 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the converter to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on the EV8774C-Q-00A: a 4-layer, 85mmx85mm PCB.
5) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C (6), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input voltage	V_{IN}		3		18	V
Supply Current						
Supply current (shutdown)	I_{SD}	V_{EN} = 0V			5	µA
Supply current (quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 0.65V		100	150	µA
MOSFET						
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)_HS}$	V_{BST-SW} = 3.3V		16		mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)_LS}$	V_{CC} = 3.3V		5.5		mΩ
Switch leakage	I_{SW_LKG}	V_{EN} = 0V, V_{SW} = 18V, T_J = 25°C			1	µA
Current Limit (I_{LIMIT})						
Valley I_{LIMIT}	I_{LIMIT_VALLEY}		12	14		A
Short hiccup duty cycle (7)	D_{HICCUP}			10		%
Negative I_{LIMIT}	I_{LIMIT_NEG}			-3.5		A
Switching Frequency (f_{SW}) and Minimum On/Off Time						
Switching frequency	f_{SW}	V_{OUT} = 1V, I_{OUT} = 6A	1200	1400	1600	kHz
Minimum on time (7)	t_{ON_MIN}			50		ns
Minimum off time (7)	t_{OFF_MIN}			100		ns
Reference and Soft Start (SS)						
Feedback voltage	V_{FB}	T_J = 25°C	594	600	606	mV
		T_J = -40°C to +125°C	591	600	609	mV
Feedback current	I_{FB}	V_{FB} = 700mV		10	50	nA
Soft-start current	I_{SS}		4	6	8	µA
Enable (EN) and Under-Voltage Lockout (UVLO)						
EN rising threshold	V_{EN_RISING}		1.1	1.25	1.4	V
EN falling threshold	$V_{EN_FALLING}$		0.9	1	1.1	V
EN pull-down resistance	R_{EN_PD}			1.2		MΩ
VCC						
VCC voltage (V_{CC}) UVLO rising threshold	$V_{CC_UVLO_RISING}$		2.6	2.8	3	V
VCC under-voltage lockout threshold	$V_{CC_UVLO_HYS}$			350		mV
VCC regulator voltage	V_{CC}			3.4		V
VCC load regulation	REG_{VCC}	I_{CC} = 5mA		3		%

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C (6), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Good (PG)						
PG under-voltage protection (UVP) rising threshold	$V_{PG_UVP_RISING}$		0.85	0.9	0.95	V_{FB}
PG UVP falling threshold	$V_{PG_UVP_FALLING}$		0.75	0.8	0.85	V_{FB}
PG over-voltage protection (OVP) rising threshold	$V_{PG_OVP_RISING}$		1.15	1.2	1.25	V_{FB}
PG OVP falling threshold	$V_{PG_OVP_FALLING}$		1.05	1.1	1.15	V_{FB}
PG delay	t_{PG_DELAY}	Both edges		50		µs
PG sink current capability	V_{PG}	Sink 4mA			0.4	V
PG leakage current	I_{PG_LKG}	V_{PG} = 5V			10	µA
Thermal Protection						
Thermal shutdown (7)	T_{SD}			150		°C
Thermal hysteresis (7)	T_{SD_HYS}			20		°C

Notes:

6) Derived by over-temperature correlation. Not tested in production.
7) Derived by sample characterization. Not tested in production.

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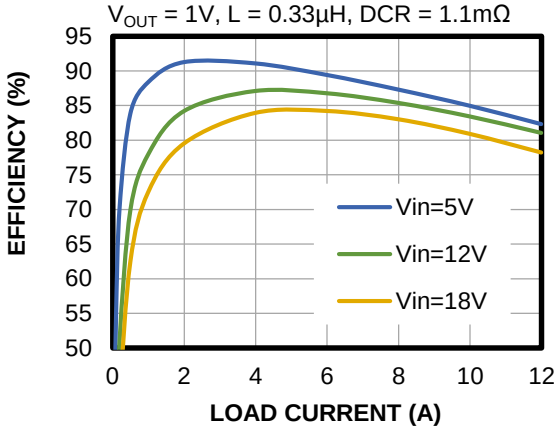
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1V, L = 0.33µH, T_A = 25°C, unless otherwise noted.

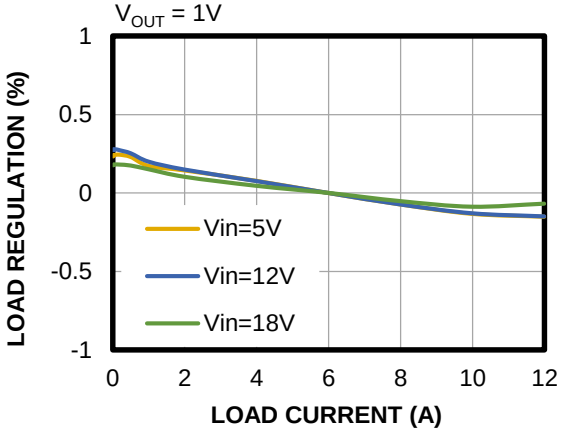
Efficiency vs. Load Current

V_{OUT} = 1V, L = 0.33µH, DCR = 1.1mΩ

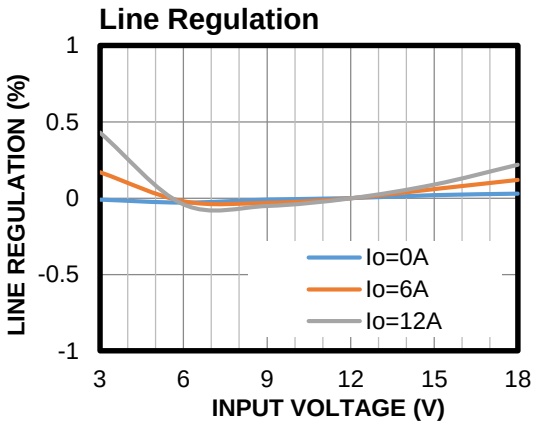


Load Regulation vs. Load Current

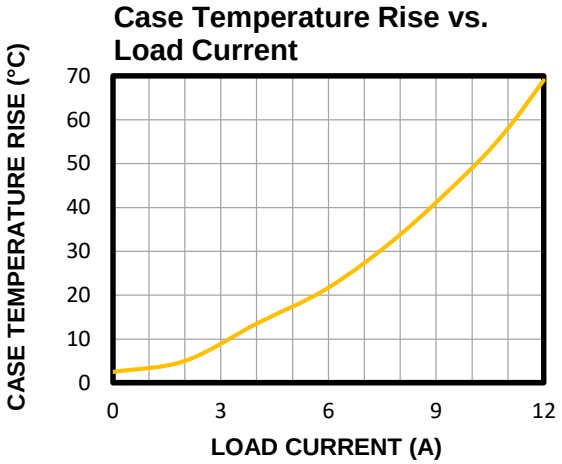
V_{OUT} = 1V



Line Regulation



Case Temperature Rise vs. Load Current



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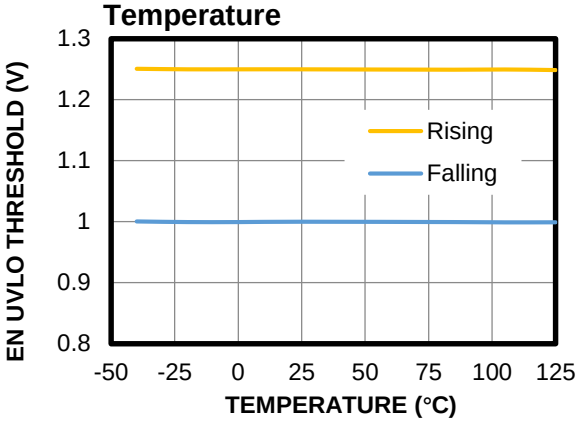
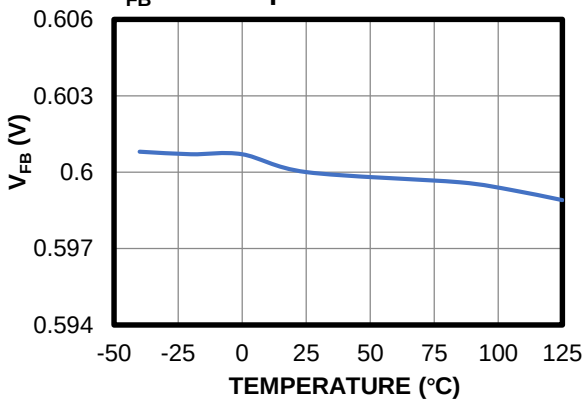
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, L = 0.33µH, T_A = 25°C, unless otherwise noted.

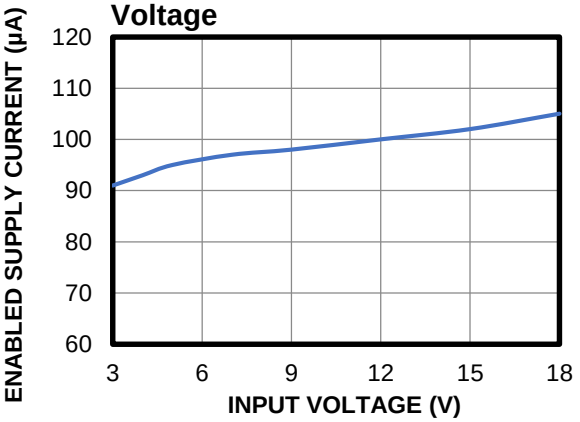
EN UVLO Threshold vs. Temperature



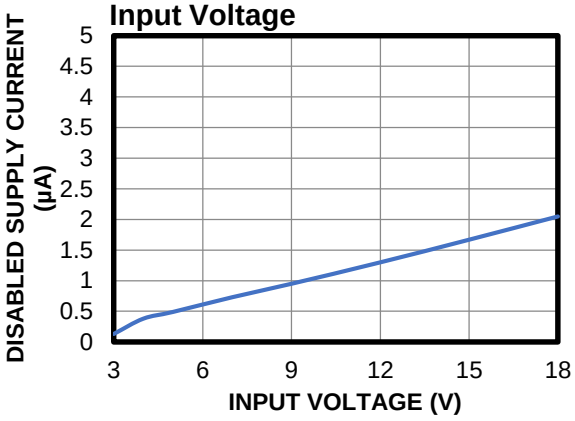
V_{FB} vs. Temperature



Enabled Supply Current vs. Input Voltage



Disabled Supply Current vs. Input Voltage



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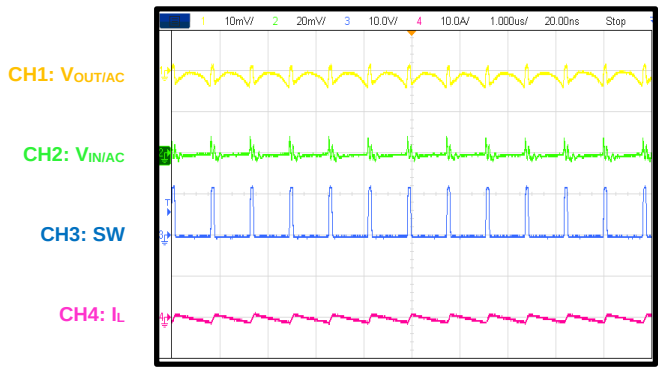
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, L = 0.33µH, T_A = 25°C, unless otherwise noted.

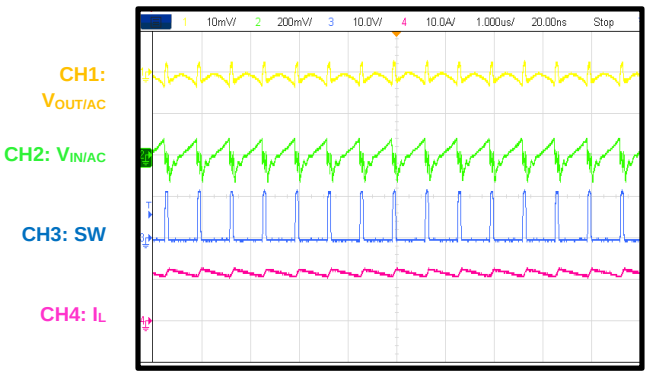
Input/Output Ripple

I_{OUT} = 0A



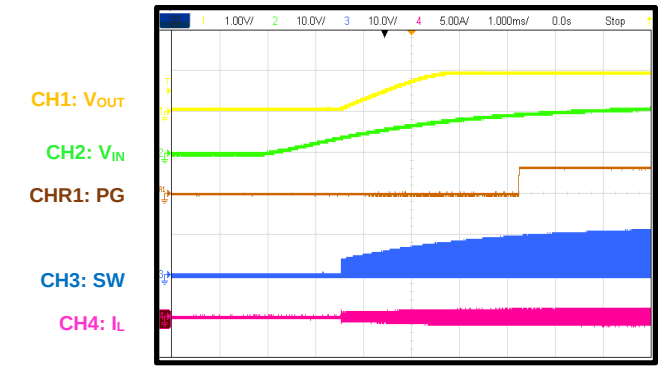
Input/Output Ripple

I_{OUT} = 12A



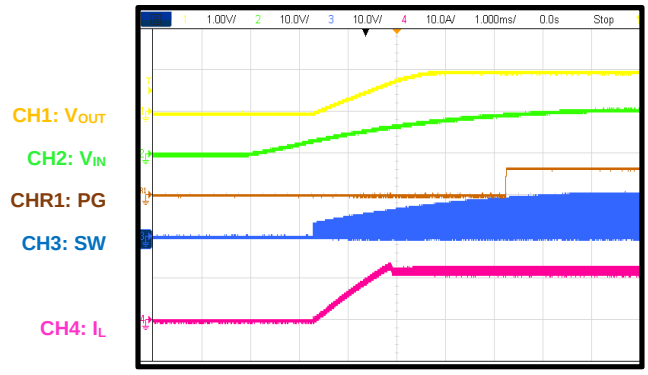
Start-Up through VIN

I_{OUT} = 0A



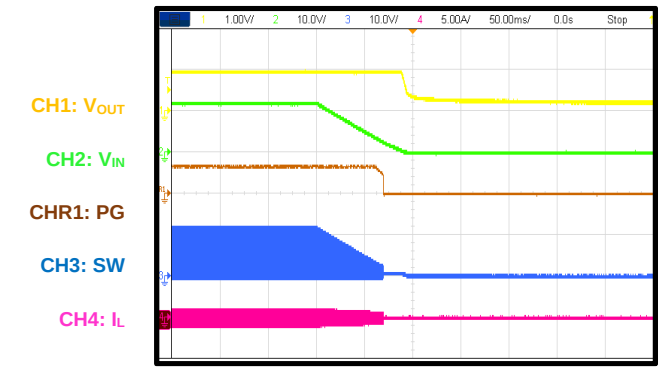
Start-Up through VIN

I_{OUT} = 12A



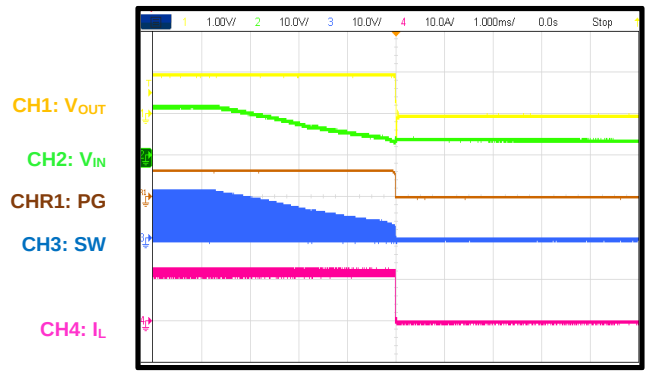
Shutdown through VIN

I_{OUT} = 0A



Shutdown through VIN

I_{OUT} = 12A



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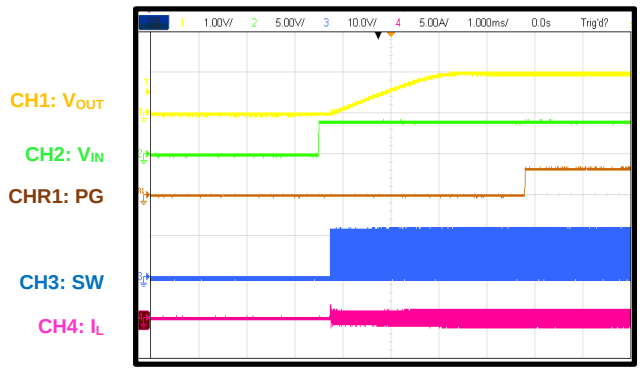
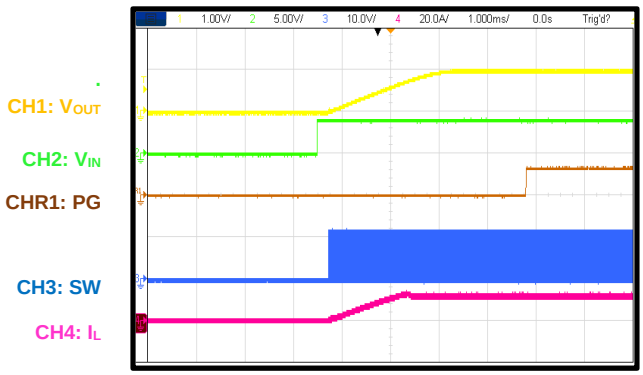
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, L = 0.33µH, T_A = 25°C, unless otherwise noted.

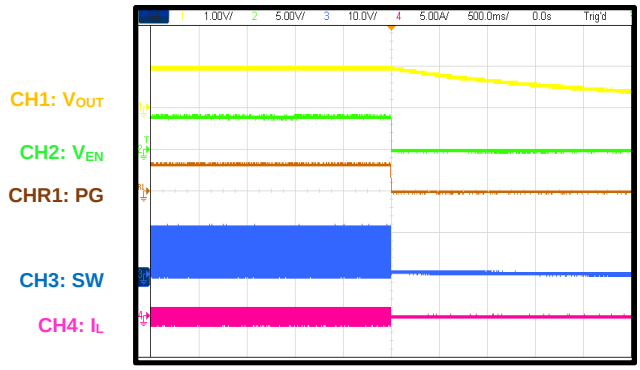
Start-Up through EN
I_{OUT} = 0A



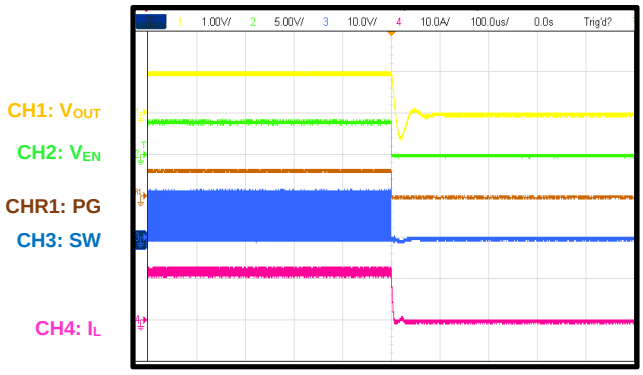
Start-Up through EN
I_{OUT} = 12A



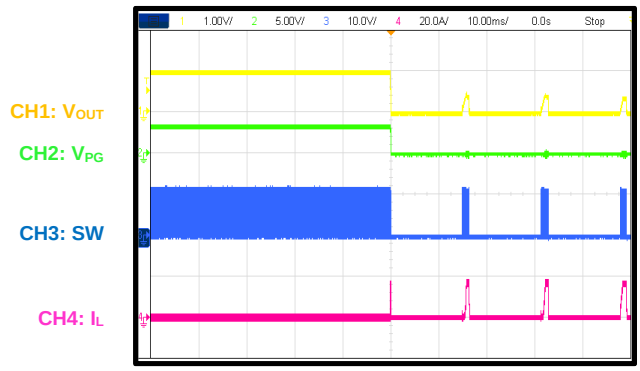
Shutdown through EN
I_{OUT} = 0A



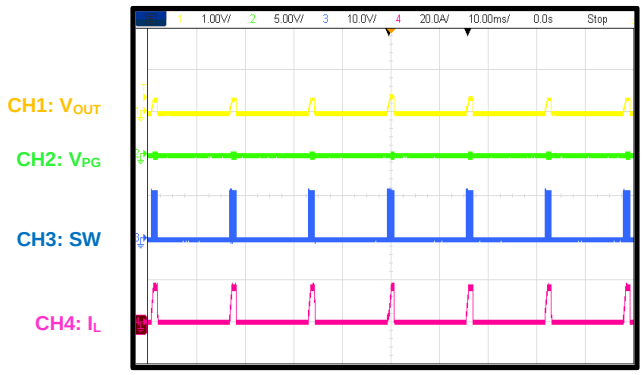
Shutdown through EN
I_{OUT} = 12A



SCP Entry
I_{OUT} = 0A



SCP Steady State



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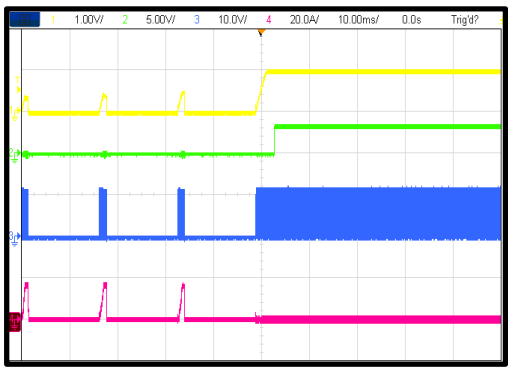
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, L = 0.33µH, T_A = 25°C, unless otherwise noted.

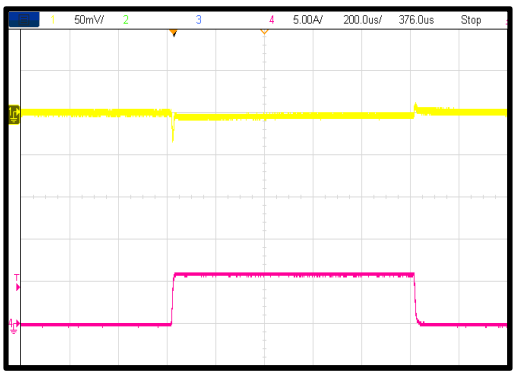
SCP Recovery

I_{OUT} = 0A



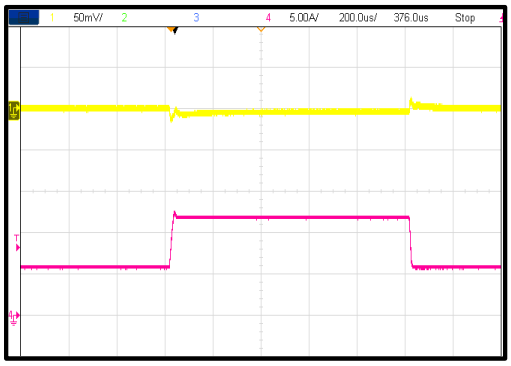
Load Transient

0A to 6A, 0.8A/µs



Load Transient

6A to 12A, 0.8A/µs



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FUNCTIONAL BLOCK DIAGRAM

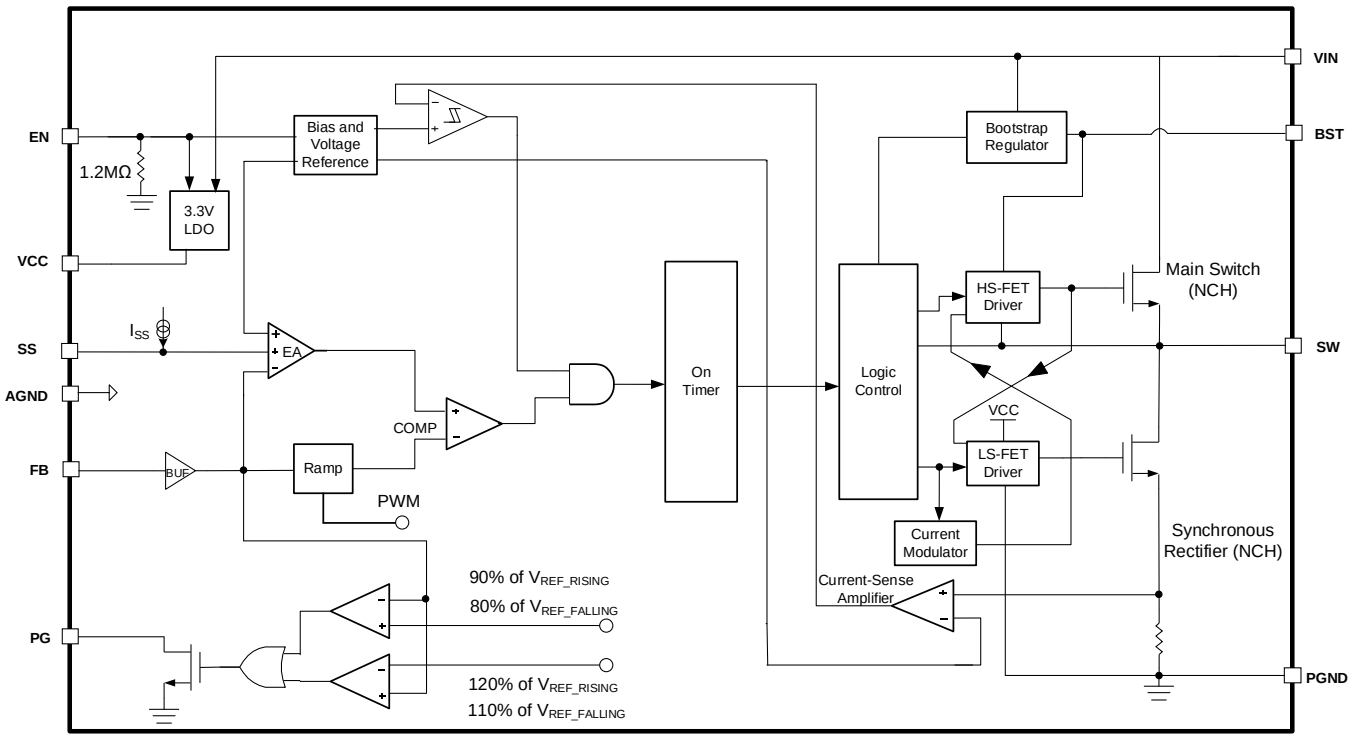

Figure 1: Functional Block Diagram

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OPERATION

The MP8774C is a fully integrated, synchronous, rectified, step-down switch-mode converter. Constant-on-time (COT) control provides fast transient response and eases loop stabilization. Figure 2 shows the simplified ramp compensation block in the MP8774C.

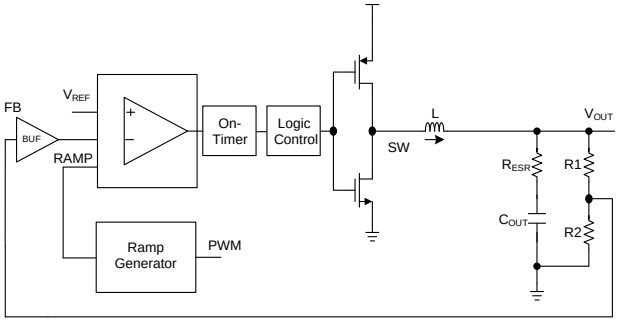

Figure 2: Simplified Ramp Compensation Block

At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on when the ramp voltage (V_{RAMP}) drops below the error amplifier's (EA's) output voltage (V_{EAO}). This indicates an insufficient output voltage (V_{OUT}). The on time is determined by both the V_{OUT} and the input voltage (V_{IN}) to make the switching frequency (f_{SW}) fairly constant across the entire V_{IN} range.

After the on time elapses, the HS-FET turns off. The HS-FET turns on again when V_{RAMP} drops below V_{EAO}. By repeating this operation, the converter regulates V_{OUT}. The integrated low-side MOSFET (LS-FET) turns on once the HS-FET turns off to minimize conduction loss. If both the HS-FET and LS-FET turn on at the same time, a dead short occurs between the input and GND. This is known as shoot-through. To avoid shoot-through, a dead time (DT) is generated internally between the HS-FET off time and LS-FET on time, and vice versa.

Internal compensation is applied for COT control to provide more stable operation, even when ceramic capacitors are used as output capacitors. This internal compensation improves jitter performance without affecting line or load regulation.

Pulse-Width Modulation (PWM) Mode

The MP8774C operates in forced continuous conduction mode (FCCM). In FCCM, f_{SW} is fairly constant, and the output ripple remains almost constant throughout the entire load range. When V_{RAMP} is below V_{EAO}, the HS-FET turns on for a fixed interval determined by the one-shot on-timer. When the HS-FET turns off, the LS-FET turns on until the next period (see Figure 3).

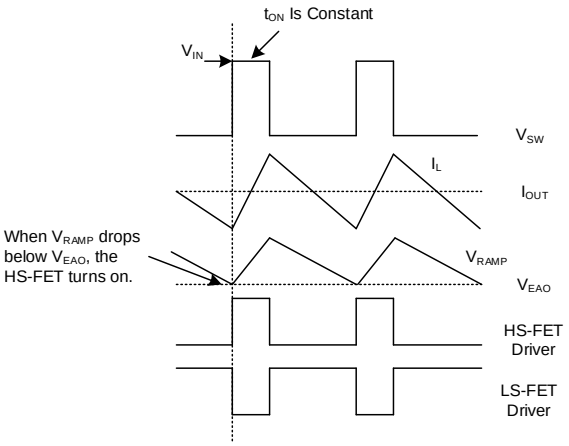

Figure 3: PWM Operation

In FCCM, f_{SW} is fairly constant. This is called pulse-width modulation (PWM) mode.

VCC Regulator

The 3.4V internal regulator (VCC) powers most of the internal circuitry. This regulator takes V_{IN} and operates across the entire V_{IN} range. When V_{IN} exceeds 3.4V, the regulator output is in full regulation. When V_{IN} falls below 3.4V, the regulator output decreases, following V_{IN}. A 1µF decoupling ceramic capacitor is required at VCC.

Enable (EN)

EN is a digital control pin that turns the converter on and off. Pull EN above 1.25V to turn the converter on; pull EN below 1V to turn it off. When floating, EN is pulled down to AGND via an internal 1.2MΩ resistor. EN can be connected directly to V_{IN}, and supports up to 18V of V_{IN}.

The MP8774C turns on when EN pulls high, and turns off when EN pulls low or is floating. EN can also be driven by an analog or digital control logic signal to enable or disable the device. The MP8774C provides accurate EN thresholds, so a resistor divider connected from VIN to AGND can configure the VIN threshold.

If there is no dedicated EN control logic signal, it is recommended to use a resistor divider in applications to avoid under-voltage lockout

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(UVLO) bouncing during start-up and shutdown. The V_{IN} UVLO can be calculated with Equation (1):

$$V_{IN\ START}(V) = 1.25V \times \frac{R_{UP} + R_{DOWN}\ //\ 1200k\Omega}{R_{DOWN}\ //\ 1200k\Omega} \quad (1)$$

For example, if R_{UP} = 499kΩ and R_{DOWN} = 100kΩ, set V_{IN_START} to 8V. Figure 4 shows how to set up the V_{IN} UVLO.

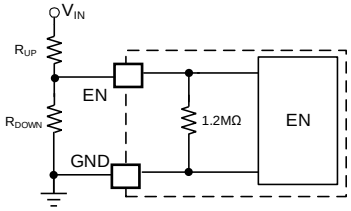

Figure 4: Setting the V_{IN} UVLO Threshold

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP8774C UVLO comparator monitors the internal regulator voltage (V_{CC}). The V_{CC} UVLO rising threshold is about 2.8V, while its falling threshold is 2.45V.

Once V_{CC} exceeds the UVLO rising threshold, the MP8774C starts up. The MP8774C shuts down if V_{CC} drops below the UVLO falling threshold. UVLO is a non-latch protection.

Soft Start (SS)

The MP8774C employs a soft start (SS) mechanism to ensure that the output ramps up smoothly during start-up. When EN goes high, an internal current source (6μA) charges up the SS capacitor (C_{SS}). When the device starts up, the SS voltage (V_{SS}) is below the reference voltage (V_{REF}). The PWM comparator uses V_{SS} as its reference, and V_{OUT} ramps up smoothly with V_{SS}. Once V_{SS} exceeds V_{REF}, the PWM comparator uses V_{REF} as its reference, and the C_{SS} continues to be charged until V_{SS} = V_{CC}. At this point, SS finishes and the device enters steady-state operation.

C_{SS} can be calculated with Equation (2):

$$C_{SS}(nF) = 0.83 \times \frac{t_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} \quad (2)$$

Where I_{SS} is 6μA, and V_{REF} is 0.6V. If the output capacitance is large, it is not recommended to set the soft-start time (t_{SS}) too short. Otherwise, the current limit (I_{LIMIT}) can be reached easily during SS.

The minimum t_{SS} is limited to 1ms internally. To set a longer t_{SS} using the capacitors, see Equation (2). For example, if C_{SS} = 22nF, then t_{SS} is about 2.7ms.

Avoid using a C_{SS} below 4.7nF.

Power Good (PG) Indicator

PG is the open drain of a MOSFET that connects to VCC or another voltage source through a resistor (e.g. 100kΩ). The MOSFET turns on when V_{IN} is applied, and PG is pulled to AGND before SS is ready. The PG pin pulls high when SS completes. When the feedback voltage (V_{FB}) drops to 80% of V_{REF}, PG is pulled low.

When UVLO or over-temperature protection (OTP) occurs, PG is pulled low immediately. When an over-current (OC) condition occurs, the PG pin immediately pulls low if the device enters hiccup mode. When an over-voltage (OV) condition occurs, PG is pulled low when V_{FB} exceeds 120% of V_{REF}. If V_{FB} falls below 110% of V_{REF}, PG is pulled high.

If the input supply fails to power the MP8774C, PG is clamped low, even though PG is tied to an external DC source through a pull-up resistor. Figure 5 shows the relationship between the PG voltage (V_{PG}) and the pull-up current.

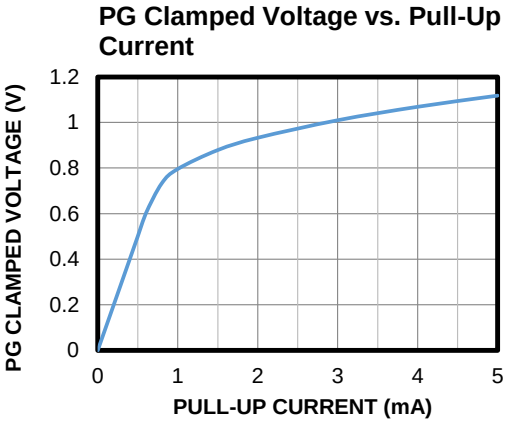

Figure 5: PG Clamped Voltage vs. Pull-Up Current

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Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MP8774C has valley I_{LIMIT} (I_{LIMIT_VALLEY}) control. The LS-FET monitors the current flowing through the LS-FET. The HS-FET waits until I_{LIMIT_VALLEY} is removed before turning on again. Meanwhile, V_{OUT} drops until V_{FB} is below the under-voltage protection (UVP) threshold (typically 50% below V_{REF}). Once UV is triggered, the device enters hiccup mode to periodically restart the part.

During over-current protection (OCP), the MP8774C attempts to recover from the over-current (OC) fault with hiccup mode. This means that the chip disables the output power stage, discharges C_{SS}, and attempts to soft start again automatically. If the OC condition still remains after SS finishes, the device repeats this operation until the OC condition disappears. Then the output rises back to the regulation level. OCP is a non-latch protection.

Pre-Biased Start-Up

The MP8774C is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the bootstrap (BST) voltage (V_{BST}) is refreshed and charged, and V_{SS} is charged as well. If V_{BST} exceeds its rising threshold and V_{SS} exceeds the sensed output voltage at FB, the part starts up and begins normal operation.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled again.

Floating Driver and Bootstrap (BST) Charging

An external BST capacitor (C_{BST}) powers the floating power MOSFET driver. This floating driver has its own UVLO protection, with a rising threshold of 1.7V and a hysteresis of 150mV. V_{IN} regulates V_{BST} internally through D1, M1, R4, C_{BST}, L_{OUT}, and C_{OUT} (see Figure 6). If (V_{IN} - V_{SW}) exceeds 3.3V, U2 regulates M1 to maintain a 3.3V V_{BST} across C_{BST} The BST resistor (R4) is recommended to be less than 4.7Ω.

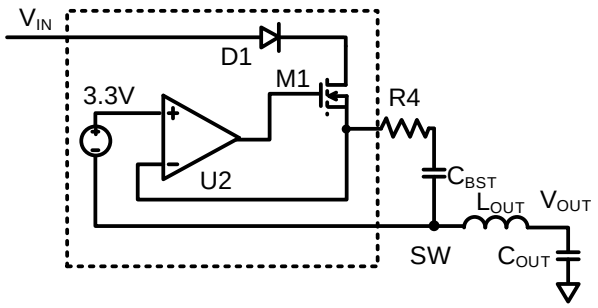

Figure 6: Internal Bootstrap Charger

Start-Up and Shutdown Circuit

If both V_{CC} and the EN voltage (V_{EN}) exceed their respective thresholds, the chip starts up. The reference block starts up first, generating a stable V_{REF} and current. Then the internal regulator is enabled to provide a stable supply for the remaining circuitry.

Three events can shut down the chip: EN being pulled low, V_{IN} going low, and thermal shutdown. The shutdown procedure starts by initially blocking the signaling path to avoid any fault triggering. Then the internal supply rail is pulled down.

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APPLICATION INFORMATION

Setting the Output Voltage

An external resistor divider is used to set the output voltage (V_{OUT}). First, choose a value for R2. R2 should be chosen carefully, as a small R2 leads to considerable quiescent current (I_Q) loss, while a large R2 makes FB noise-sensitive. R2 is recommended to be between 2kΩ and 100kΩ. Set the current through R2 to be below 250μA for a good balance between system stability and no-load loss. Then R1 can be calculated with Equation (3):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (3)$$

Figure 7 shows the feedback circuit.

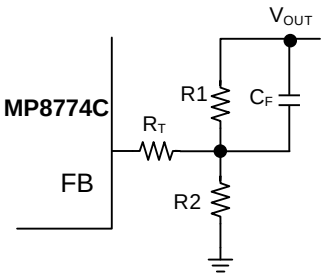

Figure 7: Feedback Network

Table 1 lists the recommended resistances for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

VOUT (V)	R1 (kΩ)	R2 (kΩ)	L (μH)	Cf (pF)	Rt (kΩ)
1	20	30	0.33	56	1
1.2	20	20	0.33	56	1
1.5	20	13	0.33	56	1
1.8	20	10	0.47	56	1
2.5	20	6.34	0.47	56	1
3.3	20	4.42	0.56	56	1
5	20	2.7	0.68	56	1

Selecting the Inductor

An inductor is required to supply constant current to the output load while being driven by the switched input voltage (V_{IN}). A larger-value inductor results in less ripple current and a lower V_{OUT} ripple (ΔV_{OUT}); however, a larger-value inductor also has a larger physical footprint, higher series resistance, and lower saturation current. A good rule for determining the inductance is to ensure that the peak inductor current (I_{LP}) is below the maximum switching current limit (I_{LIMIT}). The inductance can be calculated with Equation (4):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum I_{LP}. I_{LP} can be calculated with Equation (5):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

Selecting the Input Capacitor

The step-down converter has a discontinuous input current (I_{IN}), and requires a capacitor to supply AC current to the converter while maintaining the DC V_{IN}. For the best performance, use ceramic capacitors placed as close to the VIN pin as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable amid temperature fluctuations. The capacitors must also have a ripple current rating greater than the converter's maximum input ripple current. The input ripple current (I_{CIN}) can be estimated with Equation (6):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (6)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (7):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (7)$$

For simplification, choose an input capacitor (C_{IN}) with an RMS current rating greater than half of the maximum load current (I_{LOAD}).

C_{IN} determines the converter's V_{IN} ripple (ΔV_{IN}). If there is a ΔV_{IN} requirement in the system, choose a C_{IN} that meets the specification.

ΔV_{IN} can be estimated with Equation (8):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

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The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (9):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (9)$$

Selecting the Output Capacitor

An output capacitor (C_{OUT}) is required to maintain the DC V_{OUT}. Ceramic or POSCAP capacitors are recommended. ΔV_{OUT} can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (10)$$

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency (f_{SW}). ΔV_{OUT} is mainly caused by the capacitance. For simplification, ΔV_{OUT} can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (11)$$

For POSCAP capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (12)$$

In addition to considering ΔV_{OUT}, choosing a larger C_{OUT} can result in better load transient response. Consider the maximum C_{OUT} limitation in the design application. If C_{OUT} is too high, then V_{OUT} cannot reach the design value during the soft-start time (t_{SS}), and fails to regulate.

The maximum C_{OUT} (C_{OUT_MAX}) can be estimated with Equation (13):

$$C_{OUT_MAX} = (I_{LIMIT_AVG} - I_{OUT}) \times t_{SS} / V_{OUT} \quad (13)$$

Where I_{LIMIT_AVG} is the average start-up current during t_{SS}.

Design Example

Table 2 shows a design example when using ceramic capacitors.

Table 2: Design Example

V_{IN}	12V
V_{OUT}	1V
I_{OUT}	12A

For a detailed application schematic, see Figure 9 on page 18. The typical performance and waveforms are shown in the Typical Characteristics section on page 8. For more device applications, refer to the related evaluation board datasheet.

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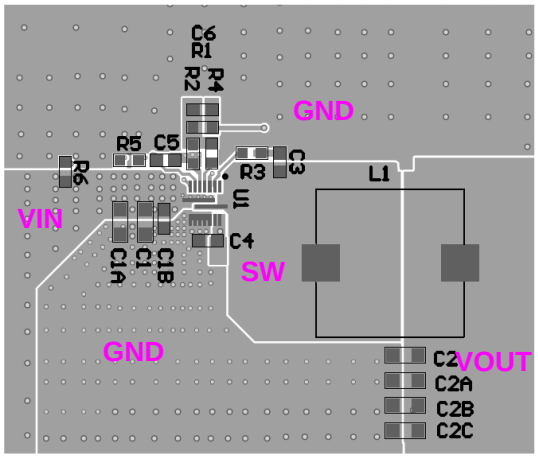
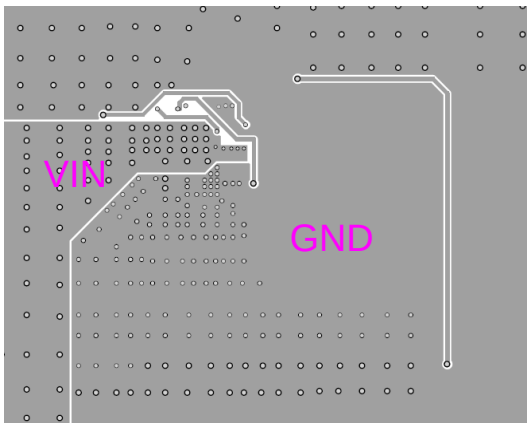
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. Poor layout design can result in poor load or line regulation and stability issues. It is recommended to use a 4-layer board layout, where the two middle layers are ground layers. For the best results, refer to Figure 8 and follow the guidelines below:

1. Route the high-current paths (PGND, VIN, and SW) very close to the device using short, direct, and wide traces.
2. Place the input capacitor as close to VIN and PGND as possible.
3. Place a VCC decoupling capacitor close to the device.
4. Connect AGND and PGND at the point of the VCC capacitor's ground connection.
5. Place the external feedback resistors next to FB.
6. Keep the switching node (SW) short and away from the feedback network.



Top Layer



Bottom Layer

Figure 8: Recommended Layout

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TYPICAL APPLICATION CIRCUIT

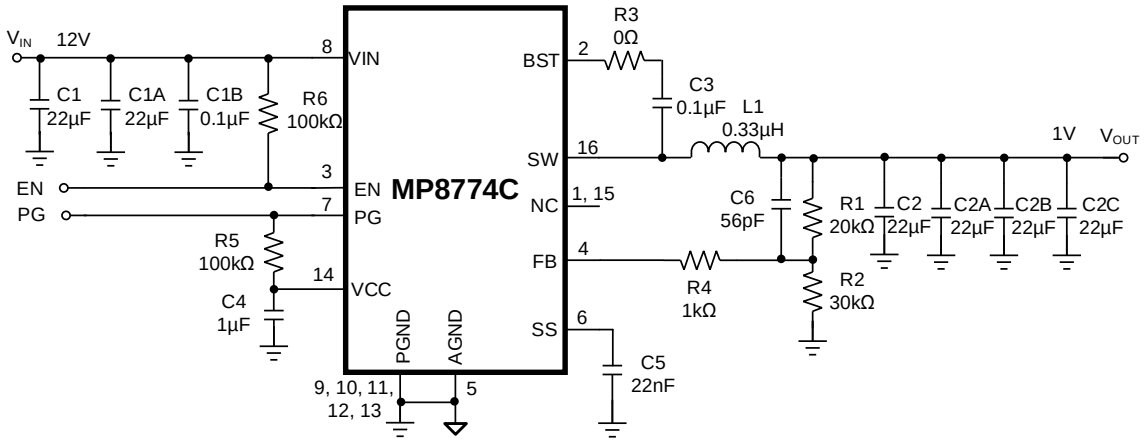

Figure 9: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 12A) (8)

Note:

8) See the Selecting the Input Capacitor section on page 15 for when V_{IN} is low.

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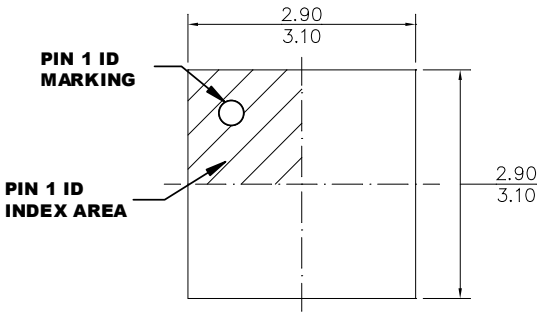
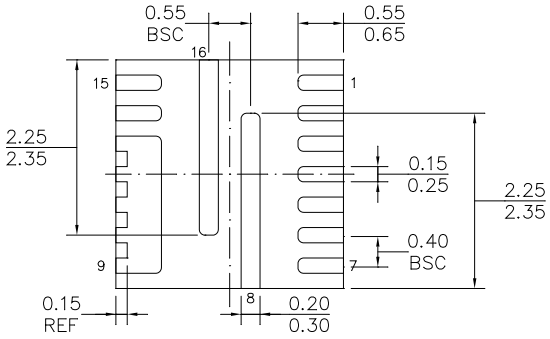
PACKAGE INFORMATION

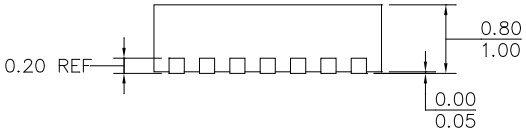
QFN-16 (3mmx3mm)



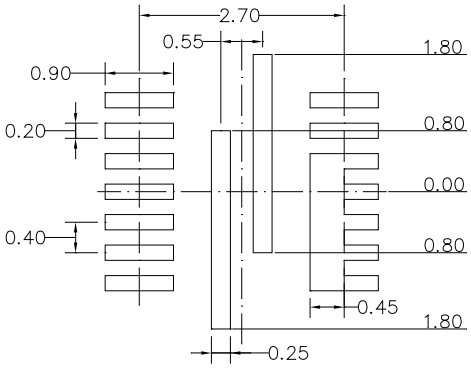
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

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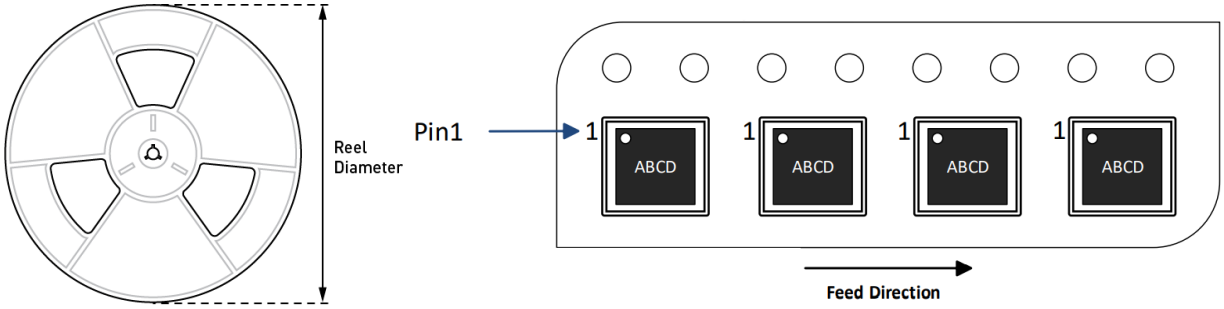
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tray	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP8774CGQ-Z	QFN-16 (3mmx3mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/10/2023	Initial Release	-

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