MP8719

26V, 12A, Low I_Q, High-Current, Synchronous Buck Converter with ±1A LDO and Buffered Reference

The Future of Analog IC Technology

DESCRIPTION

The MP8719 provides a complete power supply with the highest power density for DDR3, DDR3L, LPDDR3, and DDR4 memory. The MP8719 integrates a high-frequency, synchronous, rectified, step-down, switch-mode converter (VDDQ) with a 1A sink/source LDO (VTT) and buffered low-noise reference (VTTREF).

The MP8719 operates at high efficiency over a wide output current load range based on MPS's proprietary switching loss reduction technology and internal low $R_{DS(ON)}$ power MOSFETs.

Adaptive constant-on-time (COT) control mode provides fast transient response and eases loop stabilization. The DC auto-tune loop provides good load and line regulation.

The VTT LDO provides 1A of sink/source current capability and requires only a 22µF ceramic capacitor. The VTTREF tracks VDDQ/2 with excellent 1% accuracy.

Full protection features include over-current (OC) limit, over-voltage protection (OVP), under-voltage protection (UVP), over-temperature warning (OTW), and thermal shutdown.

The MP8719 requires a minimal number of external components and is available in a QFN-16 (3mmx3mm) package.

FEATURES

- Wide 4.5V to 26V Operating Input Range
- 135µA Low Quiescent Current
- 12A Continous Output Current
- 13A Peak Output Current
- Selectable Ultrasonic Mode (USM)
- Selectable 500kHz/700kHz Switching Frequency
- Built-In ±1A VTTLDO
- 1% Buffered VTTREF Output
- Adaptive COT for Fast Transient
- DC Auto-Tune Loop
- Stable with POSCAP and Ceramic Output Capacitors
- Over-Temperature Warning (OTW)
- Internal Soft Start (SS)
- Output Discharge
- OCL, OVP, UVP, and Thermal Shutdown
- Latch-Off Reset via EN or Power Cycle
- Available in a QFN-16 (3mmx3mm) Package

APPLICATIONS

- Televisions
- Networking Systems
- Distributed Power Systems
- Set-Top-Box

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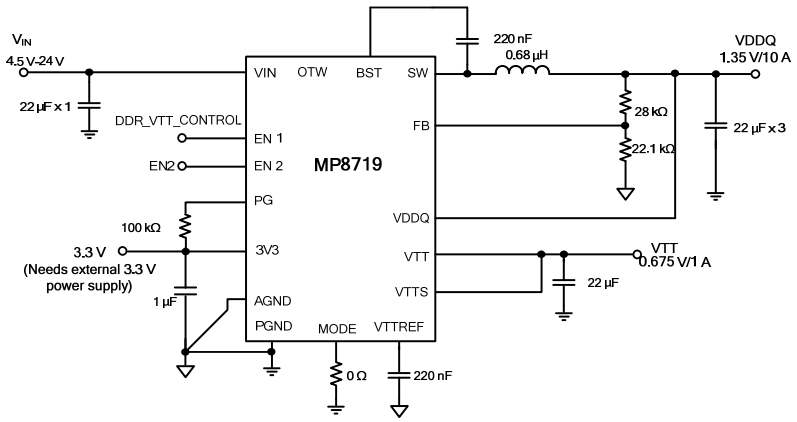
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP8719GQ	QFN-16 (3mmx3mm)	*See Below*

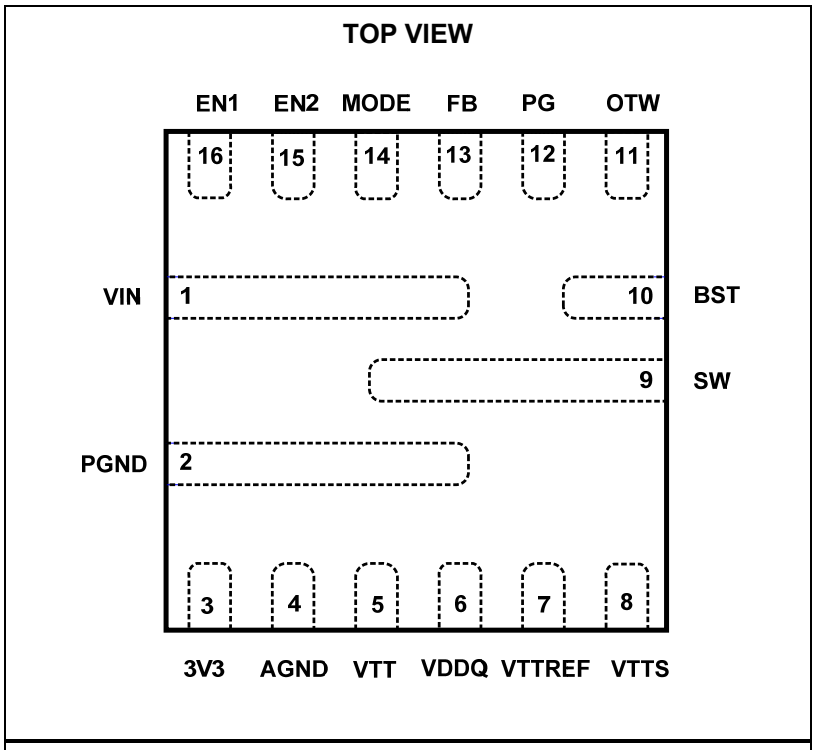
* For Tape & Reel, add suffix –Z (e.g. MP8719GQ–Z)

TOP MARKING

AZFY
LLL

AZF: Product code of MP8719GQ
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



QFN-16 (3mmx3mm)

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (VIN) 26V
V_{SW} (DC) .....-1V to VIN + 0.3V
V_{SW} (25ns).....-3.6V to VIN + 4V
V_{BST} ..... V_{SW} + 4.5V
I_{EN1}, I_{EN2} 100µA
All other pins .....-0.3V to +4.5V
Continuous power dissipation (T_A = +25°C) (2)
QFN-16 (3mmx3mm)..... 2.3W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (VIN).....4.5V to 24V
Supply voltage (V_{CC}) .....3.15V to 3.5V
Output voltage (V_{DDQ})..... 0.6V to 3.3V (4)
I_{EN1}, I_{EN2} 50µA
Operating junction temp. (T_J)... -40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
QFN-16 (3mmx3mm).....	55.....	13...	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) For applications that need 3.3V < Vout < 5.5V, special design requirements are needed. Please refer to the Application Information section on page 16. VDDQ must be ≤3.3V.
5) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

VIN = 12V, 3V3 = 3.3V, T_J = 25°C, R_{MODE} = 0Ω, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
3V3 supply current in normal mode	I_{3V3}	V_{EN1} = V_{EN2} = 3V, no load		185		μA
3V3 supply current in S3 mode	I_{3V3_S3}	V_{EN1} = 0V, V_{EN2} = 3V, no load		135		μA
3V3 shutdown current	$I_{3V3\ SDN}$	V_{EN1} = V_{EN2} = 0V, no load			1	μA
MOSFET						
High-side switch on resistance	HS_{RDS-ON}	T_J = 25°C		19.5		mΩ
Low-side switch on resistance	LS_{RDS-ON}	T_J = 25°C		6.6		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 0V		0	1	μA
Current Limit						
Low-side valley current limit	I_{LIMIT}		12	13	14	A
Switching Frequency and Minimum Off Time						
Switching frequency	F_S	R_{MODE} = 0Ω		700		kHz
		R_{MODE} = 150kΩ		500		kHz
Constant on timer	T_{ON}	VIN = 6V, V_{OUT} = 3V, R_{MODE} = 150kΩ	1100	1200	1300	ns
Minimum on time (6)	$T_{ON\ MIN}$			70		ns
Minimum off time (6)	$T_{OFF\ MIN}$			300		ns
Ultrasonic Mode (USM)						
Ultrasonic mode operation period	T_{USM}	V_{FB} = 0.62V		32		μs
Protection						
OVP threshold	V_{OVP}		125	130	135	$\%V_{REF}$
UVP-1 threshold	V_{UVP-1}		70%	75%	80%	V_{REF}
UVP-1 foldback timer (6)	T_{UVP-1}			30		μs
UVP-2 threshold	V_{UVP-2}		45%	50%	55%	V_{REF}
Reference and Soft Start, Soft Stop						
Reference voltage	V_{REF}		594	600	606	mV
Feedback current	I_{FB}	V_{FB} = 0.62V		10	50	nA
Soft-start time	T_{SStart}	EN to PG up	1.8	2.2	2.6	ms
Soft-stop time	T_{SStop}			2		ms
Enable (EN) and Under-Voltage Lockout (UVLO)						
EN1 rising threshold	$V_{EN1\ TH}$		0.54	0.59	0.64	V
EN1 hysteresis	$V_{EN1-HYS}$			125		mV
EN2 rising threshold	$V_{EN2\ TH}$		1.12	1.22	1.32	V
EN2 hysteresis	$V_{EN2-HYS}$			125		mV
Enable input current	$I_{EN1/2}$	$V_{EN1/2}$ = 2V			5	μA
		$V_{EN1/2}$ = 0V			1	

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ELECTRICAL CHARACTERISTICS *(continued)*

VIN = 12V, 3V3 = 3.3V, T_J = 25°C, R_{MODE} = 0Ω, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VCC UVLO threshold rising	VCC_{Vth}		2.9	3.0	3.1	V
VCC UVLO threshold hysteresis	VCC_{HYS}			220		mV
VIN UVLO threshold rising	VIN_{VTH}			4.2	4.4	V
VIN UVLO threshold hysteresis	VIN_{HYS}			360		mV
Power Good (PG)						
PG when FB rising (good)	$PG_{Rising(GOOD)}$	V_{FB} rising, percentage of V_{FB}		95		%
PG when FB falling (fault)	$PG_{Falling(Fault)}$	V_{FB} falling, percentage of V_{FB}		90		
PG when FB rising (fault)	$PG_{Rising(Fault)}$	V_{FB} rising, percentage of V_{FB}		115		
PG when FB falling (good)	$PG_{Falling(GOOD)}$	V_{FB} falling, percentage of V_{FB}		105		
PG low to high delay	PG_{Td}			3		µs
EN low to PG low delay	$PG_{Td\ EN\ low}$				1	µs
PG sink current capability	V_{PG}	Sink 4mA			0.4	V
VTTREF Output						
VTTREF output voltage	V_{TTREF}			V_{DDQ}/2		
Output voltage tolerance to VDDQ	V_{TTREF}/ V_{DDQ}	I_{VTTREF} < 0.1mA, 1V < V_{DDQ} < 1.5V	49.2%	50%	50.8%	
		I_{VTTREF} < 10mA, 1V < V_{DDQ} < 1.5V	49%	50%	51%	
Current limit	$I_{LIMIT\ VTTREF}$		13	15		mA
VTT LDO						
VTT output voltage	V_{TT}			V_{DDQ}/2		
VTT tolerance to VTTREF	V_{TT}-V_{TTREF}	-10mA < I_{VTT} < 10mA, V_{DDQ} = [1V - 1.5V]	-15		15	mV
		-0.6A < I_{VTT} < 0.6A, V_{DDQ} = [1V - 1.5V]	-20		20	mV
		-1A < I_{VTT} < 1A, V_{DDQ} = [1V - 1.5V]	-25		25	mV
Source current limit	$I_{LIMIT\ SOURCE}$		1.2	1.5		A
Sink current limit	$I_{LIMIT\ SINK}$		1.2	1.5		A
OTW						
Over-temperature warning (6)	T_{OTW}			130		°C
OTW hysteresis (6)	$T_{OTW\ HYS}$			25		°C
OTW sink current capability	V_{OTW}	Sink 4mA			0.4	V
OTW leakage current	I_{OTW}	V_{OTW} = 3.3V			1	µA
OTW assertion time (6)	T_{OTW}			32		ms
Thermal Protection						
Thermal shutdown (6)	T_{SD}			145		°C
Thermal shutdown hysteresis	T_{SD_HYS}			25		°C

NOTE:

6) Guaranteed by design.

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PIN FUNCTIONS

PIN #	Name	Description
1	VIN	**Supply voltage.** VIN supplies power for the internal MOSFET and regulators. The MP8719 operates from a +4.5V to +26V input rail. An input capacitor is needed to decouple the input rail. Use wide PCB traces and multiple vias to make the connection.
2	PGND	**Power ground.** Use wide PCB traces and multiple vias to make the connection.
3	3V3	**External 3V3 VCC input for control and driver.** Place a 1μF decoupling capacitor close to 3V3 and AGND. It is recommended to form an R-C filter.
4	AGND	**Analog ground.** The internal reference is referred to AGND. Connect GND of the FB divider resistor to AGND for better load regulation.
5	VTT	**VTT LDO output.** Decouple with a minimum 22μF ceramic capacitor as close to VTT as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
6	VDDQ	**Input of VTTLDO.** VDDQ is also used for V_{OUT} sense. Do not float VDDQ at any time. Connect VDDQ to the output capacitor of the regulator directly with a thick (>100mil) trace.
7	VTTREF	**Buffered VTT reference output.** Decouple VTTREF with a minimum 0.22μF ceramic capacitor as close to it as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
8	VTTS	**VTT output sense.** Connect VTTS to the output capacitor of the VTT regulator directly.
9	SW	**Switch output.** Connect SW to the inductor and bootstrap capacitor. SW is connected to VIN when the HS-FET is on. SW is connected to PGND when the LS-FET is on. Use wide and short PCB traces to make the connection. SW is noisy, so keep sensitive traces away from SW.
10	BST	**Bootstrap.** A capacitor connected between SW and BST is required to form a floating supply across the high-side switch driver.
11	OTW	**Over-temperature status.** OTW is used to indicate that the MP8719 is close to OTP. OTW is pulled low once the junction temperature is higher than the over-temperature warning threshold. OTW can be left open if not used.
12	PG	**Power good output.** PG is an open-drain signal. PG is high if the output voltage is within a proper range.
13	FB	**Feedback.** An external resistor divider from the output to GND (tapped to FB) sets the output voltage. Place the resistor divider as close to FB as possible. Avoid vias on the FB traces.
14	MODE	**Switching frequency and ultrasonic mode selection.** A 1% pull-down resistor is needed on MODE.
15	EN2	**Enable.** EN1 and EN2 are digital inputs which are used to enable or disable the internal regulators. Once EN1 = EN2 = 1, the VDDQ regulator, VTT LDO, and VTTREF output are turned on. When EN1 = 0 and EN2 = 1, all the regulators are on except VTT LDO. All regulators are turned off when EN2 = 0 or EN1 = EN2 = 0. Do not float EN1 at any time. If the VTT LDO function is not used, tie EN1 to GND.
16	EN1	

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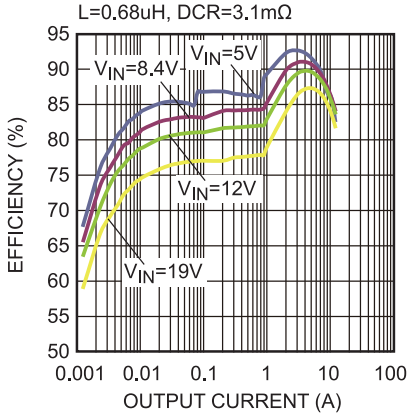
TYPICAL PERFORMANCE CHARACTERISTICS

VIN = 20V, VDDQ = 1.35V, L = 0.68μH/3.1mΩ, F_{SW} = 700kHz, unless otherwise noted.

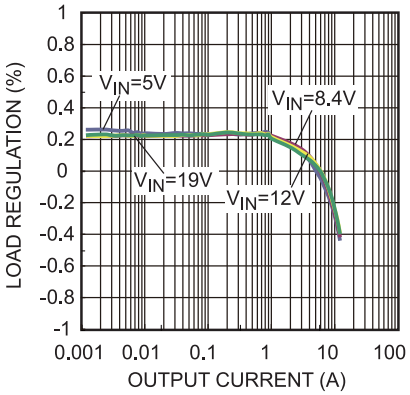
Efficiency vs. Load Current

V_{DDQ}=1.35V, F_{SW}=700kHz, L=0.68uH, DCR=3.1mΩ



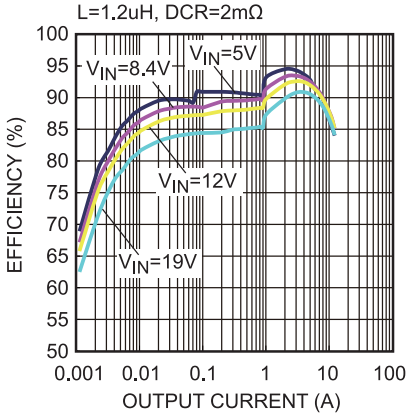
Load Regulation

V_{DDQ}=1.35V, F_{SW}=700kHz, L=0.68μH, DCR=3.1mΩ



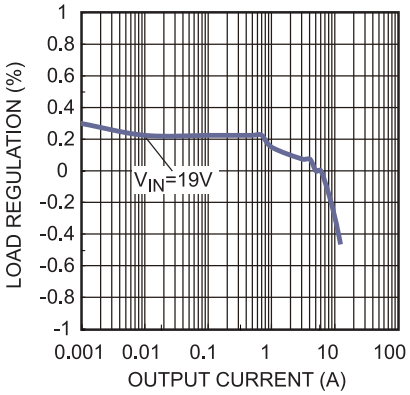
Efficiency vs. Load Current

V_{DDQ}=1.35V, F_{SW}=500kHz, L=1.2uH, DCR=2mΩ



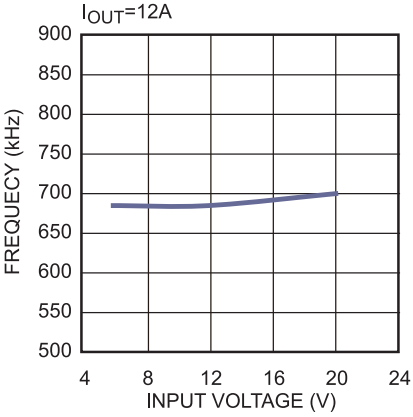
Load Regulation

V_{DDQ}=1.35V, F_{SW}=500kHz, L=1.2uH, DCR=2mΩ



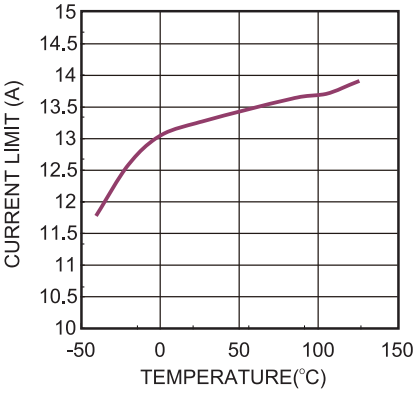
Switch Frequency vs. Input Voltage

I_{OUT}=12A



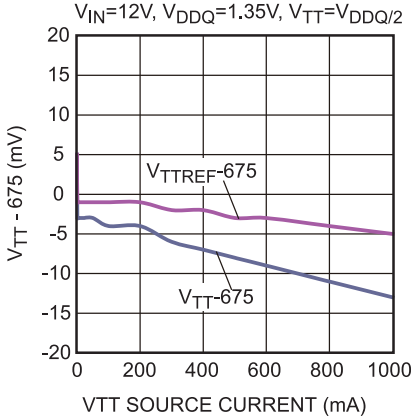
Valley Current Limit vs. Temperature

V_{IN}=12V



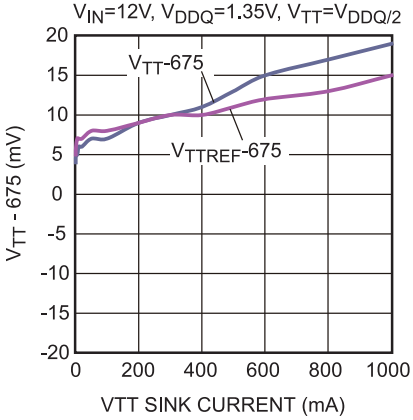
VTT Source Current Load Regulation

V_{IN}=12V, V_{DDQ}=1.35V, V_{TT}=$V_{DDQ/2}$



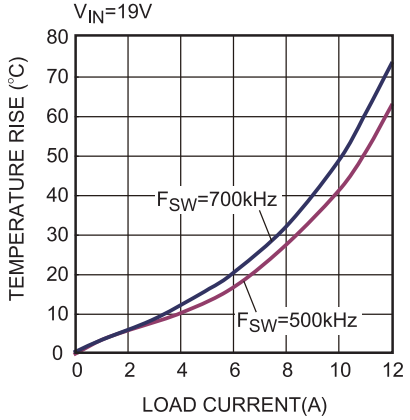
VTT Sink Current Load Regulation

V_{IN}=12V, V_{DDQ}=1.35V, V_{TT}=$V_{DDQ/2}$



Temperature Rise vs. Load Current

V_{IN}=19V



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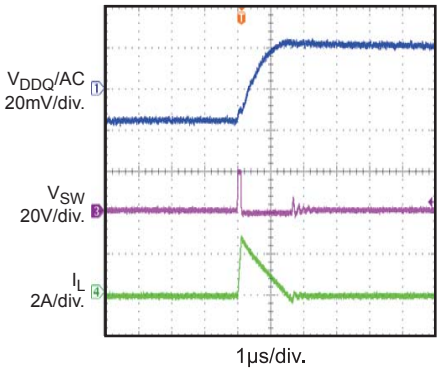
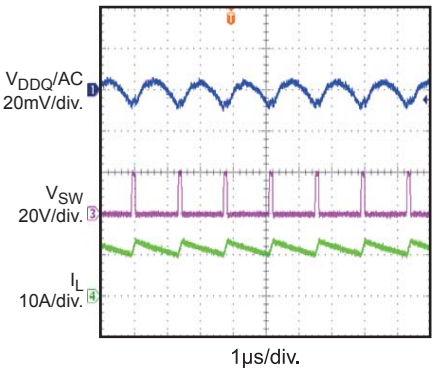
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 20V, VDDQ = 1.35V, L = 0.68µH/3.1mΩ, F_{SW} = 700kHz, unless otherwise noted.

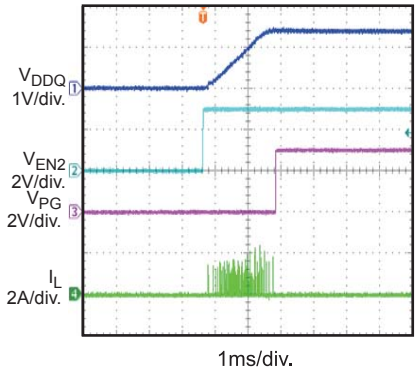
Output Voltage Ripple
I_{OUT} = 0A



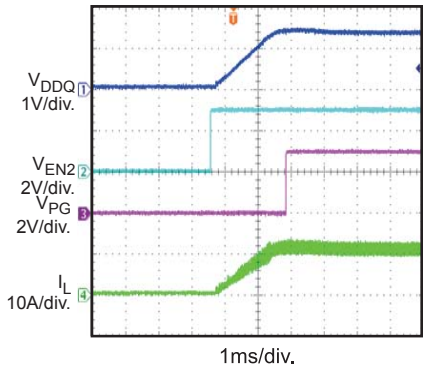
Output Voltage Ripple
I_{OUT} = 12A



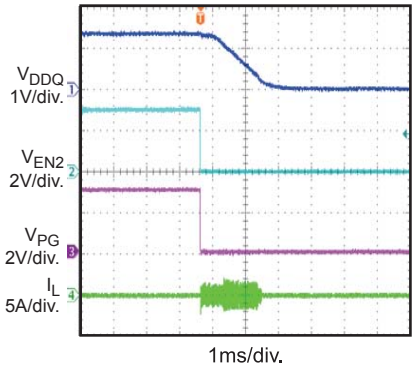
Start-Up through EN2
I_{OUT} = 0A



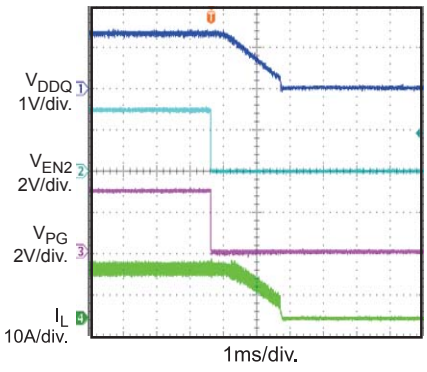
Start-Up through EN2
I_{OUT} = 12A



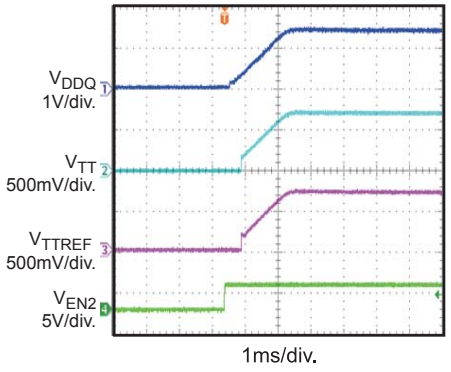
Shutdown through EN2
I_{OUT} = 0A



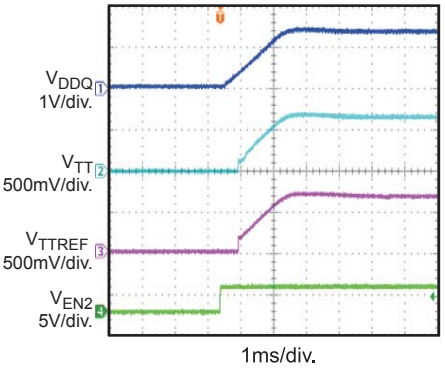
Shutdown through EN2
I_{OUT} = 12A



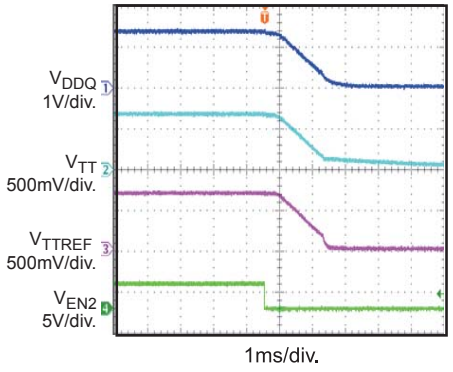
VTT Start-Up through EN2
I_{IVDDQ}=I_{VTT}=I_{VTTREF}=0A



VTT Start-Up through EN2
I_{IVDDQ}=12A, I_{VTT}=1A, I_{VTTREF}=0mA



VTT Shutdown through EN2
I_{IVDDQ}=I_{VTT}=I_{VTTREF}=0A



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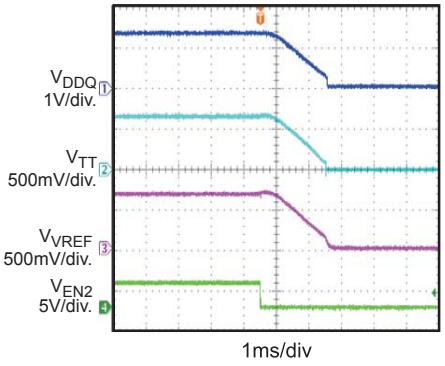
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 20V, VDDQ = 1.35V, L = 0.68µH/3.1mΩ, F_{SW} = 700kHz, unless otherwise noted.

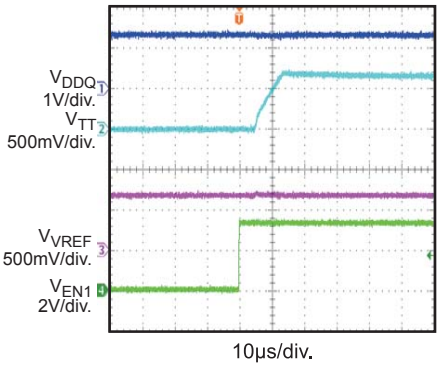
VTT Shutdown through EN2

I_{IVDDQ}=12A, I_{VTT}=1A, I_{VTTREF}=0mA



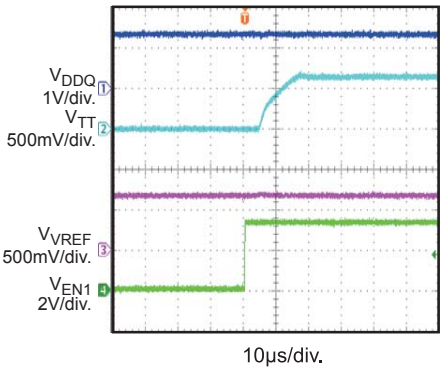
VTT Start-Up through EN1

I_{IVDDQ}=I_{VTT}=I_{VTTREF}=0A



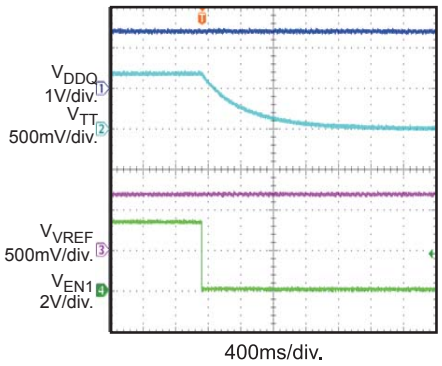
VTT Start-Up through EN1

I_{IVDDQ}=12A, I_{VTT}=1A, I_{VTTREF}=0mA



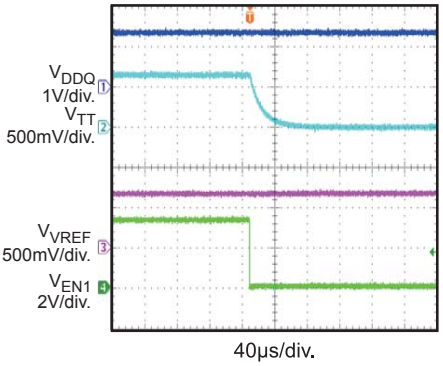
VTT Shutdown through EN1

I_{IVDDQ}=I_{VTT}=I_{VTTREF}=0A



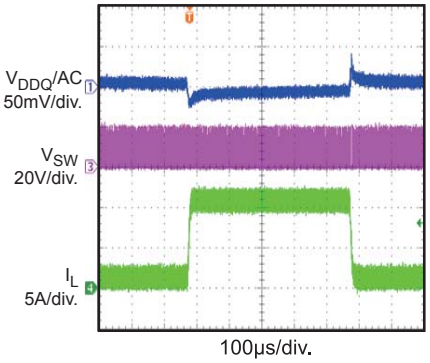
VTT Shutdown through EN1

I_{IVDDQ}=12A, I_{VTT}=1A, I_{VTTREF}=0mA



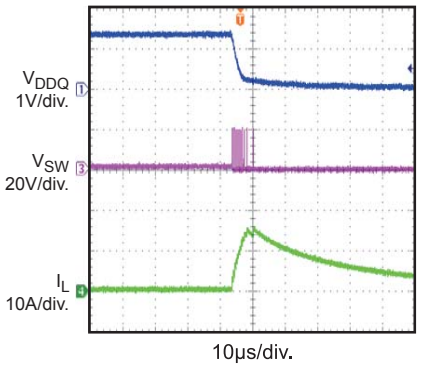
Transient

I_{OUT}=1.2-10.8A@1.6A/µs,
F_{SW}=700kHz,C_{OUT}=66µF



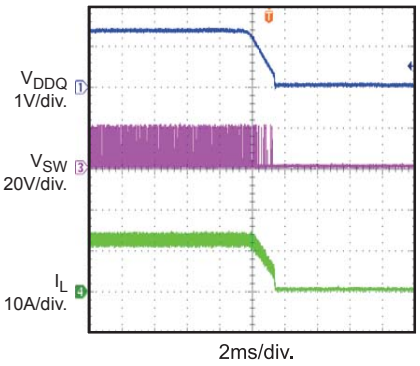
Short-Circuit Protection

I_{OUT} = 0A



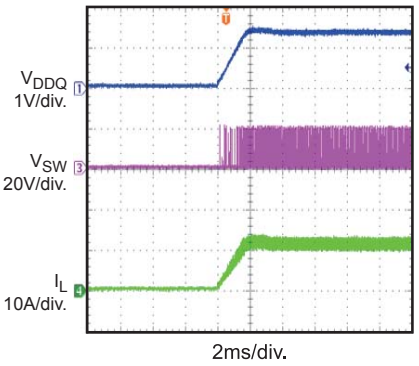
Thermal Shutdown

I_{OUT} = 12A in Temp Chamber



Thermal Recovery

I_{OUT} = 12A in Temp Chamber



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BLOCK DIAGRAM

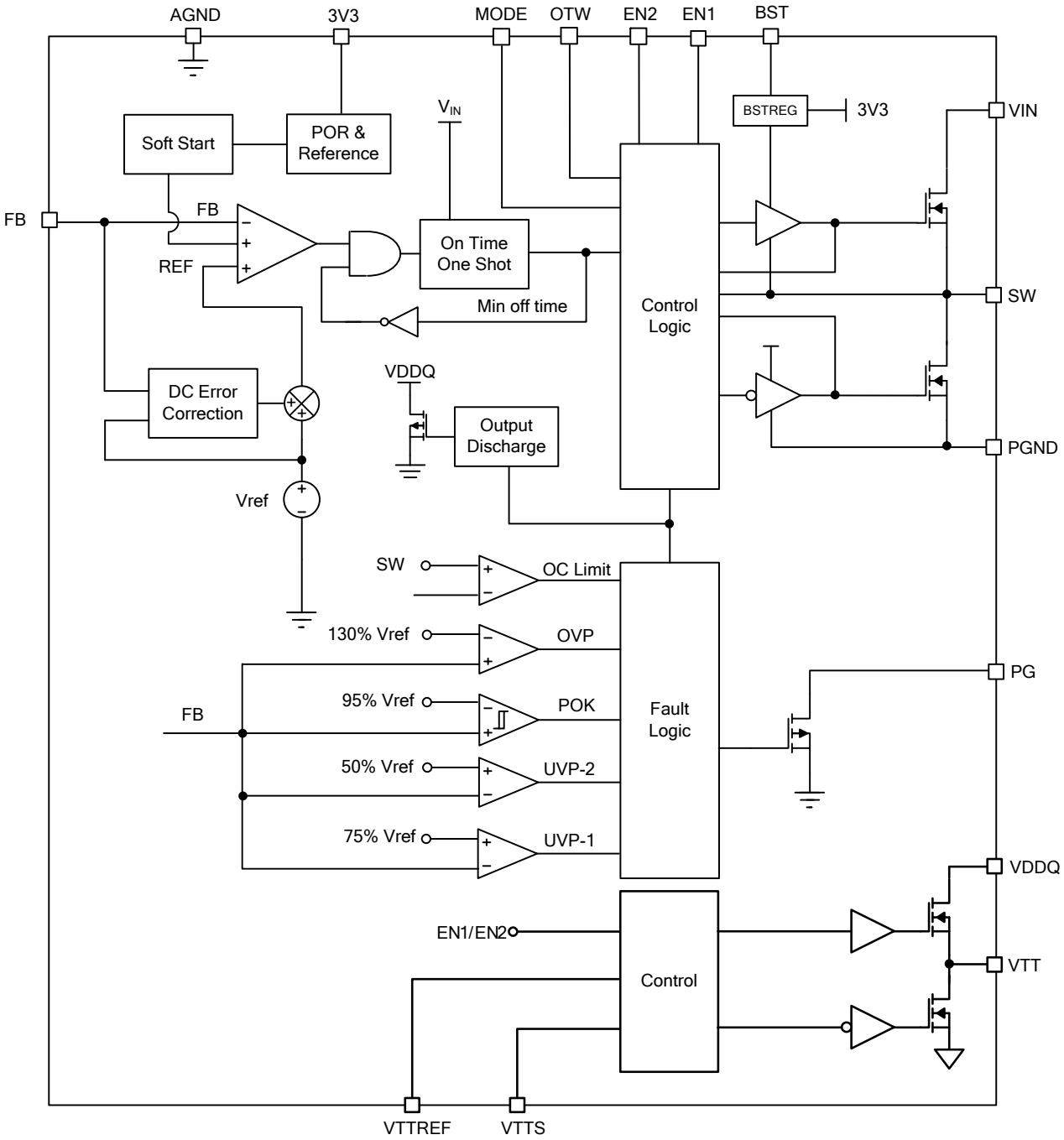

Figure 1: Functional Block Diagram

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OPERATION

Pulse-Width Modulation (PWM) Operation

The MP8719 is a fully integrated, synchronous, rectified, step-down, switch-mode converter with ±1A of LDO current. Constant-on-time (COT) control provides fast transient response and eases loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates an insufficient output voltage. The on period is determined by both the output voltage and the input voltage to make the switching frequency fairly constant over the input voltage range.

After the on period elapses, the HS-FET is turned off or enters an off state. The HS-FET is turned on again when V_{FB} drops below V_{REF}. By repeating operation this way, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS-FET is in its off state to minimize conduction loss. A dead short occurs between the input and GND if both the HS-FET and the LS-FET are turned on at the same time. This is called shoot-through. To prevent shoot-through, a dead time (DT) is generated internally between the HS-FET off and the LS-FET on period or the LS-FET off and the HS-FET on period.

Internal compensation is applied for COT control for stable operation, even when ceramic capacitors are used as output capacitors. This internal compensation improves jitter performance without affecting the line or load regulation.

Heavy-Load Operation

Continuous conduction mode (CCM) occurs when the output current is high and the inductor current is always above zero amps (see Figure 2). When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval, which is determined by the one-shot on timer. When the HS-FET is turned off, the LS-FET is turned on until the next period.

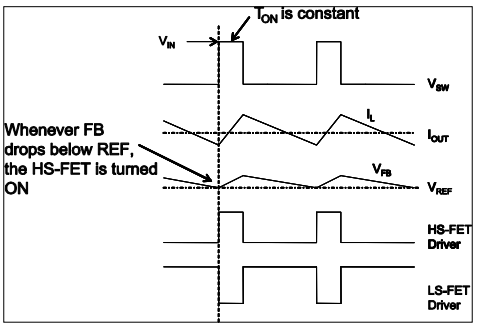

Figure 2: CCM Operation

In CCM operation, the switching frequency is fairly constant (PWM mode).

Light-Load Operation

When the load decreases, the inductor current decreases as well. Once the inductor current reaches zero, the MP8719 transitions from CCM to discontinuous conduction mode (DCM). DCM operation is shown in Figure 3.

When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval, which is determined by the one-shot on timer. When the HS-FET is turned off, the LS-FET is turned on until the inductor current reaches zero. In DCM operation, the V_{FB} does not reach V_{REF} when the inductor current is approaching zero. The LS-FET driver turns into tri-state (Hi-Z) when the inductor current reaches zero. A current modulator takes over the control of the LS-FET and limits the inductor current to less than -1mA. Therefore, the output capacitors discharge slowly to GND through the LS-FET. As a result, efficiency during light-load condition is improved greatly. The HS-FET does not turn on as frequently during light-load condition as it does during heavy-load condition (skip mode).

At a light-load or no-load condition, the output drops very slowly, and the MP8719 reduces the switching frequency naturally, achieving high efficiency at light load.

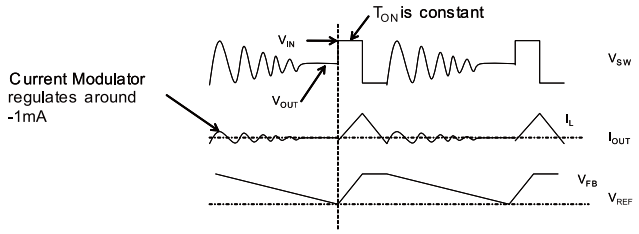

Figure 3: DCM Operation

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As the output current increases from light-load condition, the current modulation regulation time period becomes shorter. The HS-FET is turned on more frequently, making the switching frequency increase. The output current reaches the critical level when the current modulator time is zero. The critical level of the output current is determined with Equation (1):

$$I_{OUT_Critical} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_S \times V_{IN}} \quad (1)$$

The MP8719 enters PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

Jitter and FB Ramp

Jitter occurs in both PWM and skip mode when noise in the V_{FB} ripple propagates a delay to the HS-FET driver (see Figure 4 and Figure 5). Jitter affects system stability, with noise immunity proportional to the steepness of V_{FB}'s downward slope, so the jitter in DCM is usually larger than it is in CCM. However, V_{FB} ripple does not affect noise immunity directly.

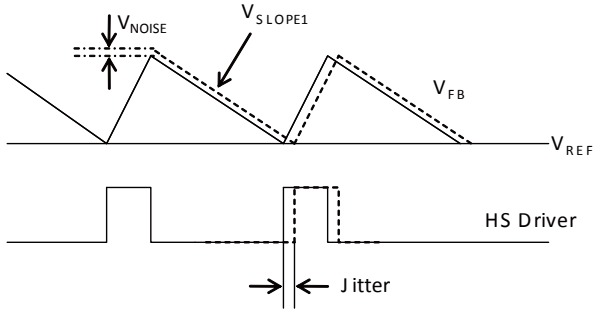

Figure 4: Jitter in PWM Mode

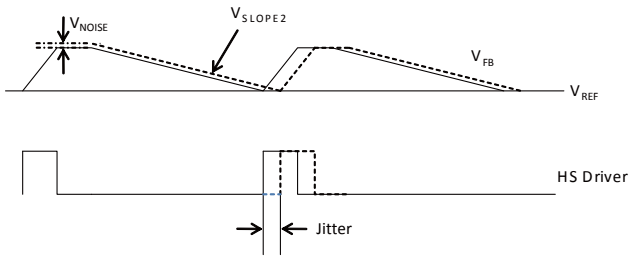

Figure 5: Jitter in Skip Mode

Operating without External Ramp Compensation

The traditional COT control scheme is intrinsically unstable if the output capacitor's ESR is not large enough to act as an effective current-sense resistor. Usually, ceramic capacitors cannot be used directly as output capacitors.

The MP8719 has built-in internal ramp compensation to ensure that the system is stable, even without the help of the output capacitor's ESR. Use the pure ceramic capacitor solution, which reduces the output ripple, total BOM cost, and board area significantly.

Figure 6 shows a typical output circuit in PWM mode without an external ramp circuit. Refer to the Application Information section on page 16 for design steps without external compensation.

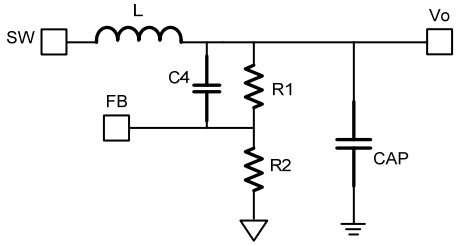

Figure 6: Simplified Output Circuit

When using a large capacitor (e.g.: OSCON) on the output, add a >10μF ceramic capacitor in parallel to minimize the effect of ESL.

Operating with External Ramp Compensation

Usually, the MP8719 is able to support ceramic output capacitors without an external ramp. However in some cases, the internal ramp may not be enough to stabilize the system, or there is too much jitter, which requires external ramp compensation. Refer to the Application Information section on page 16 for design steps with external ramp compensation.

VTT and VTTREF

The MP8719 integrates high performance, low dropout linear regulators (VTT and VTTREF) to provide complete DDR3/DDR3L power solutions. The VTTREF has a 10mA sink/source current capability and always tracks half of VDDQ with ±1% accuracy using an on-

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chip divider. A minimum 0.22μF ceramic capacitor must be connected close to the VTTREF terminal for stable operation.

VTT responds quickly to track VTTREF with ±30mV in all conditions. The current capability of the VTT regulator is up to 1A for both sink and source modes. A minimum 22μF ceramic capacitor must be connected close to the VTT terminal. VTTS should be connected to the positive node of the remote VTT output capacitor as a separate trace from the high-current line to VTT.

Configuring the EN Control

The MP8719 has two enable pins to turn the internal regulators on or off (EN1, EN2). When EN1 and EN2 are high, VDDQ, VTTREF and VTT are turned on. When EN1 is low and EN2 is high, VDDQ and VTTREF remain on while VTT is turned off and left at a high-impedance state (Hi-Z). The VTT output floats and does not sink or source current in this state. When EN1 and EN2 are low, all of the regulators remain off and discharge to GND through a soft shutdown(see Table 1).

Table 1: EN1/EN2 Control

EN1	EN2	VDDQ	VTTREF	VTT
High	High	On	On	On
Low	High	On	On	Off (Hi-Z)
Low	Low	Off	Off	Off
High	Low	Off	Off	Off

Ultrasonic Mode (USM)

Ultrasonic mode (USM) is designed to keep the switching frequency above an audible frequency area during light-load or no-load conditions. Once the part detects that both the HS-FET and the LS-FET are off for about 32μs), PWM is forced to initiate T_{ON}, so the switching frequency is out of the audible range. To prevent V_{OUT} from rising too high, the MP8719 reduces T_{ON} to control V_{OUT}. If the MP8719's FB is still too high after reducing T_{ON} to the minimum value, the output discharge function is activated and keeps V_{OUT} within a reasonable range. USM is selected by MODE.

MODE Selection

The MP8719 implements MODE for multiple applications for USM and switching frequency selection. USM and the switching frequency can be selected by a different resistor on the 3V3 logic mode pin. There are four modes that can be selected for normal application with external resistors (see Table 2). It is recommended to use a 1% accuracy resistor.

Table 2: Mode Selection

State	USM	Fs	Resistor to GND
M1	No	700kHz	0Ω
M2	Yes	700kHz	90kΩ
M3	No	500kHz	150kΩ
M4	Yes	500kHz	>230kΩ or float

VDDQ Power Good (PG)

The MP8719 uses a power good (PG) output to indicate whether the output voltage of the VDDQ regulator is ready. PG is the open drain of a MOSFET. It should be connected to V_{CC} or another voltage source through a resistor (e.g.: 100kΩ). After the input voltage is applied, the MOSFET is turned on, so PG is pulled to GND before SS is ready. After V_{FB} reaches 95% of V_{REF}, PG is pulled high (after a delay time within 10μs). When V_{FB} drops to 90% of V_{REF}, PG is pulled low.

Soft Start (SS)

The MP8719 employs a soft-start (SS) mechanism to ensure a smooth output during power-up. When EN becomes high, the internal reference voltage ramps up gradually, and the output voltage ramps up smoothly as well. Once the reference voltage reaches the target value, the soft start finishes, and the MP8719 enters steady-state operation (see Figure 7).

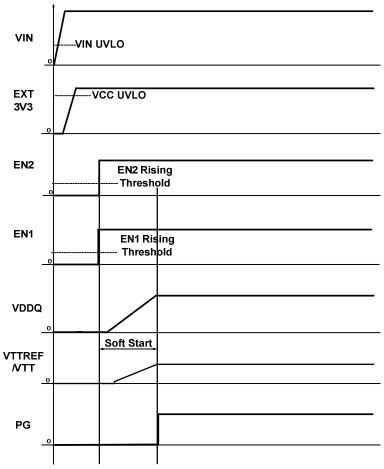

Figure 7: Start-Up Power Sequence

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If the output is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side switches until the voltage on the internal reference exceeds the sensed output voltage at the FB node.

Soft Shutdown

The MP8719 employs a soft shutdown mechanism for DDR to ensure that VTTREF and VTT follow exactly half of the VDDQ. When EN2 is low, the internal reference then ramps down gradually, so the output voltage falls linearly (see Figure 8).

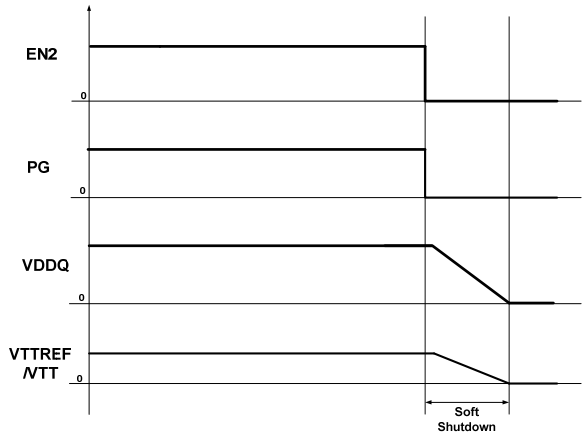

Figure 8: Soft Shutdown Sequence

VDDQ Over-Current Limit (OCL)

The MP8719 has cycle-by-cycle over-current limiting control. The current-limit circuit employs a valley current-sensing algorithm. The MP8719 uses the $R_{DS(ON)}$ of the LS-FET as a current-sensing element. If the magnitude of the current-sense signal is above the current-limit threshold, the PWM is not allowed to initiate a new cycle, even if FB is lower than REF (see Figure 9).

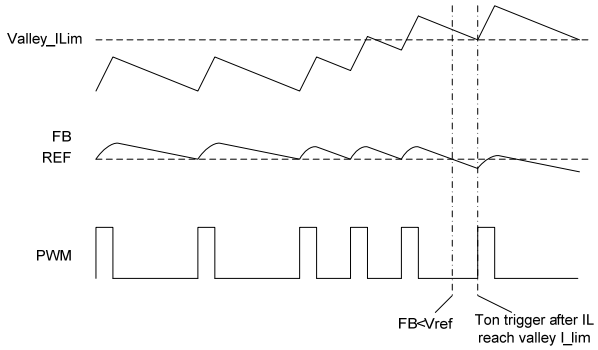

Figure 9: Valley Current-Limit Control

Since the comparison is done during the LS-FET on state, the OC trip level sets the valley level of the inductor current. The maximum load current at the over-current threshold (I_{OC}) can be calculated using Equation (2):

$$I_{OC} = I_limit + \frac{\Delta I_{inductor}}{2} \quad (2)$$

The over-current limit (OCL) limits the inductor current and does not latch off. In an over-current condition, the current to the load exceeds the current to the output capacitor, so the output voltage tends to fall off. Eventually, the currents ends up crossing the under-voltage protection (UVP) threshold and latches off. Fault latching can be reset by EN going low or cycling the power of VIN.

VTT/VTTREF Over-Current Protection (OCP)

The VTT LDO has an internal, non-latched, fixed current limit of 1.5A for both sink and source operation. Once the current limit is reached, the gate of the sink/source MOSFET is adjusted to limit the current. VTTREF also has an internal non-latch 15mA current limit.

VDDQ Over/Under-Voltage Protection (OVP, UVP)

The MP8719 monitors a resistor divided feedback voltage to detect over and under voltage. When the feedback voltage rises higher than 130% of the target voltage, the OVP comparator output goes high, the circuit latches as the HS-FET turns off, and the LS-FET turns on, acting as a -2A current source.

To protect the MP8719 from damage, there is an absolute 3.6V OVP on V_{OUT}. Once V_{OUT} reaches this value, it latches off as well. The LS-FET behaves the same as it does at 130% OVP.

When the feedback voltage drops below 75% of V_{REF}, but remains higher than 50% of V_{REF}, the UVP-1 comparator output goes high, and the MP8719 latches if V_{FB} remains in this range for about 30µs (latching the HS-FET off and the LS-FET on). The LS-FET remains on until the inductor current reaches zero. During this period, the valley current limit helps control the inductor current.

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When the feedback voltage drops below 50% of V_{REF}, the UVP-2 comparator output goes high, and the MP8719 latches off directly after the comparator and logic delay (latching the HS-FET off and the LS-FET on). The LS-FET remains on until the inductor current reaches zero. Fault latching can be reset by driving EN low or cycling the power of VIN.

Under-Voltage Lockout (UVLO) Protection

The MP8719 has two under-voltage lockout (UVLO) protections: a 3V VCC UVLO and a 4.2V VIN UVLO. The MP8719 starts up only when both VCC and VIN exceed their respective UVLO thresholds. The MP8719 shuts down when either VCC is lower than the UVLO falling threshold voltage (typically 2.8V) or VIN is lower than the 3.9V VIN falling threshold. Both UVLO protections are non-latch off.

If an application requires a higher under-voltage lockout (UVLO), use EN2 to adjust the input voltage UVLO by using two external resistors (see Figure 10).

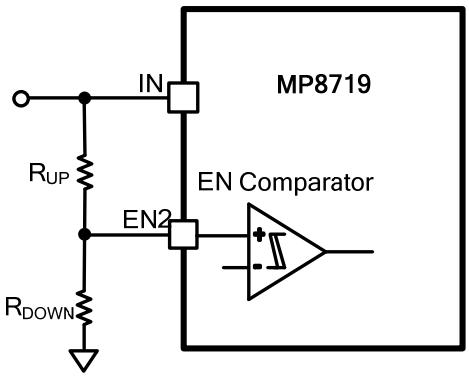

Figure 10: Adjustable UVLO

Over-Temperature Warning (OTW)

An over-temperature warning (OTW) status pin is added on the MP8719 to act as a pre-over-temperature indicator. When the IC detects that it is close to its over-temperature threshold, OTW pulls low and remains low for at least 10ms. OTW pulls high again when the device temperature has cooled below the temperature hysteresis. OTW does not trigger any protection.

Thermal Shutdown

Thermal shutdown is employed in the MP8719. The junction temperature of the IC is monitored internally. If the junction temperature exceeds the threshold value (typically 145°C), the converter shuts off. This is a non-latch protection. There is a hysteresis of about 25°C. Once the junction temperature drops to about 120°C, soft start is initiated.

Output Discharge

The MP8719 discharges all the outputs including VDDQ, VTTREF, and VTT when the controller is turned off by a protection function (UVP, OCP, OVP, UVLO, or thermal shutdown). The discharge resistor on VDDQ is 3Ω, typically. Note that the output discharge is not active during soft shutdown.

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APPLICATION INFORMATION

Setting the Output Voltage with No External Ramp

The MP8719 does not need ramp compensation for applications where POSCAP or ceramic capacitors are set as output capacitors (when VIN is over 6V), so external compensation is not needed. The output voltage is then set by feedback resistors R1 and R2 (see Figure 11).

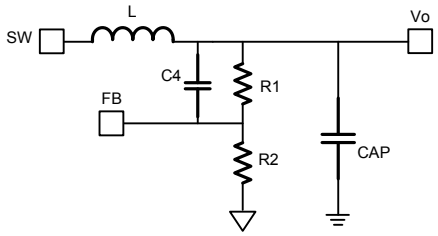

Figure 11: Simplified Circuit without External Ramp

First, choose a value for R2. R2 should be chosen reasonably. A small value for R2 leads to considerable quiescent current loss, but an R2 value that is too large makes FB noise-sensitive. It is recommended to choose a value within 5 - 50kΩ for R2. Use a comparatively larger value for R2 when V_{OUT} is low; use a smaller value for R2 when V_{OUT} is high. Considering the output ripple, determine R1 with Equation (3):

$$R_1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \cdot R_2 \quad (3)$$

C4 acts as a feed-forward capacitor to improve the transient and can be set in the range of 0 - 1000pF. A larger value for C4 leads to better transient, but it is more noise sensitive. Reserve room for a noise filter resistor (R9) (see Figure 12).

Setting the Output Voltage with External Compensation

If the system is not stable enough or there is too much jitter when a ceramic capacitor is used on the output (i.e.: with a ceramic C_{OUT} and VIN is 5V or lower), an external voltage ramp should be added to FB through resistor R4 and capacitor C4. Since there is already an internal ramp added in the system, a 1MΩ (R4) 220pF (C4) ramp should suffice.

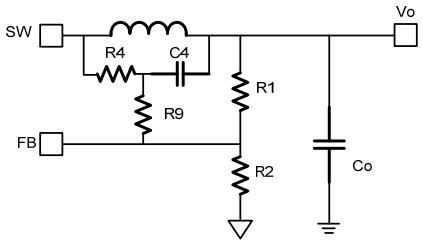

Figure 12: Simplified Circuit with External Ramp

Besides the R1 and R2 divider, the output voltage is influenced by R4 (see Figure 12). R2 should be chosen reasonably. A small value for R2 leads to considerable quiescent current loss, but a value for R2 that is too large makes FB noise sensitive. It is recommended to choose a value within 5 - 50kΩ for R2. Use a comparatively larger value for R2 when V_{OUT} is low; use a smaller value for R2 when V_{OUT} is high. The value of R1 then is determined with Equation (4):

$$R_1 = \frac{1}{\frac{V_{REF}}{V_{OUT} - V_{REF}} - \frac{R2}{R4}} \cdot R_2 \quad (4)$$

To get a pole for better noise immunity, set R9 with Equation (5):

$$R_9 = \frac{1}{2\pi \times C_4 \times 2F_{SW}} \quad (5)$$

Set R9 in the range of 100Ω to 1kΩ to reduce its influence on the ramp.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. For the best performance, use ceramic capacitors placed as close to VIN as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations.

The capacitors must have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation (6):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (6)$$

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The worst-case condition occurs at VIN = $2V_{OUT}$, shown in Equation (7):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (7)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an input capacitor that meets the specification.

The input voltage ripple can be estimated with Equation (8):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

The worst-case condition occurs at VIN = $2V_{OUT}$, shown in Equation (9):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (9)$$

Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated using Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (10)$$

When using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance, which mainly causes the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^{\ 2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (11)$$

The output voltage ripple caused by ESR is very small. Therefore, an external ramp is needed to stabilize the system. The external ramp can be generated through resistor R4 and capacitor C4.

When using POSCAP capacitors, the ESR dominates the impedance at the switching frequency. The ramp voltage generated from the ESR dominates the output ripple. The output ripple can be approximated with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (12)$$

The maximum output capacitor limitation should be considered in the design application. The MP8719 has a soft-start time period of around 1.6ms. If the output capacitor value is too high, the output voltage cannot reach the design value during the soft-start time, causing it to fail to regulate. The maximum output capacitor value (C_{o_max}) can be limited approximately with Equation (13):

$$C_{O_MAX} = (I_{LIM_AVG} - I_{OUT}) \times T_{ss} / V_{OUT} \quad (13)$$

Where I_{LIM_AVG} is the average start-up current during the soft-start period (which can be equivalent to the current limit), and T_{ss} is the soft-start time.

Selecting the Inductor

An inductor is necessary for supplying constant current to the output load while being driven by the switched input voltage. A larger-value inductor results in less ripple current, resulting in lower output ripple voltage, but also has a larger physical footprint, a higher series resistance, and a lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be in the range of 30% to 50% of the maximum output current, and the peak inductor current below the maximum switch current limit. The inductance value can be calculated with Equation (14):

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (14)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current (including a short-current), so I_{SAT} is recommended to be >13A.

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PCB Layout Guidelines

Efficient PCB layout is critical for stable operation of the IC. A 4-layer layout is strongly recommended to achieve better thermal performance. For best results, refer to Figure 13 and follow the guidelines below. For more information, refer to the application note AN087 “PCB Layout Design Guidelines for NB68X Families.”

1. Keep the VDDQ trace width greater than 100mil to avoid a voltage drop at the input of the VTTLDO.
2. Place the high-current paths (GND, VIN, and SW) very close to the device with short, direct, and wide traces.
   A thick PGND trace under the IC should be top priority.
3. Place the input capacitors as close to VIN and GND as possible on the same layer as the IC.
4. Place the decoupling capacitor as close to VCC and GND as possible.
5. Keep the switching node (SW) short and away from the feedback network.
6. Place the external feedback resistors next to FB.
7. Ensure that there is no via on the FB trace.
8. Keep the BST voltage path (BST, C3, and SW) as short as possible.
9. Keep the VIN and GND pads connected with a large copper plane to achieve better thermal performance.
10. Add several vias with 10mil drill/18mil copper width close to the VIN and GND pads to help thermal dissipation.

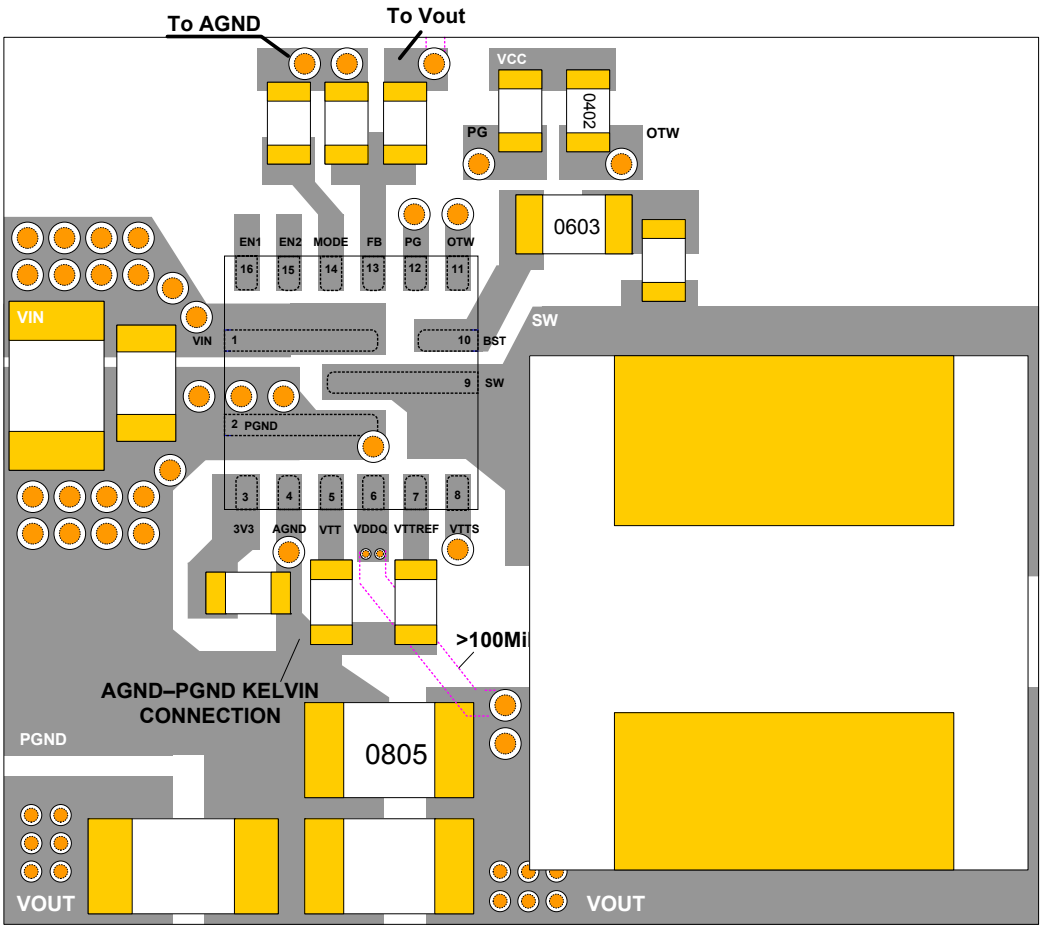

Figure 13: Recommended PCB Layout

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Design Example

For applications that need currents over 10A, it is recommended to apply a 500kHz f_{SW} part for better thermal performance and efficiency (see Table 3). Otherwise, a 700kHz f_{SW} operation makes the system more compact with faster transient (see Table 4).

There is a resistor from an external 3.3V supply to 3V3 acting as a ripple noise filter of the 3.3V power supply. It is recommended to have a resistor value from 0 - 5.1Ω depending on the noise level. A size 0402 resistor is sufficient if the 3.3V voltage rises up with SS > 100μs. Otherwise, a larger resistor (e.g.: 0603/0805) is needed.

For applications where VIN is 5V or lower, it is recommended to apply the SCH shown in Figure 14 with a proper external ramp.

The MP8719 also supports non DDR applications with very compact external components (see Figure 15).

Some design examples are provided below when ceramic capacitors are applied.

Table 3: Design Example for 500kHz f_{SW}

V_{OUT} (V)	Cout (F)	L (μH)	R_{Mode} (Ω)	C4 (pF)	R1 (kΩ)	R2 (kΩ)
1.0	22μx4	1.0	150k	220	13.3	20
1.2	22μx4	1.0	150k	220	20	20
1.35	22μx4	1.0	150k	220	28	22.1
1.5	22μx4	1.2	150k	220	30.1	20
1.8	22μx4	1.5	150k	220	40.2	20

Table 4: Design Example for 700kHz f_{SW}

V_{OUT} (V)	Cout (F)	L (μH)	R_{Mode} (Ω)	C4 (pF)	R1 (kΩ)	R2 (kΩ)
1	22μx3	0.68	0	220	13.3	20
1.2	22μx3	0.68	0	220	20	20
1.35	22μx3	0.68	0	220	28	22.1
1.5	22μx3	0.68	0	220	30.1	20
1.8	22μx3	0.68	0	220	40.2	20

Additional Design Examples with Higher V_{OUT}

The MP8719 supports designs that need V_{OUT} to be in the range of 3.3V to 5.5V. Figure 17 shows an SCH with a 5V V_{OUT} with proper external settings. Please pay attention to the red components, and please note that USM is not allowed for this application.

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TYPICAL APPLICATION CIRCUITS

DDR Application for VIN >6V

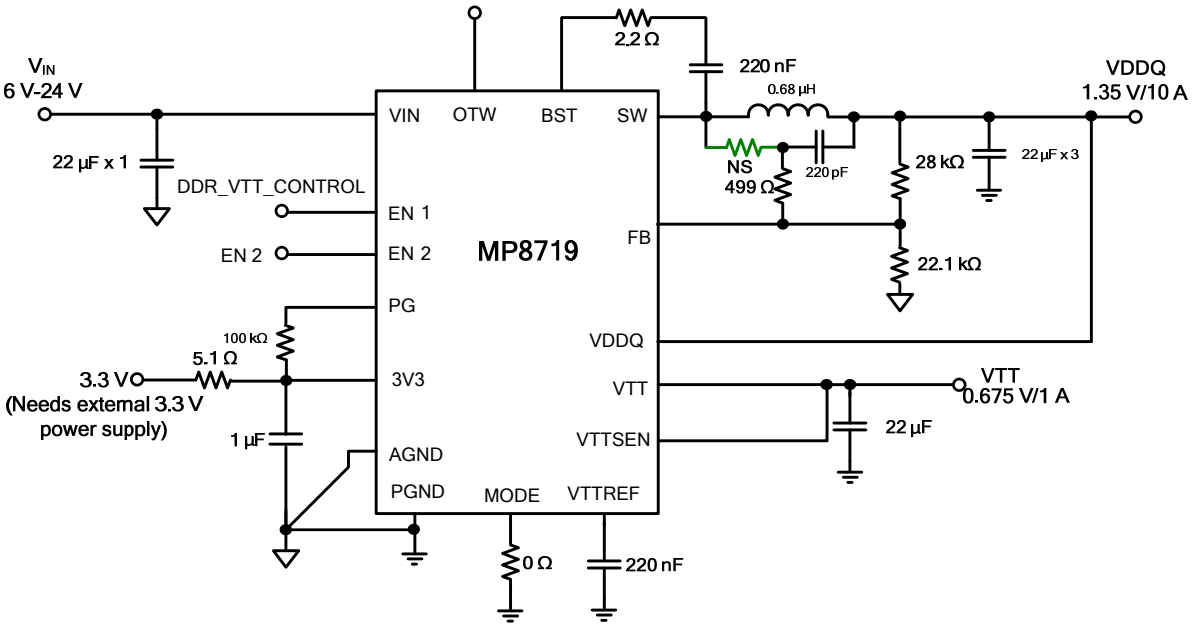

Figure 14: Typical DDR Application Circuit, VIN = 6V - 24V, V_{OUT} = 1.35V, I_{OUT} = 10A, with VTT fs = 700kHz

DDR Application Cover 5V VIN Application

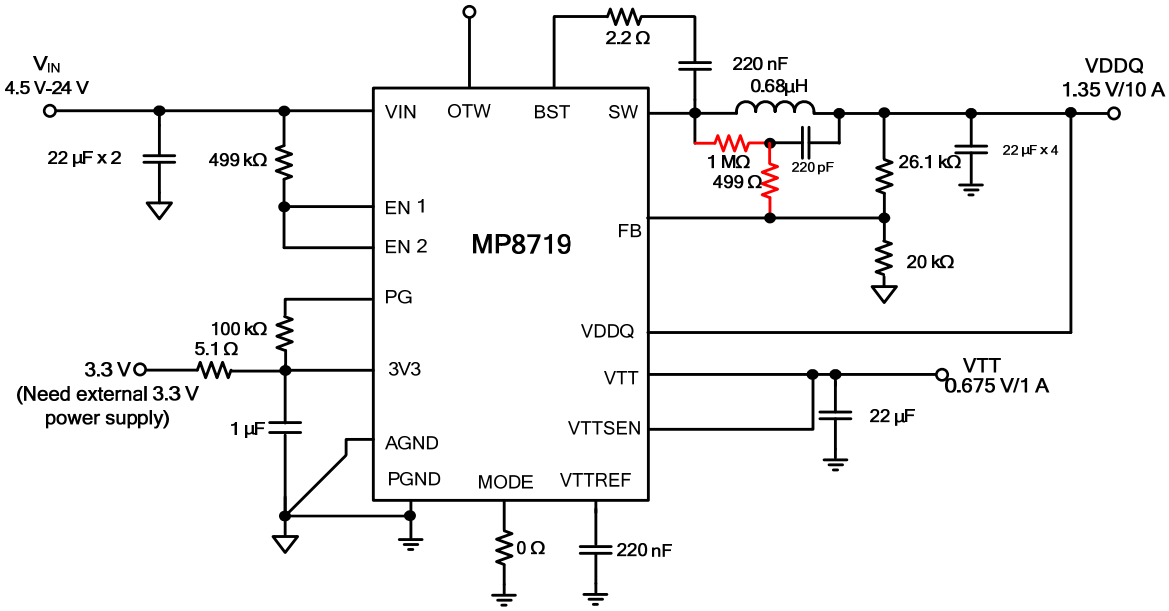

Figure 15: Typical DDR Application Circuit, VIN = 4.5V - 24V, V_{OUT} = 1.35V, I_{OUT} = 10A, with VTT fs = 700kHz

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TYPICAL APPLICATION CIRCUITS *(continued)*

Non DDR Application

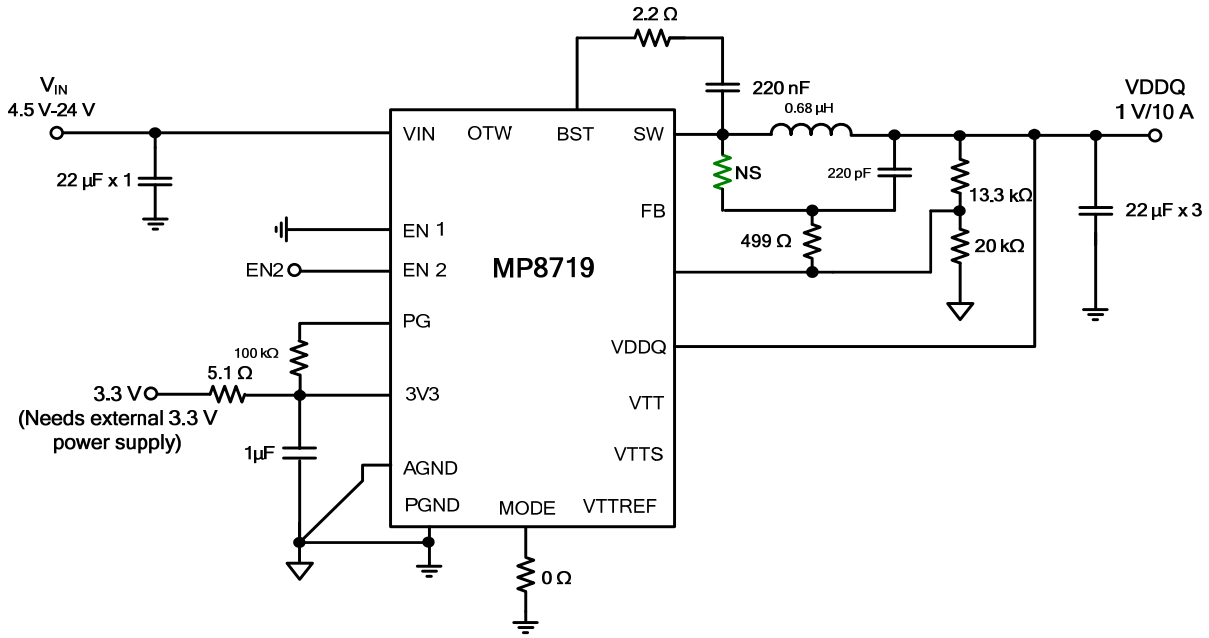

Figure 16: Normal Single Buck Application Circuit, VIN = 4.5V - 24V, V_{OUT} = 1V, I_{OUT} = 10A, without VTT fs = 700kHz

Special Application with 3.3V < VOUT < 5.5V

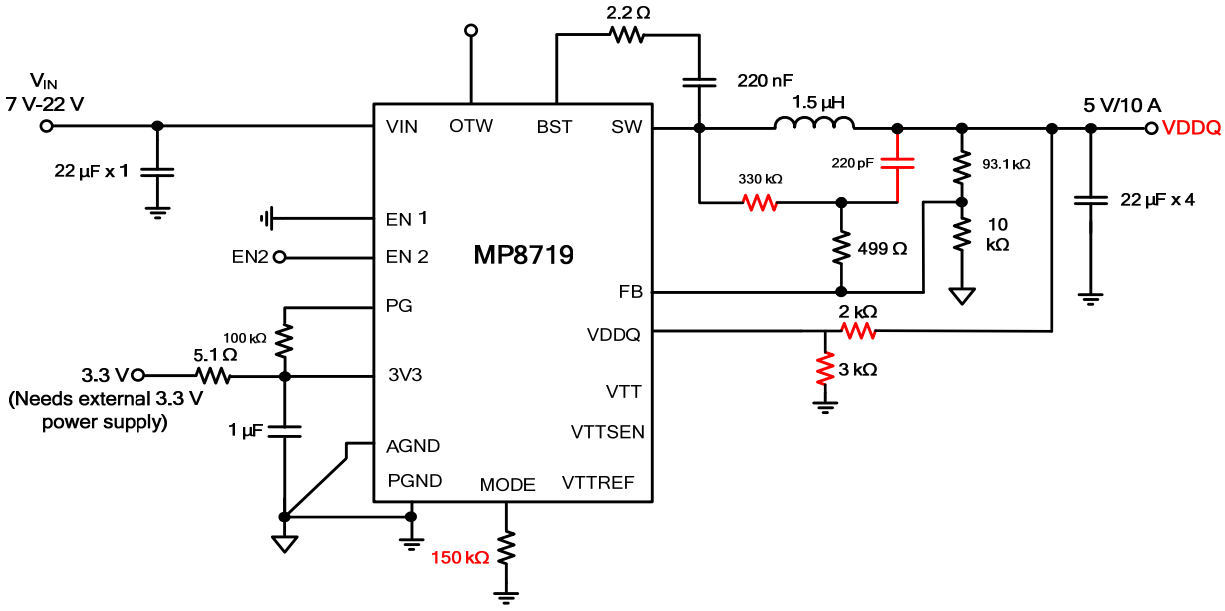

Figure 17: Special Application Circuit, VIN = 7V - 22V, V_{OUT} = 5V, I_{OUT} = 10A, fs = 700kHz

NOTE 1: Ultrasonic mode is not effective if applied in this SCH.
NOTE 2: The maximum load is 10A in this application. Fs is set with a 500kHz mode but is actually 700kHz.
NOTE 3: It is recommended to avoid VDDQ voltages over 3.3V by using the external resistors setting.

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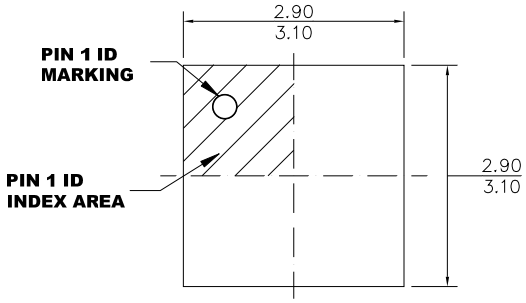
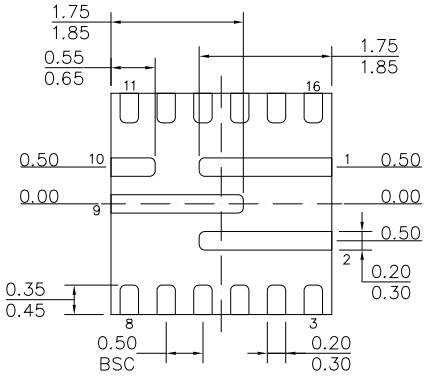
PACKAGE INFORMATION

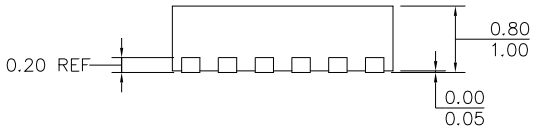
QFN-16 (3mmx3mm)



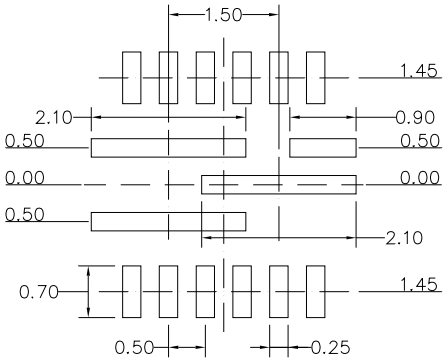
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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