MP87000-M

90A Intelli-Phase™ DrMOS Solution in 5x6 Package with Quiet Switcher™ Technology

DESCRIPTION

The MP87000-M is a monolithic half-bridge Intelli-Phase™ solution with built-in internal power MOSFETs and gate drivers. It can achieve up to 90A of continuous output current (I_{OUT}) across a wide input voltage (V_{IN}) supply range.

Quiet Switcher™ technology (QST™) utilizes a proprietary circuit design that can only be achieved in a monolithic architecture to suppress voltage ringing. This technology limits peak switching voltages to <2V above V_{IN}, improving device reliability, lowering EMI, and reducing sensitivity to PCB layout.

The MP87000-M offers many features to simplify system design. This device operates with state pulse-width modulation (PWM) signal controllers, and features Accu-Sense™ current sensing and temperature sensing to monitor the inductor current (I_L) and report the junction temperature (T_J), respectively.

The MP87000-M is ideal for server applications where efficiency and small size are at a premium. The MP87000-M is available in a TLGA-41 (5mmx6mm) package.

FEATURES

- Quiet Switcher™ Technology (QST™) Limits Peak Switching Voltages to <2V above the Input Voltage (V_{IN}) with Minimal Reliance on PCB Layout
- Wide 3V to 16V Operating V_{IN} Range
- 90A Output Current (I_{OUT})
- Accu-Sense™ Current Sense
- Temperature Sense
- Accepts Tri-State Pulse-Width Modulation (PWM) Signals
- Current-Limit Protection
- Over-Temperature Protection (OTP)
- Fault Reporting
- Available in a TLGA-41 (5mmx6mm) Package

APPLICATIONS

- Server Core Voltage
- Graphic Card Core Regulators
- Power Modules

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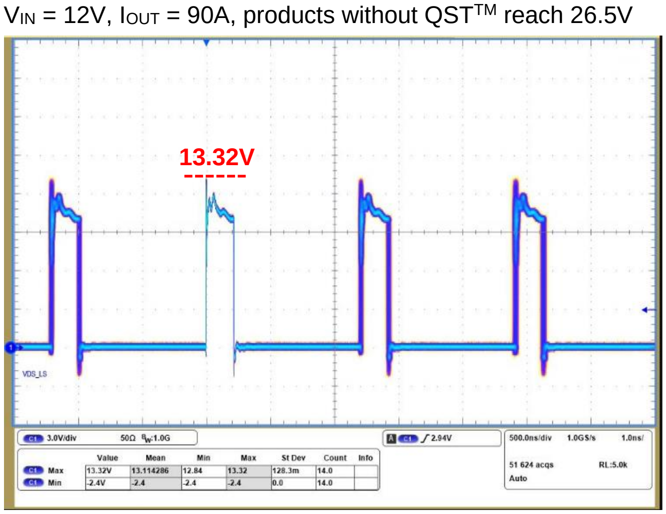
QUIET SWITCHER™ WAVEFORM

V_{IN} = 12V, I_{OUT} = 90A, products without QST™ reach 26.5V



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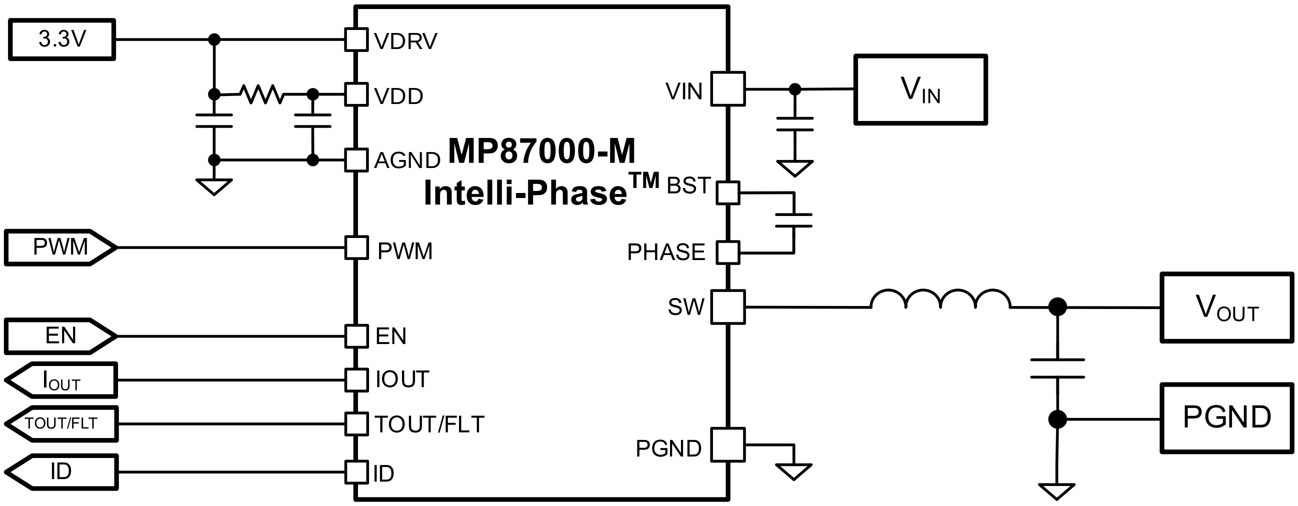
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP87000-MGMJTH	TLGA-41 (5mmx6mm)	*See Below*	3

* For Tape & Reel, add suffix -Z (e.g. MP87000-MGMJTH-Z).

TOP MARKING

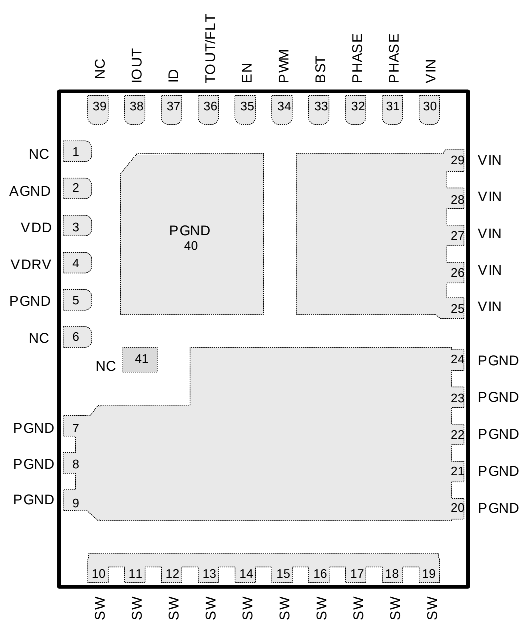
(MP87000-MGMJTH)

MPSYYWW
MP87000
LLLLLLL
MTH

MPS: MPS prefix
YY: Year code
WW: Week code
MP87000-M: Part number
LLLLLLL: Lot number
TH: Thin package

PACKAGE REFERENCE

Top View



TLGA-41 (5mmx6mm)

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PIN FUNCTIONS

Pin #	Name	Descriptions
1, 6, 39, 41	NC	**No connection.**
2	AGND	**Analog ground.**
3	VDD	**Supply voltage for internal circuitry.** Connect the VDD pin to VDRV via a 2.2Ω resistor. Decouple VDD using a 1µF capacitor (C_{VDD}) connected to AGND. Connect AGND and PGND at C_{VDD}.
4	VDRV	**Driver voltage.** Connect the VDRV pin to a 3.3V supply. Decouple VDRV using a 1µF to 4.7µF ceramic capacitor (C_{VDRV}).
5, 7, 8, 9, 20, 21, 22, 23, 24, 40	PGND	**Power ground.**
10, 11, 12, 13, 14, 15, 16, 17, 18, 19	SW	**Phase node.**
25, 26, 27, 28, 29, 30	VIN	**Input supply voltage.** Place ceramic input capacitors (C_{IN}) close to the device to support the switching current with minimal parasitic inductance.
31, 32	PHASE	**Switching node for bootstrap (BST) capacitor connection.** The PHASE pin is connected to the SW pin internally.
33	BST	**Bootstrap.** The BST pin requires a 0.1µF to 0.22µF capacitor (C_{BST}) to drive the power MOSFET's gate above the supply voltage. Connect C_{BST} between the BST and PHASE pins to form a floating supply across the power MOSFET driver.
34	PWM	**Pulse-width modulation (PWM) input.** Float the PWM pin or pull it to a middle state to force the SW pin into a high-impedance (Hi-Z) state.
35	EN	**Enable.** Pull the EN pin low to disable the device and force SW into a Hi-Z state.
36	TOUT/FLT	**Single-pin temperature sense and fault reporting.** The TOUT/FLT pin is pulled up to the VDD voltage (V_{DD}) if a fault occurs.
37	ID	**Vender ID voltage output.** Connect the ID pin to the controller that supports ID function. Float this pin if it is not used.
38	IOUT	**Current-sense (CS) output.** The IOUT pin is a bidirectional current output proportional to the inductor current (I_L). Connect IOUT to the PWM controller's CS input. Use a resistor connected to a common-mode voltage to obtain the differential voltage proportional to I_L.

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ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} to PGND ....-0.3V to +20V
V_{IN} to V_{PHASE} (DC) ....-0.3V to +24V
V_{IN} to V_{PHASE} (10ns)...........................-5V to +32V
V_{SW} to PGND (DC) ....-0.3V to +20V
V_{SW} to PGND (10ns)..........................-5V to +28V
V_{BST} .... V_{PHASE} + 4V
V_{DD}, V_{DRV} ....-0.3V to +4V
All other pins .... -0.3V to VDD + 0.3V
Instantaneous current 130A
Junction temperature (T_J) ....150°C
Lead temperature ....260°C
Storage temperature .... -65°C to +150°C

ESD Ratings

Human body model (HBM) .... Class 1C
Charged-device model (CDM) ....Class C2B

Recommended Operating Conditions (2)

Supply voltage (V_{IN}) ....3V to 16V
Driver voltage (V_{DRV}) ....3V to 3.6V
Logic voltage (V_{DD}).............................3V to 3.6V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (3) θ_{JB} θ_{JC_TOP}

TLGA-41 (5mmx6mm).........2.5.......2.5... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) θ_{JB}: Thermal resistance from the junction to the board around the PGND soldering point.
   θ_{JC_TOP}: Thermal resistance from the junction to the top of the package.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{DRV} = V_{DD} = V_{EN} = 3.3V, T_A = 25°C for typical values, T_J = -40°C to +125°C for max and min values, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input current (I_{IN}) shutdown		EN = low		5		μA
V_{IN} under-voltage lockout (UVLO) rising threshold				2.5	3	V
V_{IN} UVLO hysteresis				200		mV
VDRV current (I_{VDRV}) quiescent current		PWM = low		0.36		mA
VDD current (I_{VDD}) quiescent current		PWM = low		4.5		mA
VDD voltage (V_{DD}) UVLO rising threshold				2.75	2.95	V
V_{DD} UVLO hysteresis				200		mV
High-side (HS) current limit (4)	I_{LIM_FLT}	Cycle-by-cycle up to 10 cycles		120		A
Low-side (LS) current limit (4)		Negative current limit, cycle-by-cycle, no fault report		-50		A
LS negative current limit off time (4)				200		ns
HS current limit shutdown counter (4)				10		times
Dead time (DT) at SW rising (4)				2		ns
DT at SW falling (4)		Positive inductor current (I_L)		6		ns
		Negative I_L		15		ns
EN input high voltage			1.4			V
EN input low voltage					0.9	V
PWM high to SW rising delay (4)	t_{RISING}			15		ns
PWM low to SW falling delay (4)	$t_{FALLING}$			15		ns
PWM tri-state to SW Hi-Z delay (4)	t_{LT}			40		ns
	t_{TL}			20		ns
	t_{HT}			40		ns
	t_{TH}			20		ns
Minimum PWM pulse width (4)				15		ns
IOUT current-sense (CS) gain accuracy		T_J = 25°C	-2	0	+2	%
IOUT CS gain	G_{IOUT}			5		μA/A
IOUT voltage range (4)	V_{IOUT}		0.7		2.1	V
TOUT/FLT sense gain (4)				8		mV/°C
TOUT/FLT sense offset		T_J = 25°C		800		mV
Over-temperature (OT) shutdown and fault flag (4)				160		°C
TOUT/FLT when a fault occurs			3	3.3		V

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{DRV} = V_{DD} = V_{EN} = 3.3V, T_A = 25°C for typical values, T_J = -40°C to +125°C for max and min values, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PWM sink/source current		PWM = 0V		500		μA
		PWM = 3.3V		-500		μA
ID sink/source current		ID = 1.1V		720		μA
		ID = 1.3V		-200		μA
PWM Hi-Z voltage		PWM = Hi-Z		1.6		V
PWM logic high voltage			2.6			V
PWM tri-state region			1.1		2.1	V
PWM logic low voltage					0.6	V
ID voltage		V_{DD} = 3V to 3.6V	1.1	1.2	1.3	V
ID voltage delay		From V_{DD} > UVLO to ID > 1.1V		10		μs

Note:

4) Guaranteed by design or characterization data. Not tested in production.

PWM TIMING DIAGRAM

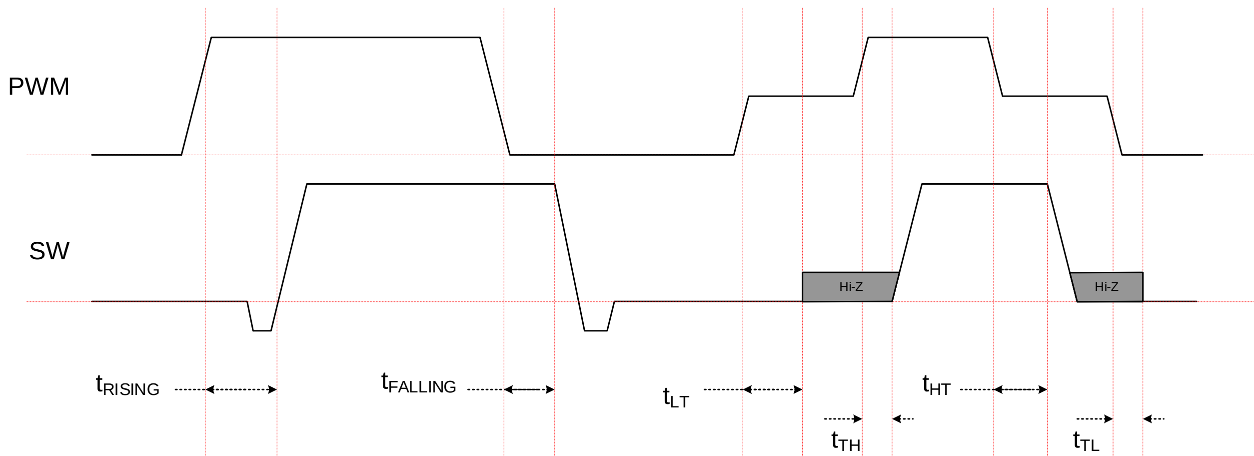

Figure 1: PWM Timing Diagram

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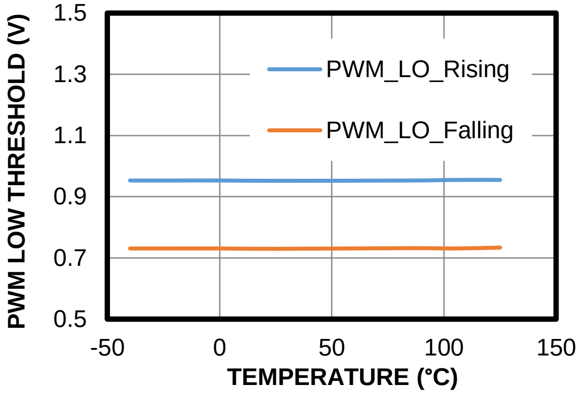
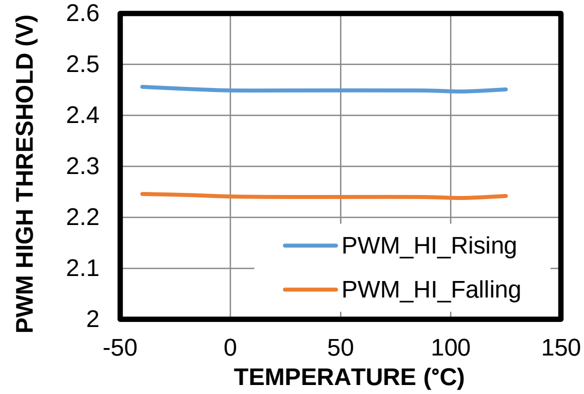
TYPICAL CHARACTERISTICS

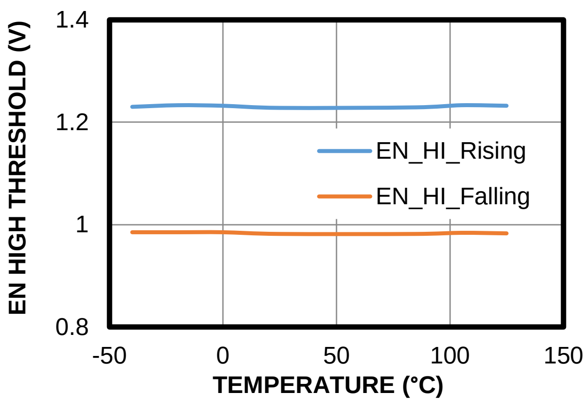
PWM Low Threshold



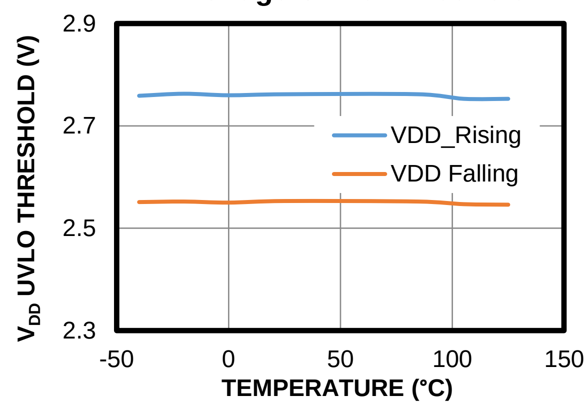
PWM High Threshold



EN High Threshold

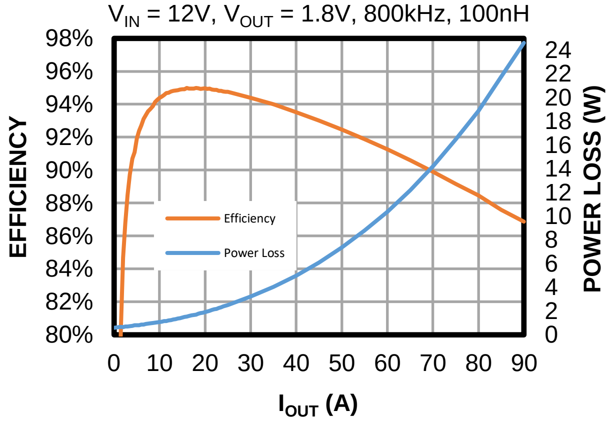


VDD Voltage UVLO Threshold



Efficiency vs. Output Current vs. Power Loss

V_{IN} = 12V, V_{OUT} = 1.8V, 800kHz, 100nH



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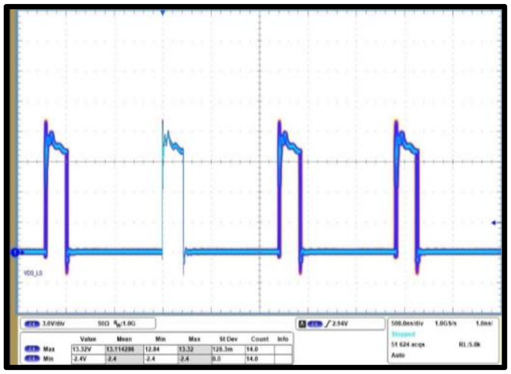
TYPICAL PERFORMANCE CHARACTERISTICS

Switching

V_{IN} = 12V, L = 120nH, load = 90A

CH1: V_{SW} 3V/div.

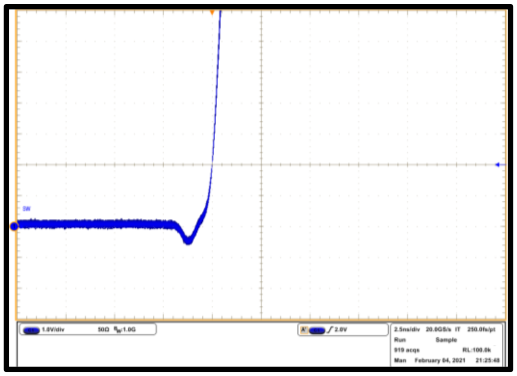


500ns/div.

Dead Time during SW Ringing

Load = 30A

CH1: V_{SW} 1V/div.



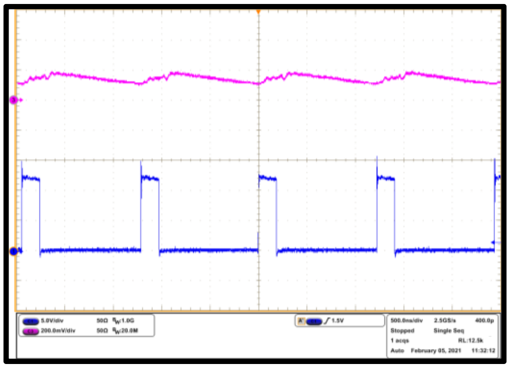
2.5ns/div.

Output Current

Load = 0A

CH3: V_{IOUT} 200mV/div.

CH1: V_{SW} 5V/div.



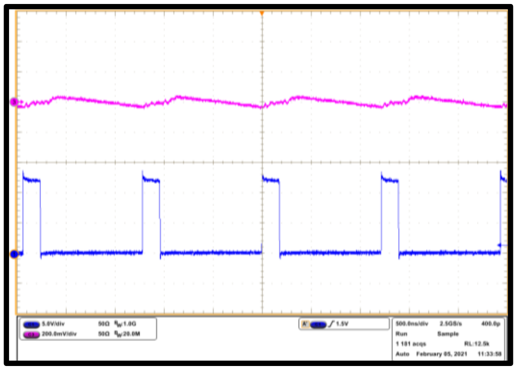
500ns/div.

Output Current

Load = 30A

CH3: V_{IOUT} 200mV/div.

CH1: V_{SW} 5V/div.



500ns/div.

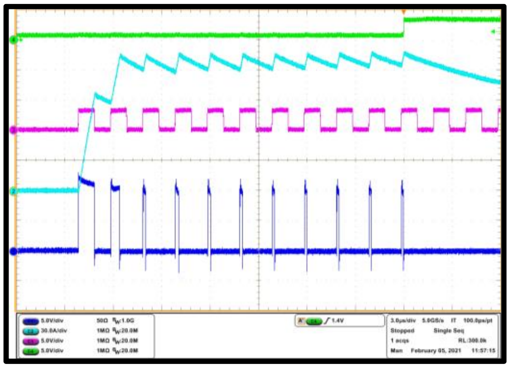
High-Side Current Limit

CH4: V_{FAULT} 5V/div.

CH3: PWM 5V/div.

CH2: I_L 30A/div.

CH1: V_{SW} 5V/div.



3μs/div.

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FUNCTIONAL BLOCK DIAGRAM

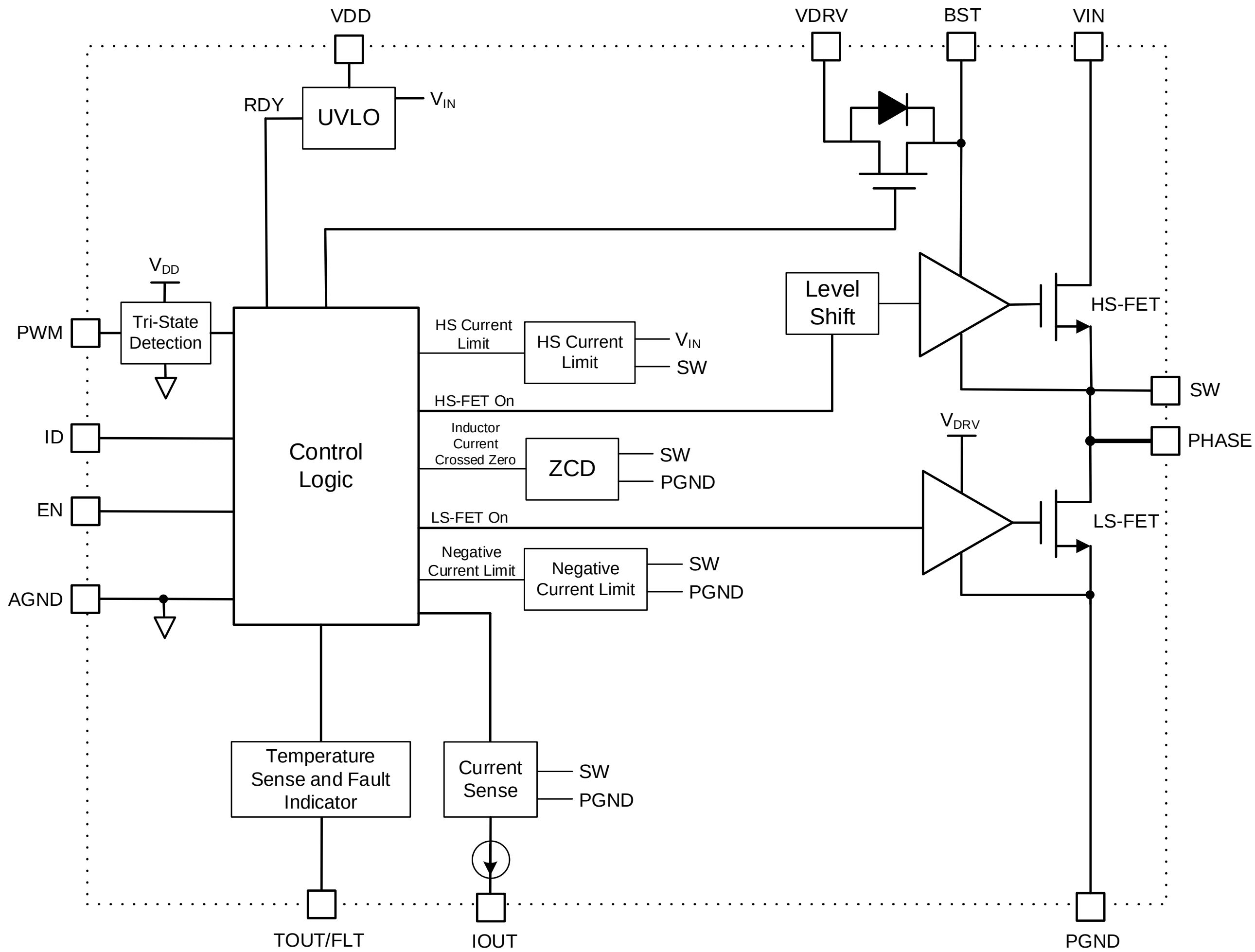

Figure 2: Functional Block Diagram

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OPERATION

The MP87000-M is a 90A, monolithic, half-bridge Intelli-Phase™ driver with built-in internal power MOSFETs. It is ideal for multi-phase buck regulators. An external 3.3V supply is required to supply the VDD and VDRV pins. Once the EN pin transitions from low to high, and the VDRV, VDD and VIN signals (V_{DRV}, V_{DD}, and V_{IN}, respectively) are sufficiently high, the device begins operation.

Quiet Switcher™ Technology (QST™)

The Quiet Switcher™ technology (QST™) is a proprietary feedback control architecture that controls the effect of parasitic kickback in the circuit to suppress the level of voltage overshoot during fast switching at frequencies up to 3MHz.

Pulse-Width Modulation (PWM)

The pulse-width modulation (PWM) pin can operate as a tri-state input. When the PWM input signal is within the tri-state threshold window (t_{HT} to t_{LT}) for a typical 40ns, the high-side MOSFET (HS-FET) turns off immediately and the low-side MOSFET (LS-FET) enters diode emulation mode. The LS-FET remains in diode emulation mode until zero-current detection (ZCD). The tri-state PWM input can come from a forced middle-voltage PWM signal or by floating the PWM input. The internal current source charges the signal to a middle voltage. Figure 1 on page 7 shows the propagation delay definition from PWM to the SW node.

Diode Emulation Mode

In diode emulation mode, PWM is in a tri-state input. If the inductor current (I_L) is positive, then the LS-FET turns on. If I_L is negative or after I_L crosses the ZCD threshold, the LS-FET turns off. Diode emulation mode can be enabled by driving PWM to a middle state or floating PWM.

Current Sense (CS)

IOUT is a bidirectional current-sense (CS) pin proportional to I_L. The CS gain (G_{IOUT}) is 5μA/A. If necessary, use a resistor to configure the voltage gain proportional to I_L.

The IOUT pin's output has two states (see Table 1). When disabled (EN = low), the CS circuit is disabled, and IOUT is in a high-impedance (Hi-Z) state regardless of the PWM state.

Table 1: IOUT Output States

PWM	EN	IOUT
PWM	Hi	Active
-	Low	Hi-Z

A 0.7V to 2.1V IOUT voltage (V_{IOUT}) range is required to achieve accurate DrMOS CS pin output current (I_{OUT}) reporting. A resistor (R_{IOUT}) is typically connected from IOUT to a reference voltage (V_{CM}) that is capable of sinking small currents in order to provide sufficient voltage to meet the required operating voltage range.

V_{CM}, which is connected to R_{IOUT}, can be calculated with Equation (1):

$$0.7V < I_{OUT} \times R_{IOUT} + V_{CM} < 2.1V \qquad (1)$$

Where V_{CM} is a reference voltage connected to R_{IOUT}.

I_{OUT} can be calculated using Equation (2):

$$I_{OUT} = I_{SW} \times G_{IOUT} \qquad (2)$$

The Intelli-Phase™'s CS output is used by the controller to accurately monitor the buck convert's output current (I_{OUT}). The cycle-by-cycle current information from IOUT can be used for phase-current balancing, over-current protection (OCP), and active voltage positioning (output voltage [V_{OUT}] droop).

Positive and Negative Inductor Current Limits

If an HS-FET over-current (OC) condition is detected, then the HS-FET turns off for the PWM cycle. If an HS-FET current limit event is detected for ten consecutive cycles, then the HS-FET latches off, the TOUT/FLT pin is pulled high to VDD, and the LS-FET turns on until ZCD. Toggle EN or recycle the power on VIN or VDD to release the fault latch and restart the device.

If the LS-FET detects a -50A valley current, then the LS-FET turns off and the HS-FET turns on for 200ns to limit the negative current cycle by cycle. The LS-FET negative current limit does not trigger a fault report.

Temperature-Sense Output with Fault Indicator (TOUT/FLT)

The TOUT/FLT pin has two functions: junction temperature (T_J) sense and fault detection.

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TOUT/FLT has an output voltage (V_{OUT}) proportional to T_J when the part is active. The gain is 8mV/°C, with an 800mV offset at 25°C. For example, the TOUT/FLT voltage is 0.8V at T_J = 25°C, and 1.6V at T_J = 125°C.

If a fault occurs, TOUT/FLT is pulled to V_{DD} to report the fault event, regardless of the temperature. If the fault event lasts for longer than 200ns, the PWM impedance changes accordingly to indicate the fault type. Table 2 shows the PWM status by the fault type.

Table 2: PWM Resistance by Fault Type

Fault Type	PWM
Over-current protection (OCP)	10kΩ to AGND
Over-temperature protection (OTP)	20kΩ to AGND
SW-to-PGND short protection	1kΩ to VDD

TOUT/FLT monitors for three different fault events:

1. OCP limit: Ten consecutive current limit faults trigger an OC fault. If this fault occurs, the MP87000-M latches off to turn off the HS-FET. The LS-FET turns off once I_L reaches 0A. OCP triggers a 10kΩ resistor to AGND on the PWM pin to indicate the fault type.
2. OTP: If T_J > 160°C, an OT fault occurs and the MP87000-M latches off to turn off the HS-FET. The LS-FET turns off when I_L reaches 0A. OTP triggers a 20kΩ resistor to AGND on the PWM pin to indicate the fault type.
3. SW-to-PGND short: If this fault occurs, the MP87000-M latches off to turn off the HS-FET. PWM is pulled high (1kΩ to V_{DD}) to indicate the fault type.

Release the fault latch by toggling EN, or by recycling the power on VIN or VDD.

For multi-phase operation, connect the TOUT/FLT pin of each Intelli-Phase™ device together (see Figure 3).

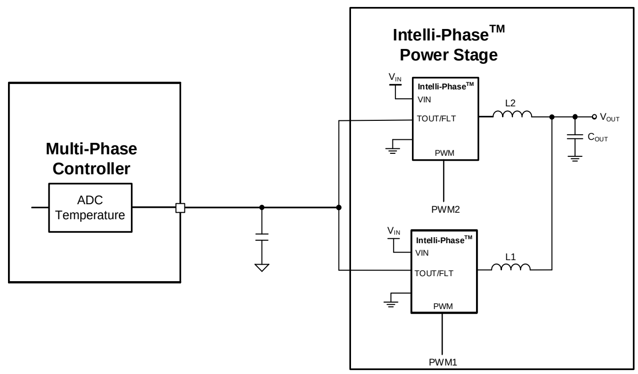

Figure 3: Multi-Phase Temperature Sense Utilization

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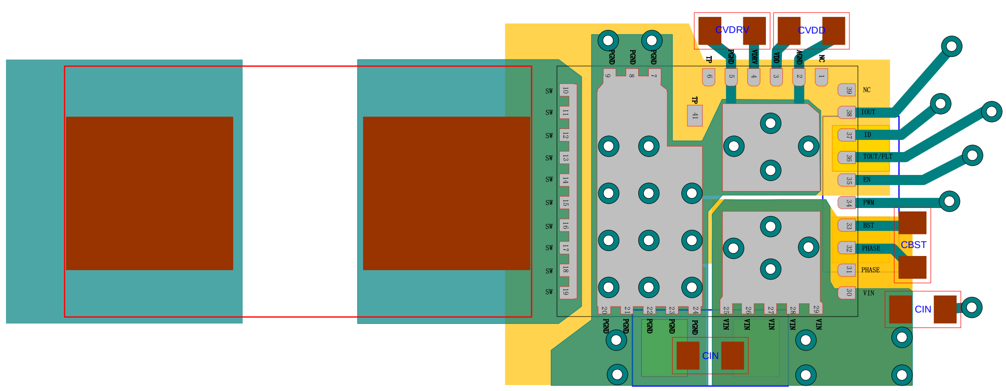
APPLICATION INFORMATION

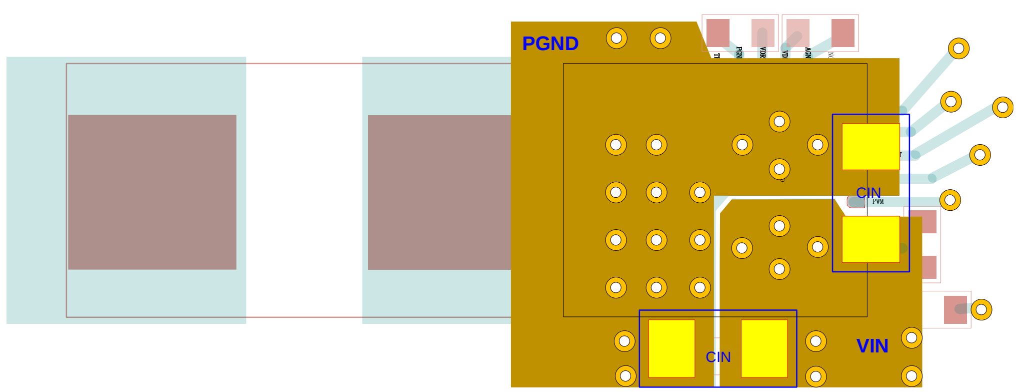
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 4 and follow the guidelines below.

1. Place the MLCC input capacitors as close to the VIN and PGND pins as possible.
2. Place as many VIN and PGND vias underneath the package as possible. Place these vias between the VIN or PGND long pads.
3. Place a VIN copper plane on mid-layer 2 to form a positive/negative/positive (+/-/+) PCB stack to reduce parasitic impedance from the MLCC input capacitor to the MP87000-M.
4. Ensure that the copper plane on the mid-layer covers at least the VIN vias underneath the package and MLCC input capacitors.
5. Place more PGND vias as close to the PGND pin and pad as possible to minimize parasitic resistance, parasitic impedance, and thermal resistance.
6. Place the BST capacitor (C_{BST}) and VDRV capacitor (C_{VDRV}) as close to the device's pins as possible.
7. Route the BST path using a >20mils trace width. Avoid placing vias on the BST driving path.
8. Place the VDD decoupling capacitor (C_{VDD}) close to the device.
9. Keep the IOUT signal trace away from high-voltage and high-current slew-rate nodes, such as SW, PWM, and the VIN and PGND vias.



Top Layer



Bottom Layer

Figure 4: Recommended PCB Layout

Input Capacitor: 0402 Package (Top Side) and 0805 Package (Bottom Side)

Inductor: 10mmx6mm Package

VDRV, VDD, and BST Capacitors: 0402 Package

Via Size: 20/10mils

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TYPICAL APPLICATION CIRCUIT

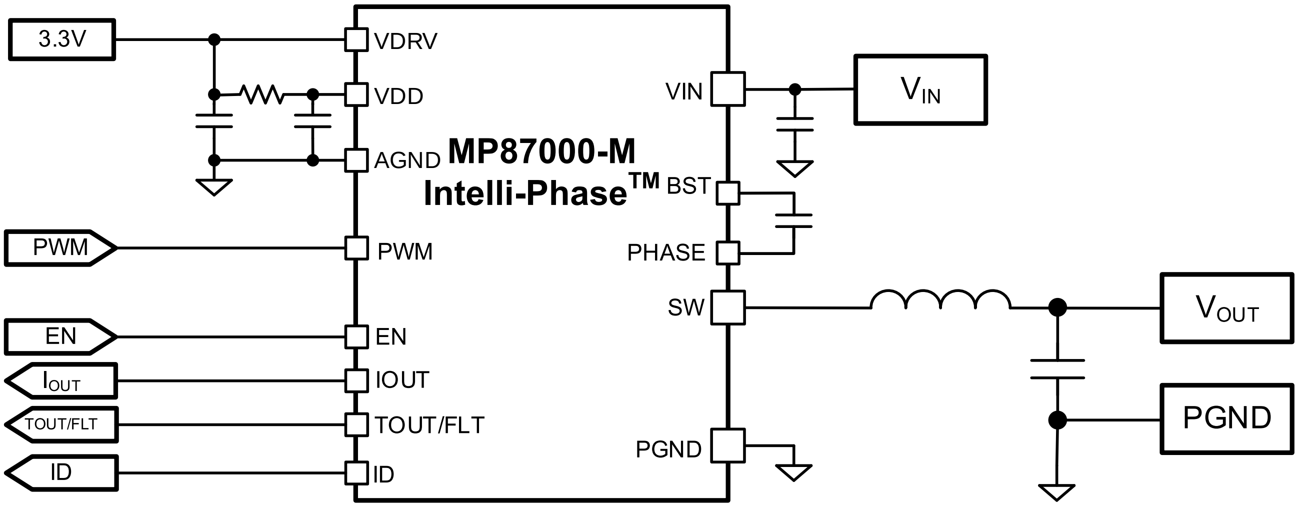

Figure 5: Typical Application Circuit

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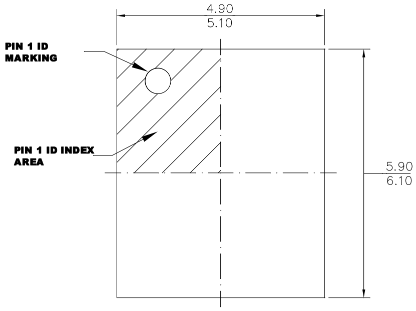
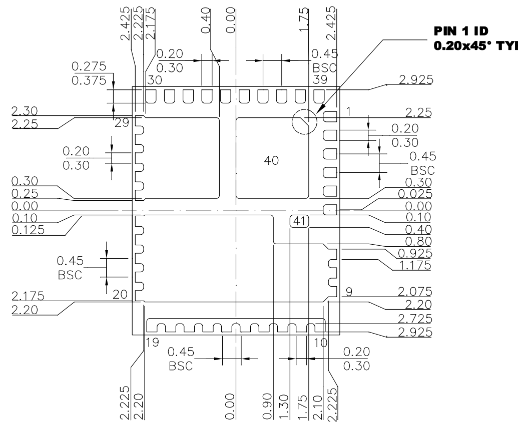
PACKAGE INFORMATION

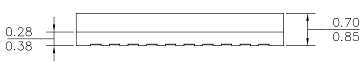
TLGA-41 (5mmx6mm)



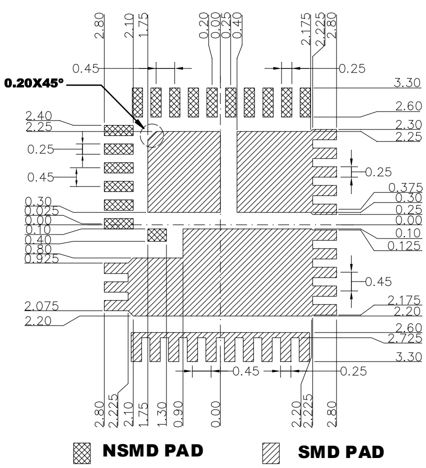
TOP VIEW



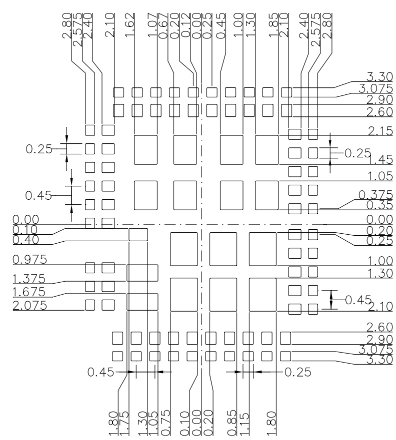
BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN



RECOMMENDED STENCIL OPENING

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-303.
4) DRAWING IS NOT TO SCALE.
5) THE ACCURACY FOR COMPONENT PLACEMENT SHOULD BE ADJUSTED TO ±30 MICROMETRES.

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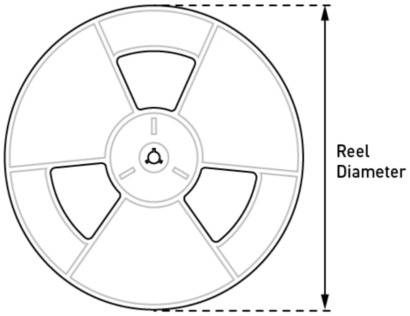
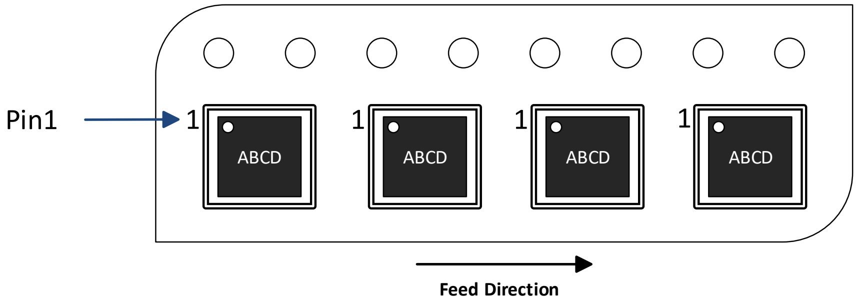
CARRIER INFORMATION





Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP87000-MGMJTH-Z	TLGA-41 (5mmx6mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	4/22/2025	Initial Release	-

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