DESCRIPTION

The MP8699B is a MOSFET driver designed to drive enhancement-mode gallium nitride (GaN) MOSFETs and N-Channel MOSFETs with low gate voltages in half-bridge or synchronous application. The device has independent high-side (HS) and low-side (LS) pulse-width modulation (PWM) inputs.

The MP8699B employs MPS's proprietary bootstrap (BST) technique for the HS-FET driver voltage, and can operate up to 100V. The BST charging technology prevents the HS-FET driver voltage from exceeding the supply voltage (V_{CC}), which prevents the gate voltage (V_{GATE}) from exceeding the enhancement-mode GaN MOSFET's maximum gate-to-source voltage (V_{GS}) rating.

The MP8699B has two separate gates for independent MOSFET turn-on and turn-off speed control by adding impedance to the gate loop.

The MP8699B is available in a WLCSP-12L (2mmx2mm) package.

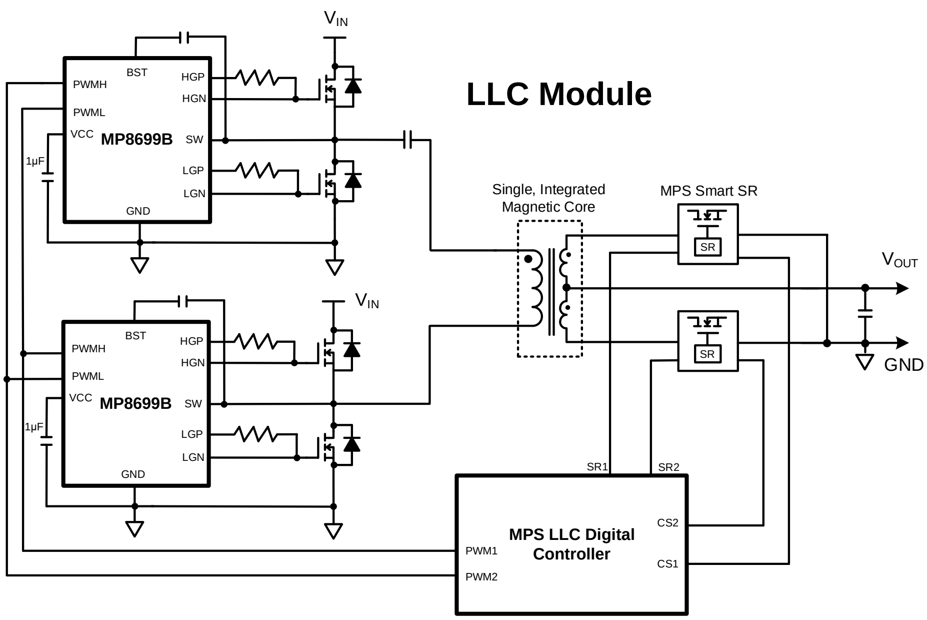
FEATURE

- Independent High-Side (HS) and Low-Side (LS) Logic Inputs
- High-Side MOSFET (HS-FET) Floating Bias Voltage Rail Operates Up to $100V_{DC}$
- Separate Gate Outputs for Adjustable Turn-On and Turn-Off Speed Control
- 4.5VV to 5.5V Supply Voltage (V_{CC}) Range
- 0.2Ω Pull-Down Resistance and 1.3Ω Pull-Up Resistance
- Fast Propagation Time (Typically 17ns)
- Excellent Propagation Delay Matching (Typically 1.5ns)
- Available in a WLCSP-12L (2mmx2mm) Package

APPLICATIONS

- Half-Bridge and Full-Bridge Converters
- Synchronous Buck Converters
- Power Modules

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP8699BGC	WLCSP-12L (2mmx2mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP8699BGC-Z).

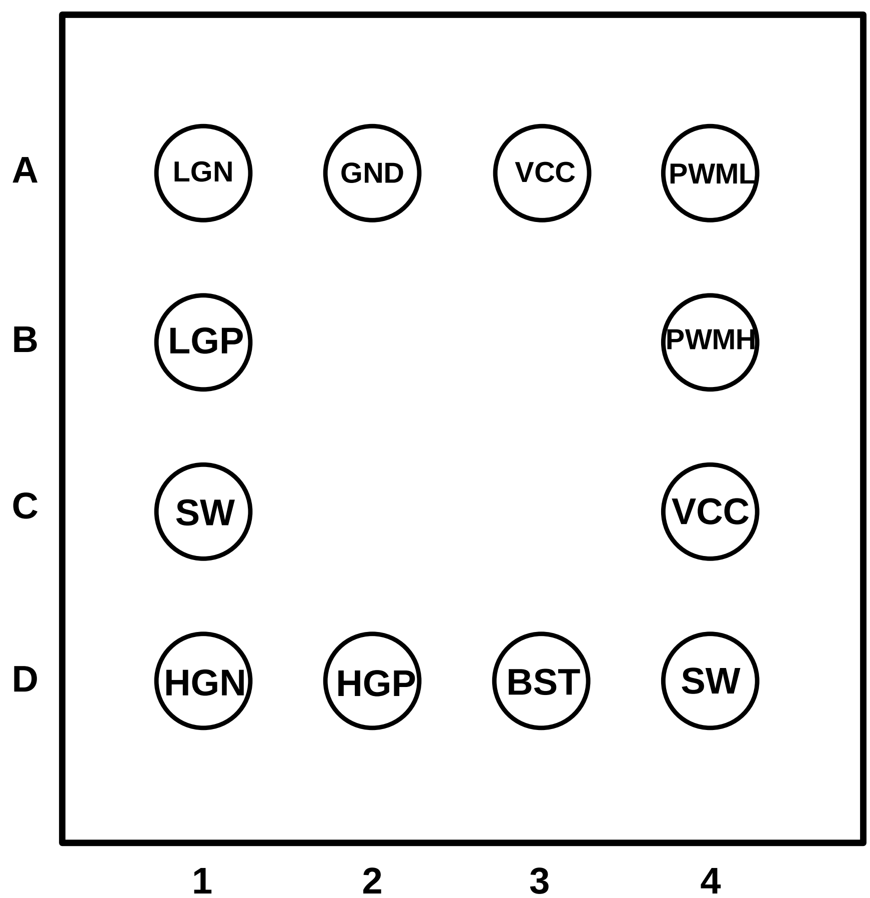
TOP MARKING

LNY
LLL

LN: Product code
Y: Year code
LLL: Lot number

PACKAGE REFERENCE

TOP VIEW



WLCSP-12L (2mmx2mm)

PIN FUNCTIONS

Pin#	Name	Description
A3, C4	VCC	**5V driver supply.** Connect a low-ESR MLCC decoupling capacitor between the VCC and GND pins.
A4	PWML	**LS-FET driver PWM input.** The PWML pin can withstand up to 5.5V. Float PWML if not used.
B4	PWMH	**HS-FET driver PWM input.** The PWMH pin can withstand up to 5.5V. Float PWML if not used.
C1, D4	SW	**Switching node.** Connect the SW pin to the high-side MOSFET (HS-FET) source and the bootstrap (BST) capacitor's negative terminal.
D3	BST	**HS-FET gate driver bootstrap rail.** Connect a capacitor between the BST and SW pins, placed as close to these pins as possible.
D2	HGP	**HS-FET gate driver source current output.** Short the HGP pin to the high-side MOSFET's (HS-FET's) gate or connect HGP to the HS-FET's gate using a resistor to adjust the turn-on speed.
D1	HGN	**HS-FET gate driver sink current output.** Short the HGN pin to the HS-FET's gate or connect HGN to the HS-FET's gate using a resistor to adjust the turn-off speed.
B1	LGP	**LS-FET gate driver source current output.** Short the LGP pin to the low-side MOSFET's (LS-FET's) gate or connect LGP to the LS-FET's gate using a resistor to adjust the turn-on speed.
A1	LGN	**LS-FET gate driver sink current output.** Short the LGN pin to the LS-FET's gate or connect LGN to the LS-FET's gate using a resistor to adjust the turn-off speed.
A2	GND	**IC ground.**

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{CC}) (DC)...............-0.3V to +6V
V_{CC} (25ns).......................................-0.3V to +8V
V_{BST-SW} (DC)....................................-0.3V to +6V
V_{BST-SW} (25ns) ....-0.3V to +8V
V_{SW} (DC) ....-0.3V to +105V
V_{SW} (25ns)....................................-5V to +108V
$V_{BST-GND}$ .... -0.3V to V_{SW} + 6V
V_{HGP}, V_{HGN}....................V_{SW} - 0.3V to V_{BST} + 0.3V
V_{LGP}, V_{LGN}..-0.3V to +6V
V_{PWMH}, V_{PWML} ....-0.3V to +6V
Junction temperature...............................150°C
Lead temperature………………………… 260°C
Storage temperature………….. -65°C to +150°C

Recommended Operating Conditions (2)

Supply voltage (V_{CC}) ....4.5V to 5.5V
PWMH, PWML.................................0V to 5.5V
V_{SW}... ....0V to 95V
Operating junction temp (T_J)…. -40°C to +125°C

Thermal Resistance (3) θ_{JB} θ_{JC_TOP}

WLCSP-12L (2mmx2mm).....8.2…….0.7…°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) θ_{JB} is the thermal resistance from the junction to the board around the S soldering point. θ_{JC_TOP} is the thermal resistance from the junction to the top of the package.

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, typical values are tested at T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VCC Supply						
Quiescent current	I_Q	PWMH = PWML = low			100	μA
VCC operating current	I_{VCC}	HGP = HGN, LGP = LGN, f_{SW} = 1MHz, no load			3	mA
Supply voltage (V_{CC}) under-voltage lockout (UVLO) rising threshold	$V_{CC\_UVLO\_RISING}$			4	4.35	V
V_{CC} UVLO hysteresis	$V_{CC\_UVLO\_HYS}$			300		mV
Pulse-Width Modulation (PWM) Input						
PWM logic high voltage	V_{HIGH_PWM}		2.1			V
PWM hysteresis	V_{HYS_PWM}			400		mV
PWM logic low voltage	V_{LOW_PWM}				1.3	V
PWM input pull-down resistance	R_{PWM_IN}			200		kΩ
High-Side (HS) Driver Supply						
BST to SW (V_{BST-SW}) UVLO rising threshold	$V_{BST\_UVLO\_RISING}$			0.7		VCC
V_{BST-SW} UVLO hysteresis				0.08		VCC
High-Side MOSFET (HS-FET) and Low-Side MOSFET (LS-FET) Gate Drivers						
Peak source current (4)	I_{SOURCE_PEAK}	HGx to SW voltage (V_{HGx-SW}) = 0V, $V_{LGx-GND}$ = 0V		1.7		A
Peak sink current (4)	I_{SINK_PEAK}	V_{HGx-SW} = 5V, $V_{LGx-GND}$ = 5V		5.2		A
Source resistance	R_{SOURCE}	I_{SOURCE} = 100mA, 5V		1.3		Ω
Sink resistance	R_{SINK}	I_{SINK} = 100mA, 5V		0.2		Ω
HGN and LGN output leakage current	I_{GN_LKG}	V_{HGN} = 5V, V_{LGN} = 5V			1.5	μA
HGP and LGP output leakage current	I_{GP_LKG}	V_{HGP} = 0V, V_{LGP} = 0V			1.5	μA
HS-FET and LS-FET Gate Driver Timing Characteristics (4)						
HGP rise time (0.5V to 4.5V) (4)	t_{RISE_SW}	3.3nF load, V_{CC} = 5V		10		ns
HGN fall time (4.5V to 0V) (4)	t_{FALL_SW}	3.3nF load, V_{CC} = 5V		3		ns
LGP rise time (0.5V to 4.5V) (4)	t_{RISE_LS}	3.3nF load, V_{CC} = 5V		10		ns
LGN fall time (4.5V to 0.5V) (4)	t_{FALL_LS}	3.3nF load, V_{CC} = 5V		3		ns
HGP turn-on propagation delay (4)	t_{HPH}	3.3nF load, V_{CC} = 5V, PWMH rising to HGP rising		17		ns
HGN turn-off propagation delay (4)	t_{HPL}	3.3nF load, V_{CC} = 5V, PWMH falling to HGN falling		17		ns
LGP turn-on propagation delay (4)	t_{LPH}	3.3nF load, V_{CC} = 5V, PWML rising to LGP rising		17		ns
LGN turn-off propagation delay (4)	t_{LPL}	3.3nF load, V_{CC} = 5V, PWML falling to LGN falling		17		ns

ELECTRICAL CHARACTERISTICS *(continued)*

V_{CC} = 5V, typical values are tested at T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
LGP on and HGN off matching delay (4)	t_{OFF_MATCH}			1.5		ns
LGN off & HGP on matching delay (4)	t_{ON_MATCH}			1.5		ns
Minimum PWM input pulse time (4)	t_{PWM_MIN}			10		ns
Minimum gate output pulse time (4)	t_{GATE_MIN}			13		ns

Note:

4) Guaranteed by design or characterization data. Not tested in production.

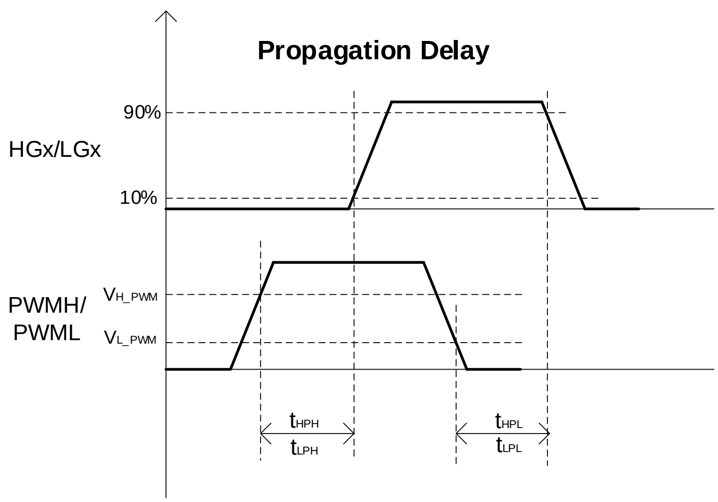


Figure 1: Propagation Delay Timing Diagram

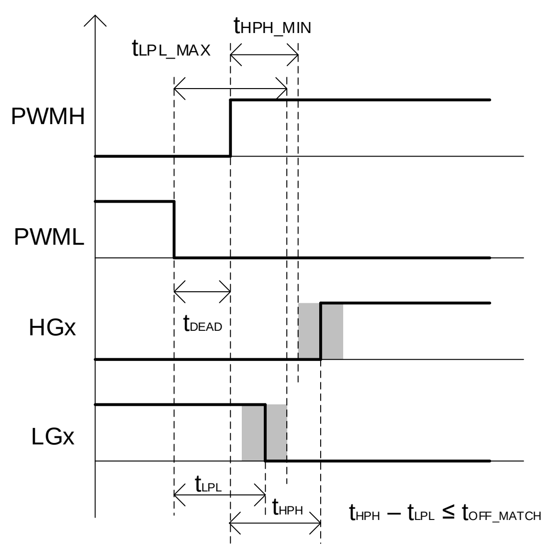
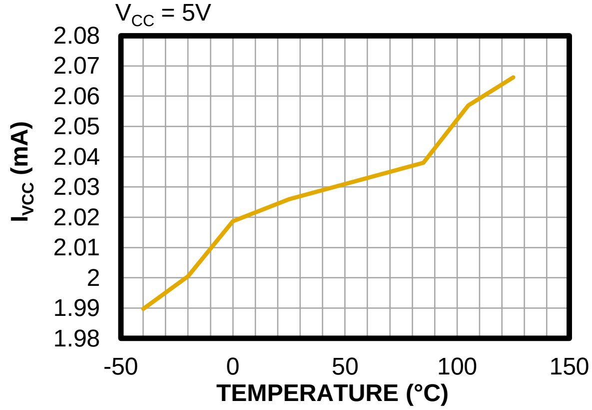


Figure 2: Matching Delay Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

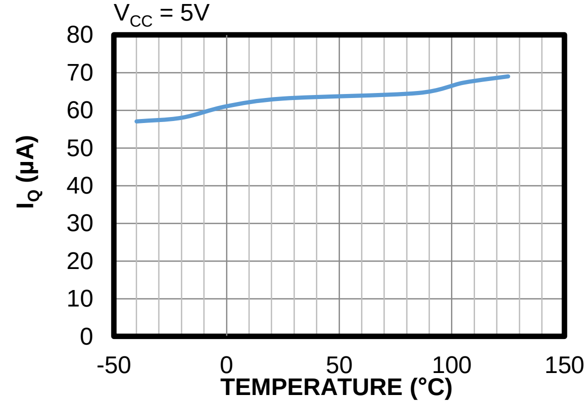
VCC Operating Current vs. Temperature

V_{CC} = 5V

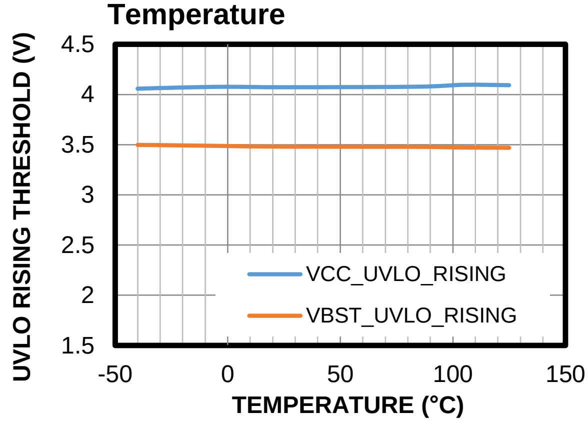


Quiescent Current vs. Temperature

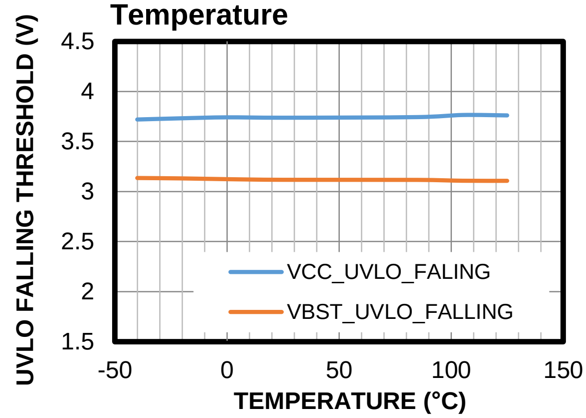
V_{CC} = 5V



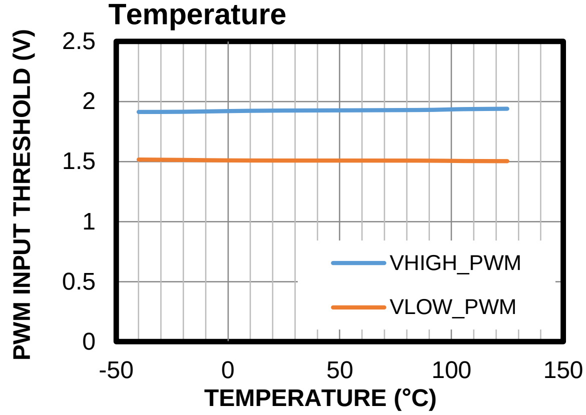
UVLO Rising Threshold vs. Temperature



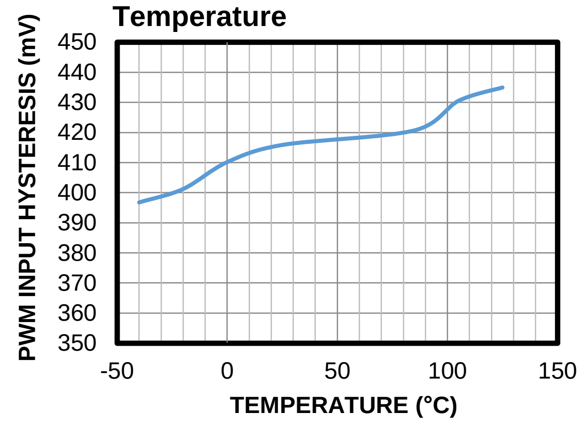
UVLO Falling Threshold vs. Temperature



PWM Input Threshold vs. Temperature



PWM Input Hysteresis vs. Temperature



FUNCTIONAL BLOCK DIAGRAM

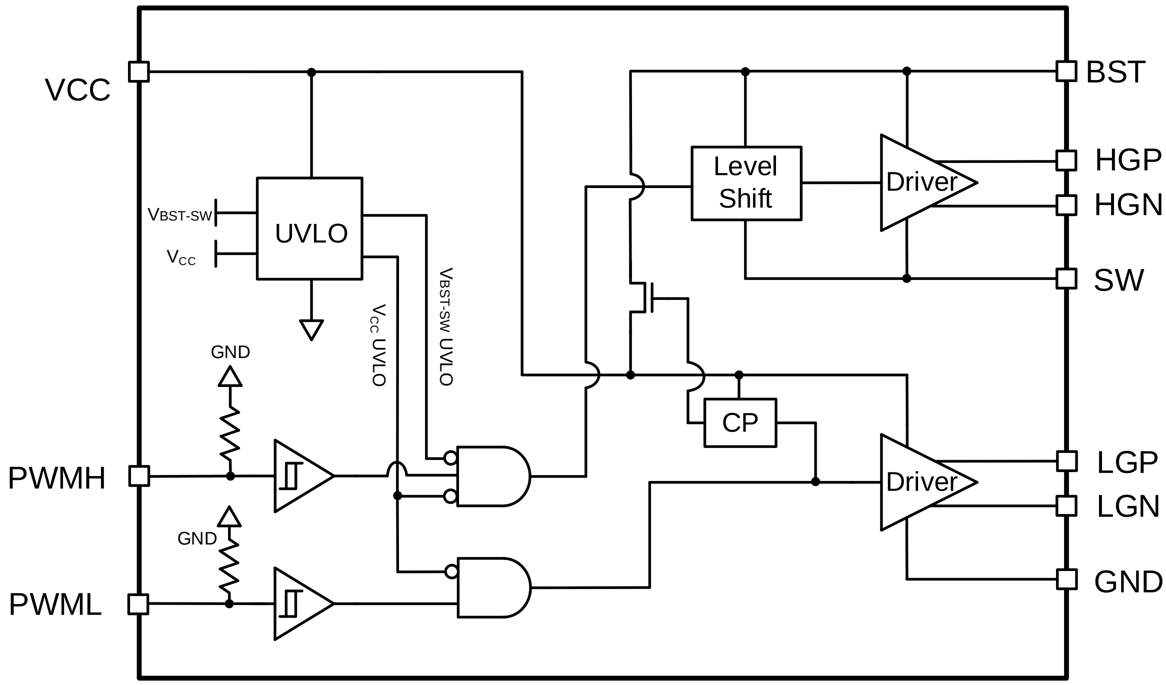


Figure 3: Functional Block Diagram

OPERATION

The MP8699B is a MOSFET driver designed to drive both high-side (HS) and low-side (LS) enhancement-mode gallium nitride (GaN) MOSFETs and N-channel MOSFETs. The floating HS bias voltage can support up to 100V of DC bus voltage.

MPS's proprietary bootstrap (BST) charging technology prevents the HS driver voltage from exceeding the supply voltage (V_{CC}), which prevents the gate voltage (V_{GATE}) from exceeding the enhancement-mode GaN MOSFET's maximum gate-to-source voltage (V_{GS}) rating.

Pulse-Width Modulation (PWM) Input and Output

The PWMH and PWML pins are independently controlled logic inputs that can withstand up to 5.5V. Float PWMH or PWML if not used. If both PWMH and PWML control the high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET) of the same bridge, then set a sufficient dead time (DT) between PWMH and PWML to avoid shoot-through (see Figure 4).

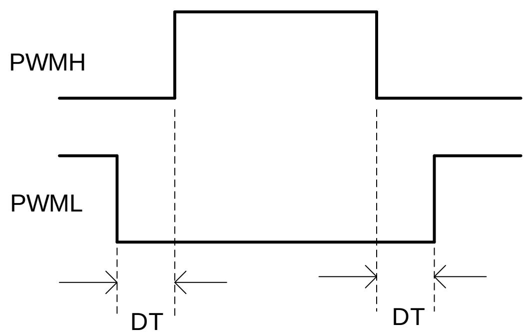


Figure 4: PWM Input Dead Time Timing

The MP8699B has separate gate outputs, which allows the user to add different gate loop resistors to adjust the turn-on and turn-off speed. The outputs have a 0.2Ω pull-down resistance and a 1.3Ω pull-up resistance. The 0.2Ω pull-down resistance keeps V_{GS} from exceeding the GaN MOSFET turn-on threshold (V_{TH}) during high dV/dt case (see Table 1 on page 8).

Under-Voltage Lockout (UVLO)

The MP8699B employs both V_{CC} and BST to SW (V_{BST-SW}) under-voltage lockout (UVLO) protection.

If V_{CC} drops below the V_{CC} UVLO rising threshold ($V_{CC\_UVLO\_RISING}$), both PWMH and PWML are ignored. If V_{BST-SW} drops below the V_{BST-SW} UVLO rising threshold ($V_{BST\_UVLO\_RISING}$), PWMH is ignored, the HS-FET gate driver is pulled low, and the LS-FET gate responds with PWML. If both V_{BST-SW} and V_{CC} exceed their respective thresholds, then both the HS-FET gate driver and LS-FET gate driver are working (see Table 2 on page 9).

Bootstrap (BST) Clamping

Due to the intrinsic nature of enhancement-mode GaN MOSFETs, the bottom switch's source-to-drain voltage (V_{SD}) typically exceeds a diode's forward-voltage drop when the gate is pulled low. This can cause a negative voltage on the SW pin. This negative voltage transient is worsened by the layout and the device's drain/source parasitic inductances. With the HS-FET driver using a floating BST configuration, the negative SW voltage (V_{SW}) can cause an excessive BST voltage (V_{BST}), which can damage the HS GaN MOSFET.

The MP8699B employs a new charging logic, where V_{BST-SW} is charged from V_{CC} only when PWML is logic high. There is no current path from VCC to BST when PWML is logic low, so V_{BST-SW} should remain below V_{CC}. An active circuit clamps V_{BST-SW} to prevent it from exceeding (1.05 x V_{CC}).

Table 1: HGx and LGx Logic Truth Table

PWMH	PWML	HGP	HGN	LGP	LGN
High	Low	High	Open	Open	Low
Low	High	Open	Low	High	Open
High	High	High	Open	High	Open
Low	Low	Open	Low	Open	Low

Table 2: V_{CC} and V_{BST-SW} UVLO PWM Distribution Logic

V_{CC} Condition	V_{BST-SW} Condition	PWMH	PWML	HGx	LGx
V_{CC} is below $V_{CC\_UVLO\_RISING}$ during start-up	-	High	Low	Low	Low
		0	High	Low	Low
		High	High	Low	Low
		Low	Low	Low	Low
V_{CC} is below ($V_{CC\_UVLO\_RISING}$ - $V_{CC\_UVLO\_HYS}$) after start-up		High	Low	Low	Low
		Low	High	Low	Low
		High	High	Low	Low
		Low	Low	Low	Low
V_{CC} exceeds $V_{CC\_UVLO\_RISING}$	V_{BST-SW} is below (0.7 x V_{CC}) during start-up	High	Low	Low	Low
		Low	High	Low	High
		High	High	Low	High
		Low	Low	Low	Low
	V_{BST-SW} is below (0.62 x V_{CC}) after start-up	High	Low	Low	Low
		Low	High	Low	High
		High	High	Low	High
		Low	Low	Low	Low

APPLICATION INFORMATION

Selecting the VCC Capacitor (C_{VCC})

The VCC bypass capacitor (C_{VCC}) provides the gate charge for the low-side and high-side transistors. The required bypass capacitance (C_{VCC}) can be calculated with Equation (1):

$$C_{VCC} > (Q_{gH} + Q_{gL}) / \Delta V \quad (1)$$

Where Q_{gH} is the HS-FET gate charge, Q_{gL} is the LS-FET gate charge, and ΔV is the maximum allowable voltage drop across the bypass capacitor.

Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are strongly recommended due to their low ESR and small temperature coefficients.

Place the VCC capacitors as close to the VCC pin as possible. For most applications, a 1µF capacitor in a small package (0402) is sufficient to maintain a small solution size. For applications with a higher PWM frequency, choose a 2.2µF to 4.7µF capacitor in a 0603 or 0805 package to improve system stability.

Selecting the Bootstrap Capacitor (C_{BST})

The bootstrap capacitor (C_{BST}) provides the gate charge for the HS-FET. The required C_{VCC} can be calculated with Equation (2):

$$C_{VCC} > Q_{gH} / \Delta V \quad (2)$$

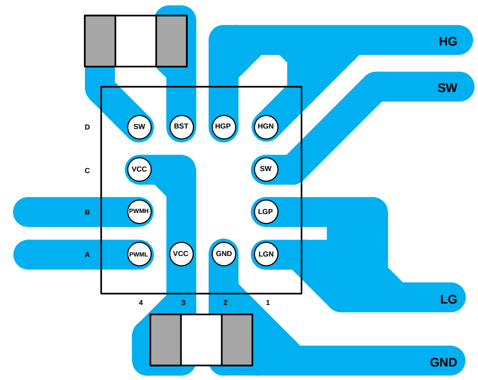
Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are strongly recommended due to their low ESR and small temperature coefficients.

Place C_{BST} as close to the BST and SW pins as possible. For most applications, a 220nF capacitor in a small package (0402) is sufficient to maintain a small solution size.

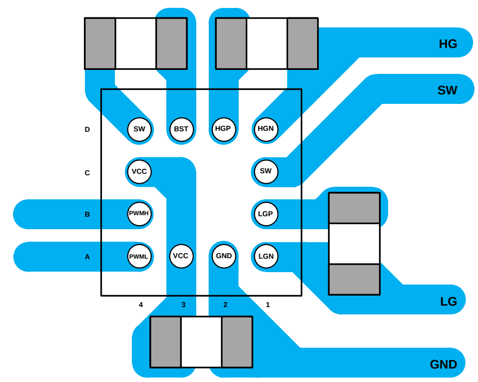
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 5 and follow the guidelines below:

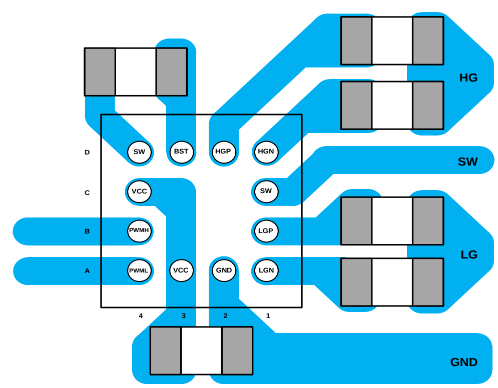
1. Place the IC as close to the GaN FETs as possible to reduce loop inductance and noise.
2. Connect low-ESR/ESL bypass capacitors between the VCC and GND pins, and the BST and SW pins. Place these capacitors as close to the IC as possible to support the high peak current being drawn from VCC when the GaN FETs and MOSFETs turn on.
3. Use a Kelvin connection between the IC and GaN FETs to minimize the common-source inductance.



PCB Layout without Gate Resistors



PCB Layout with HGP and LGP Gate Resistors



PCB Layout with HGP/HGN and LGP/LGN Gate Resistors

Figure 5: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

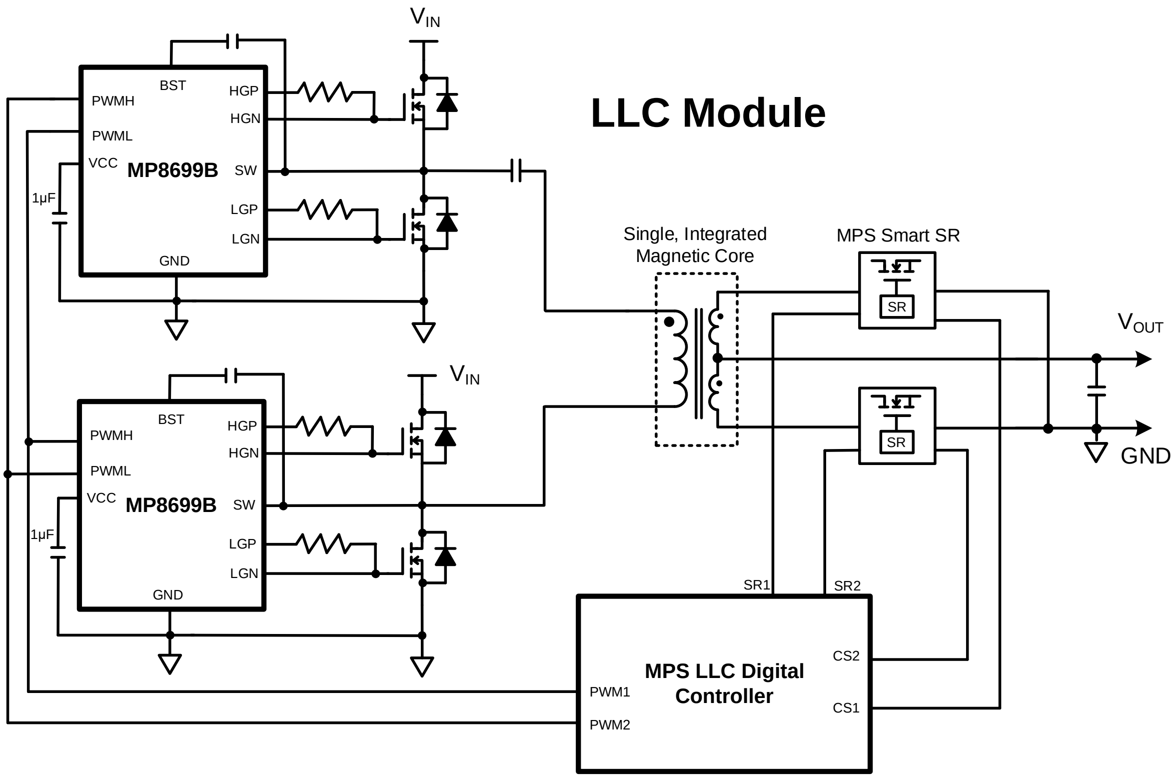
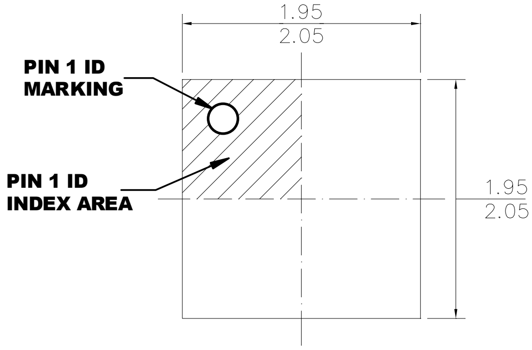


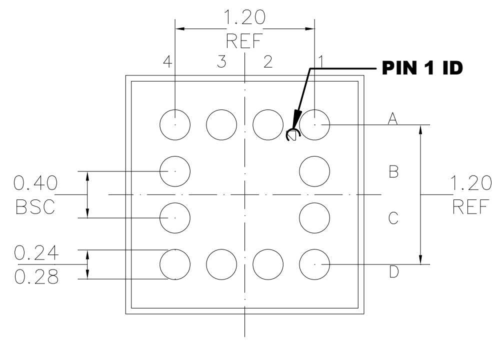
Figure 6: Typical Application Circuit

PACKAGE INFORMATION

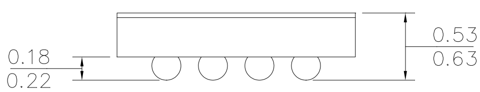
WLCSP-12L (2mmx2mm)



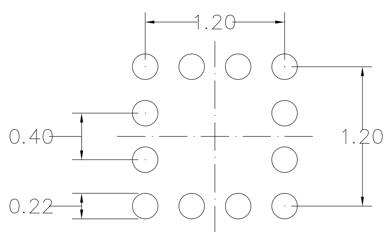
TOP VIEW



BOTTOM VIEW



SIDE VIEW

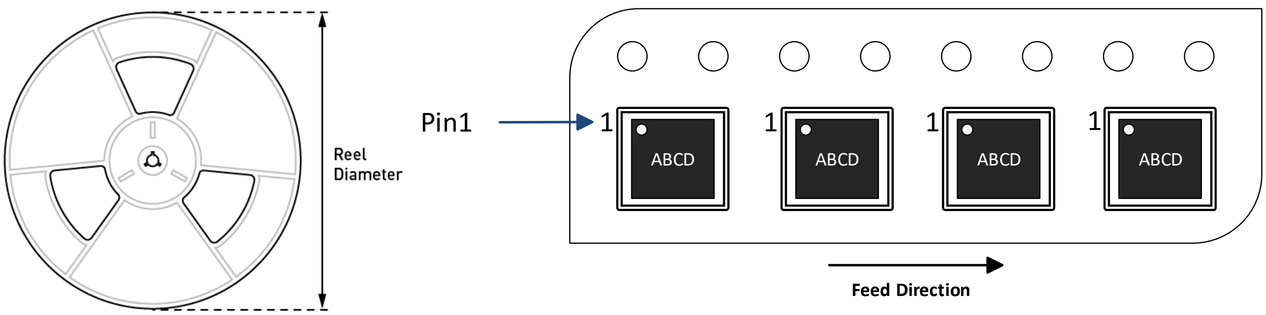


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) BALL COPLANARITY SHALL BE 0.05 MILLIMETER MAX.
3) JEDEC REFERENCE IS MO-211.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP8699BGC-Z	WLCSP-12L (2mmx2mm)	3000	N/A	N/A	7in	8mm	4mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	6/20/2023	Initial Release	-
1.1	10/9/2023	Updated parameter name for “HGN fall time”; corrected unit for LGP turn-on propagation delay	4