MP86992

16V, 50A, Intelli-Phase™ Solution in a 5mmx6mm LGA Package

DESCRIPTION

The MP86992 is a monolithic half-bridge with built-in internal power MOSFETs and gate drivers. It achieves 50A of continuous output current over a wide input supply range.

The MP86992 takes a monolithic IC approach that drives up to 50A of current per phase. The integration of drivers and MOSFETs results in high efficiency due to an optimal dead time and parasitic inductance reduction. It can operate from 100kHz to 3MHz.

The device offers many features to simplify system design. The MP86992 works with controllers with a tri-state PWM signal and comes with an accurate current sense to monitor the inductor current and temperature sense to report the junction temperature.

The device is ideal for server applications where efficiency and small size are a premium. The MP86992 is available in an LGA (5mmx6mm) package.

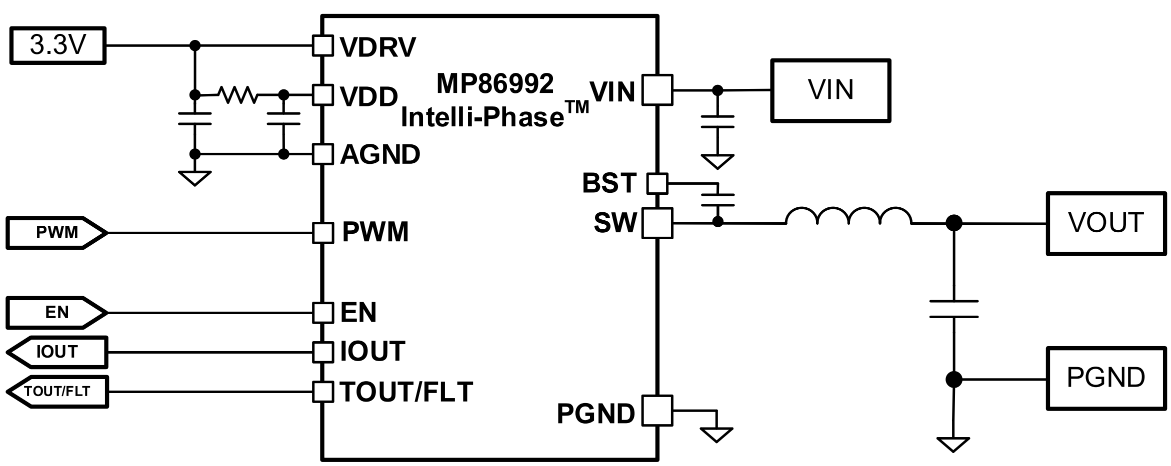
FEATURES

- Wide 3V to 16V Operating Input Range
- 50A Output Current
- Current Sense: Accu-Sense™
- Temperature Sense
- Accepts Tri-State PWM Signal
- Current-Limit Protection
- Over-Temperature Protection (OTP)
- Fault Reporting
- Available in an LGA (5mmx6mm) Package

APPLICATIONS

- Server Core Voltage
- Graphic Card Core Regulators
- Power Modules

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP86992GMJ	LGA-41 (5mmx6mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP86992GMJ-Z).

TOP MARKING

MPSYYWW

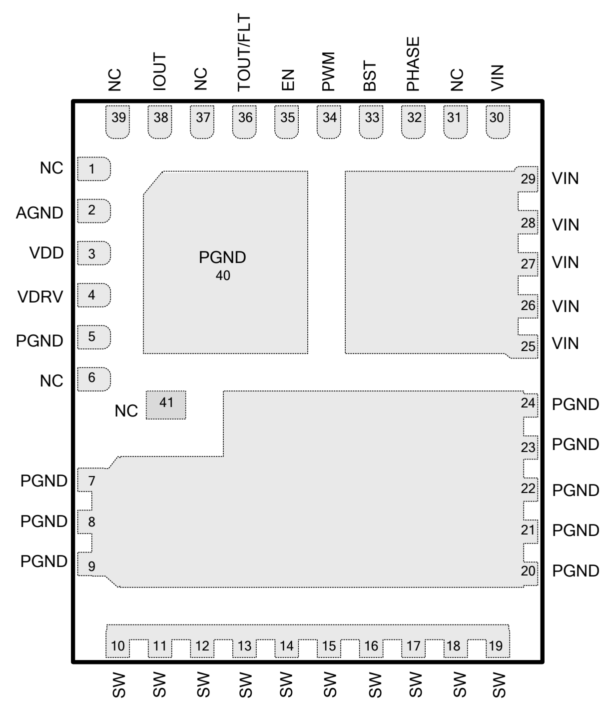
MP86992

LLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP86992: Part number
LLLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW



LGA-41 (5mmx6mm)

PIN FUNCTIONS

Pin #	Pin Name	Descriptions
1, 6, 31, 37, 39, 41	NC	**No connection.**
2	AGND	**Analog ground.**
3	VDD	**Supply voltage for internal circuitry.** Connect VDD to VDRV through a 2.2Ω resistor. Decouple VDD with a 1µF capacitor to AGND. Connect AGND and PGND at the VDD capacitor.
4	VDRV	**Driver voltage.** Connect VDRV to a 3.3V supply. Decouple VDRV with a 1µF to 4.7µF ceramic capacitor.
5, 7, 8, 9, 20–24, 40	PGND	**Power ground.**
10–19	SW	**Phase node.**
25–30	VIN	**Input supply voltage.** Place input ceramic capacitors (C_{IN}) close to the device to support the switching current with minimal parasitic inductance.
32	PHASE	**Switching node for the bootstrap capacitor connection.** The PHASE pin is connected to SW internally.
33	BST	**Bootstrap.** BST requires a 0.1µF to 0.22µF capacitor to drive the power switch's gate above the supply voltage. Connect the capacitor between SW and BST to form a floating supply across the power switch driver.
34	PWM	**Pulse-width modulation input.** Leave PWM floating or drive PWM to a mid-state level to put SW in a high-impedance state.
35	EN	**Enable.** Pull EN low to disable the MP86992 and place SW in a high-impedance state.
36	TOUT/FLT	**Single-pin temperature sense and fault reporting.** TOUT/FLT is pulled up to the VDD voltage when a fault occurs.
38	IOUT	**Current-sense output.** Use an external resistor to adjust the voltage proportional to the inductor current.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} to PGND................................ -0.3V to +25V
V_{IN} to V_{SW}.................................... -0.3V to +25V
V_{IN} to V_{SW} (10ns)...32V
V_{SW} to PGND............................... -0.3V to +21V
V_{SW} to PGND (25ns)........................ -5V to +25V
V_{BST} ....V_{SW} + 4V
V_{DD}, V_{DRV}...................................... -0.3V to +4V
All other pins......................-0.3V to VDD + 0.3V
Instantaneous current 110A
Junction temperature .... 150°C
Lead temperature .... 260°C
Storage temperature .... -65°C to +150°C

Recommended Operating Conditions (2)

Supply voltage (V_{IN}) .... 3.0V to 16V
Driver voltage (VDRV) .... 3.0V to 3.6V
Logic voltage (VDD)....................... 3.0V to 3.6V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (3)	θ_{JB}	θ_{JC_TOP}	
LGA-41 (5mmx6mm)	2.2	8.7	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) θ_{JB}: Thermal resistance from the junction to board around the PGND soldering point.
   θ_{JC_TOP}: Thermal resistance from the junction to the top of the package.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, VDRV = VDD = EN = 3.3V, T_A = 25°C for typical value, T_J = -40°C to +125°C for max and min values, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
I_{IN} shutdown		EN = low		90	180	μA
V_{IN} under-voltage lockout threshold rising				2.5	3.0	V
V_{IN} under-voltage lockout threshold hysteresis				450		mV
I_{VDRV} quiescent current		PWM = low		250	350	μA
I_{VDD} quiescent current		PWM = low		3		mA
VDD voltage UVLO rising				2.75	2.95	V
VDD voltage UVLO hysteresis				300		mV
High-side current limit (4)	I_{LIM_FLT}	Cycle-by-cycle up to 8 cycles	75			A
Low-side current limit (4)		Negative current limit, cycle-by-cycle, no fault report		-35		A
Negative current limit low-side off time (4)				200		ns
High-side current limit shutdown counter (4)				8		times
Dead time at SW rising (4)				2		ns
Dead time at SW falling (4)		Positive inductor current		6		ns
		Negative inductor current		28		ns
EN input high threshold voltage			2.30			V
EN input low threshold voltage					0.8	V
PWM high to SW rising delay (4)	t_{Rising}			20		ns
PWM low to SW falling delay (4)	$t_{Falling}$			20		ns
PWM tri-state to SW Hi-Z delay (4)	t_{LT}			40		ns
	t_{TL}			30		ns
	t_{HT}			40		ns
	t_{TH}			30		ns
Minimum PWM pulse width (4)				30		ns
IOUT sense gain accuracy (4)		20A ≤ I_{SW} ≤ 50A	-2	0	+2	%
IOUT sense gain	G_{IOUT}			5		μA/A
IOUT sense offset		I_{SW} = 0A, V_{IOUT} = 1.2V, T_J = 25°C	-2	0	+2	μA
		PWM = Hi-Z, V_{IOUT} = 1.2V	-1	0	+1	μA
IOUT pin voltage range (4)	V_{IOUT}		0.7		2.1	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, VDRV = VDD = EN = 3.3V, T_A = 25°C for typical value and T_J= -40°C to +125°C for max and min values, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
TOUT/FLT sense gain (4)				8		mV/°C
TOUT/FLT sense offset (4)		T_J = 25°C		800		mV
Over-temperature shutdown and fault flag (4)				160		°C
TOUT/FLT when fault occurs (4)			3.0	3.3		V
PWM resistor		Pull up, EN = high		6		kΩ
		Pull down, EN = high		5		kΩ
PWM logic high voltage			2.30			V
PWM tri-state region			1.10		1.8	V
PWM logic low voltage					0.80	V

Note:

4) Guaranteed by design or characterization data, not tested in production.

PWM TIMING DIAGRAM

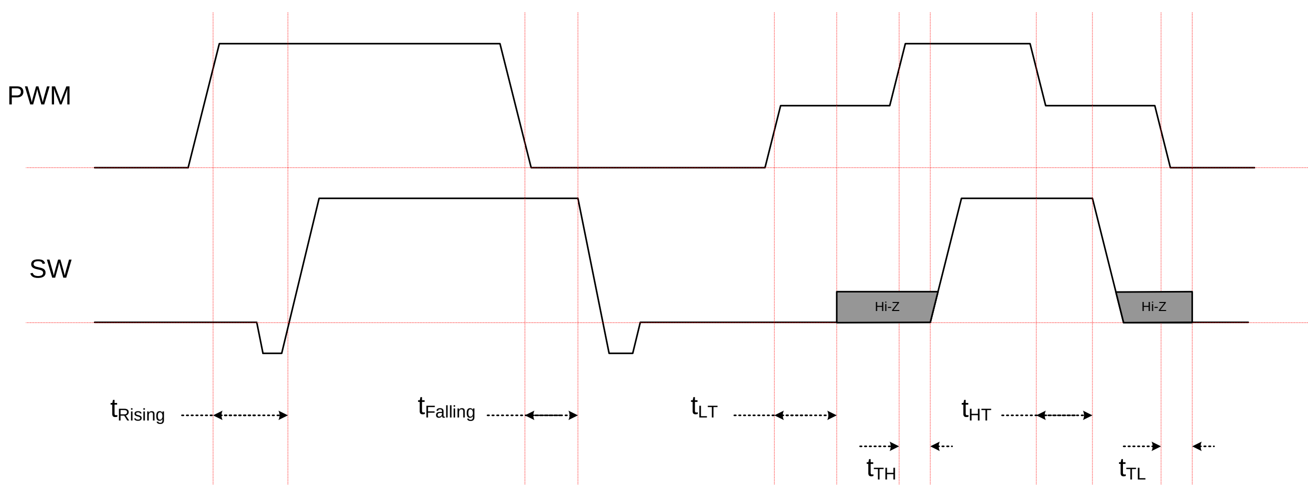
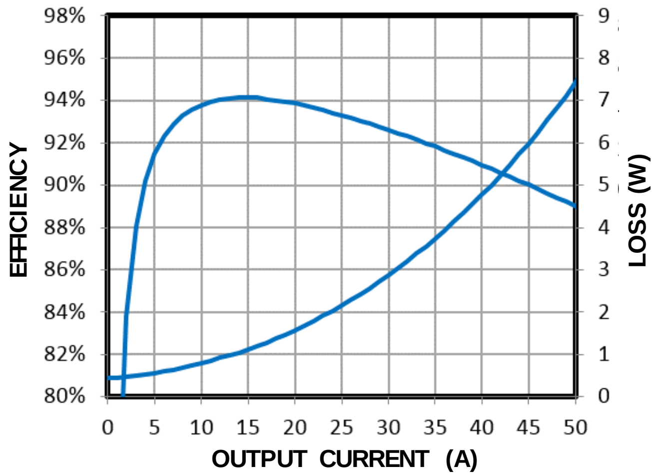


Figure 1: PWM Timing Diagram

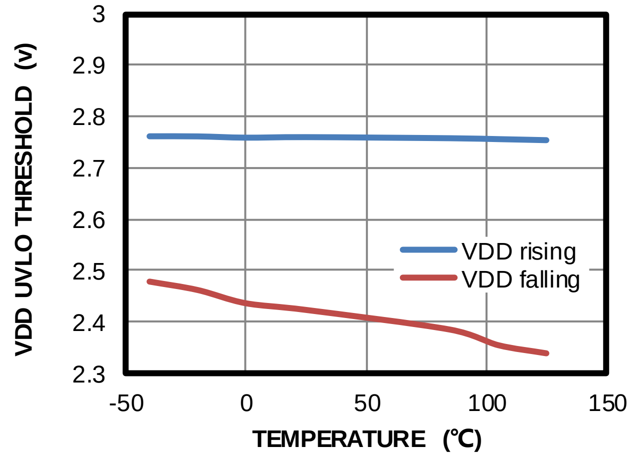
TYPICAL CHARACTERISTICS

Efficiency and Loss

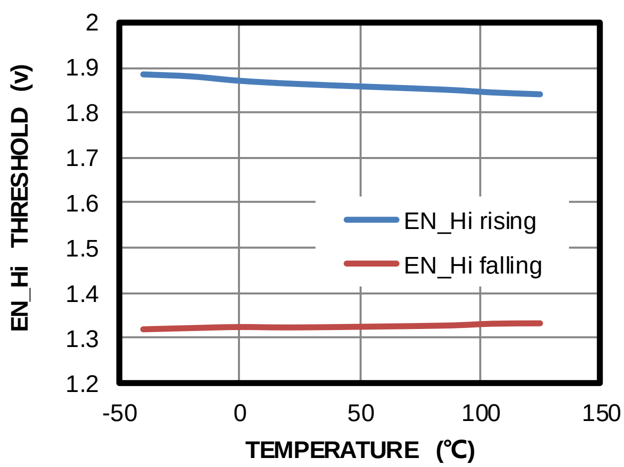
V_{IN} = 12V, V_{OUT} = 1.2V, L = 150nH, f_{SW} = 500kHz



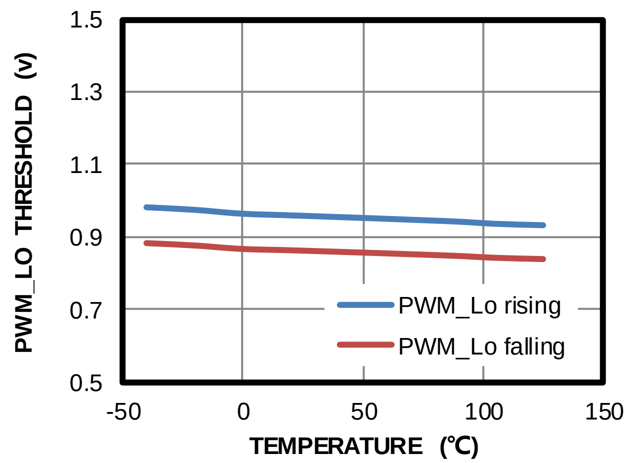
VDD UVLO



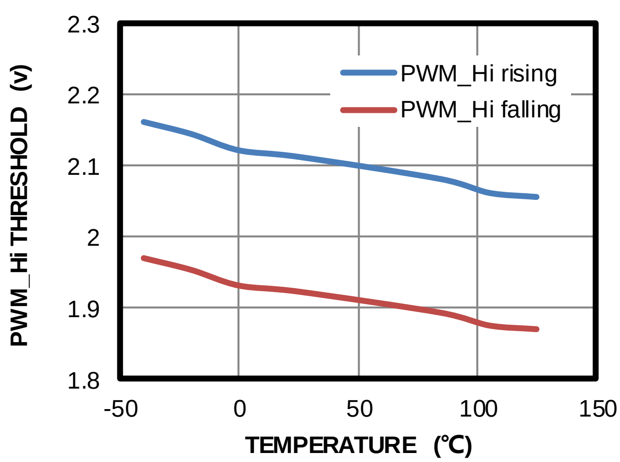
EN_HI



PWM_LO

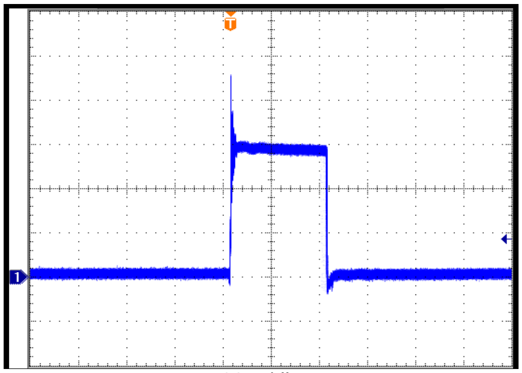


PWM_HI

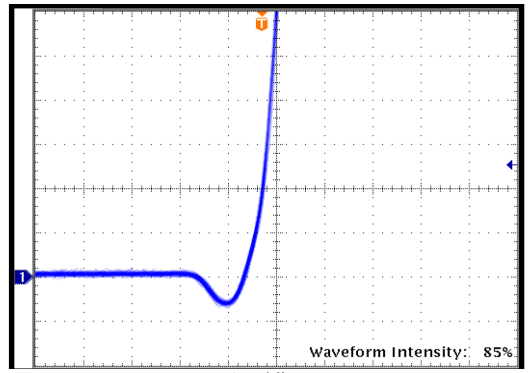


TYPICAL PERFORMANCE CHARACTERISTICS

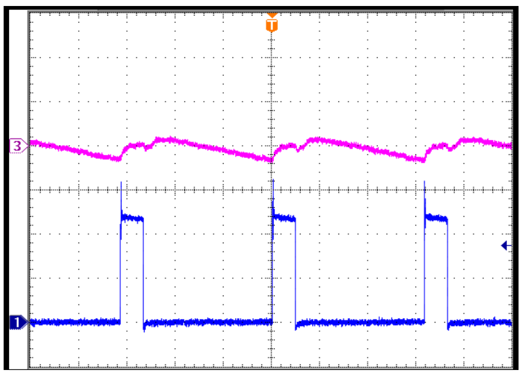
Switching
V_{IN} = 12V, L = 150nH, load = 30A



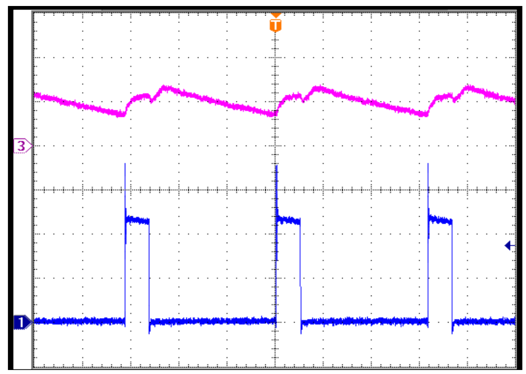
Dead Time @ SW Ringing
Load = 30A



IOUT Output
Load = 0A



IOUT Output
Load = 30A



FUNCTIONAL BLOCK DIAGRAM

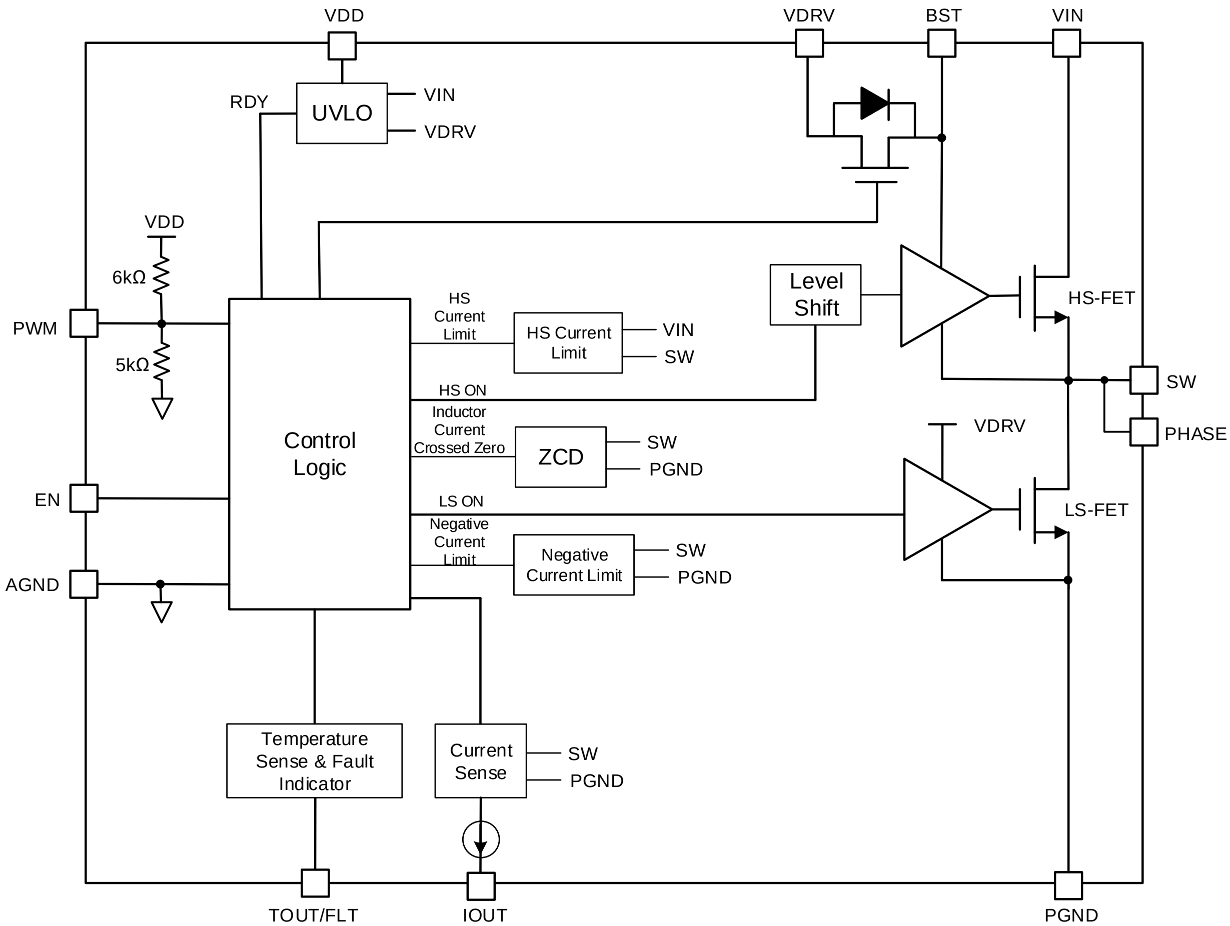


Figure 2: Functional Block Diagram

APPLICATION INFORMATION

Operation

The MP86992 is a 50A, monolithic, half-bridge driver with MOSFETs ideally suited for multi-phase buck regulators. An external 3.3V supply is required to supply both VDD and VDRV. When EN transitions from low to high and the VDRV signals are sufficiently high, operation begins.

Pulse-Width Modulation (PWM)

The pulse-width modulation (PWM) input pin is capable of tri-state input. When the PWM input signal is within the tri-state threshold window for (typically) 50ns (t_{HT} or t_{LT}), the high-side MOSFET (HS-FET) turns off immediately, and the low-side MOSFET (LS-FET) enters diode emulation mode, which is on until zero-current detection (ZCD). The tri-state PWM input can come from a forced mid-voltage PWM signal or from floating the PWM input. The internal current source charges the signal to a middle voltage. The PMW Timing Diagram shows the propagation delay definition from PWM to SW node (Figure 1).

Diode Emulation Mode

In diode emulation mode, when PWM is low or in a tri-state input, the LS-FET turns on whenever the inductor current is positive. The LS-FET turns off if the inductor current is negative or after the inductor current crosses the zero current. Diode emulation mode can be enabled by driving PWM to a middle state or floating PWM.

Current Sense

IOUT is a bidirectional current-source pin proportional to the inductor current. The current-sensing gain is 5µA/A. A resistor is used to program the voltage gain proportional to the inductor current, if needed.

The IOUT output has two states (see Table 1). In disable mode (EN = low), the current-sense circuit is disabled, and IOUT is in a Hi-Z (high-impedance) state.

Table 1: IOUT Output States

PWM	EN	IOUT
PWM	High	Active
x	Low	Hi-Z

An IOUT voltage range of 0.7V to 2.1V is required to achieve an accurate IOUT current output of up to +250µA/-175µA (e.g. +50A/-35A). Generally there is a resistor (R_{IOUT}), connected from IOUT to an external voltage, that is capable of sinking small currents to provide enough voltage level to meet the required operating voltage range. A proper reference voltage (V_{CM}) and R_{IOUT} value can be determined with Equation (1) and Equation (2):

$$0.7V < I_{IOUT} \times R_{IOUT} + V_{CM} < 2.1V \qquad (1)$$

$$I_{IOUT} = I_{SW} \times G_{IOUT} \qquad (2)$$

Where V_{CM} is a reference voltage connected to R_{IOUT}.

The Intelli-Phase™ current-sense output can be used by the controller to monitor the output current accurately. The cycle-by-cycle current information from IOUT can be used for phase-current balancing, over-current protection, and active-voltage positioning (output voltage droop).

Positive and Negative Inductor Current Limit

When HS-FET over-current is detected, the HS-FET turns off for that PWM cycle. If there are eight consecutive cycles of an HS-FET current limit event, the HS-FET latches off, TOUT/FLT pulls high to VDD, and the LS-FET turns on until ZCD. Toggle EN, or recycle V_{IN} or V_{DD} to release the latch and restart the device.

When the LS-FET detects a -35A valley current, the MP86992 turns off the LS-FET and turns on the HS-FET for 200ns to limit the negative current. The LS-FET negative current limit will not trigger a fault report.

Temperature Sense Output with Fault indicator (TOUT/FLT)

TOUT/FLT is a pin with two functions: junction temperature sense and fault detection.

TOUT/FLT has a voltage output proportional to the junction temperature whenever VDD is higher than its UVLO and the part is in active mode. The gain is 8mV/°C, and has a +800mV offset at 25°C. For example, 0.8V @ T_J = 25°C and 1.6V @ T_J = 125°C.

When any fault occurs, TOUT/FLT is pulled to the VDD voltage to report the fault event regardless of the temperature. 200ns after the fault occurs, the PWM impedance changes accordingly to indicate the fault type. Table 2 shows the PWM status regarding each fault event.

Table 2: PWM Resistance when a Fault Occurs

Fault Type	PWM
HS-FET current limit protection	10kΩ to AGND
Over-temperature protection	20kΩ to AGND
SW-PGND short protection	1kΩ to VDD

TOUT/FLT can monitor three fault events:

1. Over-current limit (HS-FET) – To trip the over-current fault, the current limit must be exceeded eight consecutive times. Once a fault occurs, the MP86992 latches off to turn off the HS-FET. The LS-FET turns off when the inductor current reaches zero. PWM uses a 10kΩ resistor to AGND to indicate the fault type.
2. Over-temperature fault at $T_J > 160°C$ – Once a fault occurs, the MP86992 latches off to turn off the HS-FET. The LS-FET turns off when the inductor current reaches zero. PWM uses a 20kΩ resistor to AGND to indicate the fault type.
3. SW to PGND shorted – Once a fault occurs, the MP86992 latches off to turn off the HS-FET. PWM is pulled high (1kΩ to VDD) to indicate the fault type.

The fault latch can be released by toggling EN, or by recycling VIN or VDD.

For multi-phase operation, connect the TOUT/FLT pin of each Intelli-Phase™ together (see Figure 3).

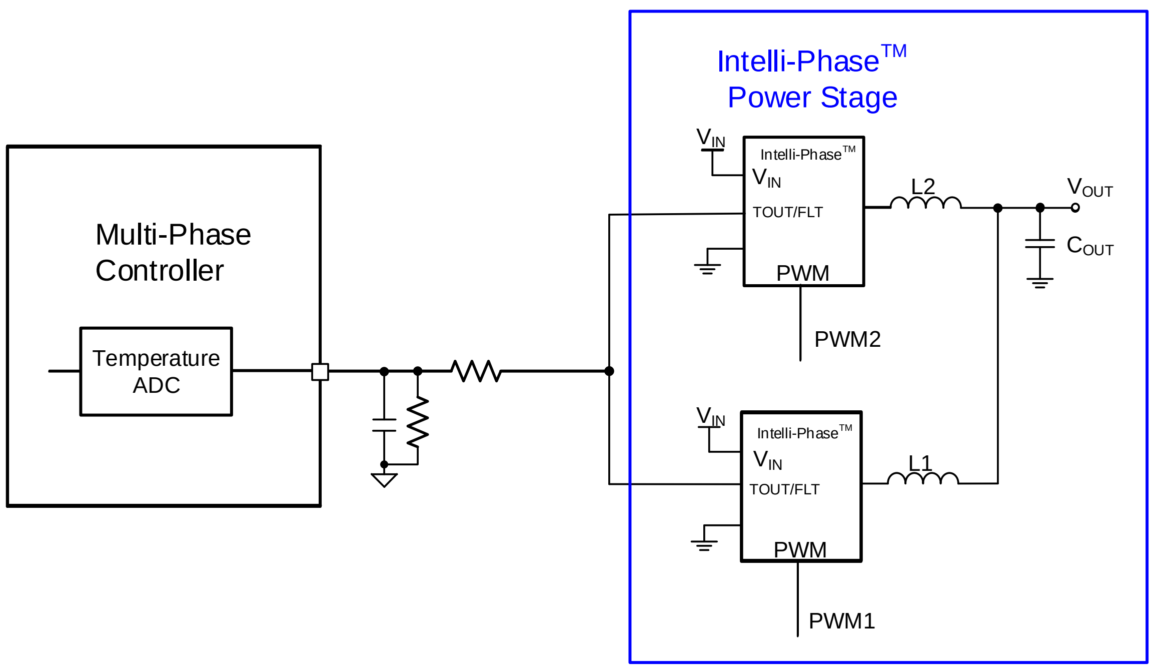


Figure 3: Multi-Phase Temperature Sense Utilization

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 4 and follow the guidelines below:

1. Place the input MLCC capacitors as close to VIN and PGND as possible.
2. Place the major MLCC capacitors on the same layer as the MP86992.
3. Place as many VIN and PGND vias underneath the package as possible.
4. Place the vias between the VIN or PGND long pads.
5. Place a VIN copper plane on the second inner layer to form the PCB stack as positive/negative/positive to reduce the parasitic impedance from the input MLCC capacitor to the MP86992.
6. Ensure that the copper plane on the inner layer covers at least the VIN vias underneath the package and the input MLCC capacitors.
7. Place more PGND vias close to the PGND pin/pad to minimize both parasitic resistance/impedance and thermal resistance.
8. Place the BST and VDRV capacitors as close to the MP86992's pins as possible.
9. Use a trace width of 20 mils or higher to route the path.
10. Avoid placing vias on the BST driving path.
11. Use a 0.1µF to 1µF bootstrap capacitor.
12. Place the VDD decoupling capacitor close to the device.
13. Connect AGND and PGND at the point of the VDD capacitor's ground connection.
14. Keep the IOUT signal trace away from high-current paths, such as SW and PWM.

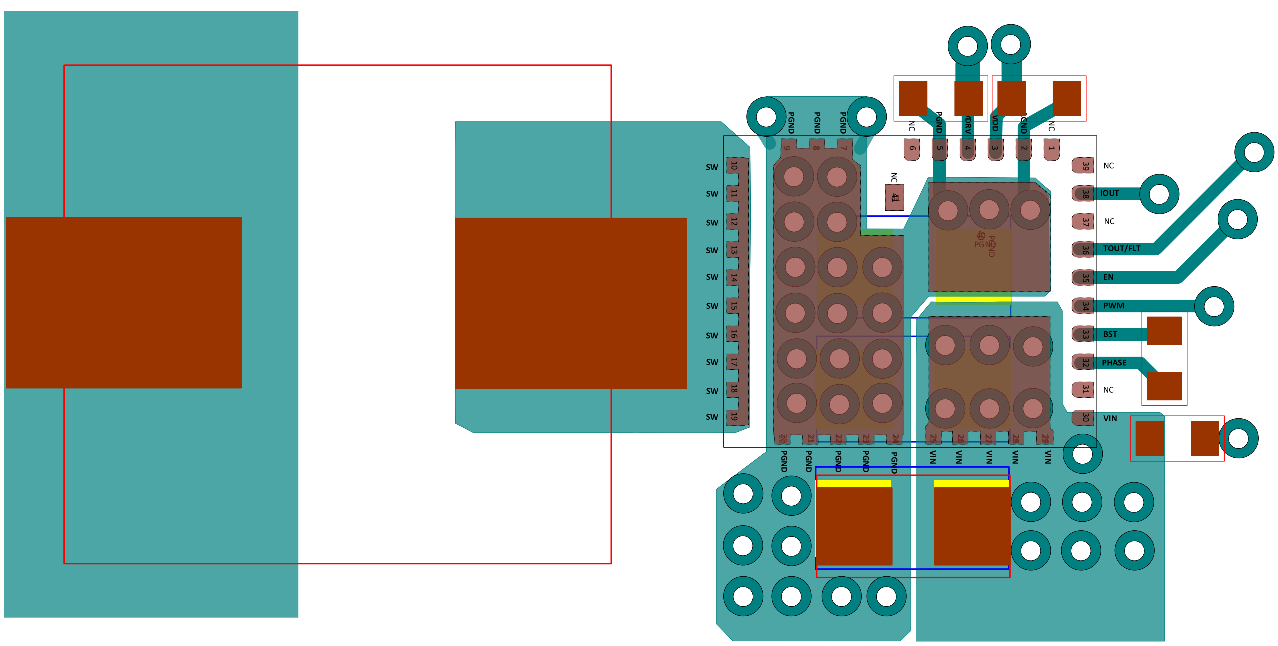


Figure 4: Recommended PCB Layout (Placement and Top Layer PCB)

Input Capacitor: 0805 package (top and bottom sides) and 0402 package (top side)

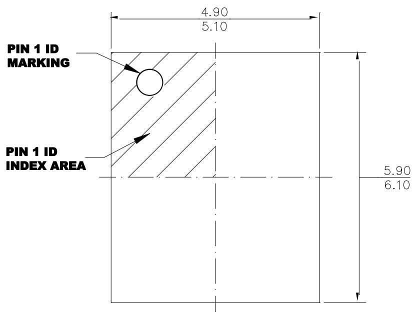
Inductor: 11x8 package

VDD/BST/VDRV capacitor: 0402 package

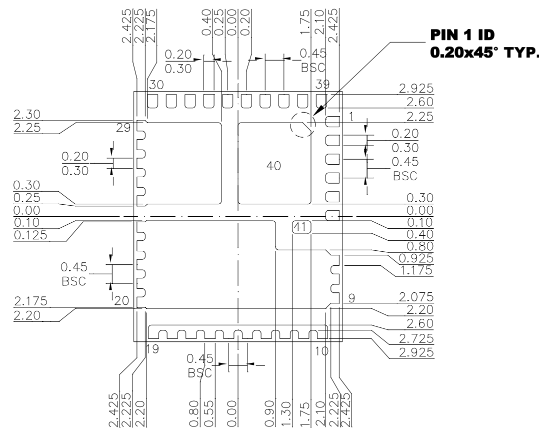
Via size: 20/10 mils

PACKAGE INFORMATION

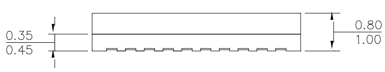
LGA-41 (5mmx6mm)



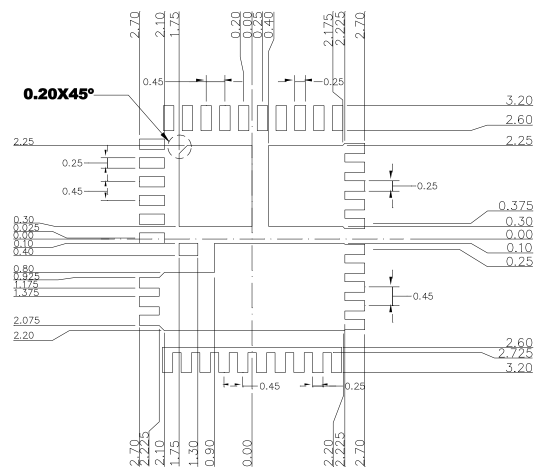
TOP VIEW



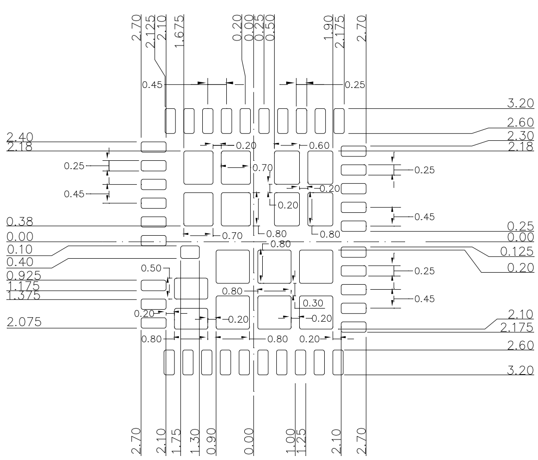
BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN



RECOMMENDED STENCIL DESIGN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-303.
4) DRAWING IS NOT TO SCALE.

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