MP86962

80A, Radiation-Tolerant Intelli-Phase™ DrMOS Solution in a TLGA-41 (5mmx6mm) Package

DESCRIPTION

The MP86962 is a monolithic half-bridge driver with built-in internal power MOSFETs and gate drivers. The MP86962 can achieve up to 80A of continuous output current (I_{OUT}) across a wide input supply voltage (V_{IN}) range.

The MP86962 uses a monolithic IC to drive up to 80A of current per phase. The integration of drivers and MOSFETs results in high efficiency due to an optimal dead time (DT) and reduction of parasitic inductance. The MP86962 can operate from 100kHz to 3MHz.

The MP86962 offers many features to simplify system design. The device includes controllers with a tri-state pulse-width modulation (PWM) signal and supports accurate current sense to monitor the inductor current (I_L) and temperature sense, which report the junction temperature (T_J).

The MP86962 is ideal for server applications, where efficiency and small size are at a premium. It is available in a TLGA-41 (5mmx6mm) package.

FEATURES

- Wide 3V to 16V Operating Input Voltage (V_{IN}) Range
- 80A Output Current (I_{OUT})
- Current Sense with Accu-Sense™
- Temperature Sense
- Accepts Tri-State Pulse-Width Modulation (PWM) Signal
- Current-Limit Protection
- Over-Temperature Protection (OTP)
- Fault Reporting
- Available in a TLGA-41 (5mmx6mm) Package

APPLICATIONS

- Server Core Voltages
- Graphics Card Core Regulators
- Power Modules

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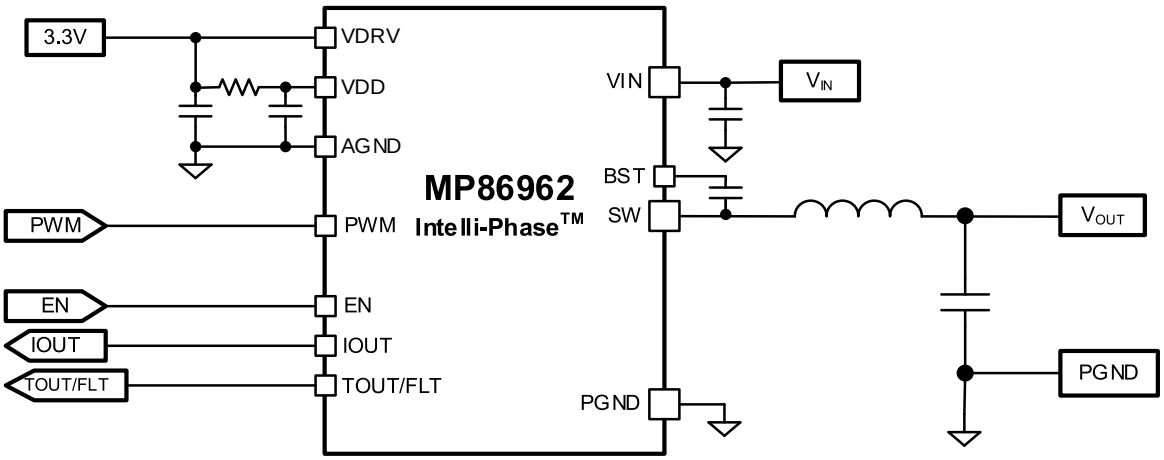
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP86962GMJT	TLGA-41 (5mmx6mm)	*See Below*	3

* For Tape & Reel, add suffix -Z (e.g. MP86962GMJT-Z).

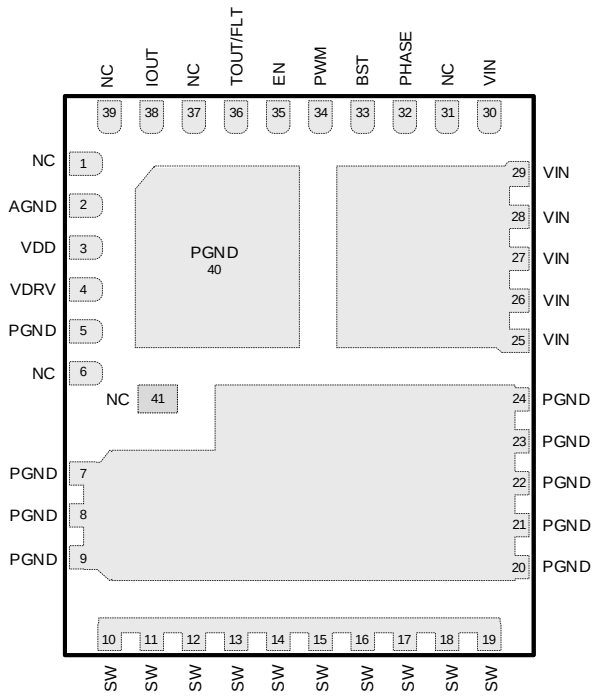
TOP MARKING

MPSYYWW
MP86962
LLLLLLL
T

MPS: MPS prefix
YY: Year code
WW: Week code
MP86962: Part number
LLLLLLL: Lot number
T: Thin

PACKAGE REFERENCE

TOP VIEW



TLGA-41 (5mmx6mm)

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PIN FUNCTIONS

Pin #	Name	Description
1, 6, 31, 37, 39, 41	NC	**No connection.**
2	AGND	**Analog ground.**
3	VDD	**Supply voltage for internal circuitry.** Connect the VDD pin to VDRV via a 2.2Ω resistor. Decouple VDD using a 1µF capacitor connected to AGND. Connect AGND and PGND at the VDD capacitor.
4	VDRV	**Driver voltage.** Connect the VDRV pin to a 3.3V supply. Decouple VDRV using a 1µF to 4.7µF ceramic capacitor.
5, 7, 8, 9, 20, 21, 22, 23, 24, 40	PGND	**Power ground.**
10, 11, 12, 13, 14, 15, 16, 17, 18, 19	SW	**Phase node.**
25, 26, 27, 28, 29, 30	VIN	**Input supply voltage.** Place input ceramic capacitors (C_{IN}) close to the device to support the switching current with minimal parasitic inductance.
32	PHASE	**Switching node for the bootstrap (BST) capacitor connection.** The PHASE pin is connected to SW internally.
33	BST	**Bootstrap.** The BST pin requires a 0.1µF to 0.22µF capacitor to drive the power MOSFET's gate above the input supply voltage (V_{IN}). Connect the capacitor between the PHASE and BST pins to form a floating supply across the power MOSFET driver.
34	PWM	**Pulse-width modulation (PWM) input.** Float the PWM pin or pull PWM to a middle-state voltage to force SW into a high-impedance (Hi-Z) state.
35	EN	**Enable.** Pull the EN pin low to disable the device and put SW in a high-impedance (Hi-Z) state.
36	TOUT/FLT	**Single-pin temperature sense and fault reporting.** The TOUT/FLT pin is pulled up to the VDD voltage (V_{DD}) when a fault occurs.
38	IOUT	**Current-sense output.** Use an external resistor to adjust the voltage proportional to the inductor current (I_L).

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 18V
V_{IN} - V_{PHASE} (DC) ..... -0.3V to +25V
V_{IN} - V_{PHASE} (10ns)..... -5V to +32V
V_{SW} (DC)..... -0.3V to V_{IN} + 0.3V
V_{SW} (25ns) ..... -5V to +25V
V_{BST} ..... V_{SW} + 4V
V_{BST} - V_{PHASE} ..... -0.3V to +4V
V_{DD}, V_{DRV}..... -0.3V to +4V
All other pins..... -0.3V to V_{DD} + 0.3V
Instantaneous current 125A
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings (2)

Human body model (HBM) ..... Class 1C
Charged device model (CDM)..... Class C2B

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 3V to 16V
Driver voltage (V_{DRV}) ..... 3V to 3.6V
Logic voltage (V_{DD})..... 3V to 3.6V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (4) θ_{JB} θ_{JC_TOP}

TLGA-41 (5mmx6mm).....2.7..... 12.4 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Followed ANSI/ESDA/JEDEC JS-001 for HBM and ANSI/ESDA/JEDEC JS-002 for CDM.
3) The device is not guaranteed to function outside of its operating conditions.
4) θ_{JB}: Thermal resistance from the junction to the board around the PGND soldering point.
   θ_{JC_TOP}: Thermal resistance from the junction to the top of the package.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{DRV} = V_{DD} = EN = 3.3V, T_A = 25°C for typical value, T_J = -40°C to +125°C for max and min values, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input current (I_{IN}) shutdown		EN = low		90	180	μA
V_{IN} under-voltage lockout (UVLO) rising threshold				2.5	3	V
V_{IN} UVLO threshold hysteresis				450		mV
VDRV quiescent current	I_{VDRV}	Pulse-width modulation (PWM) = low		250	400	μA
VDD quiescent current	I_{VDD}	PWM = low		3		mA
I_{VDRV} operation current (5)		f_{SW} = 500kHz		19.8		mA
		f_{SW} = 800kHz		31.7		mA
V_{DD} UVLO rising threshold				2.75	2.95	V
V_{DD} UVLO threshold hysteresis				300		mV
High-side (HS) current limit (5)	I_{LIM_FLT}	Cycle-by-cycle up to 8 cycles		110		A
Low-side (LS) current limit (5)		Negative current limit, cycle-by-cycle, no fault report		-35		A
LS negative current limit off time (5)				200		ns
HS current limit shutdown counter (5)				8		times
Dead time (DT) at SW rising (5)				2		ns
DT at SW falling (5)		Positive inductor current (I_L)		6		ns
		Negative I_L		28		ns
EN input high threshold voltage			2.3			V
EN input low threshold voltage					0.8	V
PWM high to SW rising delay (5)	t_{RISING}			20		ns
PWM low to SW falling delay (5)	$t_{FALLING}$			20		ns
PWM tri-state to SW high-impedance (Hi-Z) delay (5)	t_{LT}			40		ns
	t_{TL}			30		ns
	t_{HT}			40		ns
	t_{TH}			30		ns
Minimum PWM pulse width (5)				20		ns
IOUT sense gain accuracy (5)		20A ≤ I_{SW} ≤ 80A, T_J = 25°C	-2	0	+2	%
IOUT sense gain	G_{IOUT}			5		μA/A
IOUT sense offset		I_{SW} = 0A, V_{IOUT} = 1.2V, T_J = 25°C	-2	0	+2	μA
		PWM = Hi-Z, V_{IOUT} = 1.2V	-1	0	+1	μA
IOUT pin voltage range (5)	V_{IOUT}		0.7		2.1	V

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{DRV} = V_{DD} = EN = 3.3V, T_A = 25°C for typical value and T_J = -40°C to +125°C for max and min values, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
TOUT/FLT sense gain (5)				8		mV/°C
TOUT/FLT sense offset (5)		T_J = 25°C		800		mV
Over-temperature (OT) shutdown and fault flag (5)				160		°C
TOUT/FLT when fault occurs (5)			3	3.3		V
PWM resistor		Pull up, EN = high		6		kΩ
		Pull down, EN = high		5		kΩ
PWM logic high voltage			2.3			V
PWM tri-state region			1.1		1.8	V
PWM logic low voltage					0.8	V

Note:

5) Not tested in production.

PWM TIMING DIAGRAM

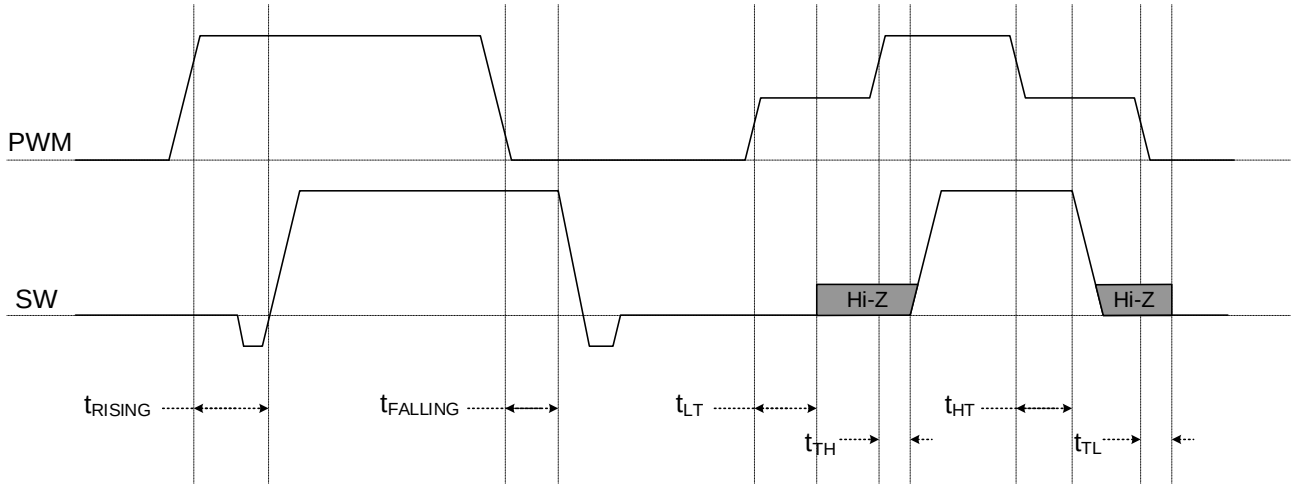

Figure 1: PWM Timing Diagram

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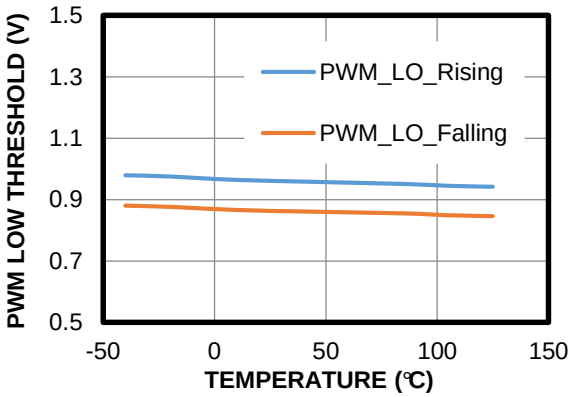
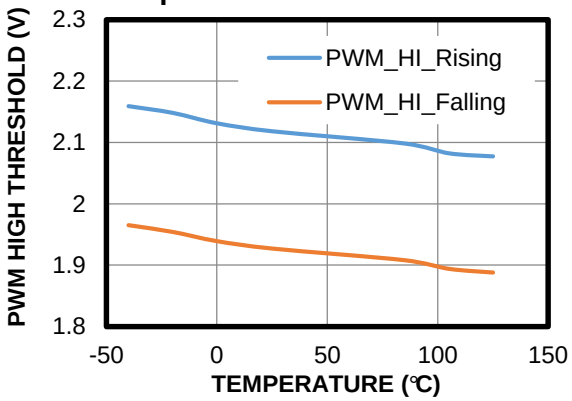
TYPICAL CHARACTERISTICS

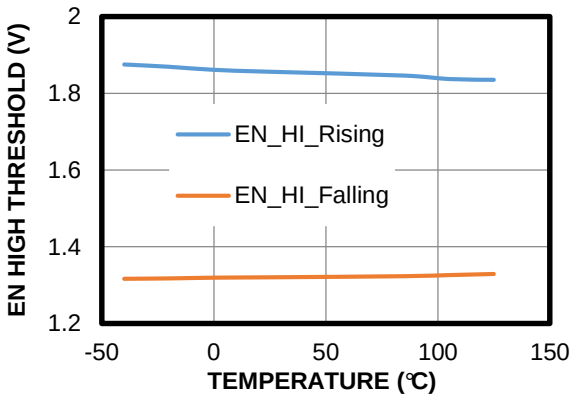
PWM Low Threshold vs. Temperature



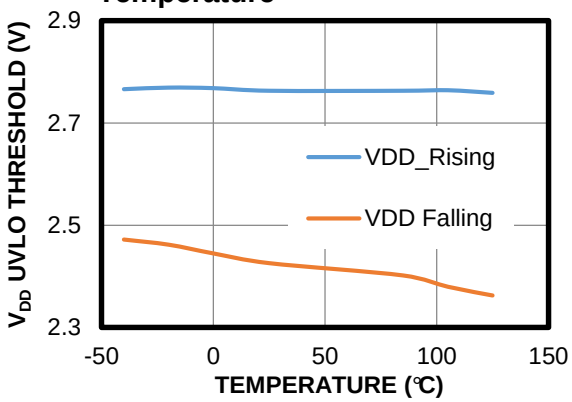
PWM High Threshold vs. Temperature



EN High Threshold vs. Temperature

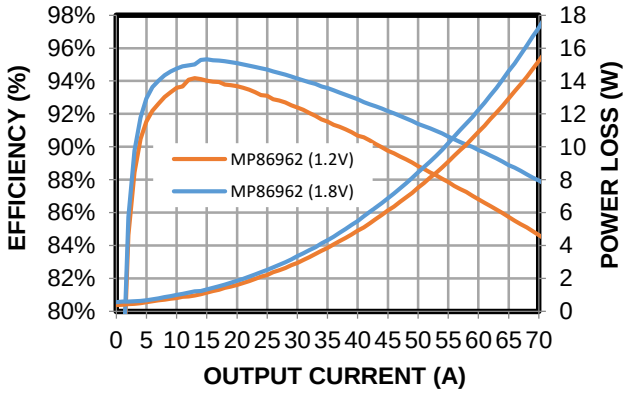


V_{DD} UVLO Threshold vs. Temperature



Efficiency vs. Output Current vs. Power Loss

V_{IN} = 12V, L = 100nH, f_{SW} = 800kHz



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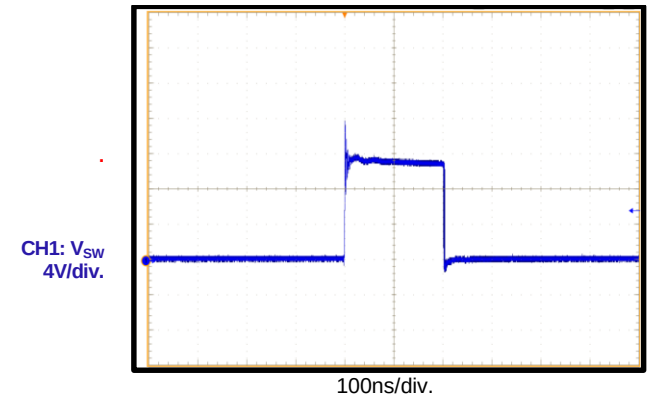
TYPICAL PERFORMANCE CHARACTERISTICS

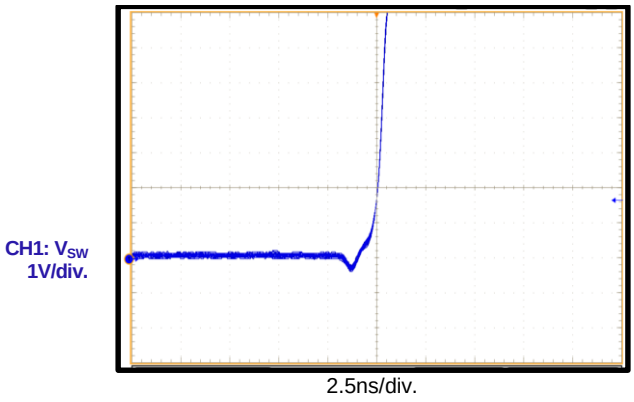
Switching

V_{IN} = 12V, L = 120nH, load = 30A



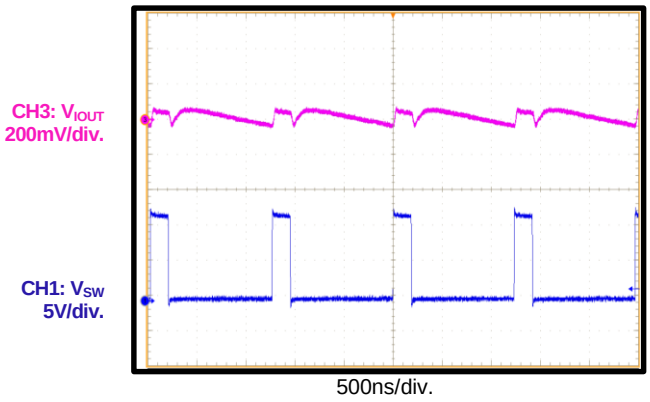
Dead Time at SW Rising

Load = 30A



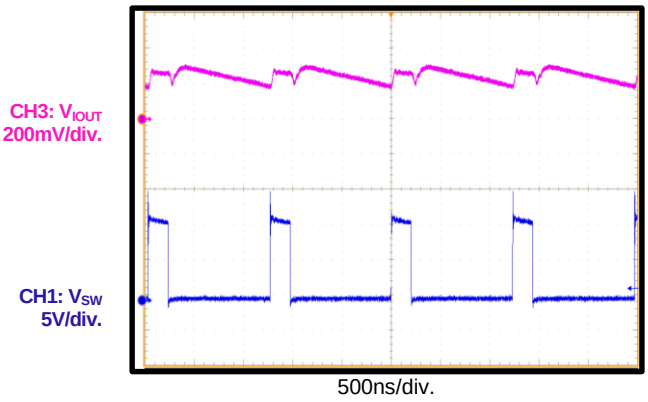
IOUT Output

Load = 0A

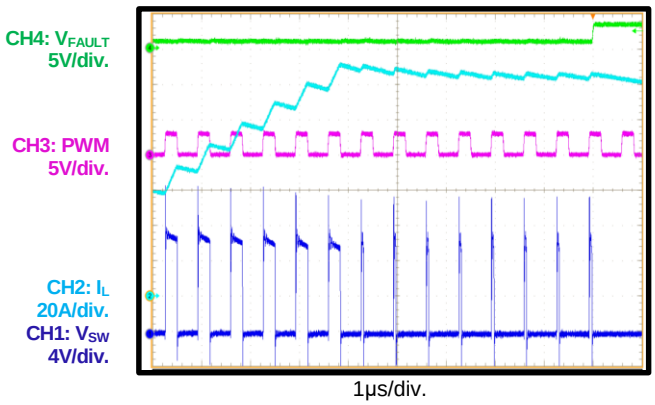


IOUT Output

Load = 30A



HS Current Limit



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FUNCTIONAL BLOCK DIAGRAM

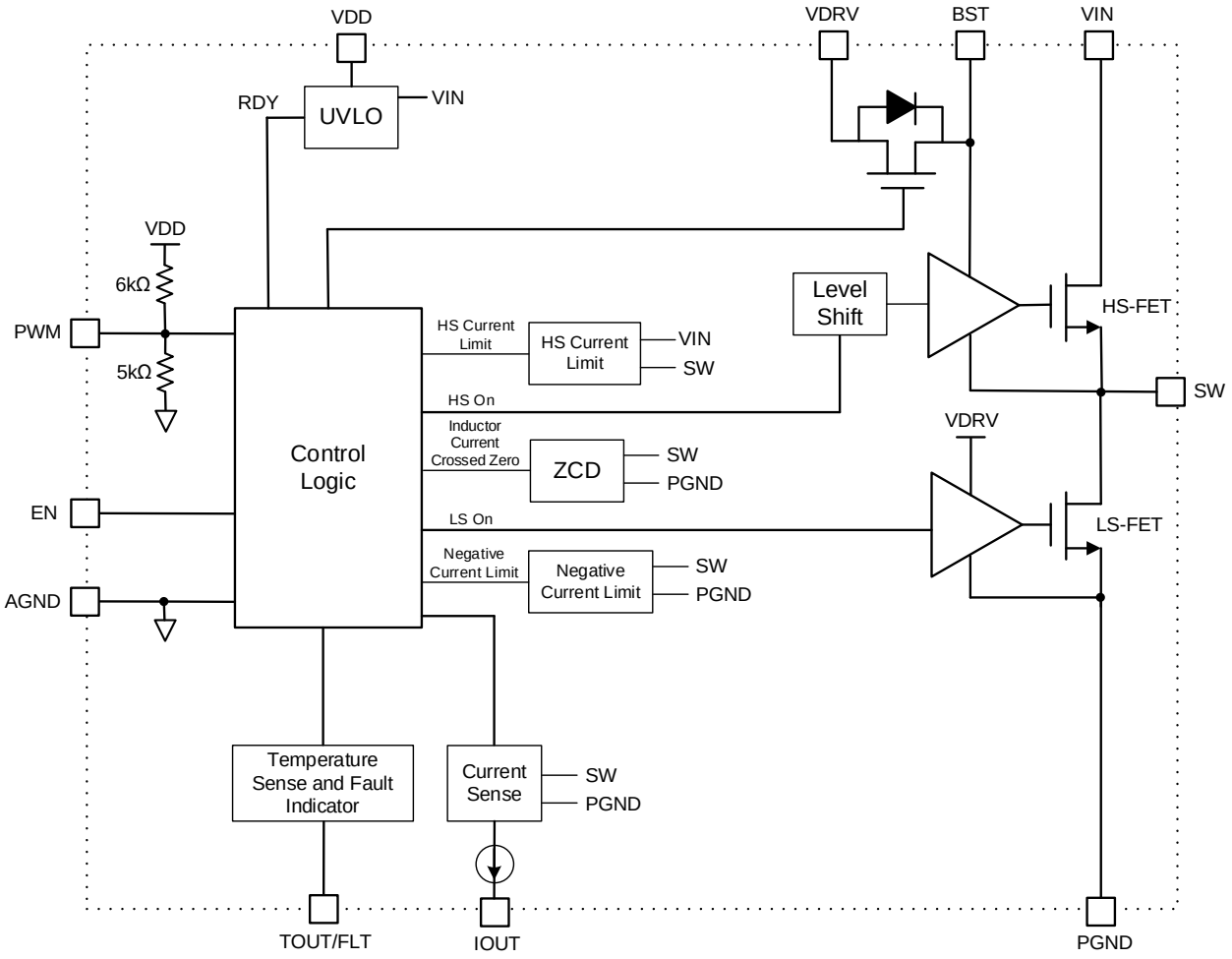

Figure 2: Functional Block Diagram

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OPERATION

The MP86962 is an 80A, monolithic half-bridge driver with internal MOSFETs. It is ideal for multi-phase buck regulators. An external 3.3V power supply is required to supply the VDD and VDRV pins. Once the EN pin transitions from low to high, and the VDRV signals are sufficiently high, the device begins operation.

Pulse-Width Modulation (PWM)

The pulse-width modulation (PWM) pin can operate as a tri-state input. When the PWM input signal is within the tri-state threshold window (t_{HT} or t_{LT}) for 40ns, the high-side MOSFET (HS-FET) immediately turns off and the low-side MOSFET (LS-FET) enters diode emulation mode. The LS-FET remains in diode emulation mode until zero-current detection (ZCD).

The tri-state PWM input can come from a forced middle-voltage PWM signal or by floating the PWM input. The internal current source charges the signal to a middle voltage. The PWM Timing Diagram shows the propagation delay definition from PWM to the SW node (see Figure 1 on page 6).

Diode Emulation Mode

In diode emulation mode, PWM is low or in a tri-state input. If the inductor current (I_L) is positive, the LS-FET turns on. If I_L is negative or after I_L crosses the ZCD threshold, the LS-FET turns off. Diode emulation mode can be enabled by driving PWM to a middle state or floating PWM.

Current Sense (CS)

When EN is pulled high, IOUT is a bidirectional current-source pin proportional to I_L. The current-sense (CS) gain is 5μA/A. If necessary, use a resistor to configure the voltage gain proportional to I_L.

The IOUT pin's output has two states (see Table 1). When disabled (EN = low), the CS circuit is disabled, and IOUT is in a high-impedance (Hi-Z) state.

Table 1: IOUT Output States

PWM	EN	IOUT
PWM	High	Active
x	Low	Hi-Z

A 0.7V and 2.1V IOUT voltage (V_{IOUT}) is required to achieve an accurate DrMOS CS pin output current (I_{IOUT}) of up to +400μA/-200μA (e.g. +80A/-40A). A resistor (R_{IOUT}) is typically connected from IOUT to an external voltage that is capable of sinking small currents in order to provide sufficient voltage to meet the required operating voltage range.

The reference voltage (V_{CM}) connected to R_{IOUT} can be calculated with Equation (1):

$$0.7V < I_{IOUT} \times R_{IOUT} + V_{CM} < 2.1V \quad (1)$$

I_{IOUT} can be estimated with Equation (2):

$$I_{IOUT} = I_{SW} \times G_{IOUT} \quad (2)$$

The Intelli-Phase™ CS output is used by the controller to accurately monitor the buck convert's output current (I_{OUT}). The cycle-by-cycle current information from IOUT can be used for phase-current balancing, over-current protection (OCP), and active voltage positioning (output voltage droop).

Positive and Negative Inductor Current Limits

If an HS-FET over-current (OC) condition is detected, then the HS-FET turns off for the PWM cycle. If an HS-FET OC condition remains for eight consecutive cycles, then the HS-FET latches off, the TOUT/FLT pin pulls high to VDD, and the LS-FET turns on until ZCD. Toggle EN or recycle the power on VIN or VDD to release the latch and restart the device.

If the LS-FET detects a -35A valley current, then the LS-FET turns off and the HS-FET turns on for 200ns to limit the negative current. The LS-FET negative current limit does not trigger a fault report.

Temperature Sense Output with Fault Indicator (TOUT/FLT)

The TOUT/FLT pin has two functions: junction temperature (T_J) sense and fault detection.

TOUT/FLT has an output voltage proportional to T_J whenever V_{DD} exceeds its under-voltage lockout (UVLO) threshold and the part is active.

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The gain is 8mV/°C, with an 800mV offset at 25°C. For example, the TOUT/FLT voltage is 0.8V at T_J = 25°C, and 1.6V at T_J = 125°C.

If a fault occurs, TOUT/FLT is pulled to V_{DD} to report the fault event, regardless of the temperature. If the fault event lasts for longer than 200ns, the PWM impedance changes accordingly to indicate the fault type. Table 2 shows the PWM status by the fault type.

Table 2: PWM Resistance by Fault Type

Fault Type	PWM
HS-FET current limit protection	10kΩ to AGND
Over-temperature protection (OTP)	20kΩ to AGND
SW to PGND short protection	1kΩ to VDD

TOUT/FLT monitors three different fault events:

1. HS-FET OC limit: Eight consecutive current limit faults trigger an OC fault. If this fault occurs, the MP86962 latches off to turn off the HS-FET. The LS-FET turns off when I_L reaches 0A. PWM uses a 10kΩ resistor connected to AGND to indicate the fault type.
2. Over-temperature (OT) fault: If T_J > 160°C, an OT fault occurs, and the MP86962 latches off to turn off the HS-FET. The LS-FET turns off once I_L reaches 0A. PWM uses a 20kΩ resistor connected to AGND to indicate the fault type.
3. SW to PGND short: If this fault occurs, the MP86962 latches off to turn off the HS-FET. PWM is pulled high (1kΩ to VDD) to indicate the fault type.

Release the fault latch by toggling EN, or by recycling the power on VIN or VDD.

For multi-phase operation, connect the TOUT/FLT pin of each Intelli-Phase™ together (see Figure 3).

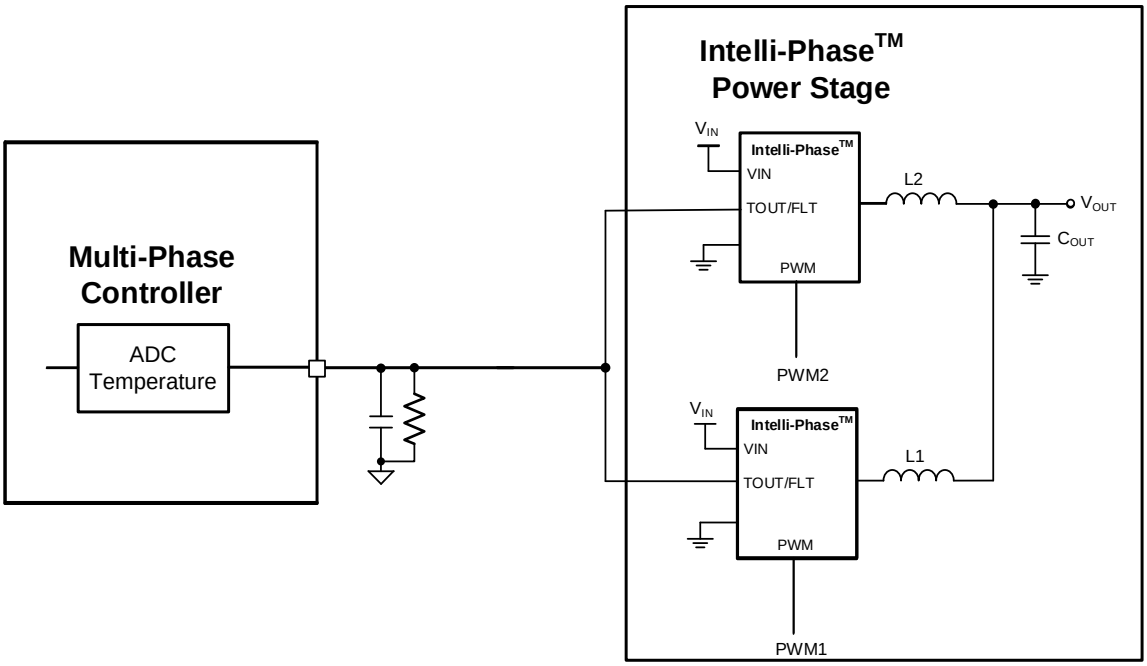

Figure 3: Multi-Phase Temperature Sense Set-Up

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APPLICATION INFORMATION

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 4 and follow the guidelines below:

1. Place the MLCC input capacitors as close to VIN and PGND as possible.
2. Place the major MLCC capacitors on the same layer as the MP86962.
3. Place as many VIN and PGND vias underneath the package as possible.
4. Place the vias between the VIN or PGND long pads.
5. Place a VIN copper plane on the second inner layer to form the positive/negative/positive PCB stack, which reduces the parasitic impedance from the MLCC input capacitor to the MP86962.
6. Ensure that the copper plane on the inner layer covers the VIN vias underneath the package and MLCC input capacitors.
7. Place more PGND vias close to the PGND pin/pad to minimize the parasitic resistance and impedance, as well as the thermal resistance.
8. Place the BST capacitor (C_{BST}) and VDRV capacitor (C_{VDRV}) as close to the MP86962's pins as possible.
9. Use a trace width that is at least 20mils to route the BST and VDRV paths.
10. Avoid placing vias on the BST driving path.
11. Use a 0.1µF to 0.22µF C_{BST}.
12. Place the VDD decoupling capacitor close to the device.
13. Connect AGND and PGND at the VDD capacitor's ground connection.
14. Keep the IOUT signal trace away from high-current paths, such as SW and PWM.

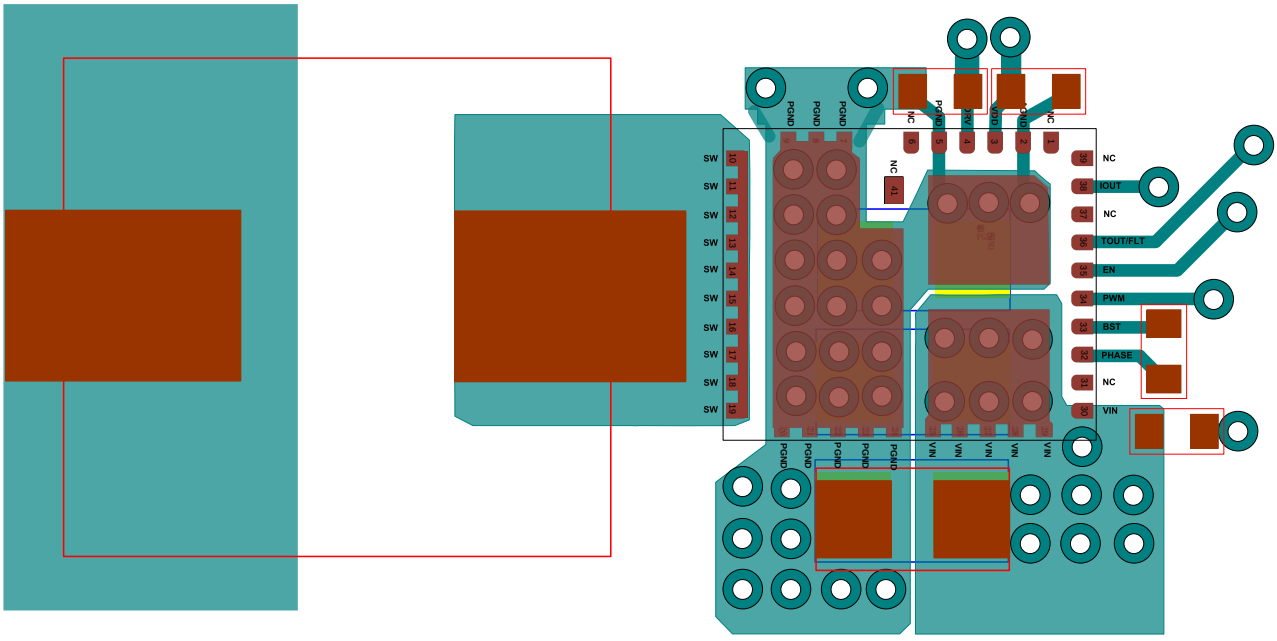

Figure 4: Recommended PCB Layout (Placement and Top Layer PCB)

Input Capacitor: 0805 Package (Top Side and Bottom Sides) and 0402 Package (Top Side)

Inductor: 11mmx8mm Package

VDD/BST/VDRV Capacitor: 0402 Package

Via Size: 20mils/10mils

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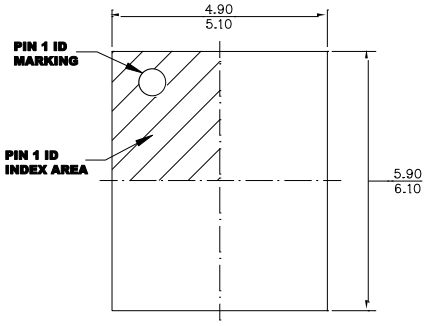
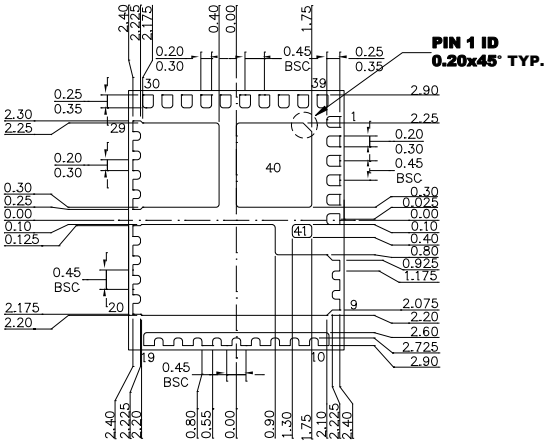
PACKAGE INFORMATION

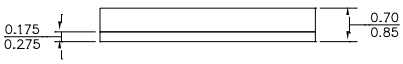
TLGA-41 (5mmx6mm)



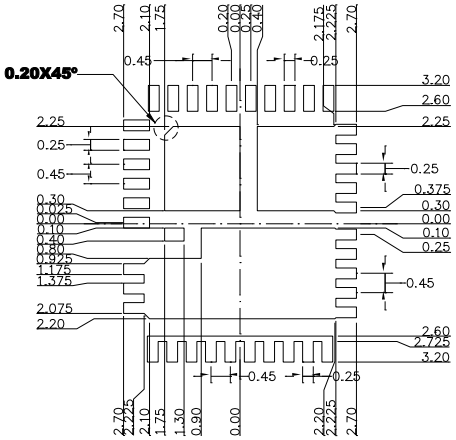
TOP VIEW



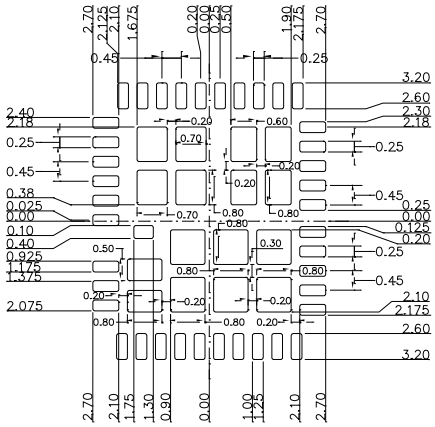
BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN



RECOMMENDED STENCIL DESIGN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-303.
4) DRAWING IS NOT TO SCALE.

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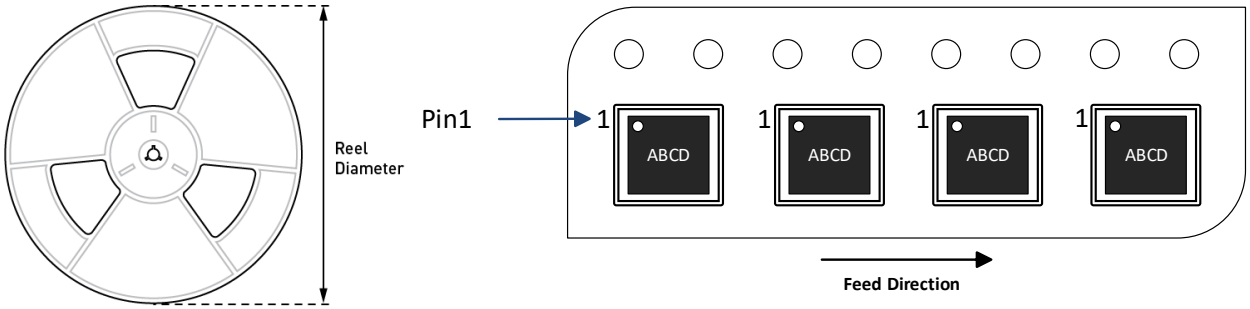
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP86962GMJT-Z	TLGA-41 (5mmx6mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	8/24/2022	Initial Release	-

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