MP86934

16V Intelli-Phase Solution in TQFN 3x4

The Future of Analog IC Technology

DESCRIPTION

The MP86934 is a monolithic half-bridge with built-in internal power MOSFETs and gate drivers. It achieves 25A of continuous output current over a wide input supply range.

Integration of the driver and MOSFETS results in high efficiency due to optimal dead time and parasitic inductance reduction.

This very small 3mm x 4mm FC-TQFN device can operate from 100kHz to 2MHz.

This device works with tri-state output controllers. It also comes with a general-purpose current sense and temperature sense.

The MP86934 is ideal for Server and Telecom applications where efficiency and small size are a premium.

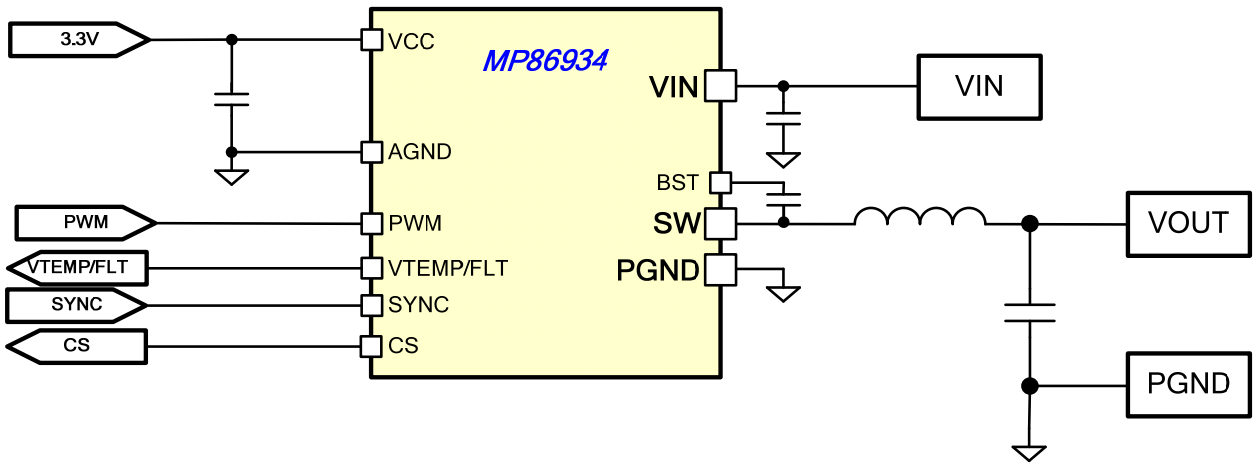
FEATURES

- Wide 4.5V to 16V Operating Input Range
- Compliant to Intel DrMOS V4.0 Spec.
- 25A Output Current
- Accepts Tri-State PWM Signal
- Built-In Switch for bootstrap
- Current Sense
- Temperature Sense
- Current Limit Protection
- Over Temperature Protection
- Fault Reporting: OC and OT
- Used for Multi-Phase Operation
- Available in TQFN-21 (3mmx4mm) Package

APPLICATIONS

- Server and Telecom Voltage Regulators
- Graphic Card Core Regulators
- Power Modules

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP86934GLT	TQFN-21 (3mmx4mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP86934GLT–Z).

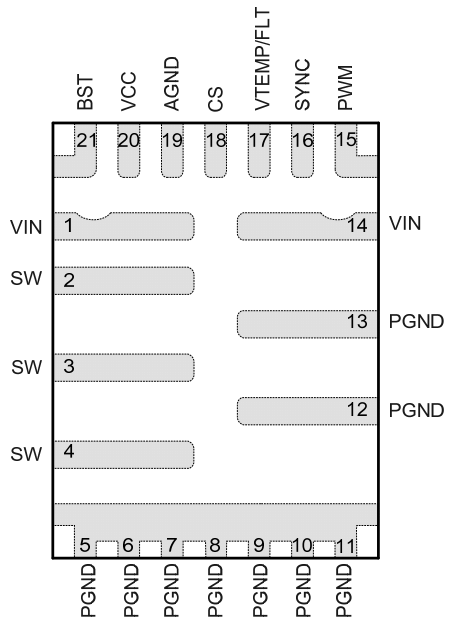
TOP MARKING

MPYW
8693
4LLL

MP: MPS prefix;
Y: year code;
W: week code:
86934: product code of MP86934GLT;
LLL: lot number;

PACKAGE REFERENCE

TOP VIEW



FC-TQFN (3x4mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} 18V
$V_{SW\ (DC)}$ ..... -0.3V to to V_{IN}+0.3V
$V_{SW\ (25ns)}$ ..... -3V to 25V
V_{IN} - $V_{SW\ (10ns)}$ ..... -5V to 32V
V_{BST} - $V_{SW\ (25ns)}$ 5V
V_{BST} ..... V_{SW} + 4V
All Other Pins ..... -0.3V to +4V
Instantaneous Current 45A
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... -65°C to +150°C

Recommended Operating Conditions (2)

Supply Voltage V_{IN} ..... 4.5V to 16V
Driver Voltage V_{CC} ..... 3.0V to 3.6V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (3) θ_{JB} θ_{JC_TOP}

TQFN-21 (3mmx4mm)	2.2	24.3	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) θ_{JB} is the thermal resistance from the junction to board around the PGND soldering point.
   θ_{JC_TOP} is the themal resistance from the junction to the top of the package.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{CC} =SYNC= 3.3V, T_A = 25°C for Typical value and T_J = -40°C to 125°C for Max and Min values, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{IN} Under Voltage Lockout Threshold Rising				4.1	4.5	V
V_{IN} Under Voltage Lockout Threshold Hysteresis				380		mV
V_{IN} Quiescent Current in Standby Mode	$I_{IN\ Stby}$	PWM=Hi-Z, SYNC=Hi-Z, V_{IN}=4.5V to 22V			1	μA
V_{CC} Quiescent Current in active mode	$I_{CC\ Quiescent}$	PWM=Low, No switching, SYNC=Hi or Low			3	mA
V_{CC} Quiescent Current in Standby Mode	$I_{CC\ Stby}$	SYNC=Hi-Z			30	μA
VCC Voltage UVLO Rising			2.5	2.7	2.9	V
VCC Voltage UVLO Hysteresis				200		mV
High Side Current Limit	I_{LIM_FLT}			60		A
High Side Current Limit Shutdown Counter(4)				4		Times
Low Side Current Limit(4)				-15		A
Low-Side OFF time in negative current limit(4)				40		ns
Dead-Time Rising(4)				3		ns
Dead-Time Falling(4)		Positive inductor current		8		ns
		Negative inductor current		40		ns
SYNC Logic High Voltage			2.40			V
SYNC Tristate Region			1.3		1.7	V
SYNC Logic Low Voltage					0.70	V
PWM High to SW Rising Delay(4)	t_{Rising}			20		ns
PWM Low to SW Falling Delay(4)	$t_{Falling}$			20		ns
PWM Tristate to SW Hi-Z Delay(4)	t_{Lo-HiZ}			50		ns
	t_{HiZ-Lo}			50		ns
	t_{HiZ-Hi}			50		ns
Minimum SW Pulse Width(4)				30		ns
Current Sense Gain Accuracy		5A ≤ I_{SW} ≤ 30A	-3	0	+3	%
Current Sense Gain				10		μA/A
Current Sense Offset		I_{OUT}= 0A	-6	0	6	μA
		SW Hi-Z	-2	0	2	μA
Current Sense Common Mode Voltage Range	V_{CS_COM}		0.8		2	V
Temperature Sense Gain(4)				10		mV/°C
Temperature Sense Offset(4)				-100		mV
Temperature Sense voltage range(4)		T=150C		1.4		V
		T=100C		0.90		V
		T=25C		0.15		V

ELECTRICAL CHARACTERISTICS

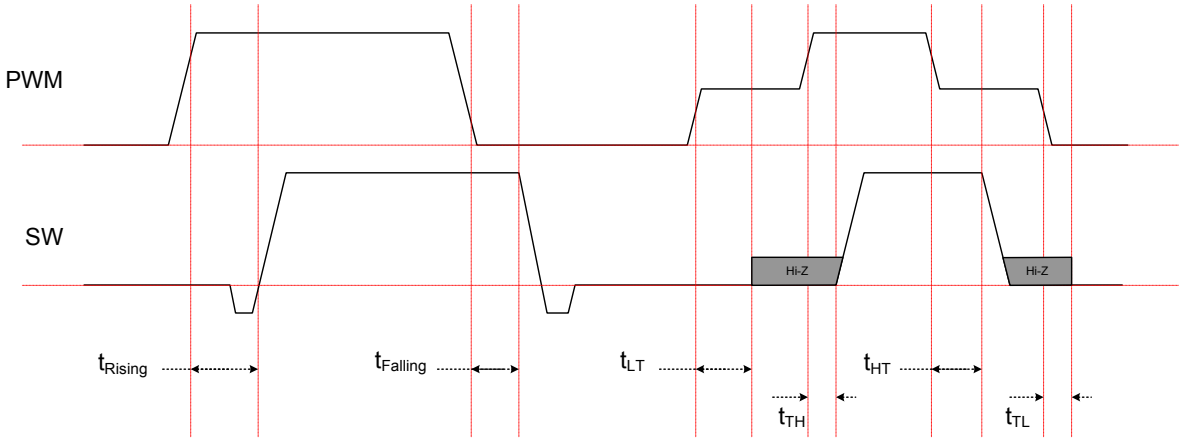
V_{IN} = 12V, V_{CC} =SYNC= 3.3V, T_A = 25°C for Typical value and T_J = -40°C to 125°C for Max and Min values, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Over Temperature Shutdown(4)				160		°C
OTP threshold hysteresis(4)				20		°C
VTEMP when Fault			3.0	3.3		V
PWM Resistor		Pull up, SYNC= Low or High		6		kΩ
		Pull down		5		kΩ
PWM Logic High Voltage			2.4			V
PWM Tristate Region			1.1		1.9	V
PWM Logic Low Voltage					0.70	V

NOTE:

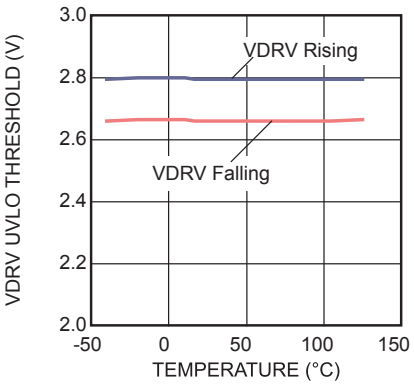
4) Guaranteed by design, not tested in production. The parameter is tested during parameters characterization.

PWM TIMING CHART

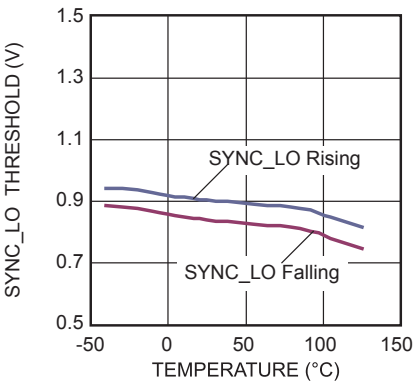


TYPICAL PERFORMANCE CHARACTERISTICS

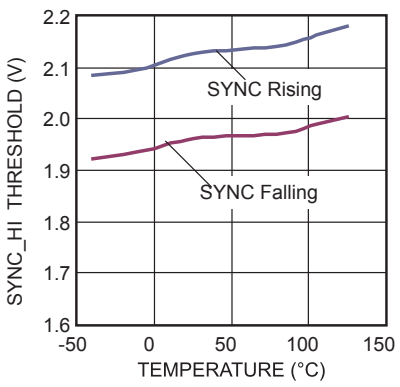
VCC UVLO



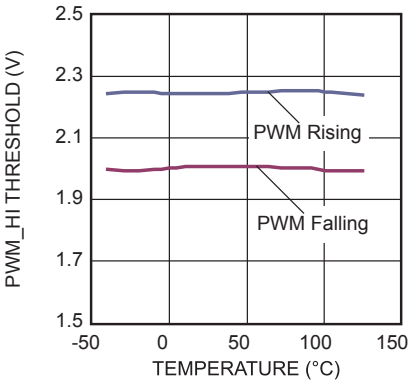
SYNC_LO



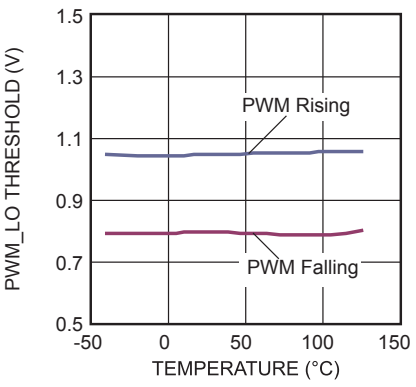
Sync_Hi



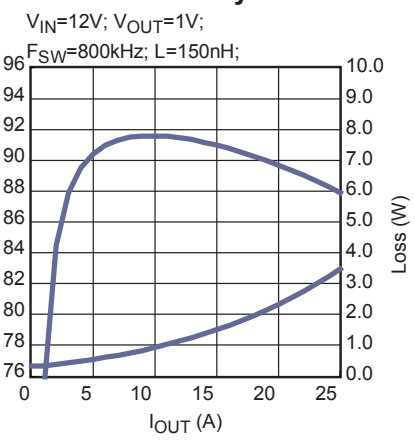
PWM Hi



PWM-Lo

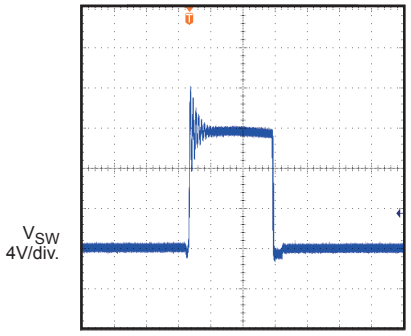


Device Efficiency/loss

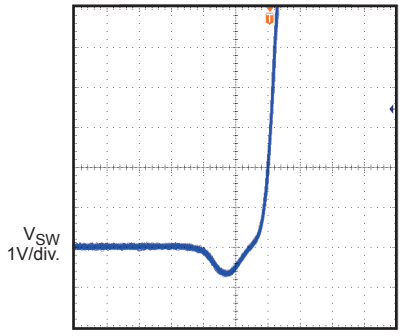


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

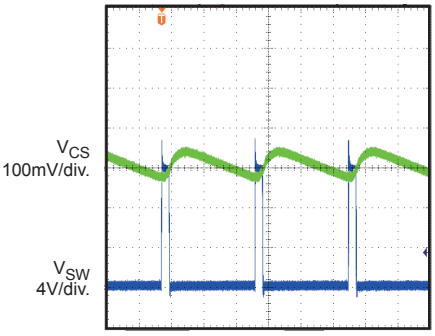
Switching Waveform
V_{IN}=12V; L=150nH; I_{OUT}=15A



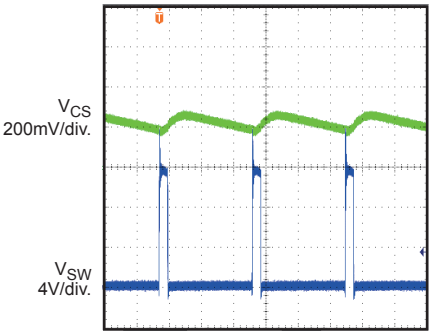
Dead Time @ SW Rising
I_{OUT}=15A



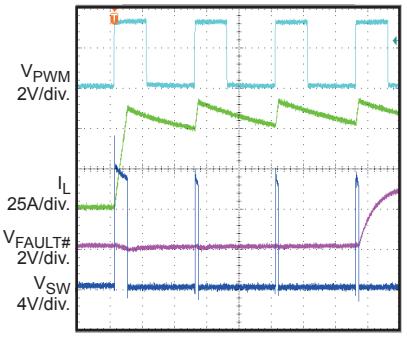
CS Output Waveform
I_{OUT}=0A



CS Output Waveform
I_{OUT}=15A



HS Current Limit



PIN FUNCTIONS

Pin #	Name	Description
1,14	VIN	Supply Voltage. Place C_{IN} close to the device to support the switching current reducing the voltage spikes at the input.
2,3,4	SW	Switch Output.
5-13	PGND	Power Ground. Place multiple Vias to inner solid ground layers to minimize the parasitic impedance and thermal resistance.
15	PWM	Pulse Width Modulation input. Leave PWM floating or drive to mid-state to enable the diode emulation mode.
16	SYNC	Diode emulation mode and standby mode selection. Leave it floating or drive to middle-state to enter standby mode. Pull pin high for normal operation. Pull pin low to enable the diode emulation mode.
17	VTEMP/FLT	Single pin temperature sense and fault reporting.
18	CS	Current Sense Output.
19	AGND	Analog Ground. Connect it to PGND plane at the VCC decoupling capacitor.
20	VCC	3.3V supply input for internal circuitry and gate drive, decouple with 1μF (or higher) ceramic capacitor to AGND.
21	BST	Bootstrap. Requires a 0.1μF to 1μF capacitor to drive the power switch's gate above the supply voltage. Connects the capacitor between SW and BST pins to form a floating supply across the power switch driver.

BLOCK DIAGRAM

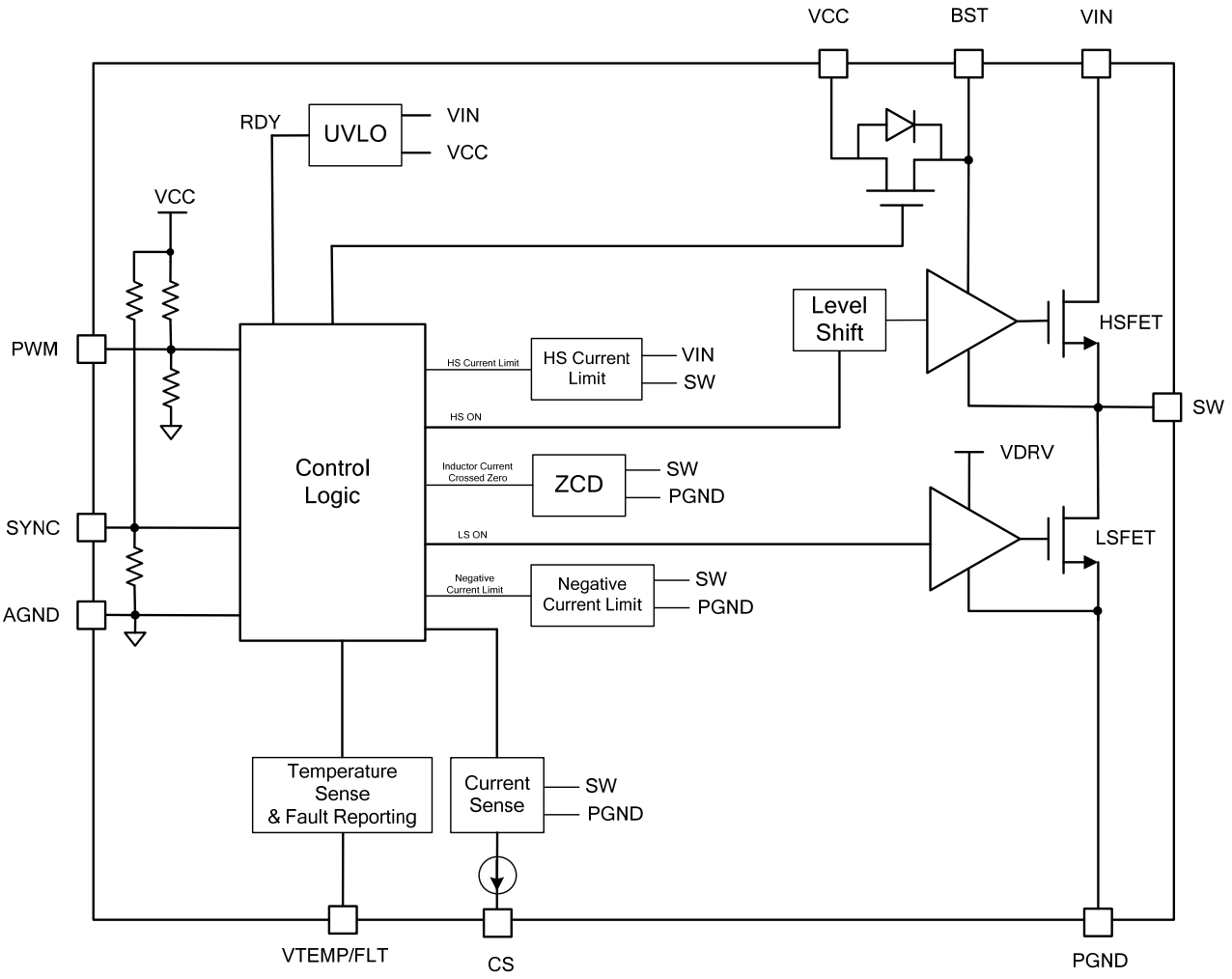


Figure 1: Functional Block Diagram

OPERATION

The MP86934 is a 25A monolithic half-bridge driver with MOSFETs ideally suited for multi-phase buck regulators.

When V_{IN}, V_{CC} and V_{BST} signals are sufficiently high, operation begins.

PWM

PWM input pin is capable to Tri-state input. When the PWM input signal is within the tri-state threshold window for 50ns (typical), T_{HT} or T_{LT}, the HSFET will be turned OFF immediately and the LSFET will be in diode emulation mode which is ON until zero current detection. The tri-state PWM input can be from a forced middle voltage PWM signal or made by floating PWM input and the internal current source will charge the signal to a middle voltage. Please refer to the PWM timing diagram for the propagation delay definition from PWM to SW node.

Standby Mode

When SYNC pin is floating or forced to middle state voltage for 2us, MP86934 will enter to standby mode. During standby mode, the part shuts down and both CS and VTEMP/FLT outputs are disabled. The fault latch will not be reset by entering standby mode.

Diode Emulation mode

In diode emulation mode, when PWM is either low or Tri-state input, the LSFET will be turned ON whenever the inductor current is positive. LSFET is off if the inductor current crossed zero current. Diode emulation mode can be enabled by:

1) Pull SYNC pin low
2) Drive PWM to middle state
3) Floating PWM pin.

Positive and Negative Inductor Current limit

When HSFET over current is detected for 4 consecutive cycles, HSFET will latch off, VTEMP/FLT will be pull to 3.3V, LSFET will turn on until zero current detection and then LSFET will be turned off. Recycling V_{IN}/VCC or toggling EN will release the latch and restart the device.

When LSFET detects a -15A current, the part will turn off LSFET for 40ns to limit the negative current. LSFET's negative current limit will not trigger fault report.

Over Temperature Protection

When the junction temperature reaches the Over Temperature Threshold, the HSFET will be latched OFF, VTEMP/FLT will be 3.3V, LSFET will turn on until zero current detection and then LSFET will turn off.

Temperature Sense Output with Fault indicator, VTEMP/FLT

VTEMP/FLT is a pin with dual functions.

1) Junction Temperature Sense: VTEMP/FLT is a voltage output proportional to junction temperature whenever the VCC is higher than its UVLO and in part is in active mode. The gain is 10mV/°C and it has -100mV offset at 25°C. i.e. 0V@T_J<10°C, 0.15V@T_J=25°C and 0.9V@T_J=100°C.
2) Fault function: When any fault occurred, the VTEMP/FLT will be pulled to 3.3V_typ (3.0V_min) regardless the temperature to report the fault event. It monitors three fault events;

   (a) Over Current limit: A consecutive 4 times current limit fault. Once fault, the part will latch OFF to turn OFF HSFET. The LSFET will be turned OFF when the inductor current reaches zero.

   (b) Over Temperature fault at TJ>160°C. Once fault, the part will latch OFF to turn OFF HSFET. The LSFET will be turned OFF when the inductor current reaches zero.

   (c) SW to PGND shorted. Once fault, the part will latch OFF to turn OFF HSFET.

   The fault latch will not be reset by entering standby mode. The release of fault latch can be done by either re-cycle VIN or VCC.

Current Sense Output, CS

CS is a bi-directional current source proportional to the inductor current. The current sensing gain is 10μA/A and a resistor is used to program the voltage gain proportional to the inductor current if needed.

The CS output has two states as shown in Table 1. In Standby mode, the CS circuit is disabled, it needs 20us to wake up to enter to Active mode if needed.

Table.1 CS Output States

PWM	SYNC	CS
PWM	Hi	Active
PWM	Hi	Active
PWM	Low	Active
x	Hi-Z (or Middle)	Standby

The CS voltage range of 0.8V to 2.0V is required for to get accurate CS's current output up to +500μA/-200μA (i.e. +50A/-25A). In general, there is a resistor, R_{CS}, connected from CS pin to an external voltage which is capable to sink small current to provide enough voltage level to meet the required operating voltage range.

Fig.2 shows the typical circuit diagram of CS pin connection for getting a differential voltage source reflected to inductor current.

Eq. 1 shows the guideline for design R_{CS} resistance to avoid the V(CS) voltage outs of operating range.

$$0.8V < I_{CS} \times R_{CS} + V_{CM} < 2.0V \quad \text{(Eq.1)}$$

$$I_{CS} = I_L \times G_{CS}$$

Where V_{CM} is the reference voltage connected to R_{CS}.

The V_{CM} can be from a voltage divider from 3.3V (i.e. V_{CC}) shown in Fig.3.

Choose R_{CS} >> (R_1//R_2) to minimize the V_{CM} voltage variation over I_{CS} current.

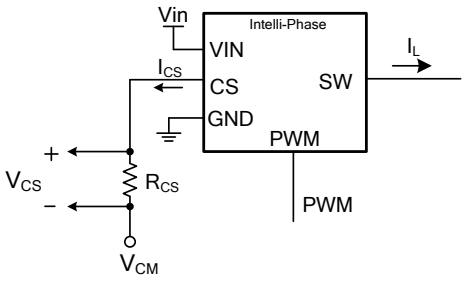


Fig.2 Typical Circuit Diagram for CS pin connection

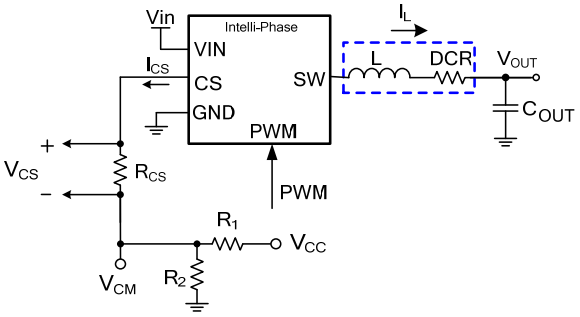


Fig.3 Use VCC to generate VCM voltage for CS signal

APPLICATION INFORMATION

PCB Layout Guidelines

PCB layout plays an important role to achieve stable operation. For optimal performance, follow these guidelines.

1. Place the input MLCC capacitors as close to the VIN and PGND pins as possible. The major MLCC capacitors should be placed on the same layer as MP86934. Maximize the VIN and PGND copper plane to minimize the parasitic impedance.
2. Place PGND Vias as many as possible and close to the pin to minimize both parasitic impedance and thermal resistance.
3. Place VCC decoupling capacitor close to the device. Connect AGND and PGND at the point of VCC capacitor's ground connection.
4. Place BST capacitor as close to the BST and SW pins as possible. Use trace width of 20 mils or higher to route the path. It is recommended to use 0.1μF to 1μF bootstrap capacitor.
5. Keep the CS signal trace away from high current path like SW and PWM.

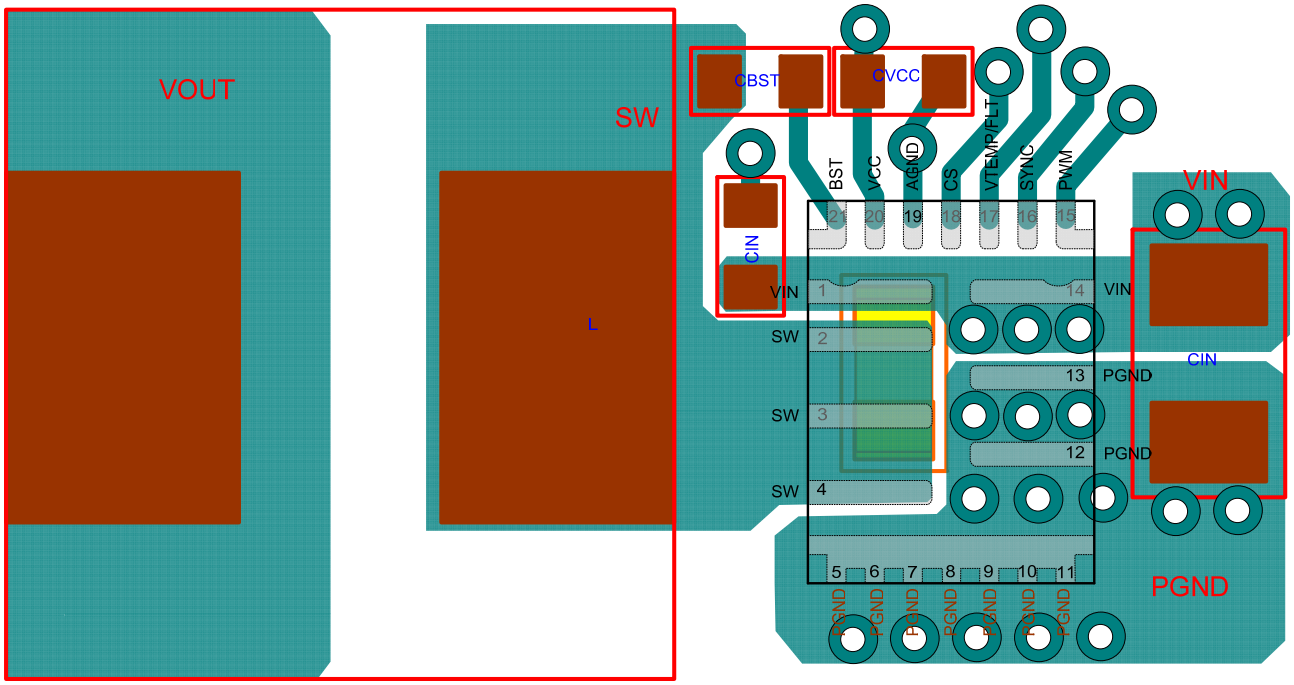
EXAMPLE OF PCB LAYOUT (PLACEMENT & TOP LAYER PCB).

Input Capacitor: 0805 & 0402 package (top side) & 0603 package (bottom side)

Inductor: 6.5 x 6.5 (mm)

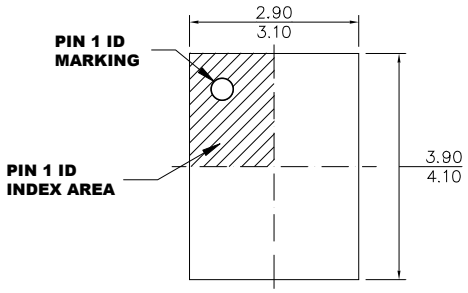
VCC/BST capacitor: 0402 package

Via size: 20/10 mils

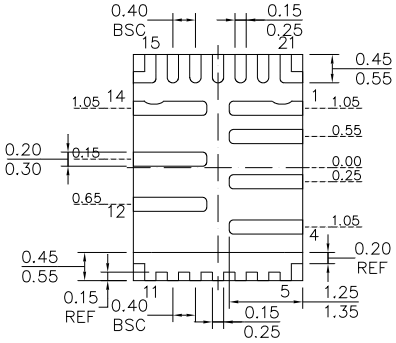


PACKAGE INFORMATION

TQFN-21 (3mmx4mm)

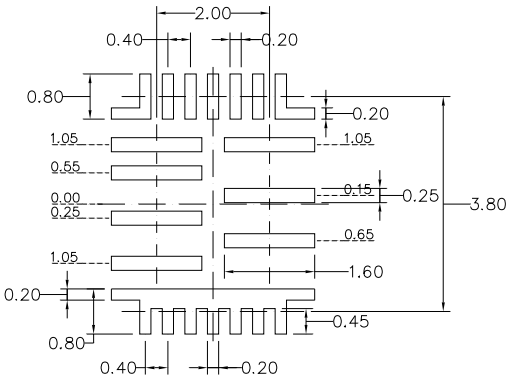


TOP VIEW



BOTTOM VIEW

SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
r1.1	5/19/2020	Correct/add the “Vin-Vsw (10ns) …… -5V to 32V” on absMax rating.	Page 3
r1.2	5/26/2021	Update the thermal impedance.	Page 3