MP86885

Intelli-Phase Solution (Integrated HS/LS FETs and Driver) in 4x6mm TQFN

NOT RECOMMENDED FOR NEW DESIGNS. REFER TO MP86905

DESCRIPTION

The MP86885 is a monolithic half-bridge with built-in internal power MOSFETs and gate drivers. It achieves 40A of continuous output current over a wide input supply range.

Integration of the driver and MOSFETS results in high efficiency due to optimal dead time control and parasitic inductance reduction.

The MP86885 is a Monolithic IC approach to drive up to 40A per phase. This very small 4mm x 6mm FC-TQFN device can operate from 100kHz to 1MHz.

This device works with tri-state output controllers. It also comes with a general-purpose current sense and temperature sense.

The MP86885 is ideal for server applications where efficiency and small size are a premium.

FEATURES

- Wide 4.5V to 14V Operating Input Range
- Simple Logic Interface
- 40A Output Current
- Accepts Tri-State PWM Signal
- Built-In Switch for bootstrap
- Current Sense
- Temperature Sense (10mV/^{o}C)
- Current Limit Protection
- Used for Multi-Phase Operation
- Fault Reporting
- Available in 4mm x 6mm FC-TQFN Package
- RoHS 6 Compliant

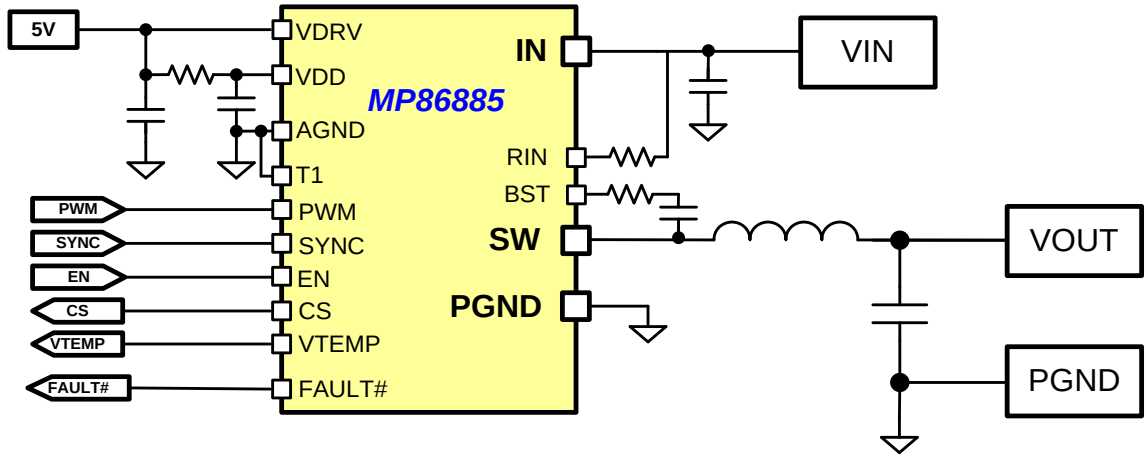
APPLICATIONS

- Server/Workstation/Desktop Core Voltage
- Graphic Card Core Regulators
- Power Modules

All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Quality Assurance. “MPS” and “The Future of Analog IC Technology” are Registered Trademarks of Monolithic Power Systems, Inc.

Intelli-Phase is Trademark of Monolithic Power Systems, Inc.

TYPICAL APPLICATION



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

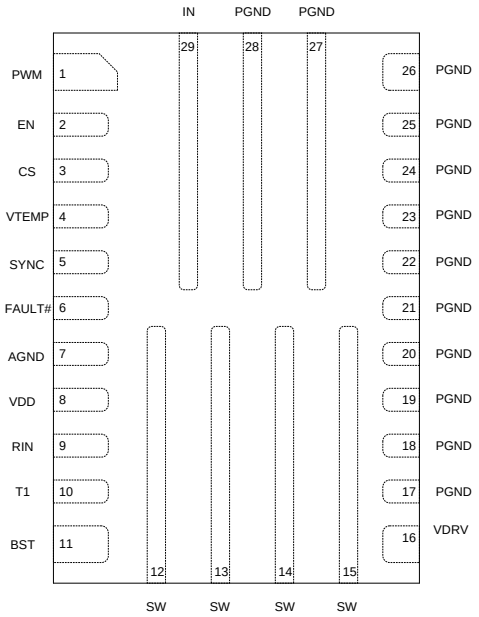
NOT RECOMMENDED FOR NEW DESIGNS. REFER TO MP86905

ORDERING INFORMATION

Part Number*	Package	Top Marking
MP86885GQWT	FC-TQFN-29 4x6(mm)	M86885

* For Tape & Reel, add suffix –Z (e.g. MP86885GQWT–Z).

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} 16V
$V_{SW\ (DC)}$ ..... -1 V to 16V
$V_{SW\ (25ns)}$ ..... -3V to 23V
V_{BST} ..... V_{SW} + 6V
All Other Pins ..... -0.3V to +6V
Instantaneous Current 65A
Continuous Power Dissipation (T_A =+25°C)(2) ..... 3.5 W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 4.5V to 14V
Driver Voltage V_{DRV} ..... 4.5V to 5.5V
Logic Voltage V_{DD} ..... 4.5V to 5.5V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

4x6mm FC-TQFN ..... 36 ..... 8 .... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{DRV}=V_{DD}=5V, T_A = 25°C, unless otherwise noted.

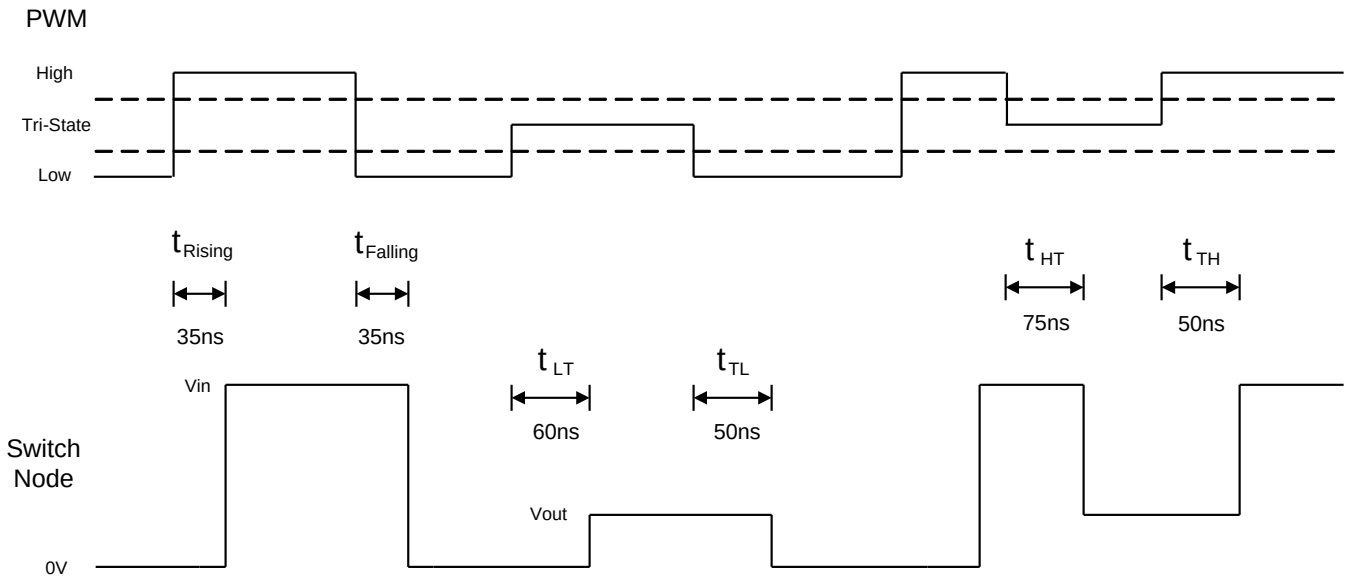
Parameters	Symbol	Condition	Min	Typ	Max	Units
I_{IN} Shutdown	$I_{IN\ Off}$	V_{DRV}=V_{DD}=0V	25	65	100	μA
I_{IN} Standby	$I_{IN\ Standby}$	V_{DRV}=V_{DD}=5V, PWM=EN=Low	30	55	60	μA
V_{IN} Under Voltage Lockout Threshold Rising			3.4	4	4.5	V
V_{IN} Under Voltage Lockout Threshold Hysteresis				340		mV
I_{DRV} Quiescent Current	$I_{DRV\ Quiescent}$	PWM=Low		1		mA
I_{DRV} Shutdown Current	$I_{DRV\ Shutdown}$		200	230	260	μA
I_{DD} Quiescent Current	$I_{DD\ Quiescent}$	PWM=Low	1.5	2.3	3	mA
I_{DD} Shutdown Current	$I_{DD\ Shutdown}$		30	46	60	μA
VDD Voltage UVLO Rising			3.3	3.9	4.4	V
VDD Voltage UVLO Hysteresis				300		mV
High Side Current Limit(5)	I_{LIM}			60		A
Low Side Current Limit(5)				-25		A
EN Input Low Voltage					0.4	V
EN Input High Voltage			2			V
Dead-Time Rising(5)				3		ns
Dead-Time Falling(5)				8		ns
SYNC Current	I_{SYNC}	V_{SYNC}=0V	-50		-43	μA
SYNC Logic High Voltage			2			V
SYNC Logic Low Voltage					0.4	V
PWM High to SW Rising Delay(5)				35		ns
PWM Low to SW Falling Delay(5)				35		ns
PWM Tristate to SW Hi-Z Delay(5)	t_{LT}			60		ns
	t_{TL}			50		
	t_{HT}			75		
	t_{TH}			50		
Minimum PWM Pulse Width(5)				30		ns
PWM Input Current	I_{PWM}	V_{PWM}=3.3V, V_{EN}=5V	80		100	μA
		V_{PWM}=0V, V_{EN}=5V	-100	-90	-80	μA
PWM Logic High Voltage			2.45			V
PWM Tristate Region			1.1		2.0	V
PWM Logic Low Voltage					0.50	V
Current Sense Accuracy(5)		I_{OUT}=15A	-4		+4	%
Current Sense Gain				10		μA/A
Current Sense Common-Mode Voltage Range			1		3.5	V
Temperature Sense Gain(5), (6)				10		mV/°C
Temperature Sense Offset(5), (6)				-100		mV
Temperature Sense Accuracy(5)				±5		°C
VTEMP Pull-Down Current		VTEMP=VDD		160		μA
Over Temperature Protection(5)				170		°C

Notes:

5) Guaranteed by design, not tested in production. The parameter is tested during parameter characterization.

6) See "Junction Temperature Sense" section for details.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.



PWM Delay Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

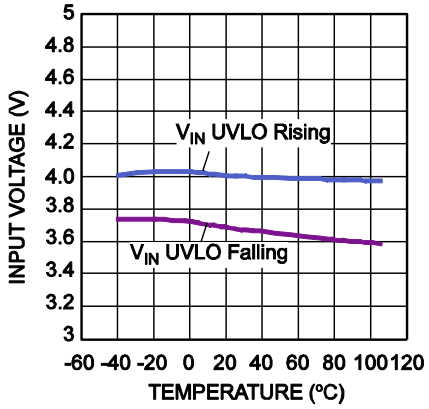
PIN FUNCTIONS

Pin #	Name	Description
1	PWM	Pulse Width Modulation. Leave PWM floating or drive to mid-state to put SW in high impedance state.
2	EN	On/Off Control. Pull low to place SW in a high impedance state.
3	CS	Current Sense Output. Requires an external resistor.
4	VTEMP	Single pin temperature sense output.
5	SYNC	Synchronous Low Switch. Leave open or pull high to enable. Pull low to enter diode emulation mode.
6	FAULT#	Fault reporting on HS current limit, Over Temperature and VDD UVLO. It is an open-drain output during normal operation and pull-low when fault occurred. Low side current limit will not pull low fault pin.
7	AGND	Analog Ground.
8	VDD	Internal Circuitry Voltage. Connect to VDRV thru 2.2Ω resistor and decouple with 1µF capacitor to AGND. Connect AGND and PGND at this point.
9	RIN	Current Sense Compensation. Connect a resistor from this pin to Vin to fine tune current sense gain.
10	T1	Test pin. Connect to ground.
11	BST	Bootstrap. Requires a 0.22µF to 1µF capacitor to drive the power switch's gate above the supply voltage. Connects between SW and BST pins to form a floating supply across the power switch driver.
12-15	SW	Switch Output.
16	VDRV	Driver Voltage. Connect to 5V supply and decouple with 1µF to 4.7µF ceramic capacitor.
17-28	PGND	Power Ground.
29	IN	Supply Voltage. Place C_{IN} close to the device to prevent large voltage spikes at the input.

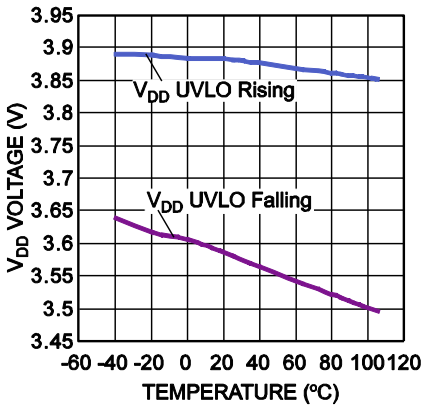
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

TYPICAL CHARACTERISTICS

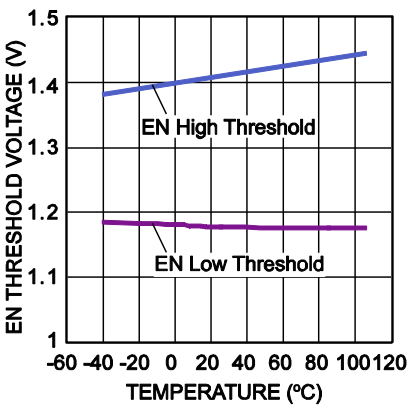
V_{IN} UVLO Threshold vs. Temperature



V_{DD} UVLO Threshold vs. Temperature

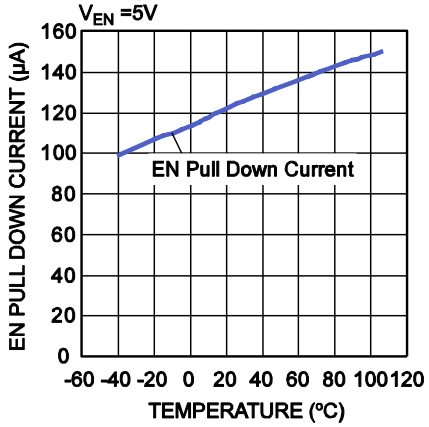


EN Threshold vs. Temperature

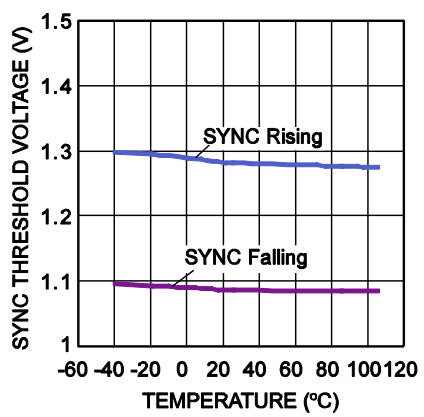


EN Pull Down Current vs. Temperature

V_{EN} =5V

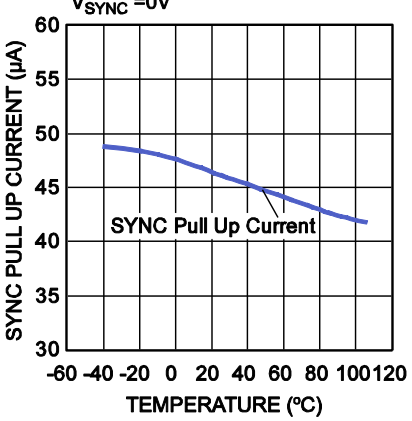


SYNC Threshold vs. Temperature

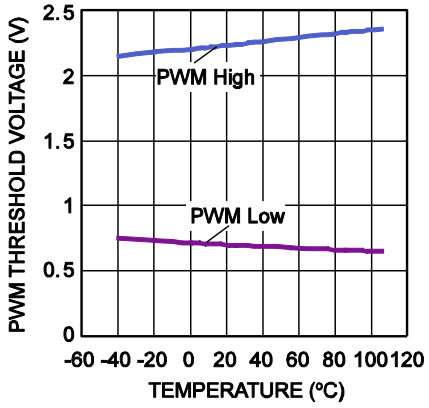


SYNC Pull Up Current vs. Temperature

V_{SYNC} =0V



PWM Threshold vs. Temperature

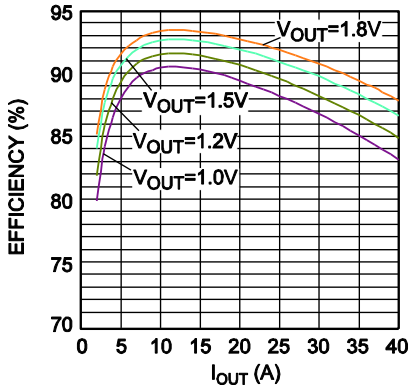


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

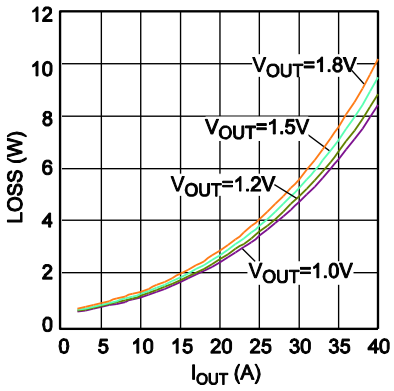
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=12V, V_{DRV}=V_{DD}=5V, V_{OUT}=1.2V, L=215nH, F_{SW}=600kHz, T_A=25°C, no droop, unless otherwise noted.

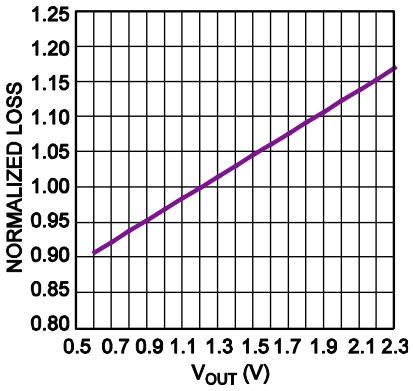
Device Efficiency vs. Output Current
L=FP1007R3-R22-R



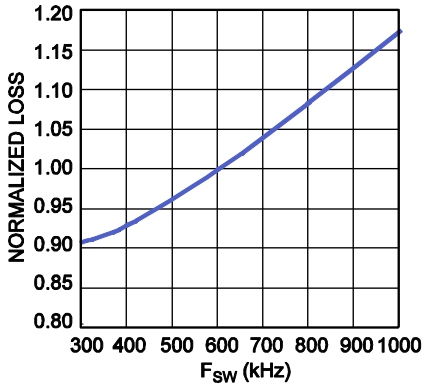
Device Loss vs. Output Current
L=FP1007R3-R22-R



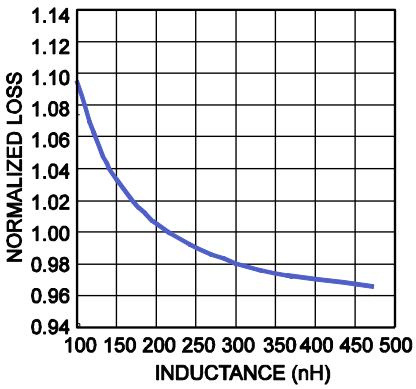
Normalized Power Loss vs. Output Voltage



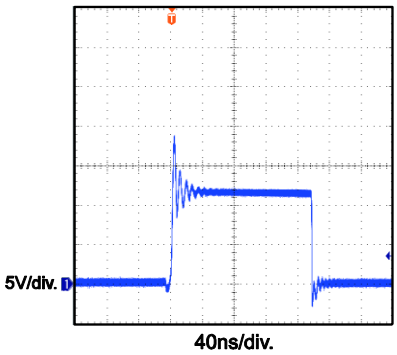
Normalized Power Loss vs. Switching Frequency



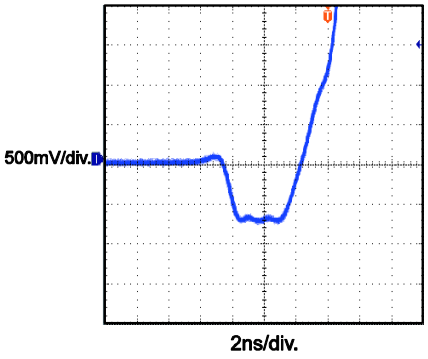
Normalized Power Loss vs. Inductance



SW Output Waveform
I_{OUT}=20A, R_{BST}=3.3Ω



SW Rising Edge Dead Time
I_{OUT}=20A



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

BLOCK DIAGRAM

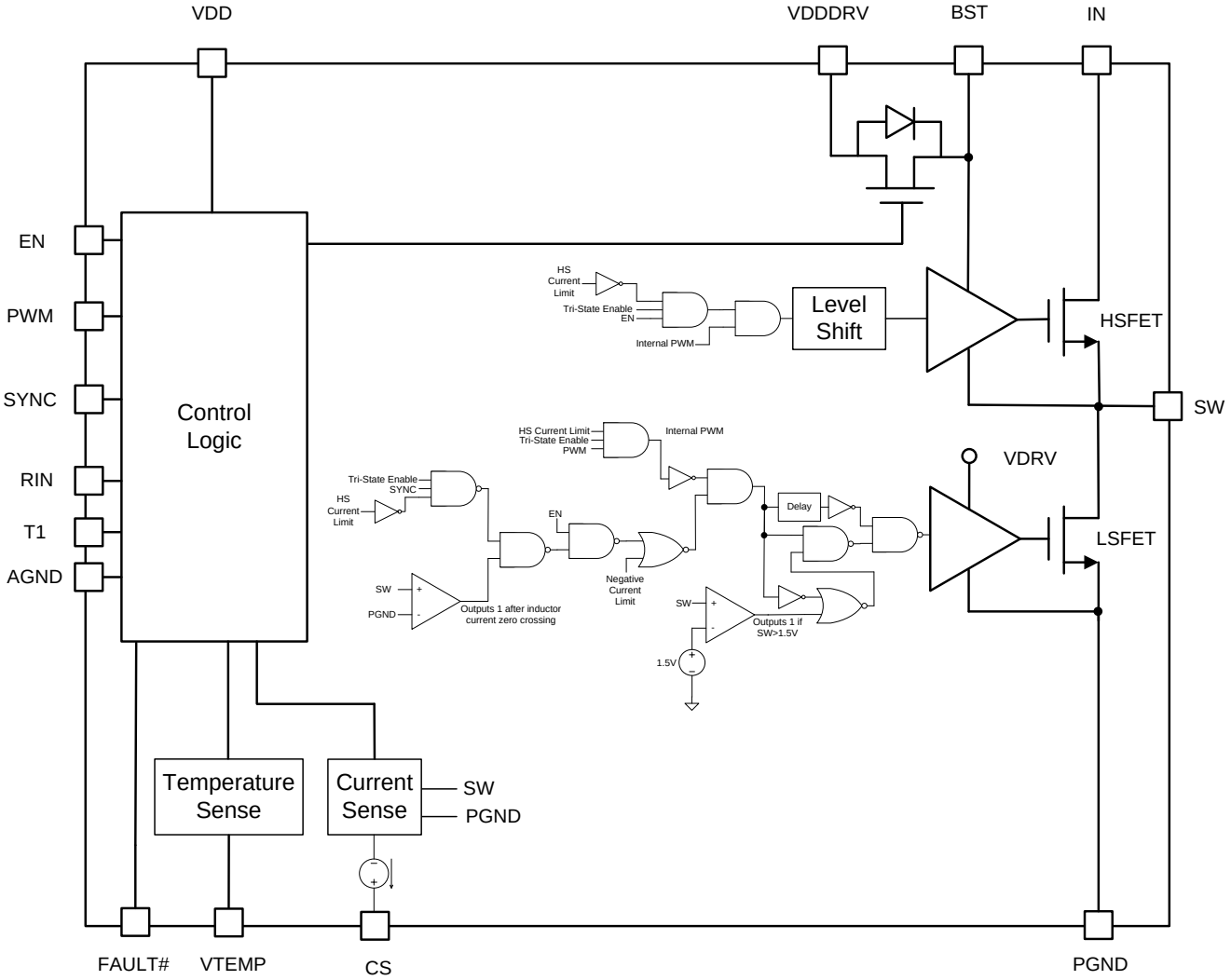


Figure 1: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

OPERATION

The MP86885 is a 40A monolithic half-bridge driver with MOSFETs ideally suited for multi-phase buck regulators.

When the EN transitions from low to high and both V_{DD} and V_{BST} signals are sufficiently high, operation begins. It is recommended to use EN pin to startup and shutdown the Intelli-Phase.

To put SW node in a high impedance state, let PWM pin float or drive PWM pin to mid-state. Drive the SYNC pin low to enter diode emulation mode. In diode emulation mode, the LSFET is off after inductor current crossed zero current.

When HSFET over current is detected, the part will latch off. Recycling VIN/VDD or toggling EN will release the latch and restart the device. When the LSFET detects -25A current, the part will turn off the LSFET for that cycle.

Current Sense

The CS pin is a bi-directional current source proportional to the inductor current. Use the following equations to select the RIN resistance to connect between RIN pin and IN pin:

$$R_{IN} = -7.55 \times I_{L_RIPPLE} + 170(k\Omega)$$

$$I_{L_RIPPLE} = \frac{t_{ON} \times (V_{IN} - V_{OUT})}{L} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times F_{SW} \times L}$$

Where I_{L_RIPPLE} is the peak to peak inductor ripple current. For example, if the ripple current is 10A, then the calculated R_{IN} is 94.5kΩ and 95.3kΩ (the closest 1% resistor value) should be selected for R_{IN}.

The current sense gain is 10μA/A. In general, there is a resistor, R_{CS}, connected from CS pin and V_{OUT} or an external voltage which is capable to sink small current to provide enough voltage shift to meet the operating voltage on CS pin.

The CS voltage range of 1V to 3.5V is required to keep CS's output current linearly proportional to inductor current. Use the following equations to determine a proper reference voltage and/or R_{CS} value:

$$1V < I_{CS} \times R_{CS} + V_{REF} < 3.5V$$

$$I_{CS} = I_L \times 10 \times 10^{-6}$$

Intelli-Phase's current sense output can be used by controller to accurately monitor the output current. The cycle-by-cycle current information from CS pin can be used for phase current balancing, over current protection and active voltage positioning (output voltage droop).
Intelli-Phase's accurate current sense can replace traditional inductor DCR current sensing scheme. In traditional inductor DCR current sense:

$$V_{CS} = I_L \times R_{DCR}$$

With Intelli-Phase's CS output, V_{CS} becomes:

$$V_{CS} = I_{CS} \times R_{CS} = I_L \times R_{CS} \times 10 \times 10^{-6}$$

Where the R_{DCR} term is replaced with $R_{CS} \times 10 \times 10^{-6}$. Figure 2 shows a circuit replacing inductor DCR sensing with Intelli-Phase's CS output. There are several advantages with this current sensing method:

1. Since current sensing is done by Intelli-Phase, user can select low DCR inductors and still have large current sense signal by selecting larger R_{CS}.
2. Tight DCR variation is not required.
3. CS signal is independent of impedance matching and inductor temperature.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

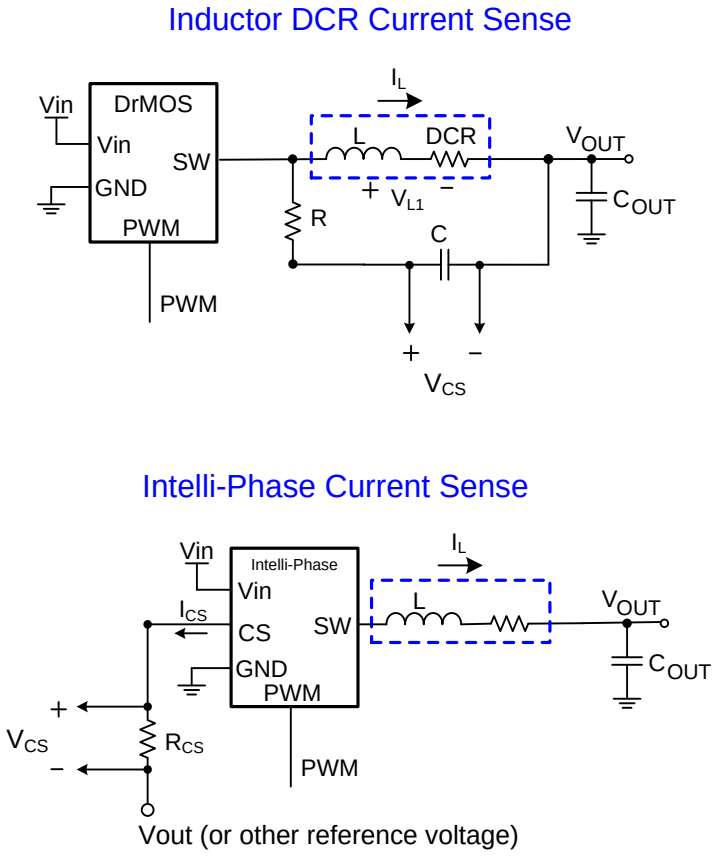


Figure 2: Replacing DCR Current Sense with Intelli-Phase's CS Output

Junction Temperature Sense

The VTEMP pin is a voltage output proportional to the junction temperature. The junction temperature can be calculated from the following equation:

$$T_{JUNCTION} = \frac{(V_{TEMP} + 100mV)}{\frac{10mV}{^{o}C}},$$

for $T_{JUNCTION}$>10°C

For example, if the VTEMP voltage is 700mV, then the junction temperature of Intelli-Phase is 80°C. VTEMP can not go below 0V, so it will read 0V for junction temperature lower than 10°C.

Be sure to measure this voltage between VTEMP and AGND pins for the most accurate reading. In multi-phase operation, the VTEMP pins of every Intelli-Phase can be connected to the temperature monitor pin of the controller. A sample circuitry is shown in Figure 3. VTEMP signals can also be used for system thermal protection as shown in Figure 4.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

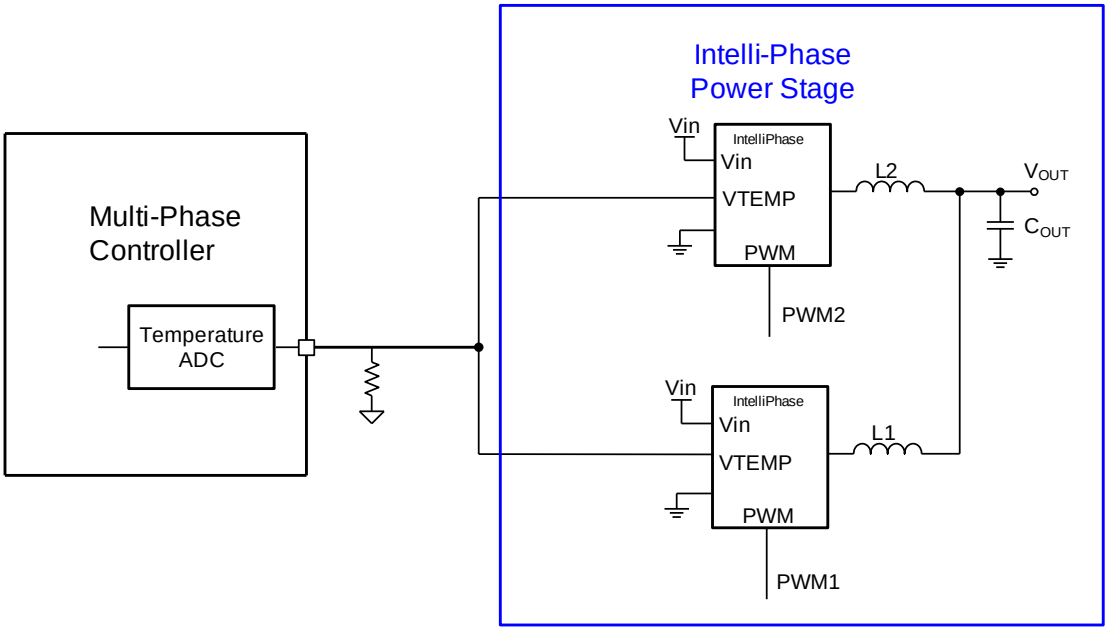


Figure 3: Multi-Phase Temperature Sense Utilization

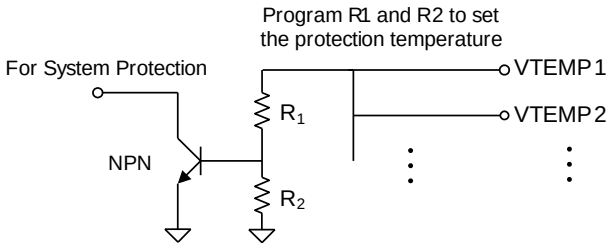


Figure 4: System Thermal Protection

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

PCB Layout Guide Line

PCB layout plays an important role to achieve stable operation. For optimal performance, follow these guidelines. The sample layout at the end of these guidelines can be used as a layout reference.

1. Always place some input bypass ceramic capacitors next to the device and on the same layer as the device. Do not put all of the input bypass capacitors on the back side of the device. Use as many via and input voltage planes as possible to reduce switching spikes. Place the BST capacitor and the VDRV capacitor as close to the device as possible.
2. Place the VDD decoupling capacitor close to the device. Connect AGND and PGND at the point of VDD capacitor's ground connection.
3. It is recommended to use 0.22µF to 1µF bootstrap capacitor and 3.3Ω bootstrap resistance. Do not use capacitance values below 100nF for the BST capacitor.
4. Connect IN, SW and PGND to large copper areas and use via to cool the chip to improve thermal performance and long-term reliability.
5. Keep the path of switching current short and minimize the loop area formed by the input capacitor. Keep the connection between the SW pin and the input power ground as short and wide as possible.

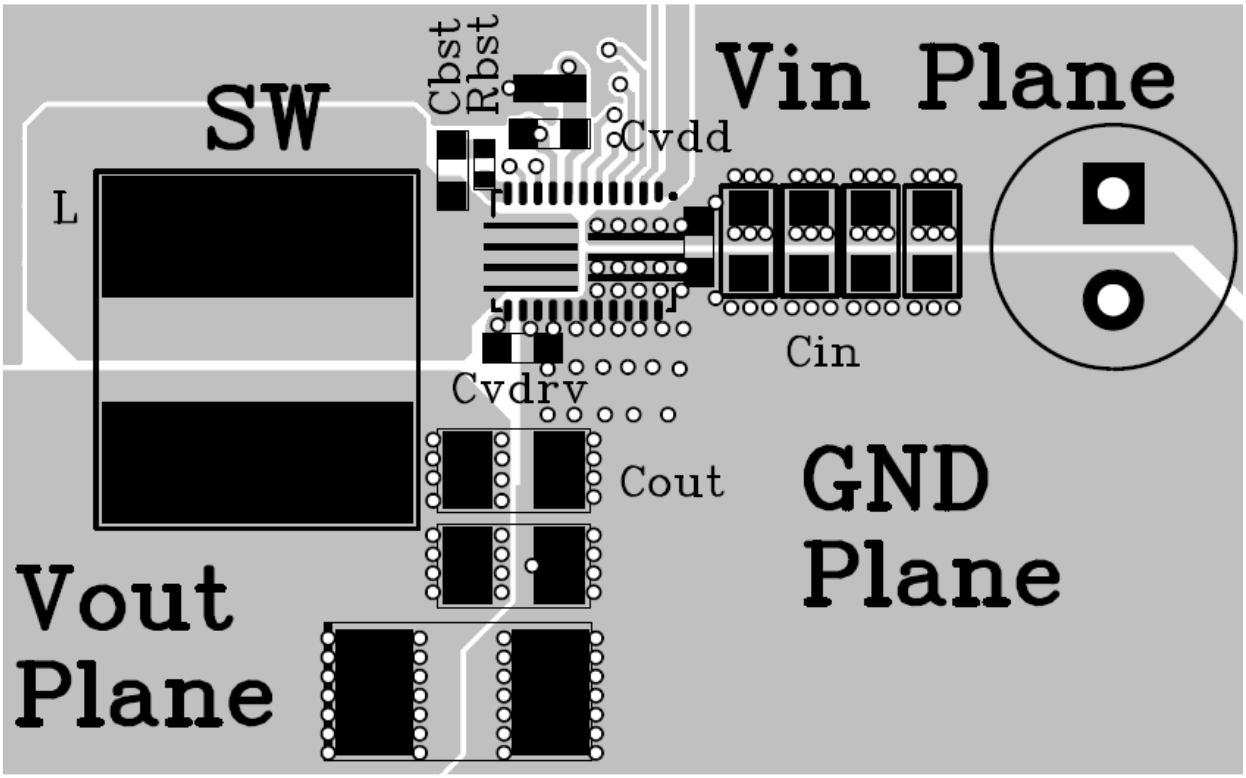


Figure 5: Sample PCB Layout

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS

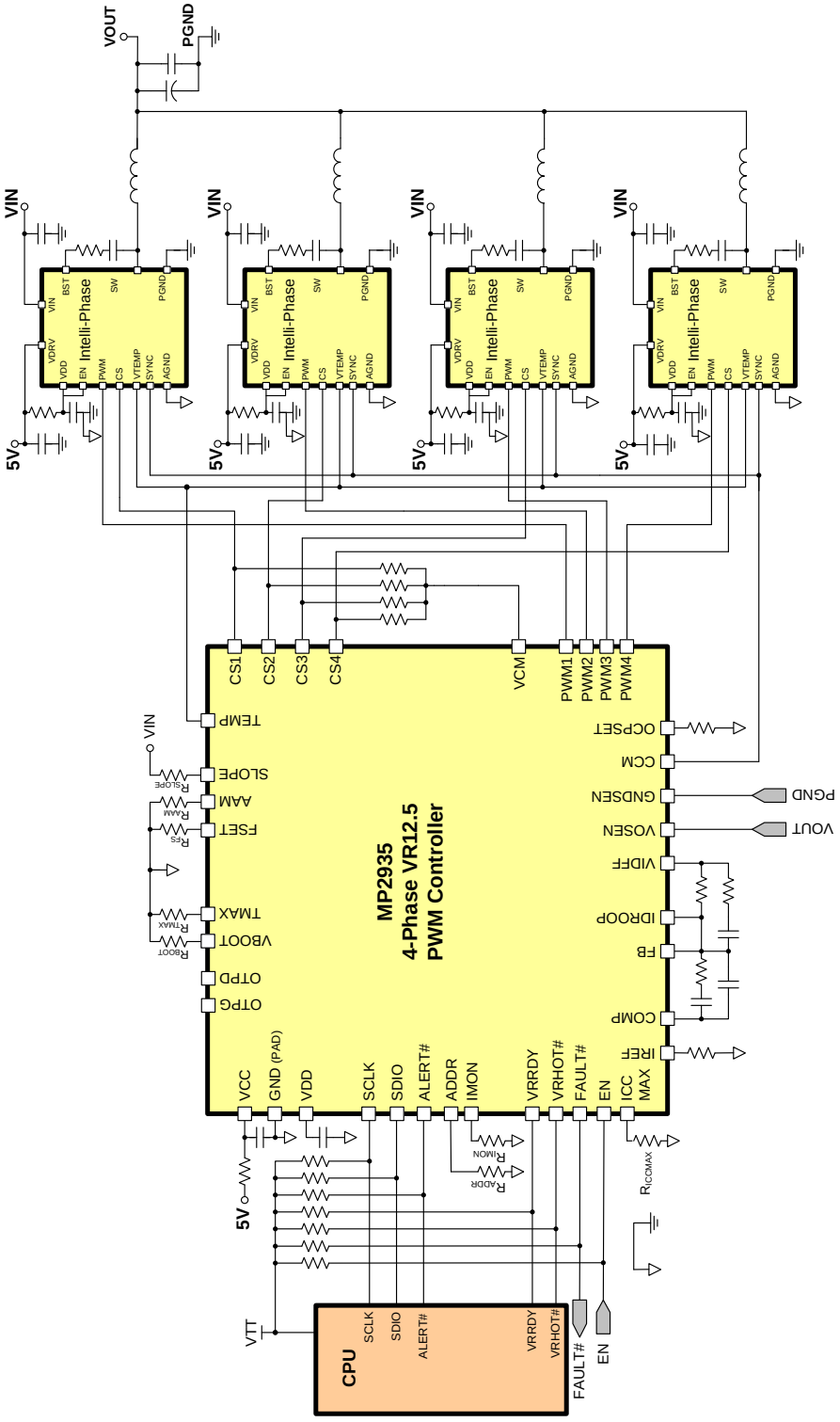
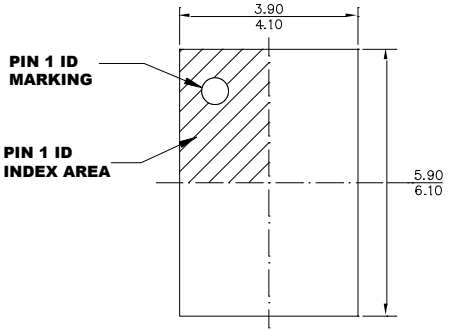


Figure 6: MP2935+Intelli-Phase Application Circuit

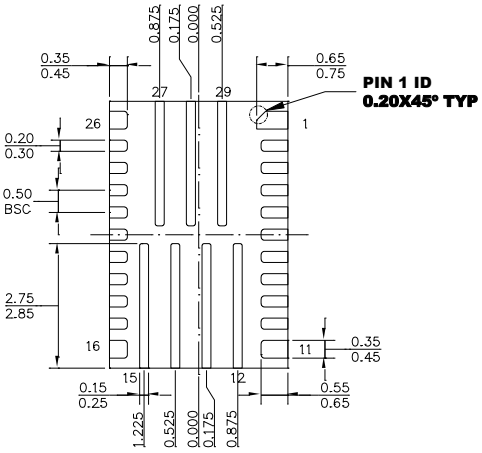
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

PACKAGE INFORMATION

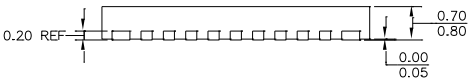
FC-TQFN (4mm x 6mm)



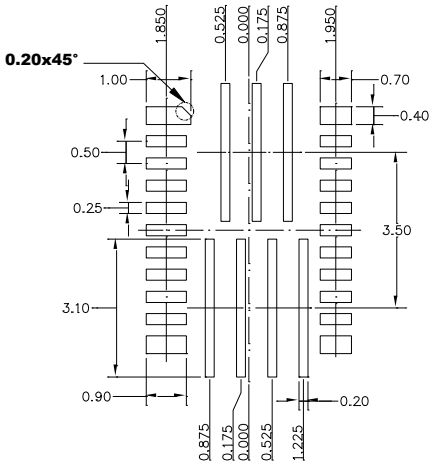
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

NOTICE: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.