MP8638

16V, 12A, Synchronous Step-Down Converter with Adjustable Current Limit

DESCRIPTION

The MP8638 is a fully integrated, high-frequency, synchronous, rectified, step-down switch-mode converter. It offers an ultra-compact solution that can achieve up to 12A of continuous output current (I_{OUT}), with an adjustable current limit (I_{LIMT}).

MPS's proprietary switching loss reduction technique and internal, low on resistance power MOSFETs allow the device to operate at high efficiency across the entire I_{OUT} load range.

Adaptive constant-on-time (COT) control mode provides fast transient response and eases loop stabilization. The DC auto-tune loop and remote differential sense provides good load and line regulation.

Full protection features include over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and thermal shutdown.

The MP8638 requires a minimal number of standard external components, and is available in a QFN-16 (3mmx3mm) package.

FEATURES

- Wide 4.5V to 16V Operating Input Voltage (V_{IN}) Range
- 100µA Low Quiescent Current (I_Q)
- 12A Continous Output Current (I_{OUT})
- Adjustable Current Limit (I_{LIMT})
- Selectable Switching Frequency (f_{SW})
- Selectable External and Internal 3V3 Power Supply
- Adaptive Constant-On-Time (COT) Control for Fast Transient Response
- DC Auto-Tune Loop and Remote Differential Sense
- Low $R_{DS(ON)}$ Internal Power MOSFETs
- Proprietary Switching Loss Reduction Technique
- Stable with POSCAP and Ceramic Output Capacitors
- 1% Reference Voltage (V_{REF})
- Internal Soft Start (SS)
- Output Discharge
- Over-Current Protection (OCP), Over-Voltage Protection (OVP), Under-Voltage Protection (UVP), and Thermal Shutdown
- Available in a QFN-16 (3mmx3mm) Package

APPLICATIONS

- Telecommunication Systems
- Networking Systems
- Servers, Cloud Computing, and Storage
- General-Purpose Point-of-Load (POL) Systems
- Base Stations
- 12V Distribution Power Systems
- High-End Televisions
- Game Consoles and Graphic Cards

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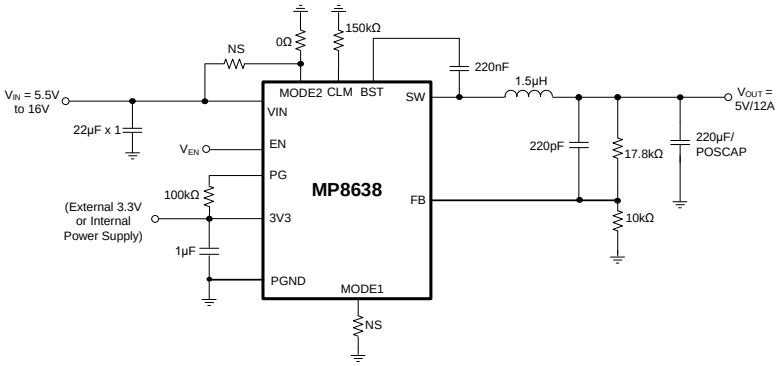
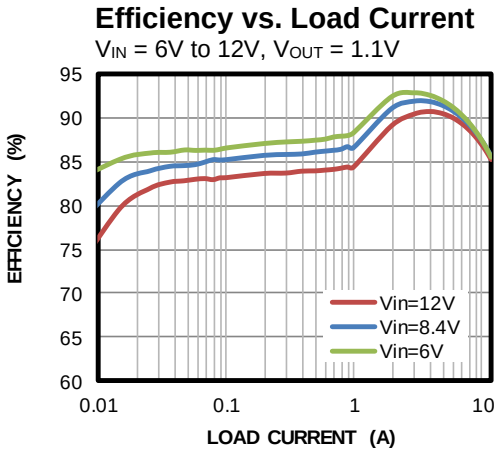
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP8638GQ	QFN-16 (3mmx3mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP8638GQ-Z).

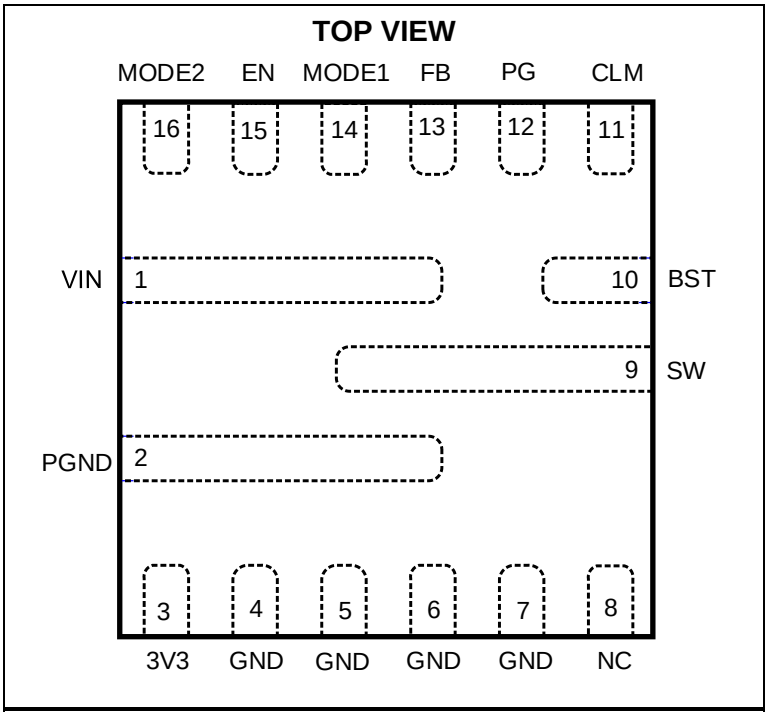
TOP MARKING

BZGY

LLLL

BZG: Product code of the MP8638GQ
Y: Year code
LLLL: Lot number

PACKAGE REFERENCE



QFN-16 (3mmx3mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	VIN	**Input voltage.** The VIN pin supplies power to the internal MOSFET and converter. The MP8638 operates from a 4.5V to 16V input rail. An input capacitor (C_{IN}) is required to decouple the input rail. Use wide PCB traces and multiple vias to make the VIN connection.
2, 4, 5, 6, 7	PGND	**Power ground.** Use wide PCB traces and multiple vias to make the PGND connection.
3	3V3	**3V3 VCC.** If the MODE2 voltage (V_{MODE2}) is equal to the input voltage (V_{IN}), then connect the 3V3 pin to an external 3V3 supply to improve efficiency. If V_{MODE2} is 0V, then the 3V3 VCC logic is powered by the IC. Place a 1µF decoupling capacitor close to the 3V3 and AGND pins. It is recommended to form an RC filter.
8	NC	**Not connected.**
9	SW	**Switch output.** Connect the SW pin to the inductor and bootstrap (BST) capacitor (C_{BST}). If the HS-FET is on, then SW is connected to VIN. If the LS-FET is on, then SW is connected to PGND. Use short and wide PCB traces to make the SW connection. SW is noisy, and should be routed away from sensitive traces.
10	BST	**Bootstrap.** Connect a capacitor between the SW and BST pins to form a floating supply across the high-side MOSFET (HS-FET) driver.
11	CLM	**Adjustable current limit.** Connect the CLM and PGND pins via a resistor to select the current limit (I_{LIMIT}) (7A, 10A, 13A, or 16A).
12	PG	**Power good output.** The PG pin is an open-drain signal. If the output voltage (V_{OUT}) is within its nominal range, then PG is pulled high.
13	FB	**Feedback.** V_{OUT} is set via an external resistor divider connected between the output and PGND (tapped to the FB pin). Place the resistor divider as close to FB as possible. Do not place vias on the FB traces.
14	MODE1	**Mode selection 1.** The MODE1 pin selects the V_{OUT} range and the switching frequency (f_{SW}).
15	EN	**Enable.** The EN pin is a digital input that enables and disables the converter. Pull EN high to turn the converter on; pull EN low to turn it off.
16	MODE2	**Mode selection 2.** The MODE2 pin selects the external and internal VCC power supply. Connect the MODE2 and PGND pins to select the internal VCC supply. Connect the MODE2 and VIN pins to select the external 3V3 supply. Do not float MODE2.

ABSOLUTE MAXIMUM RATINGS (1)

Input voltage (V_{IN}) 18V
V_{SW} (DC) ..... -1V to V_{IN} + 0.3V
V_{SW} (25ns) ..... -3.6V to V_{IN} + 4V (2)
V_{BST} ..... V_{SW} + 4.5V
V_{MODE2} 18V
All other pins ..... -0.3V to +4.5V
Continuous power dissipation (T_A = 25°C) (3)
QFN-16 (3mmx3mm) 2.3W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (4)

Input voltage (V_{IN}) ..... 4.5V to 16V
Supply voltage (V_{CC}) ..... 3.15V to 3.5V
Output voltage (V_{OUT}) ..... 0.6V to 5.5V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (5)	θ_{JA}	θ_{JC}
QFN-16 (3mmx3mm)	55	13	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Measured using a differential oscilloscope probe.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the device to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{3V3} = 3.3V, T_J = 25°C, R_{MODE1} = 0Ω, V_{MODE2} = V_{IN}, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current (External 3V3)						
3V3 supply current	I_{3V3}	V_{EN} = 3V, V_{FB} = 0.62V, V_{MODE2} = V_{IN}		115	150	μA
3V3 shutdown current	I_{3V3_SD}	V_{EN} = 0V, no load, V_{MODE2} = V_{IN}			2	μA
Supply Current (Internal)						
Input current	I_{IN}	V_{EN} = 3V, V_{FB} = 0.62V, V_{MODE2} = 0V		135	170	μA
Shutdown current	I_{IN_SD}	V_{EN} = 0V, no load, V_{MODE2} = 0V			1	μA
MOSFETs						
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)_HS}$	T_J = 25°C		11		mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)_LS}$	T_J = 25°C		6		mΩ
Switch leakage	I_{SW_LKG}	V_{EN} = 0V, V_{SW} = 0V		0	1	μA
Current Limit						
LS-FET valley current limit	I_{LIMIT}	R_{CLM} = 0Ω		7		A
		R_{CLM} = 90kΩ	8.5	10	11.5	A
		R_{CLM} = 150kΩ		13		A
		R_{CLM} = float		16		A
Switching Frequency and Minimum Off Time						
Switching frequency	f_{SW}	R_{MODE1} = 0Ω		700		kHz
		R_{MODE1} = 90kΩ		1000		kHz
Constant on-timer	t_{ON}	V_{IN} = 5V, V_{OUT} = 1.48V, R_{MODE1} = 0Ω	400	480	560	ns
		V_{IN} = 5V, V_{OUT} = 1.48V, R_{MODE1} = 90kΩ	250	325	400	ns
Minimum on time (6)	t_{ON_MIN}			40		ns
Minimum off time (6)	t_{OFF_MIN}			150		ns
Over-Voltage Protection (OVP) and Unver-Voltage Protection (UVP)						
OVP threshold	V_{OVP}		125	130	135	% of V_{REF}
UVP1 threshold	V_{UVP1}		70	75	80	% of V_{REF}
UVP1 foldback timer (6)	t_{UVP1}			30		μs
UVP2 threshold	V_{UVP2}		50	55	60	% of V_{REF}
Reference, Soft Start, and Soft Shutdown						
Reference voltage	V_{REF}	V_{OUT} < 3V	594	600	606	mV
		V_{OUT} > 3V	1.78	1.8	1.82	V
Feedback current	I_{FB}	V_{FB} = 0.62v, V_{RMODE} = 0V		10	50	nA
Soft-start time	t_{SS}	EN is pulled up to PG	1.6	2.1	2.6	ms
MODE1						
MODE1 current	I_{MODE1}		9	10	11	μA
MODE2						
MODE2 low voltage	V_{MODE2_LOW}				0.3	V
MODE2 high voltage	V_{MODE2_HIGH}		1.5			V

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{3V3} = 3.3V, T_J = 25°C, R_{MODE1} = 0Ω, V_{MODE2} = V_{IN}, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Enable (EN) and Under-Voltage Lockout (UVLO) Protection						
EN rising threshold	V_{EN_RISING}		1.1	1.2	1.3	V
EN hysteresis	V_{EN_HYS}			110		mV
EN current	I_{EN}	V_{EN} = 2V			5	µA
		V_{EN} = 0V			1	
VCC UVLO rising threshold	$V_{CC_UVLO_RISING}$		2.7	2.9	3.1	V
VCC UVLO hysteresis	$V_{CC_UVLO_HYS}$			200		mV
V_{IN} UVLO rising threshold	$V_{IN_UVLO_RISING}$			4.05	4.4	V
V_{IN} UVLO hysteresis	$V_{IN_UVLO_HYS}$			300		mV
VCC Regulator						
VCC voltage	V_{CC}	V_{MODE2} = 0V	3.35	3.535	3.7	V
VCC load regulation	V_{CC_REG}	V_{MODE2} = 0V, I_{CC} = 5mA		5		%
Power Good (PG)						
V_{PG} rising (good)	$V_{PG_RISING_GOOD}$	V_{FB} rising		95		% of V_{FB}
V_{PG} falling (fault)	$V_{PG_FALLING_FAULT}$	V_{FB} falling		90		% of V_{FB}
V_{PG} rising (fault)	$V_{PG_RISING_FAULT}$	V_{FB} rising		115		% of V_{FB}
V_{PG} falling (good)	$V_{PG_FALLING_GOOD}$	V_{FB} falling		105		% of V_{FB}
PG low to high delay	t_{DELAY_PG}			200	300	µs
EN low to PG low delay	t_{DELAY_PG/EN_LOW}				12	µs
PG sink current capability	V_{PG}	4mA sink			0.4	V
Thermal Protection						
Thermal shutdown (6)	T_{SD}			155		°C
Thermal shutdown hysteresis (6)	T_{SD_HYS}			25		°C

Note:

6) Guaranteed by design.

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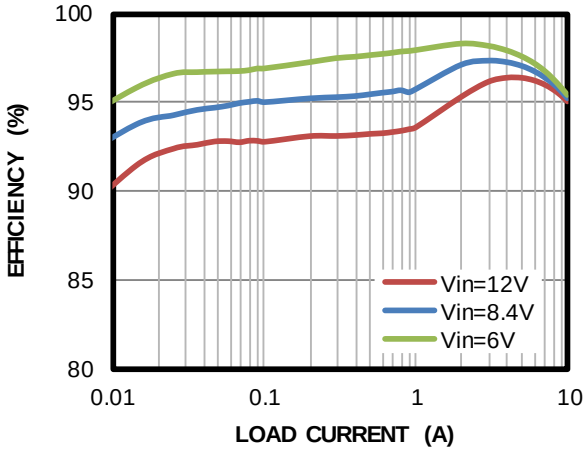
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 1.5µH, DCR = 10mΩ, f_{SW} = 700kHz, DCM, I_{LIMIT} = 16A, T_J = 25°C, unless otherwise noted.

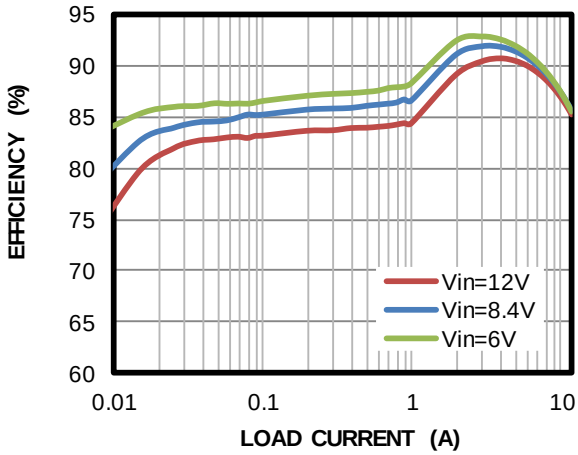
Efficiency vs. Load Current

V_{IN} = 6V to 12V, V_{OUT} = 5.1V



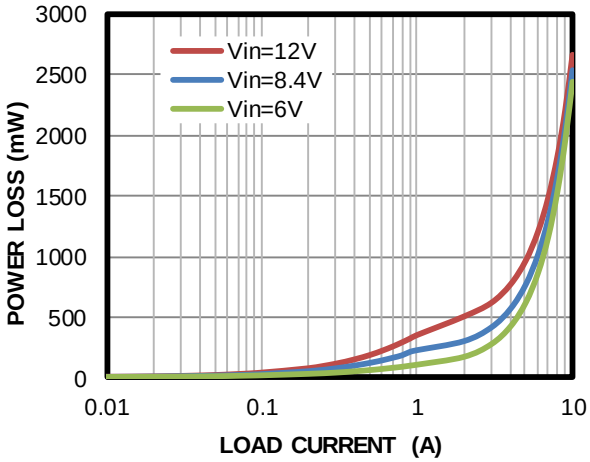
Efficiency vs. Load Current

V_{IN} = 6V to 12V, V_{OUT} = 1.1V



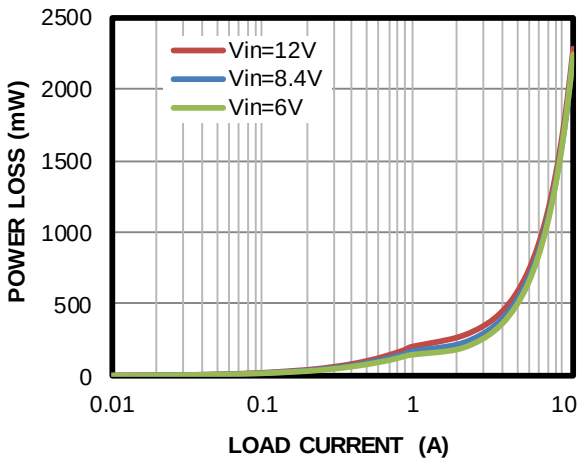
Power Loss vs. Load Current

V_{IN} = 6V to 12V, V_{OUT} = 5.1V



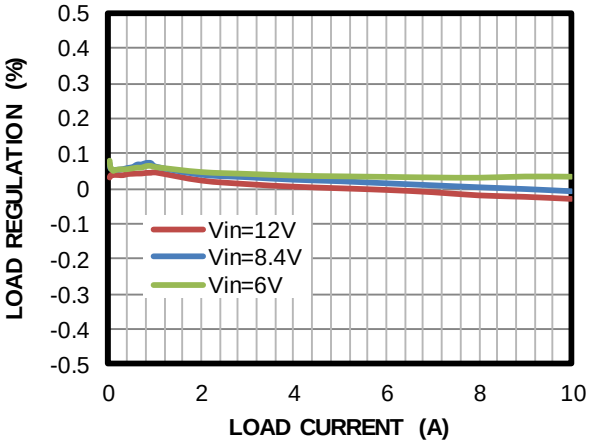
Power Loss vs. Load Current

V_{IN} = 6V to 12V, V_{OUT} = 1.1V



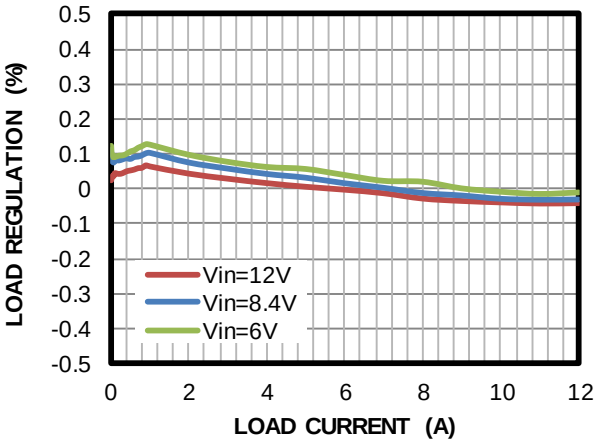
Load Regulation

V_{IN} = 6V to 12V, V_{OUT} = 5.1V



Load Regulation

V_{IN} = 6V to 12V, V_{OUT} = 1.1V



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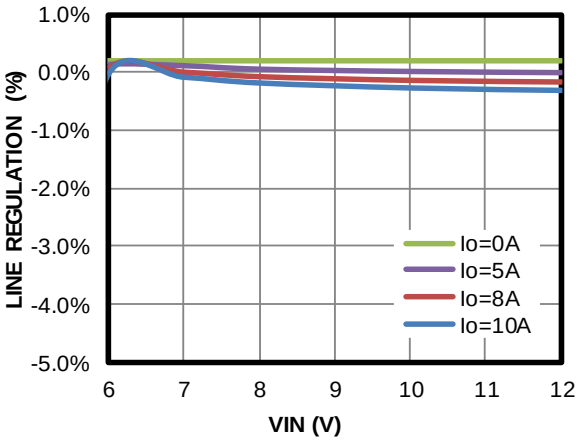
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

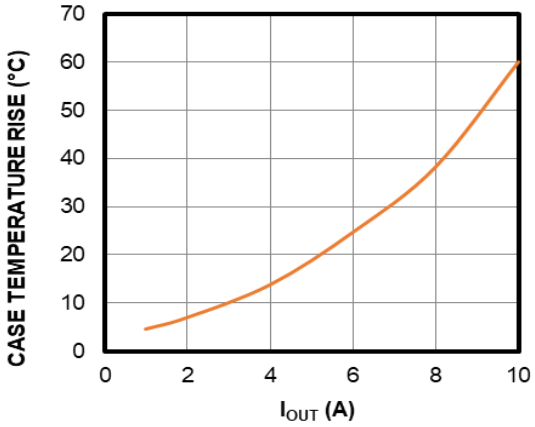
V_{IN} = 12V, V_{OUT} = 5V, L = 1.5µH, DCR = 10mΩ, f_{SW} = 700kHz, DCM, I_{LIMIT} = 16A, T_J = 25°C, unless otherwise noted.

Line Regulation



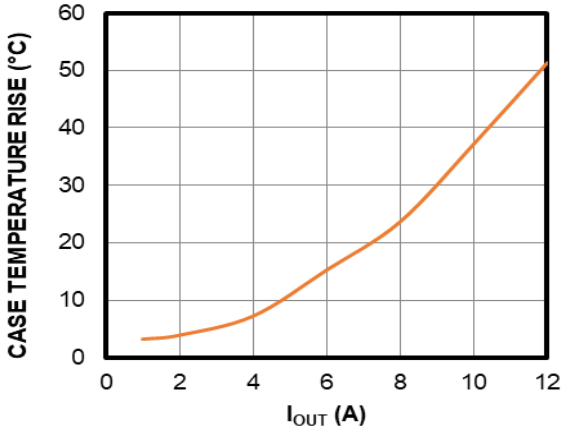
Case Temperature Rise

V_{IN} = 12V, V_{OUT} = 5V, external 3V3, f_{SW} = 700kHz



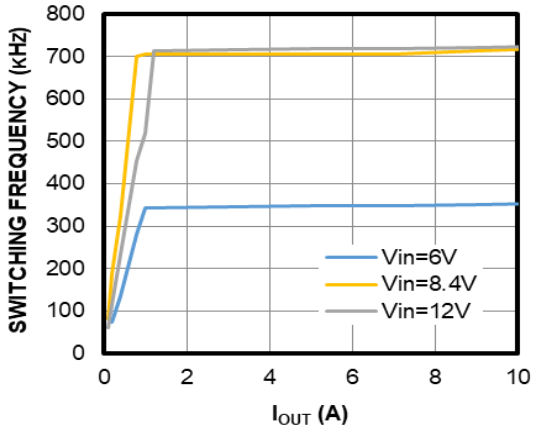
Case Temperature Rise

V_{IN} = 12V, V_{OUT} = 1.1V, external 3V3, f_{SW} = 700kHz



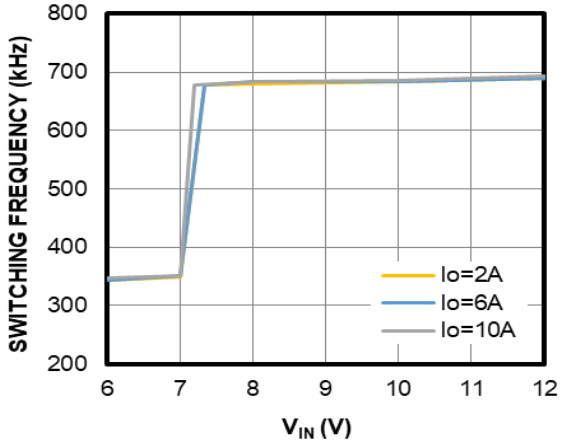
Switching Frequency vs. I_{OUT}

V_{OUT} = 5V, I_{OUT} = 0A to 10A, f_{SW} = 700kHz, L = 1.5µH



Switching Frequency vs. V_{IN}

V_{OUT} = 5V, V_{IN} = 6V to 12V, f_{SW} = 700kHz, L = 1.5µH



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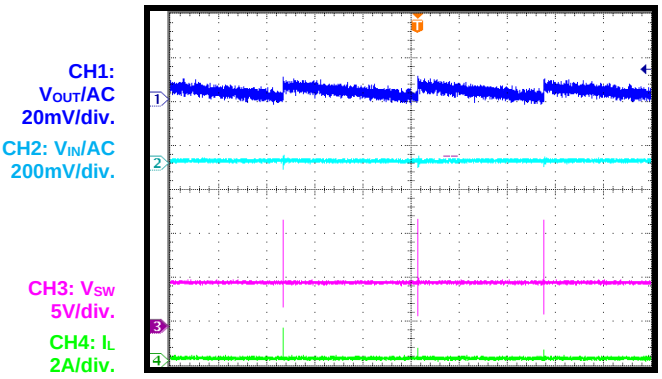
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1.5µH, DCR = 10mΩ, f_{SW} = 700kHz, DCM, I_{LIMIT} = 16A, T_J = 25°C, unless otherwise noted.

Input/Output Voltage Ripple

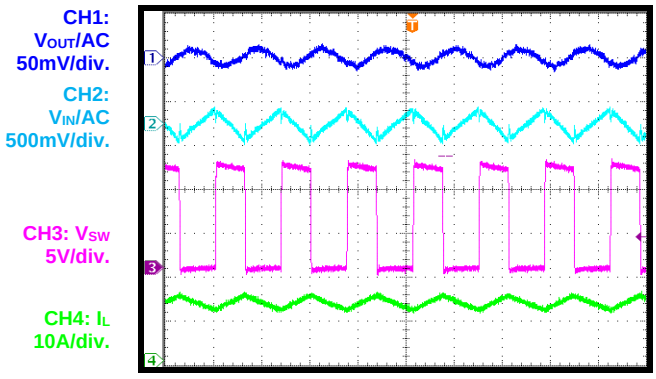
V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A, L = 1.5µH, C_{OUT} = 100µF (25mΩ) + 3 x 22µF



1ms/div.

Input/Output Voltage Ripple

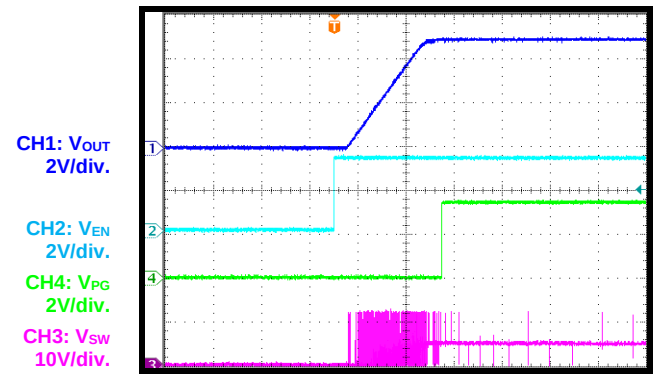
V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 10A, L = 1.5µH, C_{OUT} = 100µF (25mΩ) + 3 x 22µF



1µs/div.

PG Start-Up through EN

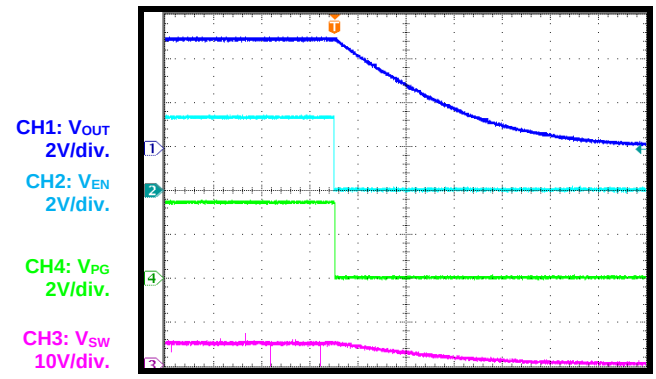
V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A, f_{SW} = 700kHz, L = 1.5µH



1ms/div.

PG Shutdown through EN

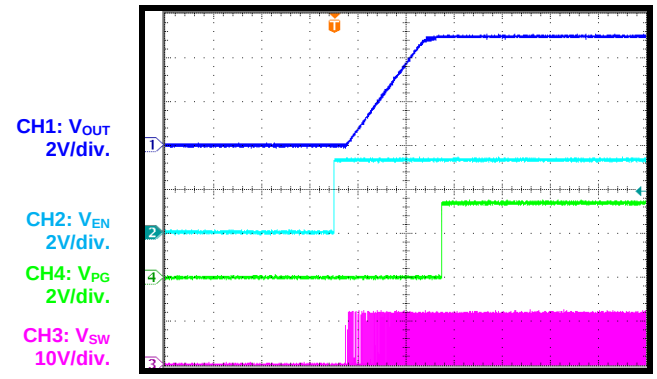
V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A, f_{SW} = 700kHz, L = 1.5µH



4ms/div.

PG Start-Up through EN

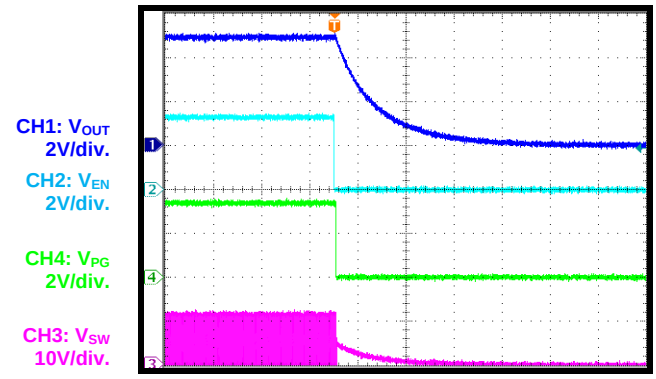
V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 5A, f_{SW} = 700kHz, L = 1.5µH



1ms/div.

PG Shutdown through EN

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 5A, f_{SW} = 700kHz, L = 1.5µH



200µs/div.

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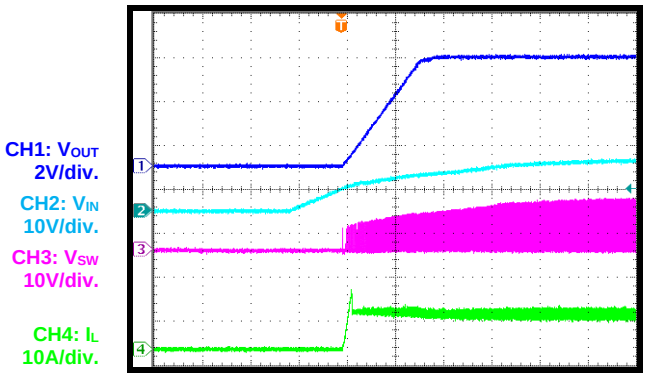
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1.5µH, DCR = 10mΩ, f_{SW} = 700kHz, DCM, I_{LIMIT} = 16A, T_J = 25°C, unless otherwise noted.

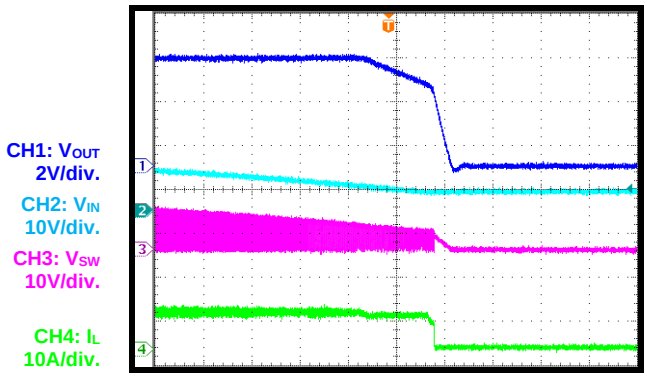
PG Start-Up through VIN

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 8A, f_{SW} = 700kHz, L = 1.5µH



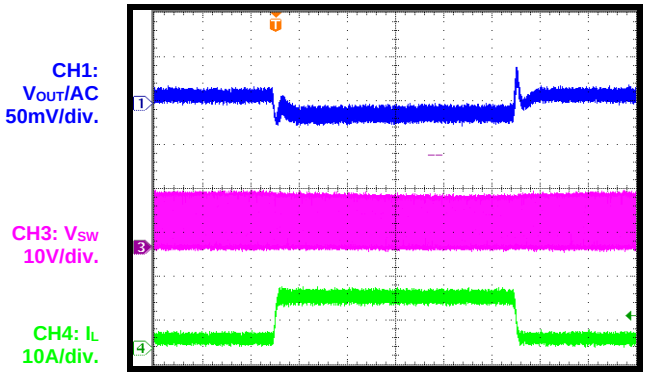
PG Shutdown through VIN

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 8A, f_{SW} = 700kHz, L = 1.5µH



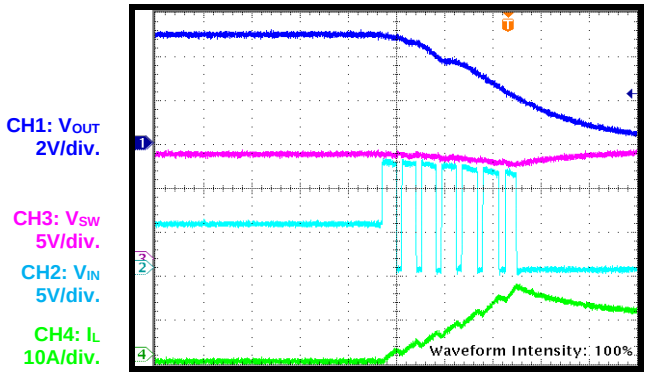
Transient

V_{IN} = 12V, V_{OUT} = 5V, L = 1.5µH, f_{SW} = 700kHz, I_{OUT} = 1.2A to 10.8A at 1.6A/µs, C_{OUT} = 100µF (25mΩ) + 3 x 22µF



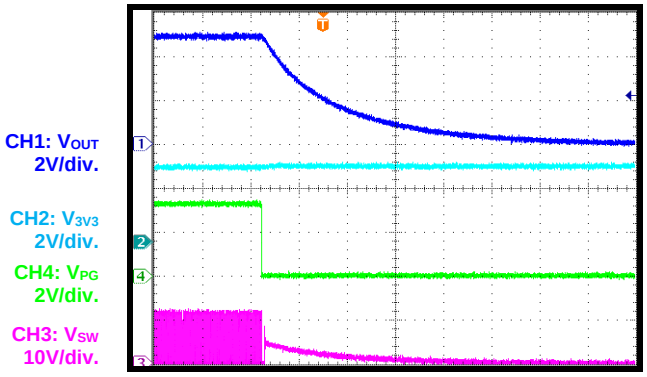
Short-Circuit Protection

V_{IN} = 12V, V_{OUT} = 5V, L = 1.5µH



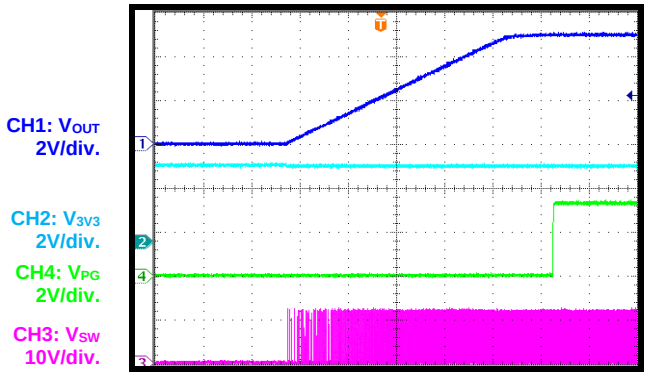
Thermal Shutdown

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 5A, L = 1.5µH



Thermal Recovery

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 5A, L = 1.5µH



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FUNCTIONAL BLOCK DIAGRAM

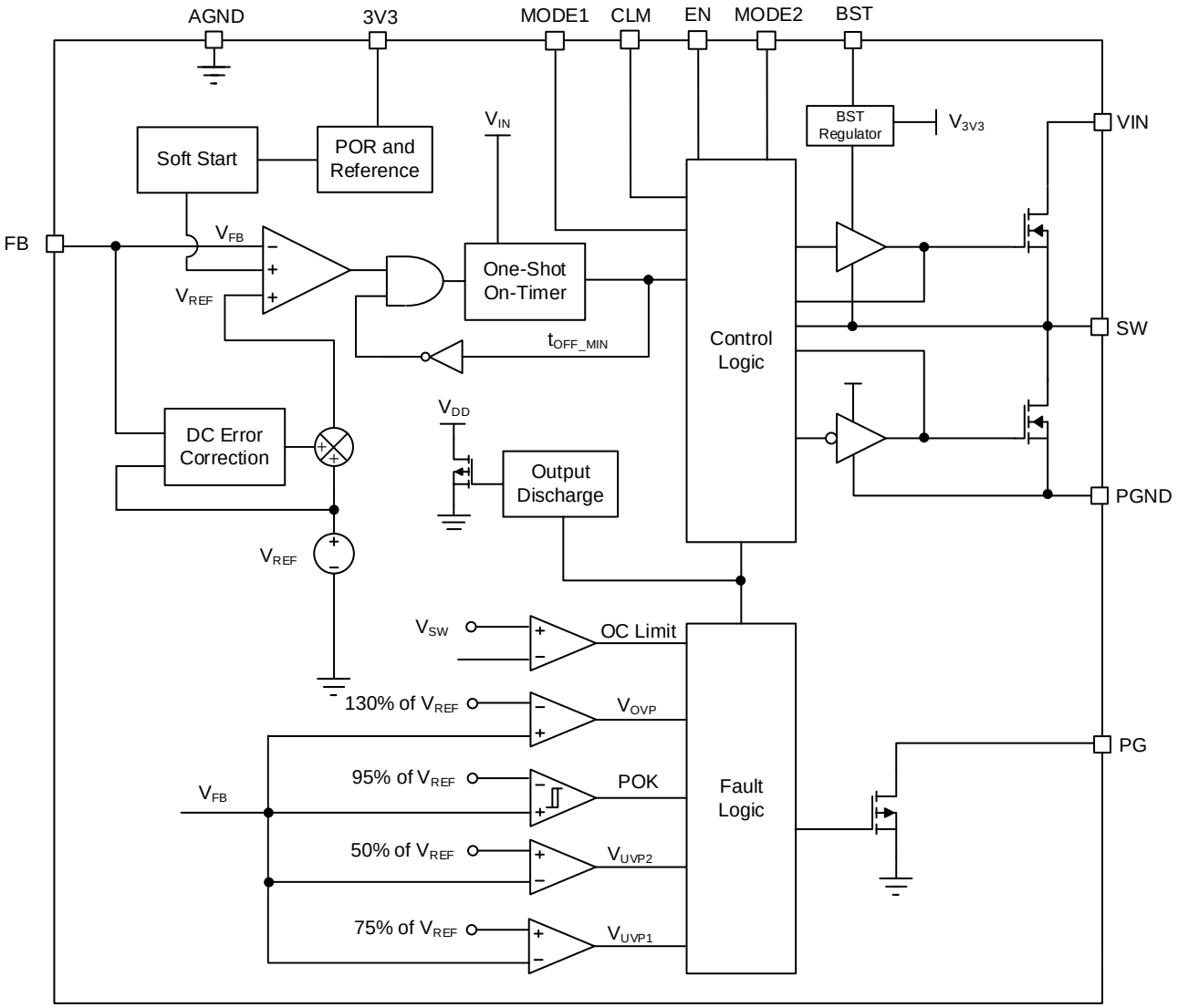

Figure 1: Functional Block Diagram

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OPERATION

Pulse-Width Modulation (PWM) Operation

The MP8638 is a fully integrated, synchronous, rectified, step-down, switch-mode converter with an adjustable current limit (I_{LIMIT}). Constant-on-time (COT) control provides fast transient response and eases loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on once the feedback (FB) voltage (V_{FB}) drops below the reference voltage (V_{REF}), which indicates an insufficient output voltage (V_{OUT}). The on time (t_{ON}) is determined by both the input voltage (V_{IN}) and V_{OUT} to make the switching frequency (f_{SW}) fairly constant across the entire V_{IN} range.

After t_{ON} has elapsed, the HS-FET turns off. It turns on again once V_{FB} drops below V_{REF}. By repeating operation in this way, the converter regulates V_{OUT}. The integrated low-side MOSFET (LS-FET) turns on once the HS-FET turns off to minimize conduction loss. If both the HS-FET and the LS-FET are turned on at the same time, then a dead short occurs between the input and ground. This is called shoot-through. To prevent shoot-through, a dead time (DT) is generated internally between the HS-FET off time (t_{OFF}) and LS-FET t_{ON}, and vice versa.

Internally compensation COT control provides stable operation, even when ceramic capacitors are used as the output capacitors. This internal compensation improves jitter performance without affecting the line or load regulation.

Heavy-Load Operation

If the output current (I_{OUT}) is high and the inductor current exceeds 0A, then the part operates in continuous conduction mode (CCM) (see Figure 2).

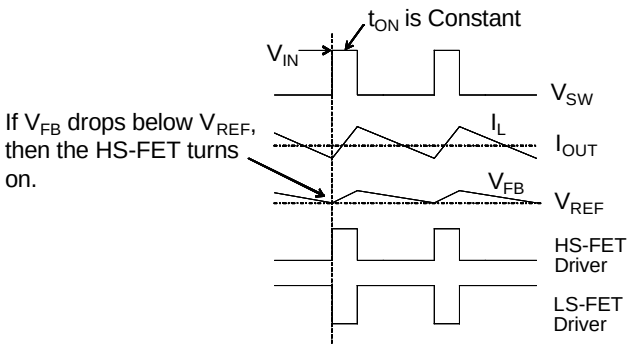

Figure 2: CCM during Heavy-Load Operation

If V_{FB} drops below V_{REF}, then the HS-FET turns on for a fixed interval determined by the one-shot on-timer. Once HS-FET turns off, the LS-FET turns on until the next period begins.

In CCM, f_{SW} fairly constant (pulse-width modulation (PWM) mode).

Light-Load Operation

The inductor current (I_L) decreases as the load decreases. Once I_L reaches 0A, the MP8638 transitions from CCM to discontinuous conduction mode (DCM) (see Figure 3).

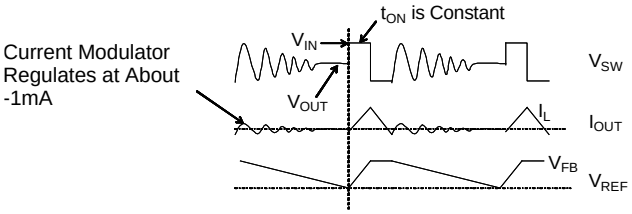

Figure 3: DCM during Light-Load Operation

If V_{FB} drops below V_{REF}, then the HS-FET turns on for a fixed interval determined by the one-shot on-timer. Once the HS-FET turns off, the LS-FET turns on until I_L reaches 0A. In DCM, V_{FB} does not reach V_{REF} as I_L reaches 0A. The LS-FET driver enters a high-impedance (Hi-Z) state once I_L reaches 0A. A current modulator takes control of the LS-FET and limits the I_L to less than -1mA. The output capacitors discharge to ground slowly via the LS-FET. As a result, the efficiency during light-load condition is improved greatly. The HS-FET does not turn on as frequently under light-load conditions as it does under heavy-load conditions. This is called skip-mode operation.

At light-loads or no load, the output drops slowly, which reduces f_{SW} naturally and achieves high efficiency at light loads.

As I_{OUT} increases under light-load conditions, the current modulator regulation time shortens. The HS-FET turns on more frequently, and f_{SW} increases. I_{OUT} reaches its critical level once the current modulator time is 0s. The critical level of I_{OUT} ($I_{OUT_CRITICAL}$) can be calculated with Equation (1):

$$I_{OUT_CRITICAL} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad (1)$$

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The MP8638 enters PWM mode once I_{OUT} exceeds its critical level. Then f_{SW} remains fairly constant across the entire I_{OUT} range.

Jitter and Feedback (FB) Ramp

Jitter occurs in both PWM mode and pulse-skip mode (PSM) while noise in the V_{FB} ripple propagates a delay to the HS-FET driver.

Figure 4 shows jitter in PWM mode.

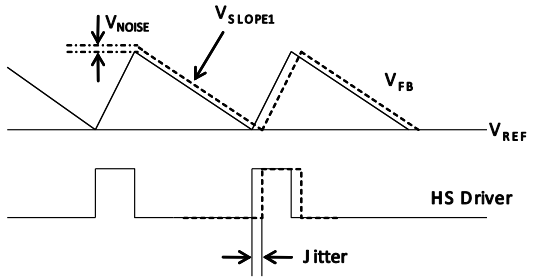

Figure 4: Jitter in PWM Mode

Figure 5 shows jitter in PSM.

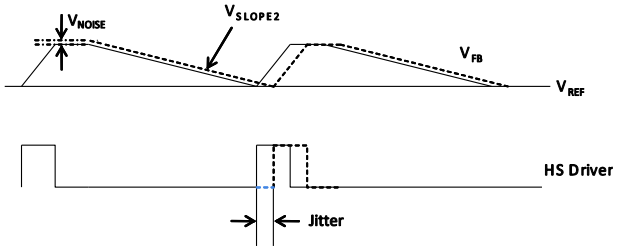

Figure 5: Jitter in PSM

Jitter affects system stability, with noise immunity being proportional to the steepness of the V_{FB} downward slope. Jitter in DCM is typically larger than that in CCM; however, the V_{FB} ripple does not affect noise immunity directly.

Operation without External Ramp Compensation

The traditional COT control scheme is unstable when the ESR of the output capacitor (C_{OUT}) is not large enough to act as an effective current-sense resistor (R_{CS}).

Typically, ceramic capacitors cannot be used as output capacitors.

The MP8638 provides built-in internal ramp compensation to ensure that the system is stable, even without the help of the C_{OUT} ESR. The pure ceramic capacitor solution reduces the V_{OUT} ripple (ΔV_{OUT}), the total BOM cost, and the board area significantly.

Figure 6 shows a typical output circuit in PWM mode without external ramp compensation (see the Application Information section on page 15 for more details).

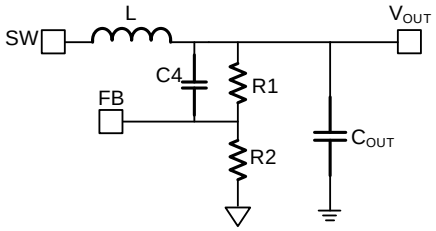

Figure 6: Output Circuit without Ramp Compensation in PWM Mode

When using a large output capacitor (e.g. OSCON), add a >10µF ceramic capacitor in parallel to minimize the effect of the ESL.

Operation with External Ramp Compensation

The MP8638 can support ceramic output capacitors without an external ramp; however, some application may require external ramp compensation to stabilize the system and reduce jitter. See to the Application Information section on page 15 for more information.

Mode Selection

The MP8638 has two mode pins (MODE1 and MODE2). MODE1 selects the V_{OUT} range and f_{SW} via an external MODE1 resistor (R_{MODE1}) (see Table 1). It is recommended to use a 1% accuracy resistor.

Table 1: MODE1 Selection

State	V_{OUT} (7)	f_{SW}	R_{MODE1}
M1	<3V	700kHz	0Ω
M2	<3V	1000kHz	90kΩ
M3	≥3V	1000kHz	150kΩ
M4	≥3V	700kHz	>230kΩ or floating

Note:

7) If V_{OUT} drops below 3V, then V_{REF} is 600mV. If V_{OUT} exceeds ≥3V, then V_{REF} is 1.8V.

MODE2 determines whether VCC power is supported externally or internally (see Table 2).

Table 2: MODE2 Selection

VCC	MODE2
Internal VCC	Connected to AGND
External VCC	Connected to VIN

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Power Good (PG)

The MP8638's power good (PG) output indicates whether V_{OUT} is ready. PG is the open drain of a MOSFET, and should be connected to V_{CC} or another voltage source via a resistor (e.g. 100kΩ). Once V_{IN} is applied, the MOSFET turns on, and PG is pulled to ground before soft start (SS) is ready. Once V_{FB} reaches 95% of V_{REF}, PG is pulled high after a delay time (≤12μs). If V_{FB} drops to 90% of V_{REF}, then PG is pulled low.

Soft Start (SS)

The MP8638 employs a soft-start (SS) mechanism to ensure a smooth output during start-up. Once EN is pulled high, the internal V_{REF} ramps up gradually, and V_{OUT} ramps up smoothly as well. SS is complete once V_{REF} reaches the target value, and the parts begins steady-state operation (see Figure 7).

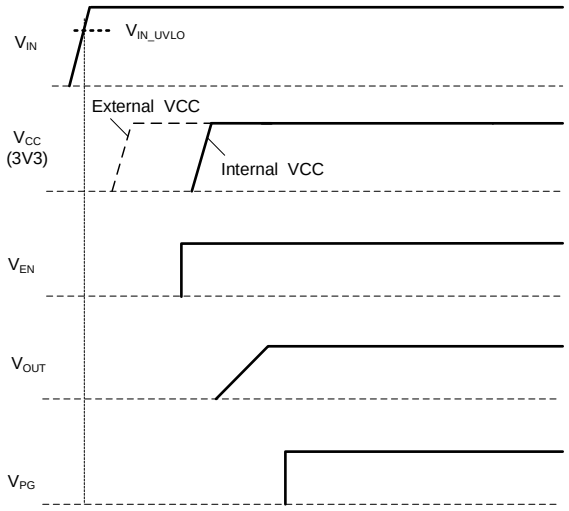

Figure 7: Start-Up Sequence

If the output is pre-biased to a certain voltage during start-up, then both the HS-FET and LS-FET are turned off until the internal V_{REF} exceeds the sensed V_{OUT} at the FB node.

If the part is operating in external 3V3 mode, place a 5.1Ω resistor in series between the 3V3 supply and the 3V3 pin. 3V3 should be shut down before VIN, or keep V_{IN} above V_{3V3}.

Output Discharge

If the converter is shut down via a protection function (under-voltage protection (UVP), over-voltage protection (OVP), over-current protection (OCP), under-voltage lockout (UVLO) protection, or thermal shutdown), then the device discharges the output via an internal 100Ω resistor.

Over-Current Protection (OCP)

The MP8638 provides cycle-by-cycle over-current (OC) limiting. The current-limit circuit employs a valley current-sensing algorithm. The on resistance of the LS-FET is used as a current-sensing element. If the magnitude of the current-sense signal exceeds the current-limit threshold, then PWM cannot initiate a new cycle, regardless of whether V_{FB} is below V_{REF} Figure 8 shows the valley current-limit control (see Figure 8).

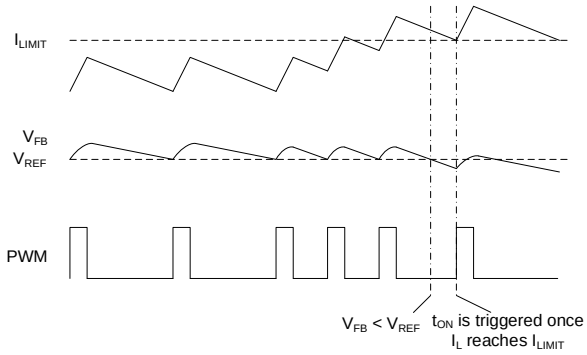

Figure 8: Valley Current-Limit Control

Since the comparison is done during the LS-FET t_{ON}, the OC trip level sets the valley level of I_L. The maximum load current (I_{LOAD_MAX}) can be calculated with Equation (2):

$$I_{OC} = I_{LIMIT} + \frac{\Delta I_L}{2} \quad (2)$$

The OC limit (I_{OC_LIMIT}) limits I_L, and does not latch off. If an OC fault occurs, then the current to the load exceeds the current to C_{OUT}, and V_{OUT} drops. If the current drops below the UVPx threshold (V_{UVPx}), then the part latches off. The fault latch can be reset by pulling V_{EN} low or by cycling the power on VIN.

Current Limit Selection

The MP8638 features an adjustable I_{LIMIT} that can be set via the CLM resistor (R_{CLM}). Table 3 on page 15 shows the recommended resistor values for the selectable current limits.

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Table 3: Recommended Resistor Values for the Selectable Current Limit

I_{LIMIT}	R_{CLM}
7A	0Ω
10A	90kΩ
13A	150kΩ
16A	>230kΩ or floating

Over-Voltage Protection (OVP) and Under-Voltage Protection (UVP)

The MP8638 monitors a resistor-divided V_{FB} to detect over-voltage (OV) and under-voltage (UV) faults. If V_{FB} exceeds 130% of the target voltage, then the OVP comparator output goes high. The OVP circuit latches, the HS-FET turns off, and the LS-FET turns on until zero-current detection (ZCD).

To protect the MP8638 from damage, there is an absolute 3.6V OVP on the output while the system is in V_{OUT} < 3V mode. Once V_{OUT} reaches this value, it latches off. The LS-FET behaves the same as it does at 130% of the target voltage.

If V_{FB} is between 50% and 75% of V_{REF}, then the UVP1 comparator output goes high. The MP8638 latches if V_{FB} remains in this range for about 30µs (latching the HS-FET off and the LS-FET on). The LS-FET remains on until I_L reaches 0A. During this period, I_{LIMIT} controls I_L.

If V_{FB} drops below 50% of V_{REF}, then the UVP2 comparator output goes high. The MP8638 latches off once the comparator and logic delay latch off (latching the HS-FET off and the LS-FET on). The LS-FET remains on until I_L reaches 0A. The fault latch can be reset by pulling V_{EN} low or cycling the power on VIN.

Under-Voltage Lockout (UVLO) Protection

The MP8638 has two UVLO protections: a V_{CC} UVLO (3V) and a V_{IN} UVLO (4.2V). The MP8638 starts up once both V_{CC} and V_{IN} have exceeded their respective UVLO thresholds. The MP8638 shuts down if either V_{CC} or V_{IN} drops below its UVLO falling threshold (2.8V and 3.8V, respectively). Both UVLO protections are non-latch protections.

If an application requires a higher UVLO, adjust the V_{IN} UVLO threshold via an external resistor divider (R_{UP} + R_{DOWN}) (see Figure 9).

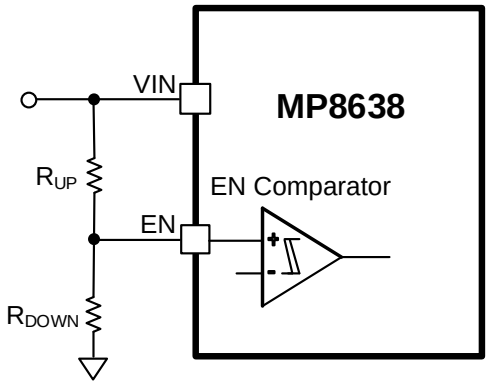

Figure 9: Adjustable UVLO

Thermal Shutdown

The MP8638 employs thermal shutdown to prevent the IC from operating at exceedingly high temperatures. The IC monitors the junction temperature (T_J) internally. If T_J exceeds the thermal shutdown threshold (typically 150°C), the converter shuts down. Once T_J drops to about 125°C, a new SS is initiated. There is a hysteresis of about 25°C. Thermal shutdown is a non-latch protection.

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APPLICATION INFORMATION

Setting the Output Voltage without External Ramp Compensation

The MP8638 does not require ramp compensation for applications where POSCAP or ceramic capacitors are used as output capacitors (V_{IN} > 6V). V_{OUT} can then be set by the FB resistors (R1 and R2) (see Figure 10).

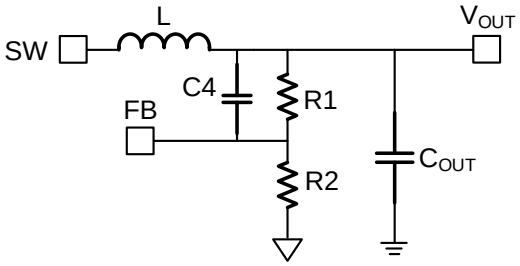

Figure 10: Simplified Circuit without External Ramp Compensation

Choose a value for R2. Consider that a small R2 can lead to considerable quiescent current (I_Q) loss, while a large R2 can make FB noise-sensitive. It is recommended to choose R2 to be between 5kΩ and 50kΩ. If V_{OUT} is low, choose a larger R2 resistance. If V_{OUT} is high, choose a smaller R2 resistance. Considering the V_{OUT} ripple (ΔV_{OUT}), R1 can be calculated with Equation (3):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (3)$$

A capacitor (C4) acts as a feed-forward capacitor to improve the transient response. C4 can be set between 0pF and 1000pF. A larger-value C4 improves transient response, but creates more noise sensitivity.

Setting the Output Voltage with External Ramp Compensation

If the system is not stable enough or if the jitter is too large when using ceramic capacitors (e.g. when using a ceramic C_{OUT} and V_{IN} is 5V or lower), an external voltage ramp should be added to FB through resistor R4 and capacitor C4. Since an internal ramp is already added to the system, a 1MΩ (R4) and 220pF (C4) ramp is sufficient.

V_{OUT} is influenced by the resistor divider (R1 + R2), as well as R4 (see Figure 11).

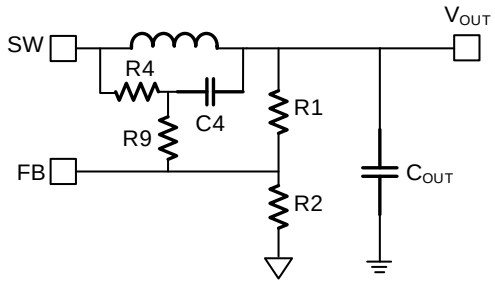

Figure 11: Simplified Circuit with External Ramp Compensation

Choose a reasonable R2, as a small R2 can lead to considerable I_Q loss, but a large R2 can make FB noise-sensitive. Choose an R2 resistance between 5kΩ and 50kΩ. If V_{OUT} is low, choose a larger R2 resistance. If V_{OUT} is high, choose a smaller R2 resistance. Then R1 can be calculated with Equation (4):

$$R1 = \frac{1}{\frac{V_{REF}}{V_{OUT} - V_{REF}} - \frac{R2}{R4}} \times R2 \quad (4)$$

Add a noise-filtering resistor (R9) when designing the PCB layout (see Figure 11). R9 can be set to create a pole to reduce noise. R9 can be calculated with Equation (5):

$$R9 \le \frac{1}{2\pi \times C4 \times 2f_{SW}} \quad (5)$$

Choose R9 to be between 1kΩ and 100Ω to reduce its influence on the ramp.

Selecting the Input Capacitor (C_{IN})

The step-down converter has a discontinuous input current (I_{IN}), and requires a capacitor to supply AC current to the step-down converter while maintaining the DC V_{IN}. Place the ceramic input capacitors as close to VIN as possible for the best performance. Capacitors with X5R and X7R ceramic dielectrics are recommended due to their stability amid temperature fluctuations.

The capacitors should also have a ripple current rating greater than the maximum input ripple current (I_{CIN}) of the converter. I_{CIN} can be estimated with Equation (6):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (6)$$

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The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (7):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (7)$$

For simplification, choose an input capacitor (C_{IN}) with an RMS current rating greater than half of the maximum load current (I_{LOAD_MAX}).

C_{IN} determines the converter's V_{IN} ripple (ΔV_{IN}). If there is ΔV_{IN} requirement in the system, choose an input capacitor that meets the specification.

ΔV_{IN} can be estimated with Equation (8):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (9):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (9)$$

Selecting the Output Capacitor (C_{OUT})

An output capacitor (C_{OUT}) is required to maintain the DC V_{OUT}. It is recommended to use ceramic or POSCAP capacitors. ΔV_{OUT} can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (10)$$

When using ceramic capacitors, the impedance dominates the capacitance at f_{SW}. The majority of ΔV_{OUT} is caused by the capacitance. For simplification, ΔV_{OUT} can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (11)$$

ΔV_{OUT} caused by the ESR is small; therefore, an external ramp is required to stabilize the system. The external ramp can be generated via R4 and C4.

When using POSCAP capacitors, the ESR dominates the impedance at f_{SW}. The ramp voltage generated from the ESR dominates the ΔV_{OUT}. ΔV_{OUT} can be estimated with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (12)$$

The maximum output capacitance should be considered in the design application. The MP8638 has a soft-start time (t_{SS}) of about 1.6ms. If the output capacitance is too high, then V_{OUT} cannot reach the design value during t_{SS} and fails to regulate. The maximum output capacitance (C_{OUT_MAX}) can be calculated with Equation (13):

$$C_{OUT_MAX} = (I_{LIMIT_AVG} - I_{OUT}) \times t_{SS} / V_{OUT} \quad (13)$$

Where I_{LIMIT_AVG} is the average start-up current during soft start (which can be equivalent to I_{LIMIT}).

Selecting the Inductor

An inductor is required to supply constant current to the output load, while being driven by the switched V_{IN}. A larger-value inductor results in a smaller ripple current and a lower ΔV_{OUT}; however, a large-value inductor has a larger physical footprint, higher series resistance, and lower saturation current. A good rule for determining the inductance is to design the peak-to-peak inductor ripple current (ΔI_L) in the inductor to be between 30% and 50% of the maximum I_{OUT} (I_{OUT_MAX}), and to keep the peak inductor current (I_{L_PEAK}) below the maximum switching I_{LIMIT}. The inductance (L) can be calculated with Equation (14):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (14)$$

The inductor should not saturate under the maximum I_{L_PEAK} (including a short current), so the saturation current (I_{SAT}) should exceed I_{LIMIT}.

Design Example

Table 4 on page 18 shows design examples for when ceramic capacitors are used.

A resistor connected between an external 3.3V supply and the 3V3 pin acts as a ripple-noise filter for the 3.3V power supply. This resistor should be between 0Ω and 5.1Ω, depending on the noise level. A 0402-package resistor is sufficient if V_{3V3} rises during t_{SS} (>100µs); otherwise, a larger-package resistor (e.g. 0603 or 0805) is required.

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Table 4: Design Example (8)

V_{OUT} (V)	C_{OUT} (µF)	L (µH)	R_{MODE} (Ω)	C4 (pF)	R1 (kΩ)	R2 (kΩ)	R4 (kΩ)
1	22 x 3	0.68	0	220	13.3	20	NS
1.2	22 x 3	0.68	0	220	20	20	NS
5	220 (POSCAP)	1.5	Floating	220	17.8	10	NS
5	22 x 6	1.5	Floating	220	19.1	10	274

Note:

8) f_{SW} = 700kHz.

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PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. A 4-layer layout is recommended to improve thermal performance. For best results, refer to Figure 12 and follow the guidelines below:

1. Place the high-current paths (PGND, VIN, and SW) as close to the IC as possible using short, direct, and wide traces.
2. Place a thick PGND trace under the IC.
3. Place the input capacitors as close to VIN and PGND as possible. Place these capacitors on the same layer as the IC.
4. Place the decoupling capacitor as close to VCC and PGND as possible.
5. Keep the switching node (SW) short, and away from the feedback network.
6. Place the external feedback resistors next to FB. Do not place vias on the FB trace.
7. Keep the BST voltage path (BST, C3, and SW) as short as possible.
8. Connect the VIN and PGND pads using a large copper plane to improve thermal performance.
9. Place multiple vias with a 10mil drill and 18mil copper width close to the VIN and PGND pads to improve thermal dissipation.

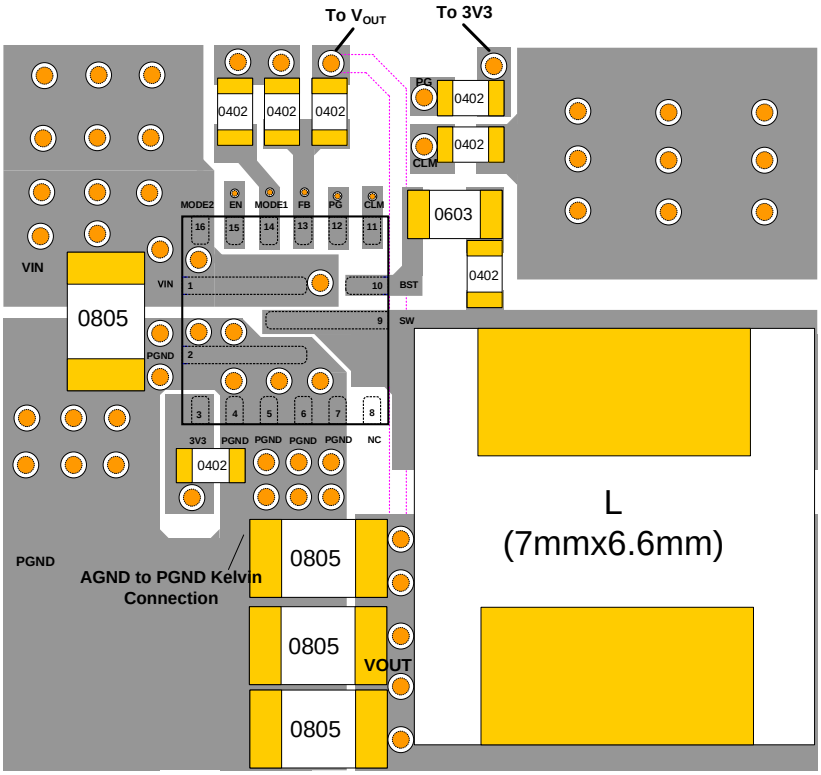

Figure 12: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

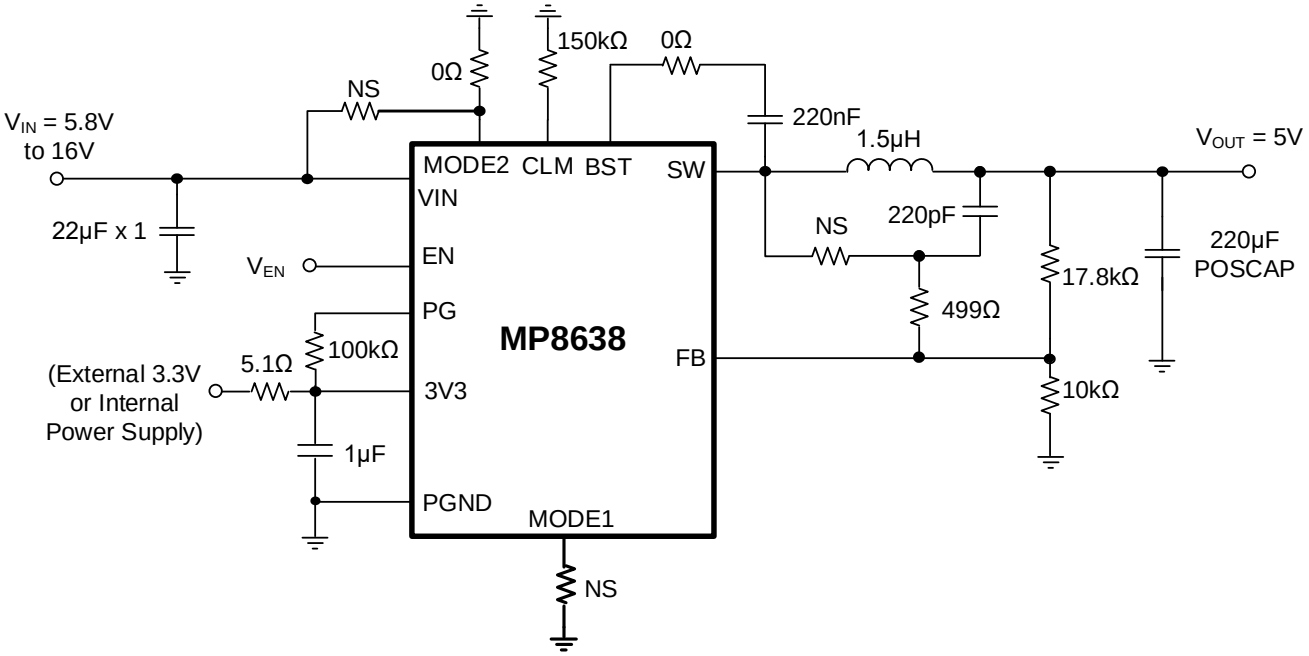

Figure 13: Typical Application Circuit with 5V Output and POSCAP C_{OUT}

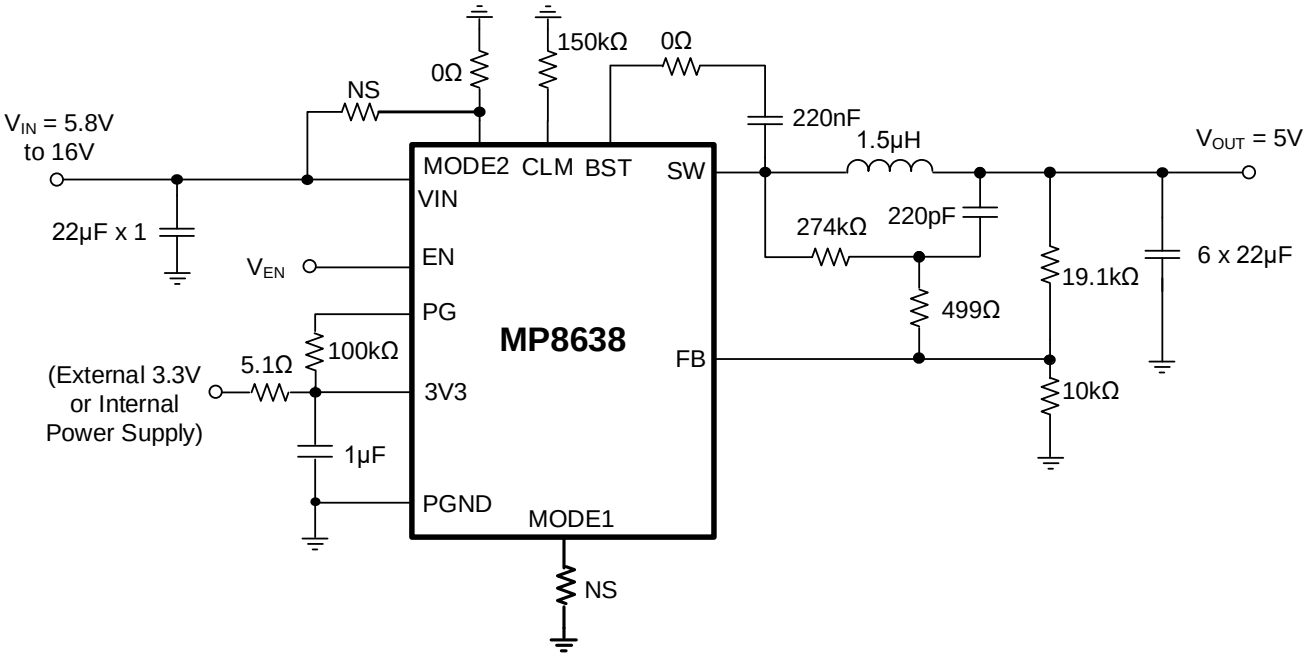

Figure 14: Typical Application Circuit with 5V Output and Ceramic C_{OUT}

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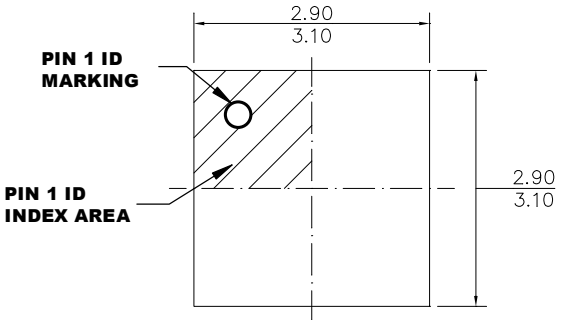
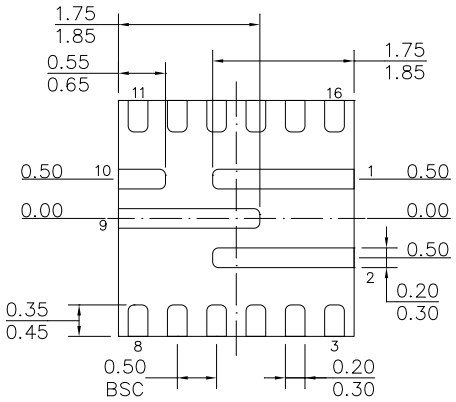
PACKAGE INFORMATION

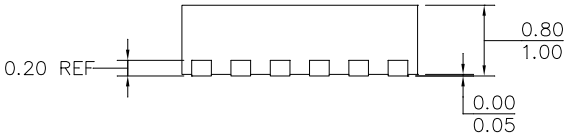
QFN-16 (3mmx3mm)



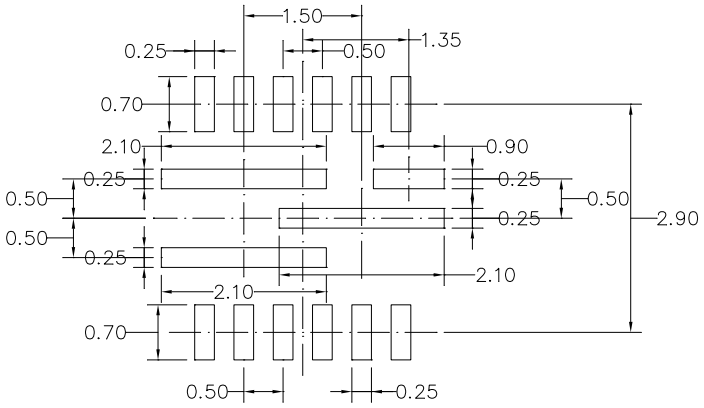
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITIES SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

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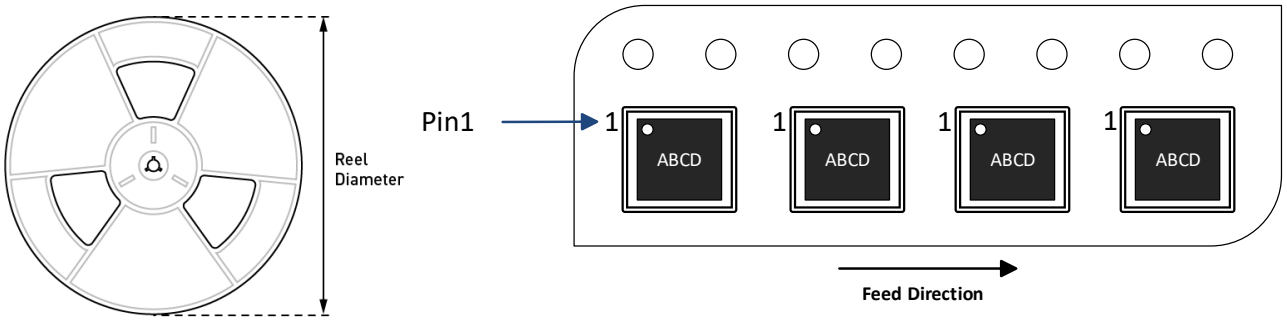
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP8638GQ-Z	QFN-16 (3mmx3mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	7/13/2022	Initial Release	-

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