DESCRIPTION
The MP8130 is a rail-to-rail output, high voltage operational amplifier in a TSOT-23 package. This amplifier provides 200KHz bandwidth while consuming an incredibly low 10µA of supply current. The MP8130 can operate over a single supply range of 2.7V to 36V. It is available in tiny TSOT23-5 packages.

FEATURES
- Single Supply Operation: 2.7V to 36V
- TSOT23-5 Package
- 200KHz –3dB Bandwidth
- 10µA Supply Current
- Rail-to-Rail Output
- Unity-Gain Stable
- Input Common Mode to Ground
- Drives Up to 1000pF of Capacitive Loads
- Available in a TSOT23-5 Package

APPLICATIONS
- Precision Micropower Amplifiers
- Micropower Signal Processing
- Test Equipment

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PACKAGE REFERENCE

<table>
<thead>
<tr>
<th>Part Number*</th>
<th>Package</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>MP8130DJ</td>
<td>TSOT23-5</td>
<td>–40°C to +85°C</td>
</tr>
</tbody>
</table>

For Tape & Reel, add suffix –Z (eg. MP8130DJ–Z)
For RoHS compliant packaging, add suffix –LF (eg. MP8130DJ–LF–Z)

ABSOLUTE MAXIMUM RATINGS (1)
Supply Voltage (V+ to V-)....................... +40.0V
Differential Input Voltage (V_{in+} – V_{in-})....... +6.0V
Input Voltage
V_{in+} = V_{in-}.............................. (V-) – 0.3V, (V+) + 0.3V

Recommended Operating Conditions (2)
Supply Voltage ................................+2.7V to +36V
Operating Temperature .....................–40°C to +85°C

Thermal Resistance (3) \( \theta_{JA} \quad \theta_{JC} \)
TSOT23-5.................................. 220.. 110..°C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) Measured on approximately 1" square of 1 oz copper.

ELECTRICAL CHARACTERISTICS

\( V_+ = +20V, V_- = 0V, V_{CM} = V+//2, R_L = 50\Omega, T_A = +25°C, \) unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Offset Voltage</td>
<td>V_{OS}</td>
<td></td>
<td>–5</td>
<td>1</td>
<td>+5</td>
<td>mV</td>
</tr>
<tr>
<td>Input Offset Voltage Temp Coefficient</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>μV/°C</td>
</tr>
<tr>
<td>Input Bias Current (4)</td>
<td>I_B</td>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td>pA</td>
</tr>
<tr>
<td>Input Offset Current (4)</td>
<td>I_{OS}</td>
<td></td>
<td>0.2</td>
<td></td>
<td></td>
<td>pA</td>
</tr>
<tr>
<td>Input Voltage Range</td>
<td>V_{CM}</td>
<td>CMRR &gt; 60dB (V+ = 36V)</td>
<td>0</td>
<td></td>
<td>36</td>
<td>V</td>
</tr>
<tr>
<td>Common-Mode Rejection Ratio</td>
<td>CMRR</td>
<td>0 &lt; V_{CM} &lt; 36.0V (V+ = 36V)</td>
<td>80</td>
<td>82</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Power Supply Rejection Ratio</td>
<td>PSRR</td>
<td>Supply Voltage change of 2.7V/36V</td>
<td></td>
<td></td>
<td>80</td>
<td>dB</td>
</tr>
<tr>
<td>Large Signal Voltage Gain</td>
<td>A_{VOL}</td>
<td>R_L = 100kΩ, V_{OUT} = 5.0 Peak to Peak</td>
<td>60</td>
<td>88</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Maximum Output Voltage Swing</td>
<td>V_{OUT}</td>
<td>R_L = 100k</td>
<td></td>
<td></td>
<td>(V+) – 50mV</td>
<td>V</td>
</tr>
<tr>
<td>Minimum Output Voltage Swing</td>
<td>V_{OUT}</td>
<td>R_L = 100k</td>
<td></td>
<td></td>
<td>(V–) + 50mV</td>
<td>V</td>
</tr>
<tr>
<td>Gain-Bandwidth Product (4)</td>
<td>GBW</td>
<td>R_L = 1MΩ, C_L = 2pF, V_{OUT} = 0V</td>
<td>100</td>
<td></td>
<td></td>
<td>KHz</td>
</tr>
<tr>
<td>–3dB Bandwidth (4)</td>
<td>BW</td>
<td>A_V = 1, C_L = 2pF, R_L = 1MΩ</td>
<td>200</td>
<td></td>
<td></td>
<td>KHz</td>
</tr>
<tr>
<td>Slew Rate (4)</td>
<td>SR</td>
<td>A_V = 1, C_L = 2pF, R_L = 1MΩ</td>
<td>0.1</td>
<td></td>
<td></td>
<td>V/μs</td>
</tr>
<tr>
<td>Short Circuit Current</td>
<td>I_{SC}</td>
<td>Source</td>
<td>–20</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Supply Current</td>
<td>I_{sup}</td>
<td>No Load</td>
<td>10</td>
<td>15</td>
<td></td>
<td>μA</td>
</tr>
</tbody>
</table>

Note:
4) Guaranteed by design.
TYPICAL PERFORMANCE CHARACTERISTICS
C1= C3 =0.1 μF, C2=C4=10 μF, R_L = 1MΩ (Reference Figure 3)

Output Voltage vs. Output Current
Sourcing

Output Voltage vs. Output Current
Sinking

Gain Bandwidth and Phase Margin
R_L=1MΩ, Gain=1

Short Circuit Current vs. Supply Voltage
Sourcing

Short Circuit Current vs. Supply Voltage
Sinking

Gain Bandwidth and Phase Margin
R_L=1MΩ, Gain=10

Offset Voltage vs. Common Mode Voltage

Offset Voltage vs. Supply Voltage

PSRR

Gain
Phase
PSRR (dB)

V+=20V
V- =20V

V+=20V
V- =20V

V+=20V
V- =20V

V+=20V
V- =20V

V+=20V
V- =20V

V+=10V
V- =10V

V+=10V
V- =10V

V+=10V
V- =10V

V+=10V
V- =10V

V+=10V
V- =10V

V+=10V
V- =10V
TYPICAL PERFORMANCE CHARACTERISTICS
C1= C3 =0.1μF, C2=C4=10μF, RL = 1MΩ (Reference Figure 3)
TYPICAL PERFORMANCE CHARACTERISTICS
C1 = C3 = 0.1 μF, C2 = C4 = 10 μF, R\textsubscript{L} = 1 MΩ (Reference Figure 3)

**Large Signal Pulse Response**

\[ A_V = -1, \ V_+ = V_- = 2.5 V, R_L = 1 MΩ \]

\[ A_V = 6, \ V_+ = V_- = 12 V, R_L = 1 MΩ \]

\[ A_V = 2, \ V_+ = V_- = 5 V, R_L = 1 MΩ \]

\[ \text{VIN} \quad 0.5 V/\text{div.} \quad \text{VO} \quad 0.5 V/\text{div.} \quad 40 \mu s/\text{div.} \]

\[ \text{VIN} \quad 1 V/\text{div.} \quad \text{VO} \quad 5 V/\text{div.} \quad 40 \mu s/\text{div.} \]

\[ \text{VIN} \quad 1 V/\text{div.} \quad \text{VO} \quad 2 V/\text{div.} \quad 40 \mu s/\text{div.} \]

**Rail to Rail Output Operation**

\[ A_V = 6, \ V_+ = V_- = 2.5 V, R_L = 1 MΩ \]

\[ A_V = 3, \ V_+ = V_- = 2.5 V, R_L = 1 MΩ \]

\[ A_V = 2, \ V_+ = V_- = 2.5 V, R_L = 1 MΩ \]

\[ \text{VIN} \quad 0.5 V/\text{div.} \quad \text{VO} \quad 2 V/\text{div.} \quad 200 \mu s/\text{div.} \]

\[ \text{VIN} \quad 0.5 V/\text{div.} \quad \text{VO} \quad 2 V/\text{div.} \quad 200 \mu s/\text{div.} \]

\[ \text{VIN} \quad 1 V/\text{div.} \quad \text{VO} \quad 2 V/\text{div.} \quad 200 \mu s/\text{div.} \]
## PIN FUNCTIONS

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>OUT</td>
<td>Output</td>
</tr>
<tr>
<td>2</td>
<td>V+</td>
<td>Supply Voltage</td>
</tr>
<tr>
<td>3</td>
<td>IN+</td>
<td>Non-Inverting Input</td>
</tr>
<tr>
<td>4</td>
<td>IN-</td>
<td>Inverting Input</td>
</tr>
<tr>
<td>5</td>
<td>V-</td>
<td>Ground or Supply Return Pin</td>
</tr>
</tbody>
</table>

## TEST CIRCUITS

![AC Test Circuit Diagram](image)

Notes: Close S3 for positive gain. Input signal to RF(+Av) connector.
The gain $Av = 1 + \frac{RFB}{RIN}$.
For unity gain, remove $RIN$ and short $RFB$.
Open S3 for negative gain. Input signal to RF(-Av) connector.
The gain $Av = -\frac{RFB}{RIN}$.
S1 and S2 are switches for possible resistor and capacitor load connections.

Figure 1—AC Test Circuit
TEST CIRCUITS (continued)

Figure 2—Positive Power Supply Rejection Ratio Measurement
APPLICATION INFORMATION

Power Supply Bypassing

Regular supply bypassing techniques are recommended. A 10\(\mu\)F capacitor in parallel with a 0.1\(\mu\)F capacitor on both the positive and negative supplies is ideal. For the best performance, all bypassing capacitors should be located as close to the op amp as possible and all capacitors should be low ESL (Equivalent Series Inductance) and low ESR (Equivalent Series Resistance). Surface mount ceramic capacitors are ideal.

For large input signals, the op amp needs two clamp diodes to the input side. (See Figure 3 Large Input Signal Schematic).

\[\text{Figure 3—Large Input Signal Schematic Sold}\]
PACKAGE INFORMATION

TSOT23-5

TOP VIEW

RECOMMENDED LAND PATTERN

FRONT VIEW

SIDE VIEW

NOTE:
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

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