



The Future of Analog IC Technology™

# MP8103

## Dual Ultra Low Power 1.8V, 600kHz Op Amp

### DESCRIPTION

The MP8103 is a single supply, dual rail-to-rail output operational amplifier. This amplifier provides 600kHz bandwidth while consuming an incredibly low 14µA of supply current. The MP8103 can operate with a single supply voltage as low as 1.8V. The input common mode can go below the negative rail. The maximum supply voltage is 5.5V which allows the device to operate from ±0.9V to ±2.75V or a single supply. The MP8103 is available in an 8-pin 3mm x 5mm MSOP package.

### FEATURES

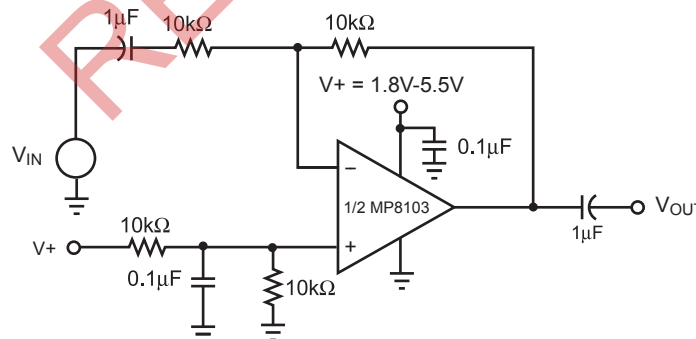
- Single Supply Operation: 1.8V to 5.5V
- 600kHz -3dB Bandwidth
- 14µA Supply Current
- Rail-to-Rail Output
- Unity-Gain Stable
- Input Common Mode to Ground
- Drives Up to 1000pF of Capacitive Loads
- High Slew Rate: 0.1V/µs
- Available in a MSOP8 Package

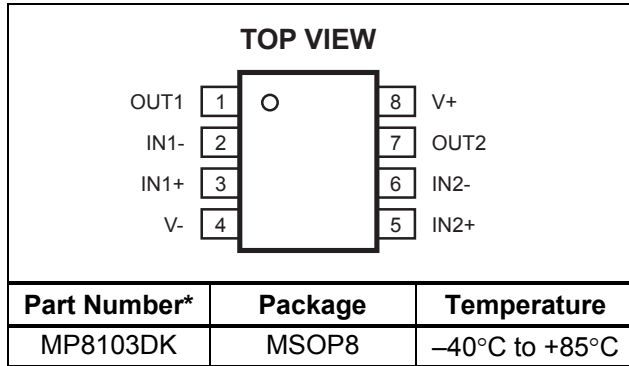
### APPLICATIONS

- Portable Equipment
- PDAs
- Pagers
- Cordless Phones
- Handheld GPS
- Consumer Electronics
- Smoke Detector
- Portable Medical Equipment

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### TYPICAL APPLICATION



**PACKAGE REFERENCE**


\* For Tape & Reel, add suffix -Z (eg. MP8103DK-Z)  
 For RoHS Compliant Packaging, add suffix -LF (eg. MP8103DK-LF-Z)

**ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>**

Supply Voltage (V+ to V-) ..... +6.0V  
 Differential Input Voltage ( $V_{IN+} - V_{IN-}$ ) ..... +6.0V  
 Input Voltage ( $V_{IN+} - V_{IN-}$ )..  $V_{IN+} + 0.3V, V_{IN-} - 0.3V$

**Recommended Operating Conditions <sup>(2)</sup>**

Supply Voltage ..... +1.8V to +5.5V  
 Operating Temperature ..... -40°C to +85°C

**Thermal Resistance <sup>(3)</sup>**

$\theta_{JA}$   $\theta_{JC}$   
 MSOP8 ..... 150 ..... 65... °C/W

**Notes:**

- Exceeding these ratings may damage the device.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on approximately 1" square of 1 oz copper.

**ELECTRICAL CHARACTERISTICS**

$V_+ = +5V, V_- = 0V, V_{CM} = V_+/2, R_L = 10k\Omega, T_A = +25^\circ C$ , unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Offset Voltage	$V_{OS}$		-5	1	+5	mV
Input Offset Voltage Temp Coefficient				15		$\mu V/^\circ C$
Input Bias Current <sup>(4)</sup>	$I_B$			2		pA
Input Offset Current <sup>(4)</sup>	$I_{OS}$			0.2		pA
Input Voltage Range	$V_{CM}$	CMRR > 60dB	0		3.8	V
Common-Mode Rejection Ratio	CMRR	$0 < V_{CM} < 3.5V$		82		dB
Power Supply Rejection Ratio	PSRR	Supply Voltage change of 1.0V		80		dB
Large Signal Voltage Gain	$A_{VOL}$	$R_L = 100k\Omega, V_{OUT} = 5.0$ Peak to Peak	60	88		dB
Maximum Output Voltage Swing	$V_{OUT}$	$R_L = 10k\Omega$		$V_+ - 23mV$		V
Minimum Output Voltage Swing	$V_{OUT}$	$R_L = 10k\Omega$		$V_- + 19mV$		V
Gain-Bandwidth Product <sup>(4)</sup>	GBW	$R_L = 200k\Omega, C_L = 2pF, V_{OUT} = 0$		200		KHz
-3dB Bandwidth	BW	$A_V = 1, C_L = 2pF, R_L = 1M\Omega$		600		KHz
Slew Rate <sup>(4)</sup>	SR	$A_V = 1, C_L = 2pF, R_L = 1M\Omega$		0.1		V/ $\mu s$
Short Circuit Current	$I_{SC}$	Source		20		mA
		Sink		20		mA
Supply Current		No Load		14	22	$\mu A$

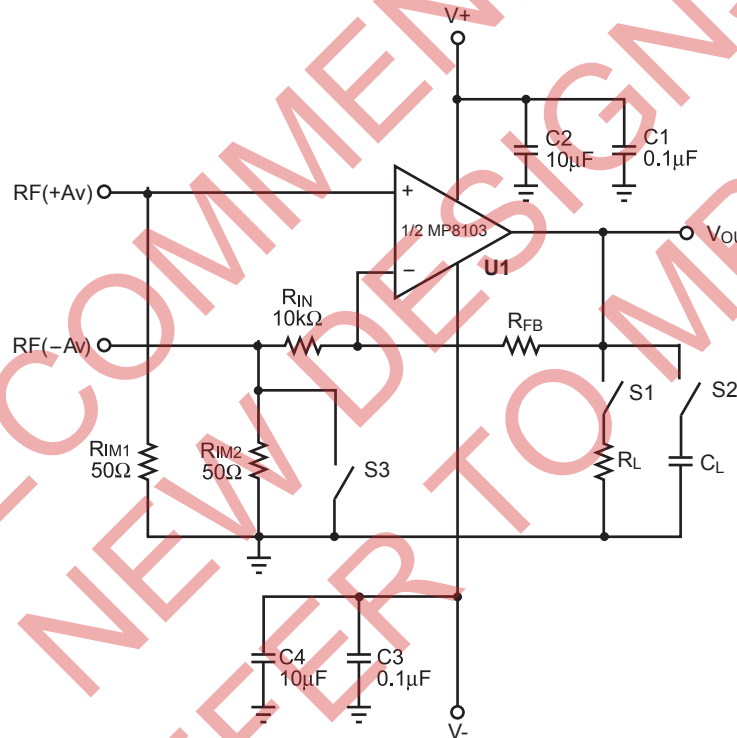
**Note:**

4) Guaranteed by design.

## PIN FUNCTIONS

Pin #	Name	Description
1	OUT1	Output of First Op-Amp..
2	IN1-	Inverting Input of First Op-Amp.
3	IN1+	Non-Inverting Input of First Op-Amp.
4	V-	Ground or Supply Return Pin.
5	IN2+	Non-Inverting Input of Second Op-Amp.
6	IN2-	Inverting Input of Second Op-Amp.
7	OUT2	Output of Second Op-Amp.
8	V+	Supply Voltage.

## TEST CIRCUITS



Notes: Close S3 for positive gain. Input signal to RF(+Av) connector.  
 The gain  $A_v = 1 + R_{FB}/R_{IN}$ .  
 For unity gain, remove  $R_{IN}$  and short  $R_{FB}$ .  
 Open S3 for negative gain. Input signal to RF(-Av) connector.  
 The gain  $A_v = -R_{FB}/R_{IN}$ .  
 S1 and S2 are switches for possible resistor and capacitor load connections.

**Figure 1—AC Test Circuit**

TEST CIRCUITS (continued)

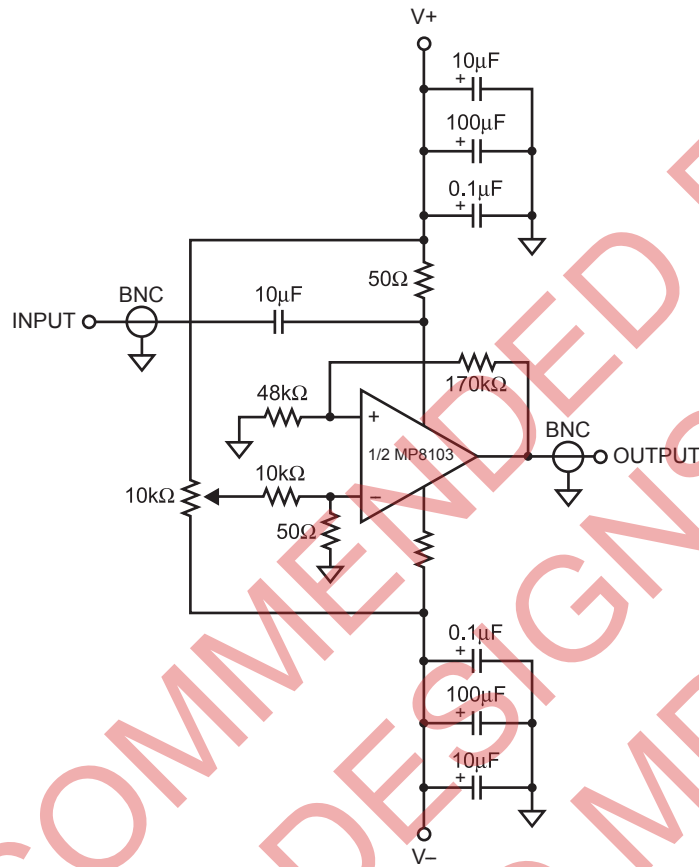
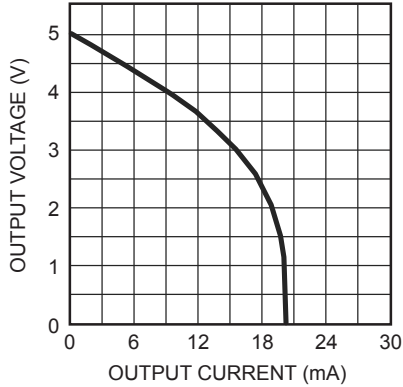


Figure 2—Positive Power Supply Rejection Ratio Measurement

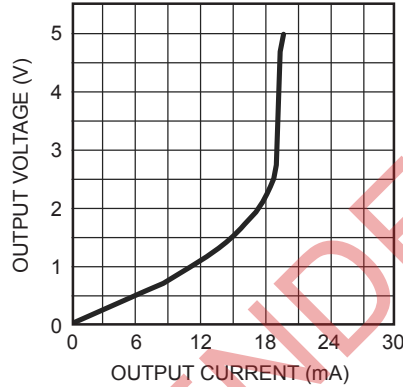
**TYPICAL PERFORMANCE CHARACTERISTICS**

$T_A = +25^\circ\text{C}$ , unless otherwise noted.

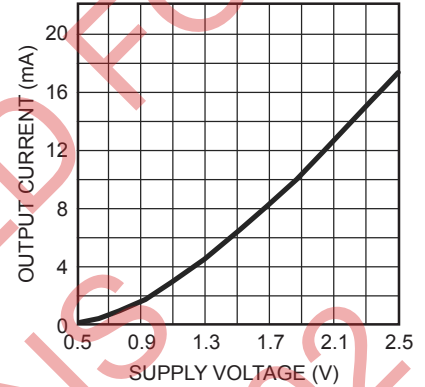
**Output Voltage vs. Output Current**  
Sourcing



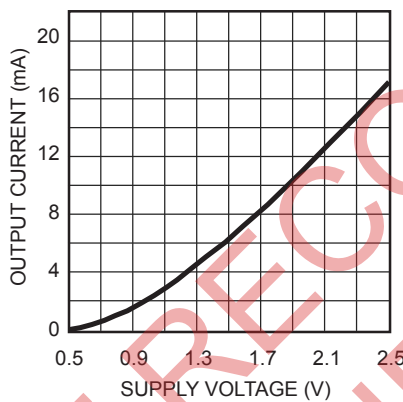
**Output Voltage vs. Output Current**  
Sinking



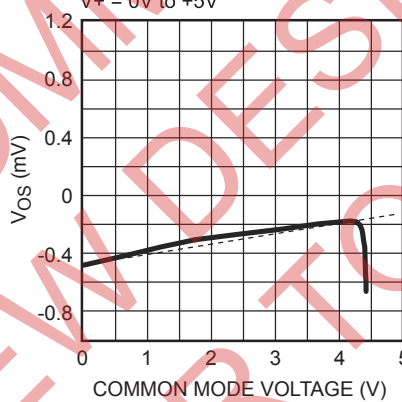
**Short Circuit Current vs Supply Voltage**  
Sourcing



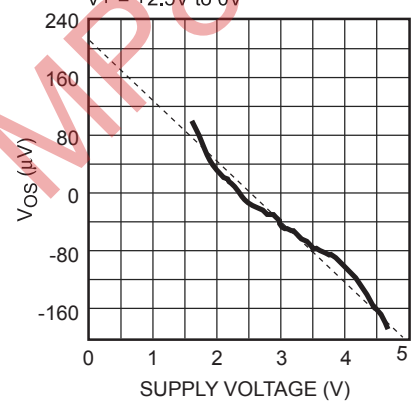
**Short Circuit Current vs Supply Voltage**  
Sinking



**Offset Voltage vs. Common Mode Voltage**  
 $R_{FB} = 50\text{k}\Omega$ ,  $V_- = -5\text{V}$  to  $0\text{V}$ ,  
 $V_+ = 0\text{V}$  to  $+5\text{V}$



**Offset Voltage vs. Supply Voltage**  
 $R_{FB} = 50\text{k}\Omega$ ,  $V_- = -2.5\text{V}$  to  $0\text{V}$ ,  
 $V_+ = +2.5\text{V}$  to  $0\text{V}$

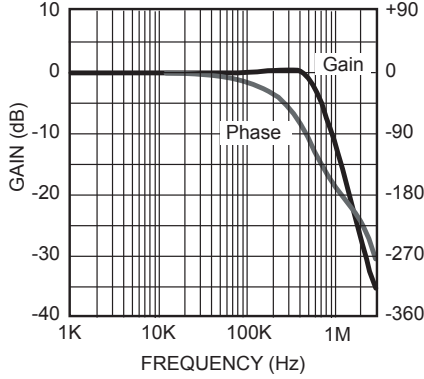


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

$T_A = +25^\circ\text{C}$ , unless otherwise noted.

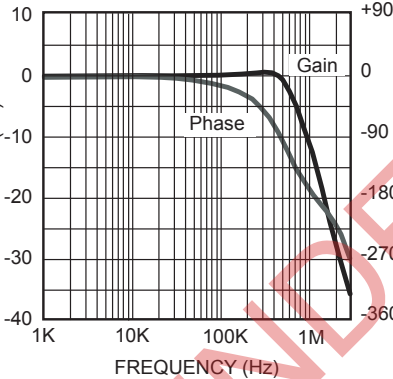
**Gain Bandwidth and Phase Margin**

$V_{+/-} = +/-1.35\text{V}$ , Gain = 1,  $R_L = 1\text{M}\Omega$



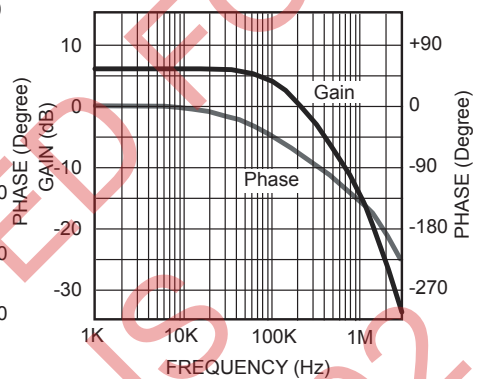
**Gain Bandwidth and Phase Margin**

$V_{+/-} = +/-2.50\text{V}$ , Gain = 1,  $R_L = 1\text{M}\Omega$



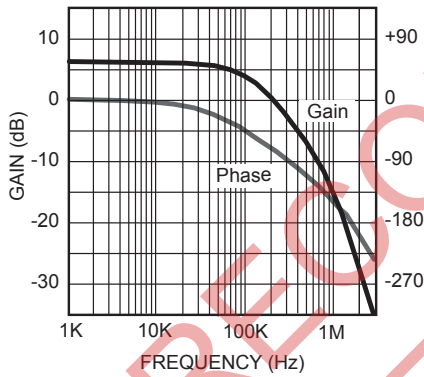
**Gain Bandwidth and Phase Margin**

$V_{+/-} = +/-1.35\text{V}$ , Gain = 2,  $R_L = 1\text{M}\Omega$



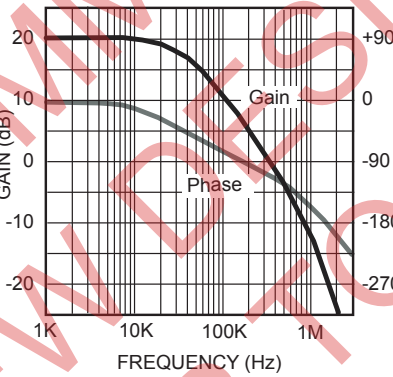
**Gain Bandwidth and Phase Margin**

$V_{+/-} = +/-2.50\text{V}$ , Gain = 2,  $R_L = 1\text{M}\Omega$



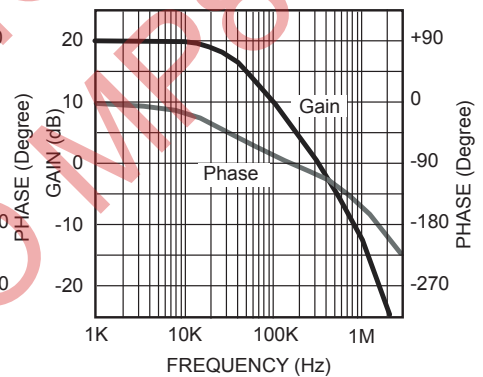
**Gain Bandwidth and Phase Margin**

$V_{+/-} = +/-1.35\text{V}$ , Gain = 10,  $R_L = 1\text{M}\Omega$



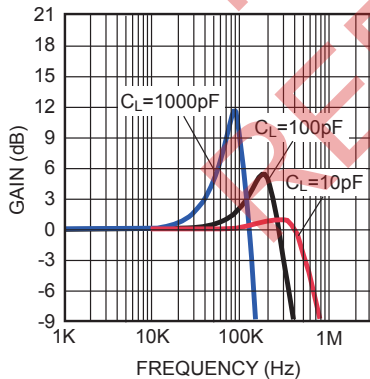
**Gain Bandwidth and Phase Margin**

$V_{+/-} = +/-2.50\text{V}$ , Gain = 10,  $R_L = 1\text{M}\Omega$



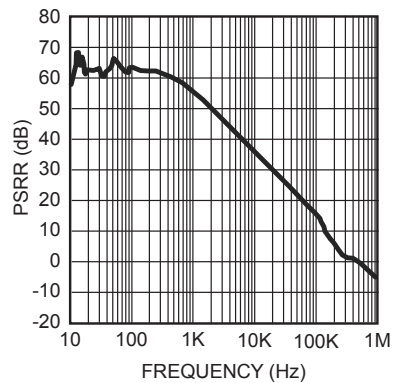
**Close-Loop Unity Gain Frequency Response**

$V_{+/-} = +/-2.50\text{V}$ , Gain = 1



**PSRR vs. Frequency**

$V_- = -2.5\text{V}$ ,  $V_+ = 2.5\text{V}$

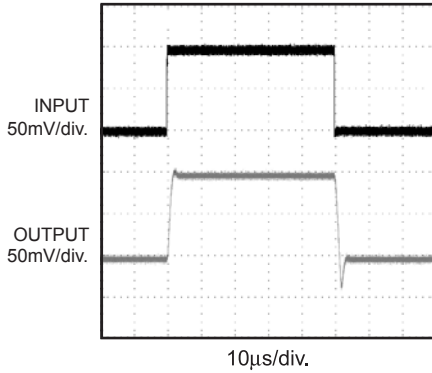


**TYPICAL PERFORMANCE CHARACTERISTICS** *(continued)*

$T_A = +25^\circ\text{C}$ , unless otherwise noted.

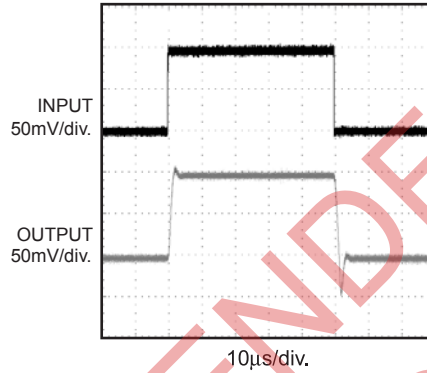
**Small Signal Pulse Response**

$A_V = 1, V_+ = 2.5\text{V}, V_- = -2.5\text{V}$   
 $R_L = 1\text{M}\Omega, C_L = 8\text{pF}$



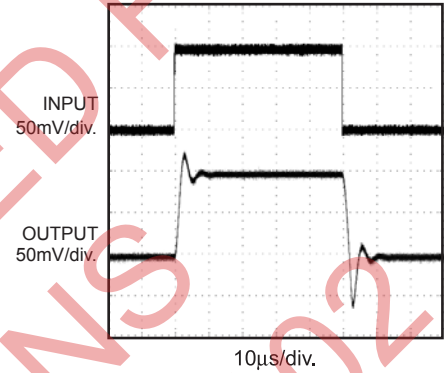
**Small Signal Pulse Response**

$A_V = 1, V_+ = 1.25\text{V}, V_- = -1.25\text{V}$   
 $R_L = 1\text{M}\Omega, C_L = 8\text{pF}$



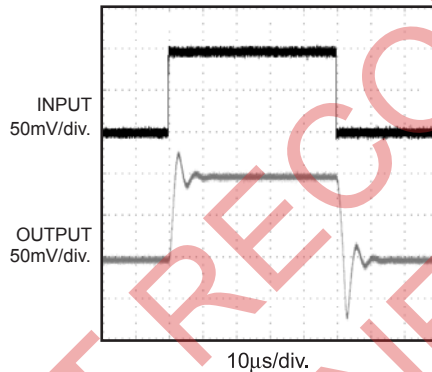
**Small Signal Pulse Response**

$A_V = 1, V_+ = 2.5\text{V}, V_- = -2.5\text{V}$   
 $R_L = 1\text{M}\Omega, C_L = 50\text{pF}$



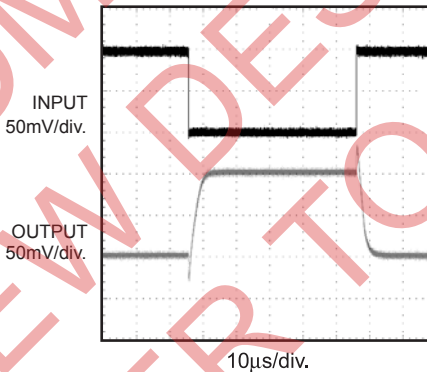
**Small Signal Pulse Response**

$A_V = 1, V_+ = 1.25\text{V}, V_- = -1.25\text{V}$   
 $R_L = 1\text{M}\Omega, C_L = 50\text{pF}$



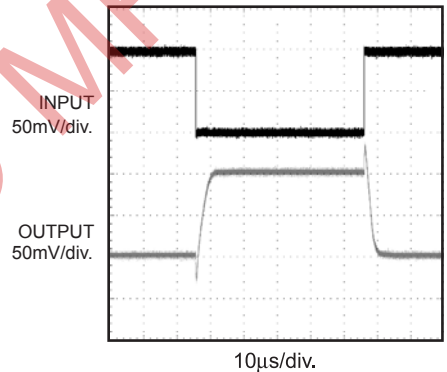
**Small Signal Pulse Response**

$A_V = -1, V_+ = 2.5\text{V}, V_- = -2.5\text{V}$   
 $R_L = 1\text{M}\Omega, C_L = 8\text{pF}$



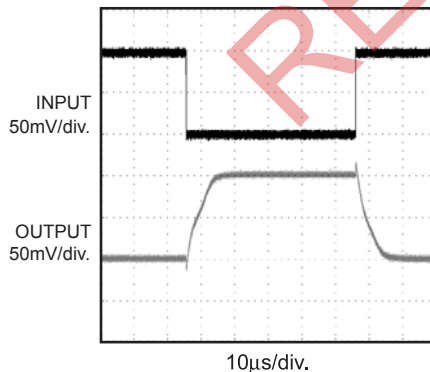
**Small Signal Pulse Response**

$A_V = -1, V_+ = 1.25\text{V}, V_- = -1.25\text{V}$   
 $R_L = 1\text{M}\Omega, C_L = 8\text{pF}$



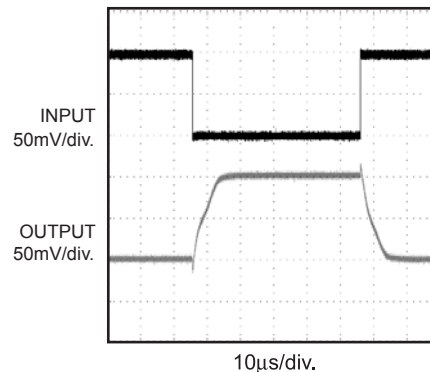
**Small Signal Pulse Response**

$A_V = -1, V_+ = 2.5\text{V}, V_- = -2.5\text{V}$   
 $R_L = 5\text{k}\Omega, C_L = 8\text{pF}$

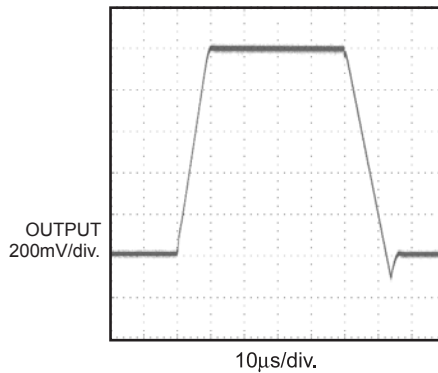
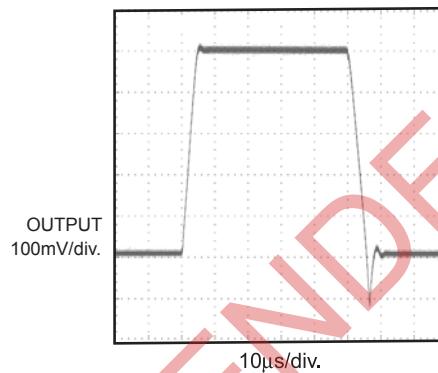
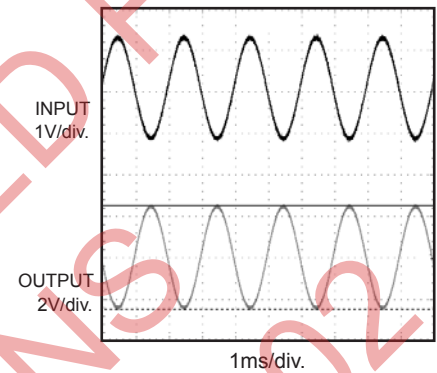
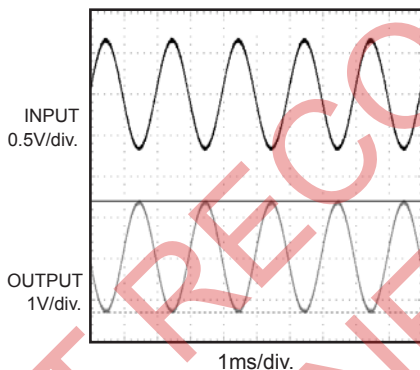
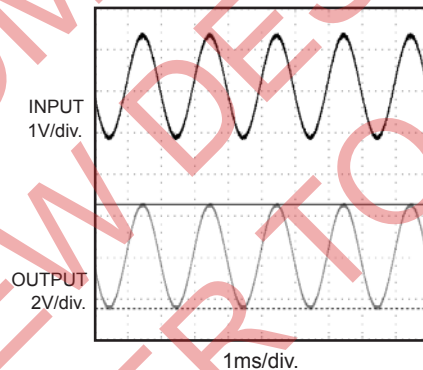
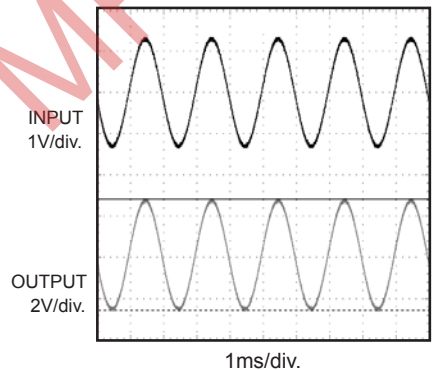


**Small Signal Pulse Response**

$A_V = -1, V_+ = 1.25\text{V}, V_- = -1.25\text{V}$   
 $R_L = 5\text{k}\Omega, C_L = 8\text{pF}$



**TYPICAL PERFORMANCE CHARACTERISTICS** *(continued)*
 $T_A = +25^\circ\text{C}$ , unless otherwise noted.

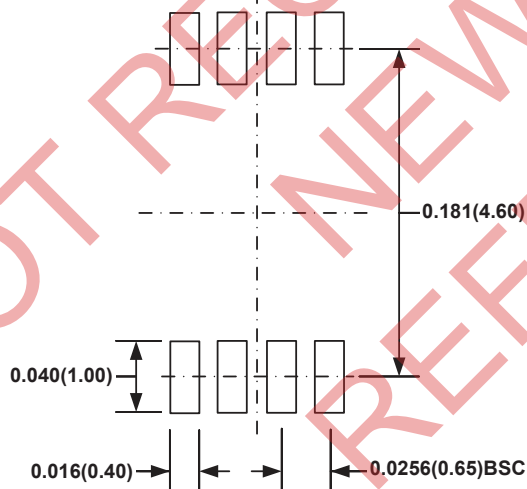
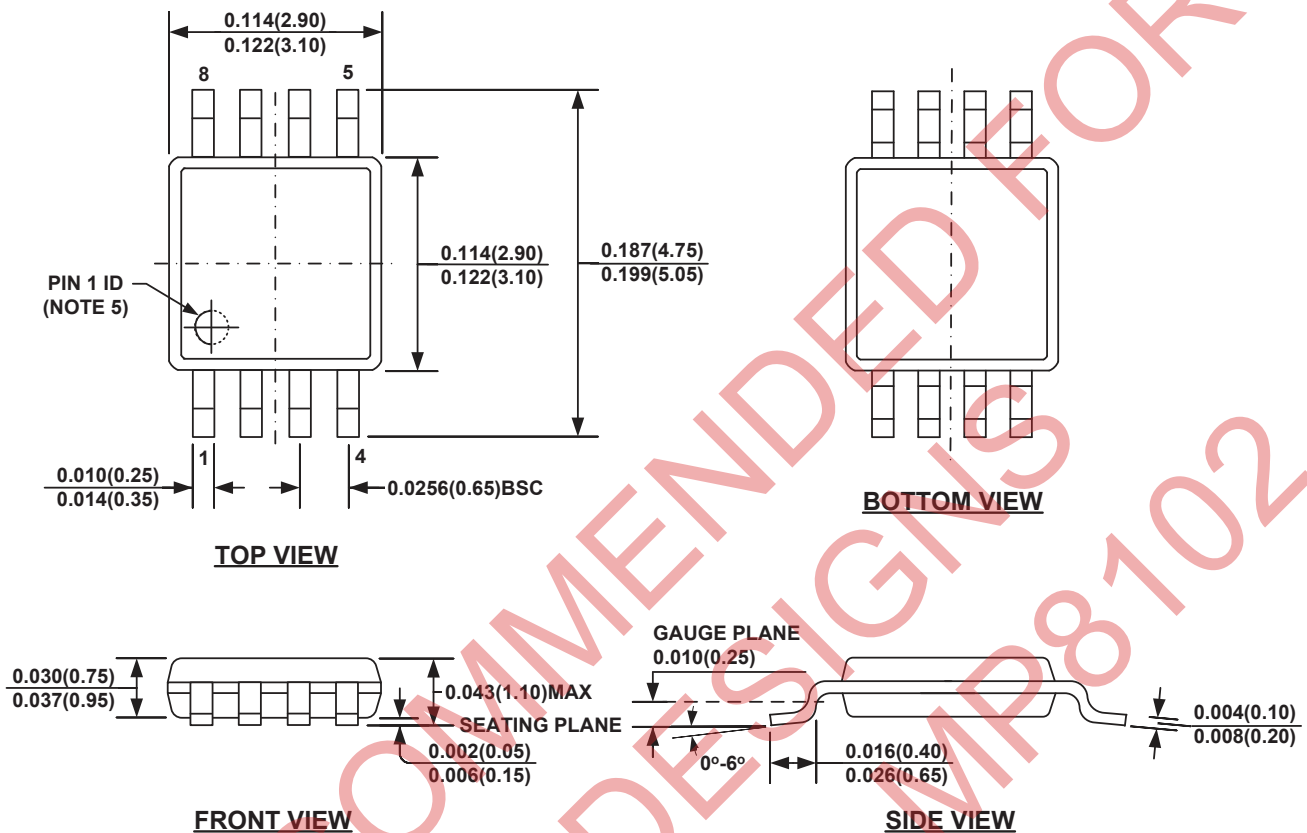
**Large Signal Pulse Response**
 $A_V = 1, V_+ = 2.5\text{V}, V_- = -2.5\text{V}$   
 $R_L = 1\text{M}\Omega, C_L = 8\text{pF}$ 

**Large Signal Pulse Response**
 $A_V = 1, V_+ = 1.25\text{V}, V_- = -1.25\text{V}$   
 $R_L = 1\text{M}\Omega, C_L = 8\text{pF}$ 

**Rail to Rail Output Operation**
 $A_V = -2, V_+ = 2.5\text{V}, V_- = -2.5\text{V}$   
 $R_L = 1\text{M}\Omega, C_L = 8\text{pF}$ 

**Rail to Rail Output Operation**
 $A_V = -2, V_+ = 1.25\text{V}, V_- = -1.25\text{V}$   
 $R_L = 1\text{M}\Omega, C_L = 8\text{pF}$ 

**Rail to Rail Output Operation**
 $A_V = 2, V_+ = 2.5\text{V}, V_- = -2.5\text{V}$   
 $R_L = 1\text{M}\Omega, C_L = 8\text{pF}$ 

**Rail to Rail Output Operation**
 $A_V = 2, V_+ = 1.25\text{V}, V_- = -1.25\text{V}$   
 $R_L = 1\text{M}\Omega, C_L = 8\text{pF}$ 

**APPLICATION INFORMATION**
**Power Supply Bypassing**

Regular supply bypassing techniques are recommended. A  $10\mu\text{F}$  capacitor in parallel with a  $0.1\mu\text{F}$  capacitor on both the positive and negative supplies is ideal. For the best performance, all bypassing capacitors should be located as close to the op amp as possible and all capacitors should be low ESL (Equivalent Series Inductance) and low ESR (Equivalent Series Resistance). Surface mount ceramic capacitors are ideal.



## PACKAGE INFORMATION

### MSOP8



#### NOTE:

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) PIN 1 IDENTIFICATION HAS HALF OR FULL CIRCLE OPTION.
- 6) DRAWING MEETS JEDEC MO-187, VARIATION AA.
- 7) DRAWING IS NOT TO SCALE.

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