MP8044

22V, 4A Dual Channel Power Half-Bridge

The Future of Analog IC Technology

DESCRIPTION

The MP8044 is a dual channel power half bridge that can be configured as the output stage of a Class-D audio amplifier. Each channel can be driven independently as stereo single ended audio amplifiers or driven complementary in a bridge tied load (BTL) audio amplifier configuration.

The MP8044 features a low current shutdown mode, standby mode, input under voltage protection, current limit, thermal shutdown and fault flag signal output. Both channels of drivers interface with standard logic signals.

The MP8044 is available in a 20-pin TSSOP package with exposed pad.

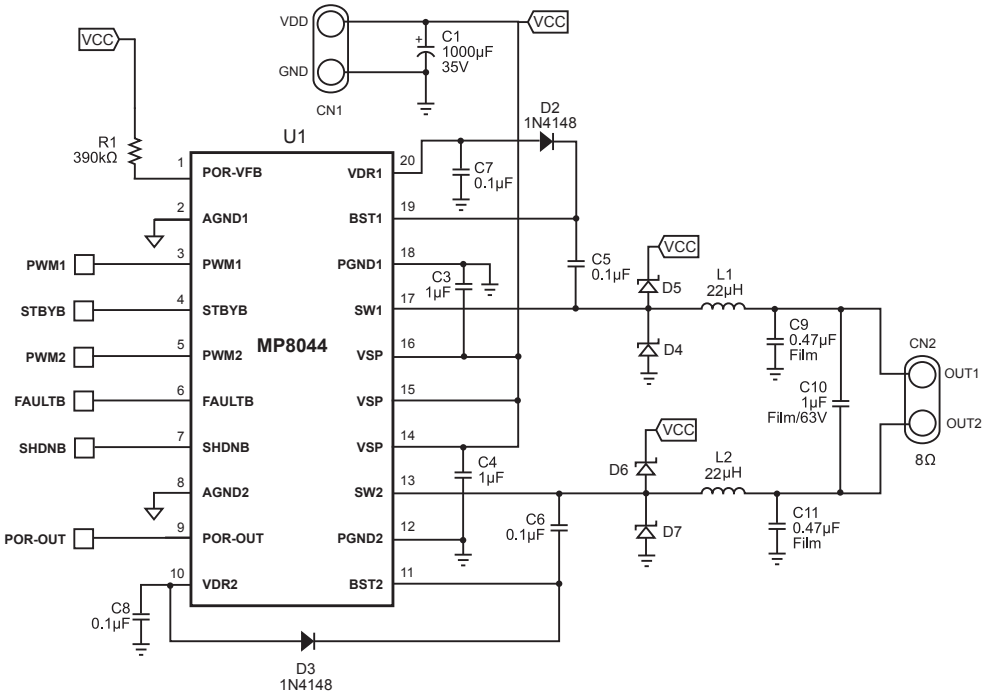
FEATURES

- 4A Peak Current Output
- Up to 600kHz Switching Frequency
- Protected Integrated Power 0.2Ω Switches
- 30ns Switch Dead Time
- All Switches Current Limited
- Internal Under Voltage Protection
- Internal Thermal Protection
- 2.1mA Operating Current
- Fault Output Flag
- Stereo Single Ended Output Power: 8W/Channel at 22V, 8Ω Load
- Bridge Tied Load Output Power: 30W at 22V, 8Ω Load

APPLICATIONS

- Class D Audio Drivers
- Motor Drivers

TYPICAL APPLICATION

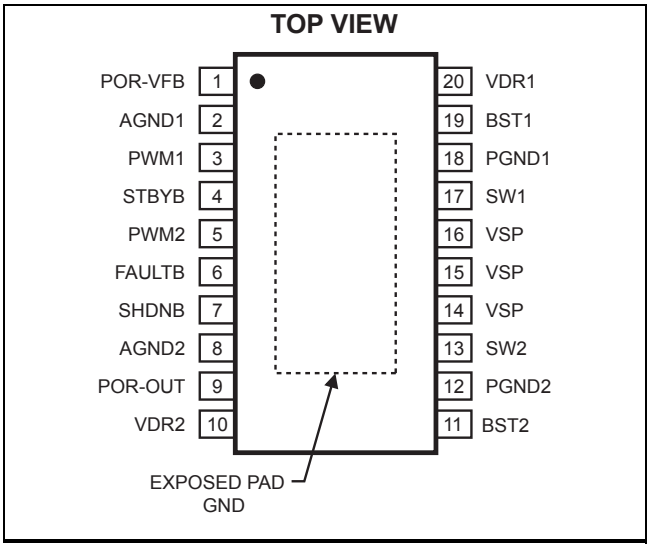


ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
MP8044DF	TSSOP20F	MP8044DF	–40°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP8044DF–Z). For Lead Free, add suffix –LF (e.g. MP8044DF–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

VSP Supply Voltage 24V
SW1/2 Pin Voltage..... –0.3V to V_{SP} + 0.3V
SW1/2 to BST1/2 .....–0.3V to +6V
Voltage at All Other Pins.....–0.3V to +6V
Continuous Power Dissipation (T_A = +25°C) (2)
……...3.1W
Storage Temperature..... –55°C to +150°C
Junction Temperature.....150°C
Lead Temperature .....260°C

Recommended Operating Conditions (3)

VSP Supply Voltage .....7.5V to 22V
Peak Output Current.....4A Maximum
Operating Junct. Temp (T_J) .....-40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TSSOP20F .....40 ..... 6.... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{SP} = 12V, V_{SHDNB} = 5V, T_A = +25°C, unless otherwise specified.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VSP Operating Current		I_{LOAD} = 0A， PWM1,2=0		2.1	2.5	mA
VSP Shutdown Current		V_{SHDN} = 0V		1.0	10	μA
Operating VSP Threshold Low			4.8	5.3		V
Operating VSP Threshold High				6.5	7.2	V
STBYB Threshold Low			0.9	1.1		V
STBYB Threshold High				1.9	2.2	V
PWM Input Bias Current				0.1	1.0	μA
SHDNB Threshold Low			0.9	1.1		V
SHDNB Threshold High				1.9	2.2	V
PWM1,2 Threshold Low			0.9	1.4		V
PWM1,2 Threshold High				1.8	2.2	V
POR-VFB Threshold High				1.25		V
POR-VFB hysteresis		R_{EXT}=50kΩ		104		mV
$V_{POR-OUT}$		$V_{POR-VFB}$ =0V		3.3		V
$V_{POR-OUT}$		$V_{POR-VFB}$ =2V		0.5		V
SW1/2 On Resistance		V_{SP} = 7.5V, High-Side and Low-Side		0.2		Ω
SW1/2 Current Limit (5)		V_{PWM} = 0V, Sinking		4		A
		V_{PWM} = 5V, Sourcing		4		A
SW1/2 Switching Frequency		V_{PWM} = 0 to 5V, 50% Duty Cycle			0.6	MHz
SW1/2 Maximum Duty Cycle (6)		V_{SP} = 7.5V, V_{PWM} = 5V, C_{BST} = 100nF, f_{SW} = 3.3kHz		99.5		%
SW1/2 Rise/Fall Time		V_{PWM} = 0V to 5V		10		ns
PWM Pulse Width		V_{PWM} = 0V to 5V, High or Low Pulse		200		ns
Dead Time (5)		I_{OUT}= ±100mA		30		ns
PWM1,2 to SW1,2 Delay Time Rising		V_{PWM} = 0V to 5V		40		ns
PWM1,2 to SW1,2 Delay Time Falling		V_{PWM} = 5V to 0V		40		ns
Thermal Shutdown Temperature (5)		T_J Rising, Hysteresis = 20°C		150		°C

Notes:

5) Not production tested.

6) OUT drives low for 1.5μs every 300μs to charge the BST to SW capacitor.

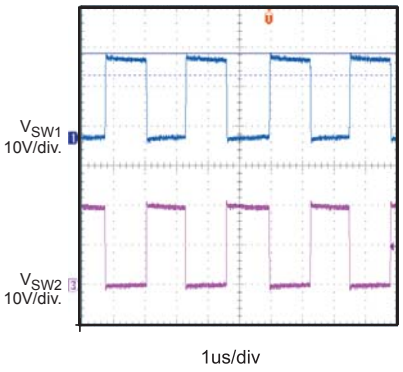
PIN FUNCTIONS

Pin #	Name	Description
1	POR-VFB	Feedback Point for Power-On-Reset Comparator. An external resistor is connected between the supply to be monitored and this pin.
2	AGND1	Analog Ground 1.
3	PWM1	Driver Logic Input 1. Drive PWM1 with the signal that controls the MP8044 SW1. Drive PWM high to turn on the high side switch; drive PWM low to turn on the low-side switch.
4	STBYB	Standby Input. Default low (internal pull-down). If driven high, the output of the drivers is determined by the PWM1/2. If driven low, the output of both drivers is high impedance.
5	PWM2	Driver Logic Input 2. Drive PWM2 with the signal that controls the MP8044 SW2. Drive PWM high to turn on the high side switch; drive PWM low to turn on the low-side switch
6	FAULTB	Fault Output. A low output at FAULTB indicates that the MP8044 has detected an over temperature or over current condition. This output is open drain.
7	SHDNB	Shutdown Input. When low, the IC will be shut off.
8	AGND2	Analog Ground 2.
9	POR-OUT	Output of the Power-On-Reset. A high indicates the voltage at POR_VFB is lower than 1.25V.
10	VDR2	Gate Drive Supply Bypass. The voltage at VDR2 is supplied from an internal regulator from its respective VSP. VDR2 powers the internal circuitry and internal MOSFET gate drive for its respective SW2 stage. Bypass VDR2 to PGND with a 0.1µF to 10µF capacitor.
11	BST2	Bootstrap Supply. BST2 powers the high-side gate of the SW2 stage. Connect a 0.1µF or greater capacitor between BST2 and SW2.
12	PGND2	Power Ground of channel 2. Connect the exposed pad on bottom side to the ground plane.
13	SW2	Switched Output 2. Connect the output LC filter to SW2. SW2 is valid approximately 100µs after VSP goes high.
14,15, 16	VSP	Power Supply Input. Connect VSP to the positive side of the input power supply. Bypass VSP to PGND as close to the IC as possible.
17	SW1	Switched Output 1. Connect the output LC filter to SW1. SW1 is valid approximately 100µs after VSP goes high.
18	PGND1	Power Ground of Channel 1. Connect the exposed pad on bottom side to the ground plane.
19	BST1	Bootstrap Supply. BST1 powers the high-side gate of the SW1 stage. Connect a 0.1µF or greater capacitor between BST1 and SW1.
20	VDR1	Gate Drive Supply Bypass. The voltage at VDR1 is supplied from an internal regulator from its respective VSP. VDR1 powers the internal circuitry and internal MOSFET gate drive for its respective SW1 stage. Bypass VDR1 to PGND with a 0.1µF to 10µF capacitor.

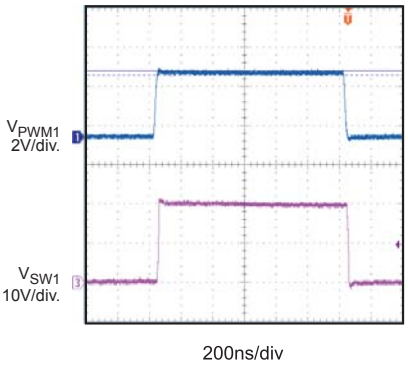
TYPICAL PERFORMANCE CHARACTERISTICS

V_{SP} = 20V, V_{SHDNB} = 5V, R_{LOAD} = 8Ω, T_A = +25°C, unless otherwise noted.

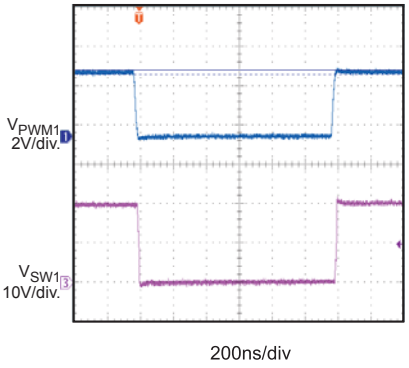
Normal Switch Waveform



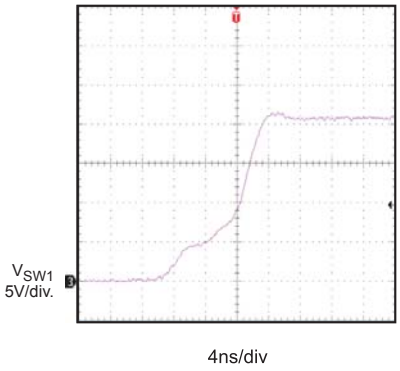
Input/Output Waveform Positive Pulse



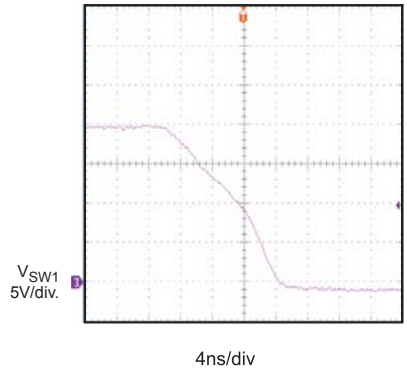
Input/Output Waveform Negative Pulse



Output Rise-Time

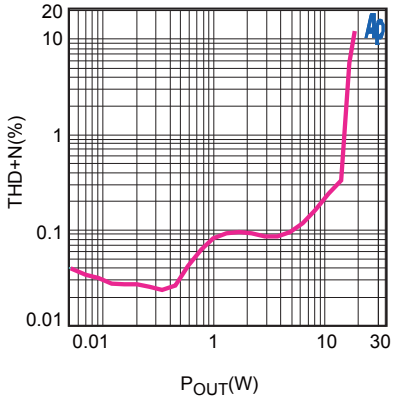


Output Fall-Time



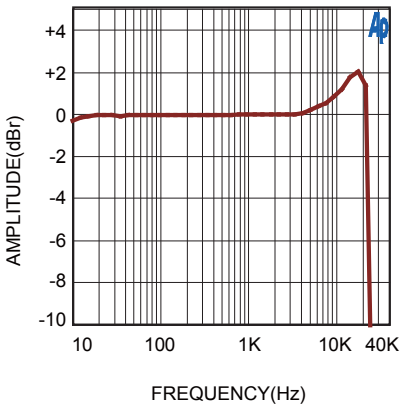
THD+N vs. P_{OUT}

20V, 8Ω, 1kHz

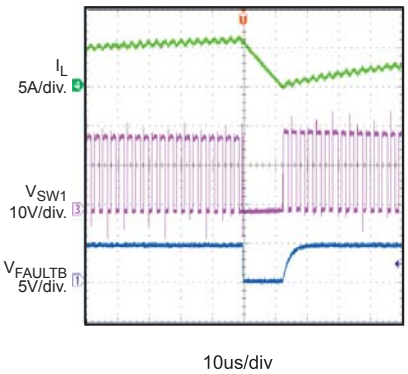


Frequency Response

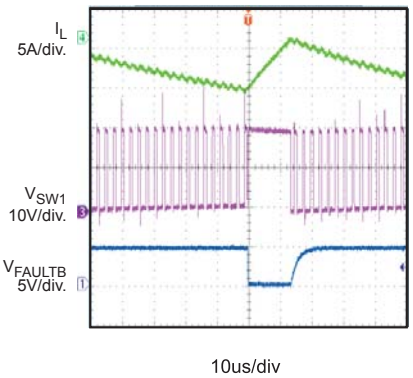
20V, 8Ω, 1W



Short Circuit Positive Current



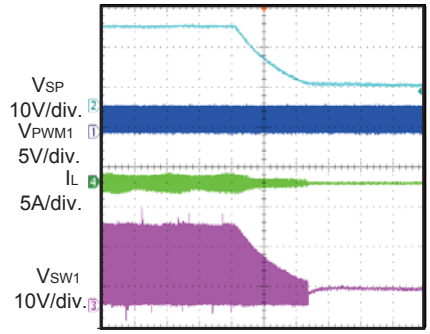
Short Circuit Negative Current



TYPICAL PERFORMANCE CHARACTERISTICS (*continued*)

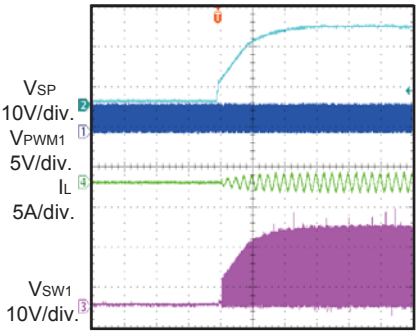
V_{SP} = 20V, V_{SHDNB} = 5V, R_{LOAD} = 8Ω, T_A = +25ºC, unless otherwise noted.

Power off



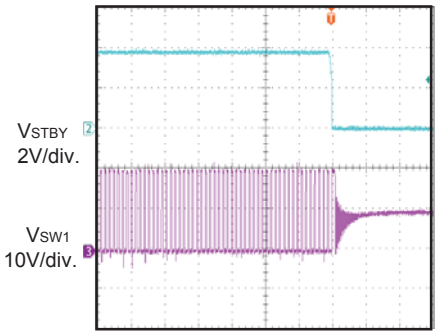
100ms/div

Power on



4ms/div

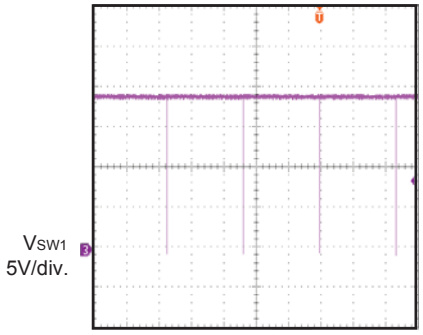
Standby



20µs/div

BS Recharge Cycling

20V, R_L=16Ω



1ms/div

OPERATION

The MP8044 is a high voltage, dual channel power half-bridge driver that can be configured as the output of a Class D amplifier. The output is in phase with the input and the dead time is optimized for symmetrical performance, regardless of load conditions.

When the shutdown (SHDNB) pin is low, both channels 1 and 2 will be off. When the standby (STBYB) is pulled low, it causes the outputs of both channels to go into high impedance. However, when the voltage across the BST1/2 and SW1/2 pins drops sufficiently low, the bottom MOSFET will be turned on to refresh the external bootstrap capacitor. For a bootstrap capacitor of 100nF, the refresh time is approximately 300ns.

In order to prevent erratic operation, two under voltage lockout (UVLO) circuits are used. One of them is to ensure that the supply for the bottom gate drive circuit is sufficiently high and the other is for the top gate driver.

Voltage Monitoring

The MP8044 contains a hysteretic comparator that can easily be used for supply voltage monitoring (see block diagram). The user can connect a resistor from the supply that is to be monitored to the POR_VFB pin. The trip point is given by:

$$V_{TRIP} = 1.25x \frac{55k + R_{EXT}}{55k}$$

The hysteresis is given by:

$$V_{HYS} = (2.27E - 6)xR_{EXT}$$

When the V_{FB}_POR voltage is greater than 1.25V, the POR_OUT is low. The voltage swing on the POR_VFB pin is approximately from 0.2V to 4.5V. Do not apply more than 6V to the POR_VFB.

Fault Protection

To protect the power MOSFETs, an internal current limit of 4A is set for all MOSFETs. When this limit is reached, all MOSFETs will go into high impedance for a fixed duration of approximately 8us before resuming normal operation.

However, in certain conditions, when the current through the upper MOSFET exceeds 4A, all MOSFETs will go into high impedance but normal operation will only resume if the inductor current has been reset to close to zero.

To enhance the robustness of the device under short circuit condition, a capacitor can be connected to the FaultB pin, as shown in figure 1. The time constant of the RC is selected to be greater than 50ms for the FaultB node to reach 1V. Under short circuit condition, the FaultB node will be reset to zero and the part will be place in standby mode until the voltage at the STBYB pin is above 1V.

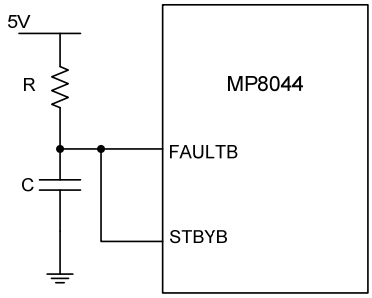


Figure 1— Fault Protection Circuit

Fault Output

The MP8044 includes an open drain, active low fault indicator output (FAULTB). A fault will be indicated if the current limit is tripped or the thermal shutdown is tripped.

A fault on any channel will cause the FAULTB pin to be pulled low. A fault on either channel will cause the outputs (SW1, SW2) to go into high impedance. When the fault goes away, the MP8044 will resume normal operation.

Do not apply more than 6V to the FAULTB pin.

BLOCK DIAGRAM

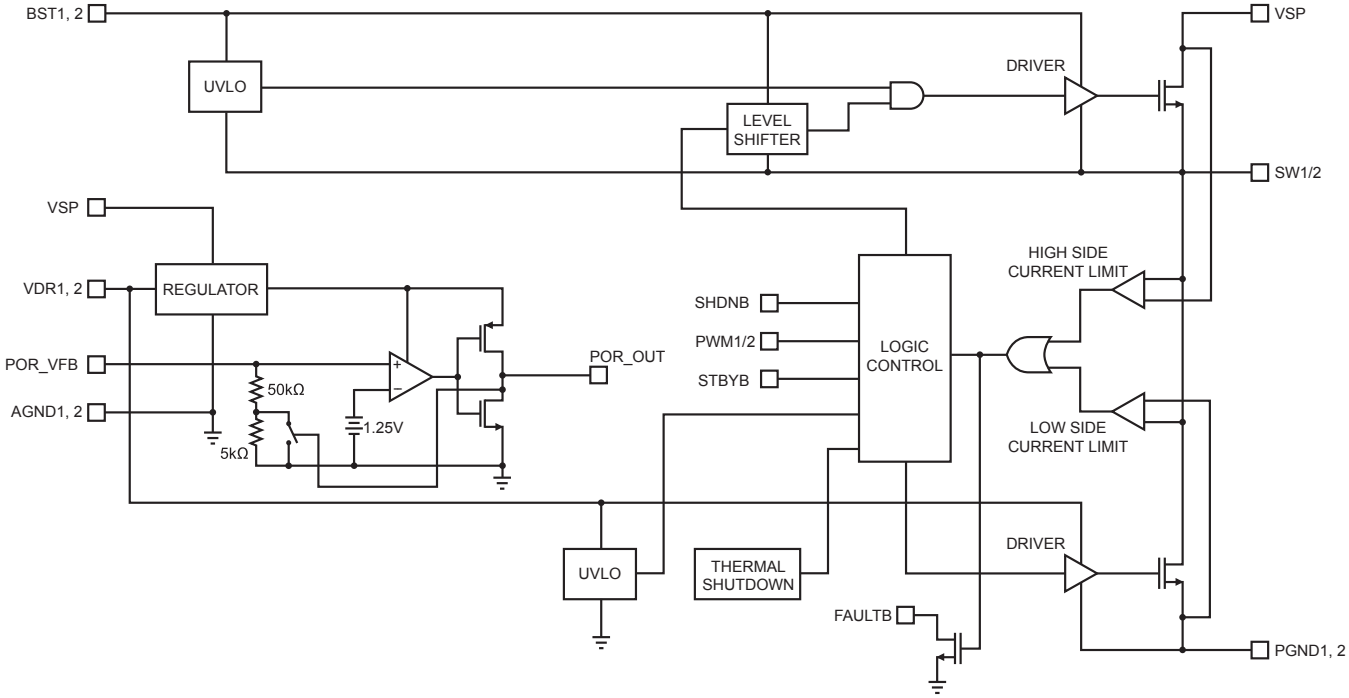
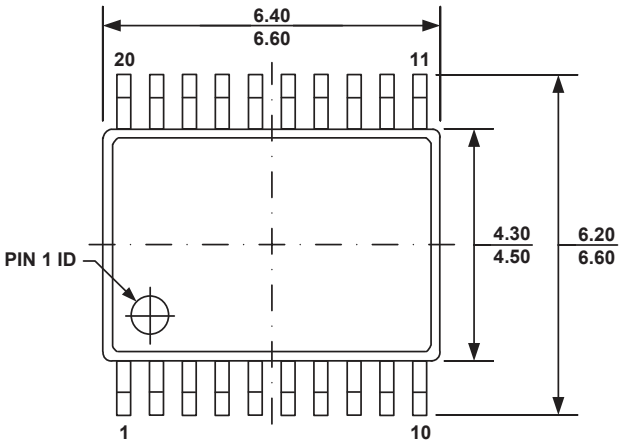


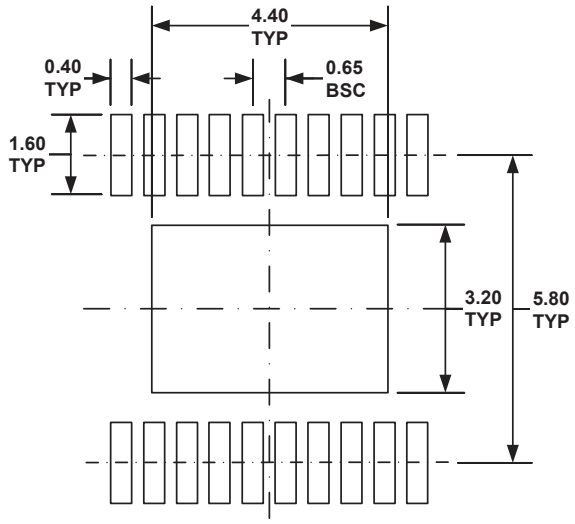
Figure 2—Function Block Diagram (1 channel only)

PACKAGE INFORMATION

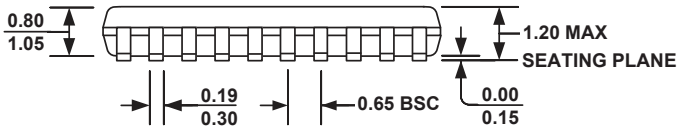
TSSOP20F
(EXPOSED PAD)



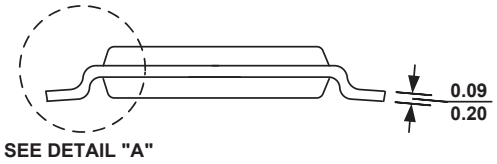
TOP VIEW



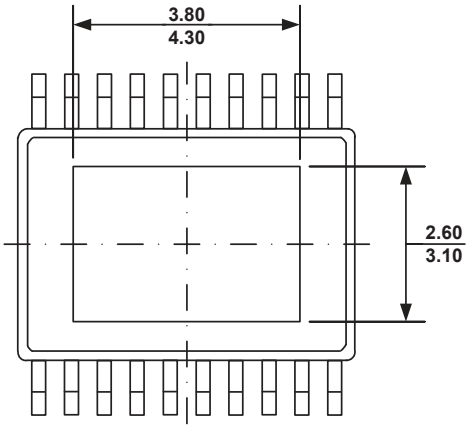
RECOMMENDED LAND PATTERN



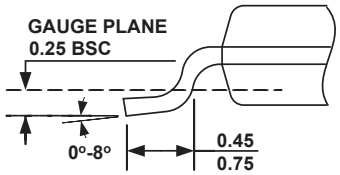
FRONT VIEW



SIDE VIEW



BOTTOM VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION ACT.
6) DRAWING IS NOT TO SCALE.