MP8030

Fully Integrated, 802.3af/at/bt-Compliant PoE PD Interface with High-Efficiency Flyback/Forward Controller

DESCRIPTION

The MP8030 is a fully integrated, IEEE 802.3af/at/bt-compliant, Power over Ethernet (PoE), powered device (PD) power supply converter. The device features a PD interface and a high-efficiency flyback/forward controller.

The PD interface has all the functions of IEEE 802.3af/at/bt. It also integrates a 100V hot-swap MOSFET for ≤51W applications and one GATE1 driver to enhance efficiency for high-power applications (>51W). The GATE2 driver supports an external, low on resistance N-channel MOSFET to prevent high power loss when the device is powered by an adapter.

The flyback/forward controller is specifically designed for primary-side regulation (PSR) flyback applications, as well as secondary-side regulation (SSR) active-clamp forward applications. It also can be used in an SSR flyback topology.

The MP8030 features overload protection (OLP) with hiccup mode, short-circuit protection (SCP), over-voltage protection (OVP), and thermal shutdown.

The MP8030 is available in a QFN-32 (5mmx6mm) package.

FEATURES

- Compliant with 802.3af/at/bt Specifications
- Internal Hot-Swap MOSFET for ≤51W Designs
- External FET with GATE1 for >51W Designs
- GATE2 N-Channel MOSFET Driver for Adapter Supply
- Supports Automatic Classification
- Automatic Maintain Power Signature Function
- Supports Flexible Topologies with DC/DC Design:
  - Primary-Side Regulation (PSR) for Flyback Applications
  - Secondary-Side Regulation (SSR) for Flyback Applications
  - SSR for Active-Clamp Forward Applications
- EMI Reduction with Frequency Dithering
- Accurate Over-Voltage Protection (OVP) for Active-Clamp Forward without Isolated Sensing Based on the Appropriate MOSFET Q_G Selection (1)
- Ethernet Alliance (EA Gen 2) Certified
- Available in a QFN-32 (5mmx6mm) Package

MPL Optimized Performance with MPS Inductor MPL-AY Series

APPLICATIONS

- IEEE 802.3af/at/bt-Compliant Devices
- Security Cameras
- Video and VoIP Phones
- WLAN Access Points
- Internet of Things (IoT) Devices
- Pico Base Stations

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Note:

1) A minimum Q_G > 17.5nC N-channel MOSFET and minimum Q_G > 5nC P-channel MOSFET are necessary in reference designs. For more details, see the OVP Design for Active-Clamp Forward section on page 37.

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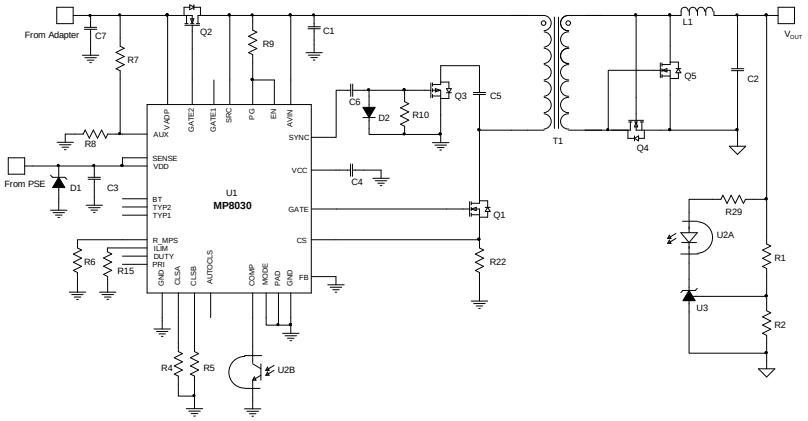
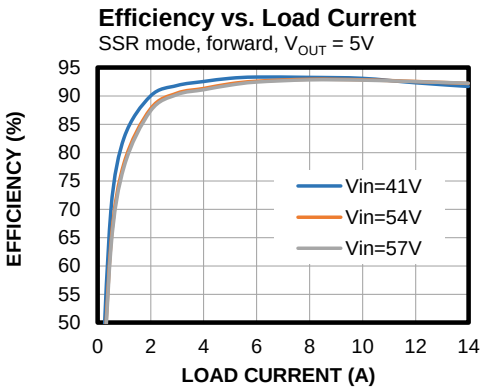
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP8030GQJ	QFN-32 (5mmx6mm)	*See Below*	2

* For Tape & Reel, add suffix -Z (e.g. MP8030GQJ-Z).

TOP MARKING

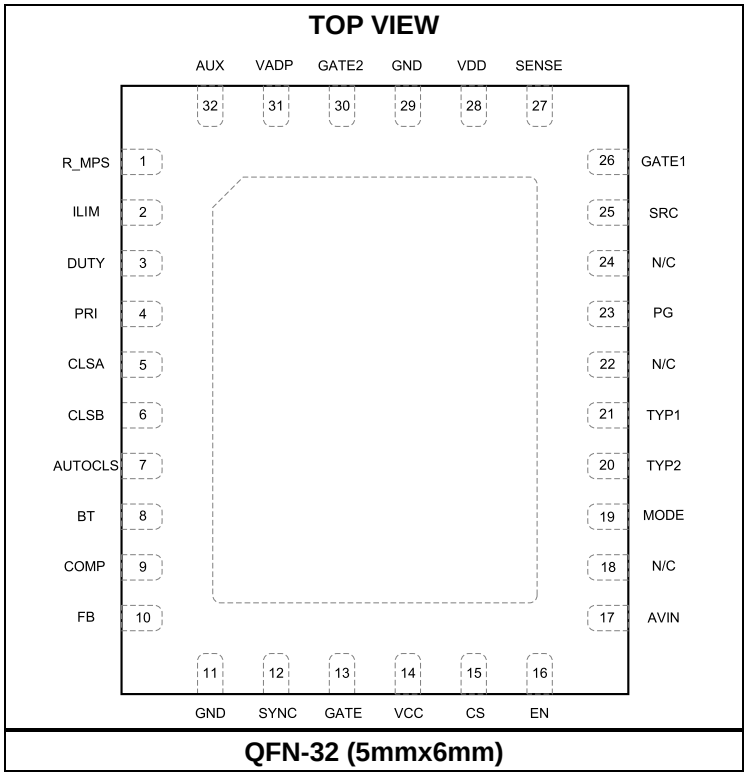
MPSYYWW

MP8030

LLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP8030: Part number
LLLLLLL: Lot number

PACKAGE REFERENCE



QFN-32 (5mmx6mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	R_MPS	**Automatically maintains power signature load resistor connection**. The R_MPS pin generates a 24V output pulse when the maintain power signature function is triggered.
2	ILIM	**PD internal hot-swap MOSFET current limit configuration**. See the Hot-Swap MOSFET and Current Limit section on page 26 for more details.
3	DUTY	**Automatic maintain power signature output duty setting pin.** See the Automatic Maintain Power Signature Function section on page 28 for more details.
4	PRI	**PSE power and adapter power priority setting pin**. Internally pull PRI up to the internal 5V power source through a 1MΩ resistor. The PSE power has a higher priority when PRI is low.
5	CLSA	**Power class signature pin.** CLSA is used during the first two class events.
6	CLSB	**Power class signature pin.** CLSB is used during the third class event and all subsequent class events.
7	AUTOCLS	**Auto-class function enable pin**. Pull AUTOCLS low to enable the auto-class function.
8	BT	**PSE type indicator.** BT is an open-drain output.
9	COMP	**DC/DC controller loop compensation pin**. COMP is the error amplifier (EA) output in PSR mode. COMP is internally pulled to 5V through a 10kΩ resistor in secondary-side regulation (SSR) mode.
10	FB	**DC/DC controller output voltage feedback pin.** Connect one resistor divider from FB to the sensing winding to regulate the output voltage in PSR mode. In SSR mode, the internal EA is disabled. FB is only used to provide over-voltage protection (OVP). OVP can be disabled by connecting the FB pin to GND in SSR mode. For information regarding when OVP is enabled to sense the VCC voltage (V_{CC}) during SSR active-clamp forward, see the OVP Design for Active-Clamp Forward section on page 37.
11, 29	GND	**PD and DC/DC controller power ground.** Pin 11 (GND) is the DC/DC controller's ground, and it is the GATE and SYNC drivers' return pin. Place the components related to the DC/DC controller close to pin 11. Pin 29 (GND) is the PD interface's ground. Place the components related to the PD close to pin 29. Connect pin 11 and pin 29 in the PCB. It is recommended to use an exposed thermal pad for thermal dissipation.
12	SYNC	**The DC/DC controller's synchronous MOSFET gate driver pin.** MOSFET selection when the MP8030 is being used as a forward controller is limited by its minimum gate charge (Q_G). For information regarding the MP8030 being designed as an active-clamp-forward circuit, see the OVP Design for Active-Clamp Forward section on page 37.
13	GATE	**The DC/DC controller's main MOSFET gate driver pin.** MOSFET selection when the MP8030 is being used as a forward controller is limited by its minimum Q_G. For information regarding the MP8030 being designed as an active-clamp-forward circuit, see the OVP Design for Active-Clamp Forward section on page 37.
14	VCC	**DC/DC controller internal circuit supply pin.** VCC is powered through the internal LDO from AVIN. Connect a capacitor between this pin and GND to bypass the internal regulator. The VCC capacitor must be at minimum 1µF for flyback applications and at minimum 4.7µF for forward applications. VCC also can be powered from an external power source to reduce internal LDO loss.
15	CS	**DC/DC controller current sense**, **PSR V_{OUT} compensation, and frequency dither setting pin.** See the Frequency Dithering section on page 32 and the Output Voltage Compensation section on page 31 for more details.
16	EN	**DC/DC controller on/off control pin.** EN is internally connected to GND through a 2.5MΩ resistor.
17	AVIN	**DC/DC controller input power supply pin.** Connect a bypass capacitor from the AVIN pin to GND. Connect AVIN to the SRC pin in application.

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PIN FUNCTIONS *(continued)*

Pin #	Name	Description
18, 22, 24	NC	**No connection**. It is recommended to connect these pins to the GND pin.
19	MODE	**DC/DC controller PSR/SSR mode and dead-time setting pin.** See the Work Mode Detection section on page 30 for more details.
20	TYP2	**Allocated PSE power type indicator.** TYP2 is an open-drain output.
21	TYP1	**Allocated PSE power type indicator.** TYP1 is an open-drain output.
23	PG	**PD power good indicator.** Open-drain output, active high. PG enables the DC/DC controller.
25	SRC	**PD hot-swap MOSFET source pin.** It is the power output from the both internal and external hot-swap MOSFETs. Connect AVIN and the DC/DC power input to the SRC pin.
26	GATE1	**PD GATE driver of the external, parallel N-channel MOSFET for the PSE power supply.**
27	SENSE	**PD external MOSFET current-sense pin.** Connect SENSE to VDD if this pin is not used.
28	VDD	**Positive power supply terminal from the PoE input power rail.**
30	GATE2	**PD GATE driver of the external N-channel MOSFET for the adapter power supply.**
31	VADP	**Positive power supply terminal from the adapter.**
32	AUX	**Auxiliary power input detector pin.** Use AUX to configure the adapter's auxiliary power under-voltage lockout (UVLO) threshold. AUX is internally pulled down to GND through a 2MΩ resistor. It is recommended to externally pull AUX to GND if this pin is not used.

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ABSOLUTE MAXIMUM RATINGS (2)

VDD, SENSE, SRC, TYP1, TYP2, PG, AUX, VADP, BT, AVIN .....-0.3V to +100V
R_MPS .....-0.3V to +30V
VCC, GATE, SYNC.....-0.3V to +18V
GATE1 to SRC .....-0.3V to +6.5V
GATE2 to VADP .....-0.3V to +6.5V
SENSE to VDD .....-6.5V to +0.3V
FB .....-0.5V to +6.5V (3)
All other pins .....-0.3V to +6.5V
PG, TYP1, TYP2, BT sinking current..... 5mA
EN sinking current 0.5mA (4)
FB sinking current..... ±2mA (3)
Continuous power dissipation (T_A = 25°C) (5)
QFN-32 (5mmx6mm)..... 3.9W (6)
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -55°C to +150°C

Recommended Operating Conditions (7)

Supply voltage (V_{DD}) .....0V to 57V
Adapter supply voltage (V_{ADP}).....0V to 57V
VCC, GATE, SYNC voltage..... 16V
PG, TYP1, TYP2, BT max sink current..... 3mA
EN maximum sink curent..... 0.4mA (4)
FB maximum sink current……..... ±1mA (3)
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-32 (5mmx6mm)			
EVL8030-QJ-00A (6)	32	2	°C/W
JESD51-7 (8)	26	1	°C/W

Notes:

2) Exceeding these ratings may damage the device.
3) FB is clamped by an internal circuit. The sink/source current should be limited. See the Output Voltage Setting section on page 36 for more details.
4) If EN is pulled above 6.5V externally, the pull-up current should be limited. Refer to Enable Control (EN) section on page 29 for more details.
5) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
6) Measured on EVL8030-QJ-00A, 4-layer, 1oz thick Cu, 160mmx55mm PCB.
7) The device is not guaranteed to function outside of its operating conditions.
8) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

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ELECTRICAL CHARACTERISTICS

PD interface section, V_{DD} = 54V, SRC and AVIN are connected together, T_J = -40°C to +125°C [9], typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Detection						
Detection on	V_{DET-ON}	V_{DD} rising		1	1.4	V
Detection off	$V_{DET-OFF}$	V_{DD} rising	10.1	11		V
Bias current	I_{BIAS}	V_{DD} = 10.1V, not in mark event, measure I_{SUPPLY}			12	µA
Detection resistance	R_{DET}	V_{DD} = 1.5V to 10.1V, calculate with ΔV / ΔI	24.1	25	26.1	kΩ
Classification						
Classification stability time		From V_{CL-ON} to CLSA or CLSB, stable voltage output		0.4	1	ms
V_{CLASS} output voltage	$V_{CLSA/B}$	13V < V_{DD} < 21V, 1mA < I_{CLASS} < 44mA	1.11	1.16	1.21	V
Classification current for both the CLSA and CLSB pins	I_{CLASS}	R_{CLASS} = 578Ω, 13V ≤ V_{DD} ≤ 21V, measure input current, guaranteed by V_{CLSA} and V_{CLSB}	1.8	2	2.4	mA
		R_{CLASS} = 110Ω, 13V ≤ V_{DD} ≤ 21V, measure input current, guaranteed by V_{CLSA} and V_{CLSB}	9.9	10.55	11.3	
		R_{CLASS} = 62Ω, 13V ≤ V_{DD} ≤ 21V, measure input current, guaranteed by V_{CLSA} and V_{CLSB}	17.7	18.7	19.8	
		R_{CLASS} = 41.2Ω, 13V ≤ V_{DD} ≤21V, measure input current, guaranteed by V_{CLSA} and V_{CLSB}	26.6	28.15	29.7	
		R_{CLASS} = 28.7Ω, 13V ≤ V_{DD} ≤ 21V, measure input current, guaranteed by V_{CLSA} and V_{CLSB}	38.2	40.4	42.6	
Auto-class signature current	I_{ACS}	After t_{ACS} when the auto-class function is enabled, generated internally.	1		3	mA
Auto-class signature timing	t_{ACS}	Change to I_{ACS}, from triggering V_{CL-ON}	76	81.5	87	ms
Long first class event	t_{LCE}	Determine type 3/4 PoE, from triggering V_{CL-ON}	76	81.5	87	ms
Classification lower threshold	V_{CL-ON}	Regulator turns on, V_{DD} rising	12	12.5	13	V
Classification lower threshold hysteresis	$V_{CL-L-HYS}$	Low threshold hysteresis	1.3	1.5	1.7	V
Classification upper threshold	V_{CL-OFF}	Regulator turns off, V_{DD} rising	21	22	23	V
Classification upper threshold hysteresis	$V_{CL-H-HYS}$	High threshold hysteresis		0.5		V
Mark event reset threshold	V_{MARK-L}		4.5	5	5.5	V
Max mark event voltage	V_{MARK-H}		10.5	11	11.5	V
Mark event current	I_{MARK}		0.5	1.1	2	mA

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ELECTRICAL CHARACTERISTICS *(continued)*

PD interface section, V_{DD} = 54V, SRC and AVIN are connected together, T_J = -40°C to +125°C (9), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Mark event resistance	R_{MARK}	2-point measurement at 5.5V and 10.1V, with ΔV / ΔI			12	kΩ
IC supply current during classification	$I_{IN-CLASS}$	V_{DD} = 17.5V, CLSA and CLSB floating		180	300	μA
Class leakage current	$I_{LEAKAGE}$	V_{CLSA} = V_{CLSB} = 0V, V_{DD} = 57V, test both the CLSA and CLSB pins			1	μA
AUTOCLS low-voltage input					0.4	V
AUTOCLS high-voltage input			1.2			V
Under-Voltage Lockout (UVLO)						
VDD turn-on threshold	V_{DD-R}	V_{DD} rising	37	38.5	40	V
VDD turn-off threshold	V_{DD-F}	V_{DD} falling	30	31.5	33	V
VDD UVLO hysteresis	V_{DD-HYS}		5	7		V
IC supply current during operation	I_{IN}	No load and no R_MPS resistor, disconnect AVIN from SRC		1	1.5	mA
Input leakage current		V_{DD} = 29.5V		150	250	μA
Hot-Swap MOSFET and Current Limit						
Internal MOSFET on resistance	R_{ON}	I_{SRC} = 500mA		0.35		Ω
Leakage current	I_{SRC-LK}	V_{DD} = 57V, V_{SRC} = 0V, AUX = high, PRI = high		1	15	μA
ILIM pin detection period				270		μs
ILIM pin detection current			130	165	180	μA
ILIM pin voltage threshold		0.9A setting voltage range			0.8	V
		1.6A setting voltage range	1		2.2	V
Internal MOSFET current limit	I_{LIMIT}	ILIM = 0V, V_{SRC} drops from VDD, V_{DD} - V_{SRC} = 1V	0.75	0.9	1.05	A
		ILIM connected to GND through a 7.15kΩ resistor, V_{SRC} drops from VDD, V_{DD} - V_{SRC} = 1V	1.4	1.6	1.8	A
Internal MOSFET inrush limit	I_{INRUSH}	ILIM = 0V, V_{SRC} ramps up from low to high, V_{DD} - V_{SRC} = 1V	70	130	190	mA
		ILIM connected to GND through a 7.15kΩ resistor. V_{SRC} ramps up from low to high, V_{DD} - V_{SRC} = 1V	170	230	290	mA
Inrush current termination	I_{TERM}	V_{SRC} rising, I_{TERM} / I_{INRUSH}		75%		I_{INRUSH}
Inrush to operation mode delay	t_{DELAY}		80	90	100	ms
Current foldback threshold		V_{SRC} falling, V_{DD} - V_{SRC}	8.2	10	11.8	V
Foldback deglitch time (10)		V_{SRC} falling to inrush current foldback		1		ms
GATE1 source current		V_{GATE1} - V_{SRC} = 4V		10		μA
GATE1 sink current		V_{GATE1} - V_{SRC} = 4V		30		μA

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ELECTRICAL CHARACTERISTICS *(continued)*

PD interface section, V_{DD} = 54V, SRC and AVIN are connected together, T_J = -40°C to +125°C (9), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
GATE1 max driving voltage				6		V
External MOSFET current limit		V_{DD} - V_{SENSE}	22	26	30	mV
SENSE pin leakage current		V_{SENSE} = V_{DD} = 54V			0.1	µA
PG, BT, TYP1, TYP2						
Output low voltage		I_{SINK} = 1mA		0.2	0.4	V
Leakage current		Logic = high, connect to 57V			1	µA
Maintain Power Signature						
Automatic maintain power signature current enable threshold	$I_{PORT-MPS}$	Load current falling		36		mA
Automatic maintain power signature current threshold hysteresis		Load current rises to disable the maintain power signature current		10		mA
R_MPS pin output voltage		1mA to 20mA	23	24	25	V
Type 1/2 PSE, R_MPS output duty cycle		Duty cycle		37%		
		On period	75	85	95	ms
		Off period	115	140	165	ms
Type 3/4 PSE, R_MPS output duty cycle with DUTY pin shorted to GND		Duty cycle		6%		
		On period	14	16	18	ms
		Off period	210	250	290	ms
Type 3/4 PSE, R_MPS output duty cycle with DUTY pin to GND through a 7.15kΩ resistor		Duty cycle		11.5%		ms
		On period	26	31	36	ms
		Off period	200	235	270	ms
Type 3/4 PSE, R_MPS output duty cycle with DUTY pin floating		Duty cycle		17%		
		On period	39	45	52	ms
		Off period	190	221	260	ms
External FET voltage drop control threshold		V_{DS} = V_{SENSE} - V_{SRC}		26		mV
DUTY pin detection current			130	165	180	µA
DUTY pin detection period				130		µs
DUTY pin voltage threshold		6% duty cycle setting voltage range			0.8	V
		11.5% duty cycle setting voltage range	1		2.2	V
		17% duty cycle setting voltage range	2.5			V
Adapter Supply						
VADP pin UVLO rising	ADP_{UV-R}		7.8	8.3	8.8	V
VADP pin UVLO falling	ADP_{UV-F}		6.5	7	7.5	V

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ELECTRICAL CHARACTERISTICS *(continued)*

PD interface section, V_{DD} = 54V, SRC and AVIN are connected together, T_J = -40°C to +125°C (9), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
AUX pin high threshold voltage	V_{AUX-H}		1.92	2	2.08	V
AUX pin threshold hysteresis	$V_{AUX-HYS}$			0.15		V
AUX leakage current		V_{AUX} = 2V		1		µA
		V_{AUX} = 57V		2.5		µA
GATE2 source current		V_{GATE2} - V_{ADP} = 4V		20		µA
GATE2 sink current		V_{GATE2} - V_{ADP} = 4V	200			µA
GATE2 max driving voltage		GATE2 to VADP		6		V
GATE2 turn-on threshold		V_{ADP} - V_{SRC} voltage after the adapter supply is enabled	0		0.45	V
Power Priority						
PRI pin input high voltage			2			V
PRI pin input low voltage					0.4	V
PRI pin internal pull up resistor		Pull up to the internal 5V V_{CC}		1		MΩ
Thermal Shutdown						
Thermal shutdown temperature (10)	T_{PD-SD}			150		°C
Thermal shutdown hysteresis (10)	T_{PD-HYS}			20		°C

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ELECTRICAL CHARACTERISTICS

Controller section, V_{DD} = 54V, SRC and AVIN are connected together, T_J = -40°C to +125°C (9), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply and UVLO						
AVIN UVLO rising threshold	V_{AVIN-R}	V_{AVIN} rising, start charging to V_{CC}	4.5	5.5	6.5	V
AVIN UVLO falling threshold	V_{AVIN-F}	V_{AVIN} falling	3.8	4.8	5.8	V
VCC regulation voltage	V_{CC}	Load = 0mA to 20mA		8.5		V
VCC dropout voltage	$V_{CC-DROP}$	V_{AVIN} = 8V, I_{VCC} = 10mA		1.5		V
VCC UVLO rising threshold	V_{CC-R}	V_{AVIN} > V_{AVIN-R}, V_{CC} rising	5.4	5.7	6.0	V
VCC UVLO falling threshold	V_{CC-F}	V_{AVIN} > V_{AVIN-R}, V_{CC} falling	5	5.3	5.6	V
Quiescent current	I_Q	MODE pin float, V_{FB} = -0.1V, CS = 100mV, COMP = 0V, I_Q = I_{DD} - I_{COMP}, GATE and SYNC floating, test AVIN pin		900		µA
		MODE = 0V, V_{COMP} = 0V, I_Q = I_{DD} - I_{COMP}, GATE and SYNC floating, test the AVIN pin		500		µA
Enable (EN) Control						
EN turn-on threshold	V_{EN-R}	Start switching	1.9	2	2.1	V
EN turn-on hysteresis	V_{EN-HYS}	Stop switching		0.2		V
EN high micro-power threshold	V_{EN-H}	Start internal logic			1.0	V
EN low micro-power threshold	V_{EN-L}	Stop internal logic	0.4			V
EN input current	I_{EN}	V_{EN} = 5V		2		µA
EN turn-on delay		EN on to GATE output		500		µs
Voltage Feedback (FB)						
FB reference voltage	V_{REF}	T_J = 25°C	1.98	2	2.02	V
		T_J = -40°C to +125°C	1.97	2	2.03	V
FB leakage current	I_{FB}	V_{FB} = 2V		10	50	nA
FB OVP threshold	V_{FBOVP}	No MOSFET Q_G limit for flyback OVP. MOSFET Q_G selection is limited for forward OVP (see the OVP Design for Active-Clamp Forward on page 37)	120%	125%	130%	V_{REF}
OVP hiccup off time				340		ms
Minimum diode conduction time for FB sample	t_{SAMPLE}			0.5	0.6 (11)	µs
Regulation compensation current into FB		V_{CS} = 50mV, R_{CS-GND} = 3.3kΩ (12)		2.7		µA
		V_{CS} = 50mV, R_{CS-GND} = 6.8kΩ (12)		5.4		µA
		V_{CS} = 50mV, R_{CS-GND} = 12.7kΩ (12)		10.8		µA
Error Amplifier (EA)						
EA transconductance	G_{EA}	MODE floating, V_{FB} is ±50mV from V_{REF}, V_{COMP} = 1.5V		0.59		mA/V
EA maximum source current	I_{EA}	MODE floating, V_{COMP} = 1.5V, V_{FB} = 1.9V		-110		µA

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ELECTRICAL CHARACTERISTICS *(continued)*

Controller section, V_{DD} = 54V, SRC and AVIN are connected together, T_J = -40°C to +125°C (9), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
EA maximum sink current	I_{EA}	MODE floating, V_{COMP} = 1.5V, V_{FB} = 2.1V		110		μA
COMP high voltage	V_{COMP}	MODE floating, V_{FB} = 1.9V		4		V
		MODE = 0V, float COMP		5		
COMP internal pull-up resistor		SSR mode		10		kΩ
Soft Start (SS)						
Internal soft-start time	t_{SS}	MODE floating, test FB from 0V to 2V		15		ms
		MODE = 0V, test COMP from 1.5V to 3.5V		20		
Current Sense (CS)						
Maximum CS limit	$I_{LIMIT-MAX}$		140	160	180	mV
Low threshold current limit	$I_{LIMIT-MIN}$	In PSR mode	33	36	39	mV
SCP limit			240	300	360	mV
Current leading edge blanking time	t_{LEB}			250		ns
CS amplifier gain	G_{CS}			11		V/V
CS input bias current		V_{CS} = 160mV		10	50	nA
Pulse-Width Modulation (PWM) Switching						
Switching frequency	f_{SW}		225	250	275	kHz
Minimum foldback frequency in PFM mode		In PSR mode, COMP = 0V		30		kHz
Mode, Dead Time, Dither, V_{OUT} Compensation Setting (MODE and CS Pin)						
MODE pin detection current	I_{MODE}		35	40	45	μA
CS pin detection current	I_{CS}		90	100	110	μA
MODE and CS pin detection period	t_{MODE}, t_{CS}			200		μs
MODE, CS pin detection threshold voltage (13)	V_{MODE}, V_{CS}	Voltage level 1 range			0.15	V
		Voltage level 2 range	0.25		0.4	V
		Voltage level 3 range	0.55		0.85	V
		Voltage level 4 range	1.1		1.5	V
		Voltage level 5 range	2.2			V
GATE Driver Signal						
GATE driver impedance (sourcing)	I_{GATE}	I_{GATE} = -20mA		2		Ω
GATE driver impedance (sinking)	I_{GATE}	I_{GATE} = 20mA		1.7		Ω
GATE source current capability (10)		V_{CC} = 8.5V, GATE = 10nF, test gate rising speed		2		A

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ELECTRICAL CHARACTERISTICS *(continued)*

Controller section, V_{DD} = 54V, SRC and AVIN are connected together, T_J = -40°C to +125°C (9), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
GATE sink current capability (10)		V_{CC} = 8.5V, GATE = 10nF, test gate falling speed		1.7		A
GATE output high voltage	V_{GATE}		V_{CC} - 0.05			V
GATE output low voltage	V_{GATE}				0.05	V
Minimum GATE on time	t_{ON-MIN}			250		ns
GATE max duty cycle	D_{MAX}			70		%
SYNC Driver Signal						
SYNC driver impedance (sourcing)	I_{SYNC}	I_{GATE} = -20mA		5		Ω
SYNC driver impedance (sinking)	I_{SYNC}	I_{GATE} = 20mA		2.3		Ω
SYNC source current capability (10)		V_{CC} = 8.5V, SYNC = 10nF, test the SYNC rising speed		0.8		A
SYNC sink current capability (10)		V_{CC} = 8.5V, SYNC = 10nF, test the SYNC falling speed		1.2		A
SYNC output high voltage	V_{SYNC}		V_{CC} - 0.05			V
SYNC output low voltage	V_{SYNC}				0.05	V
Protection						
Overload protection hiccup on time (10)				4.8		ms
Overload protection hiccup off time (10)				340		ms
Thermal shutdown temperature (10)	T_{SD}			150		°C
Thermal shutdown hysteresis (10)	T_{HYS}			20		°C

Notes:

9) Guaranteed by over-temperature correlation. Not tested in production.
10) Guaranteed by characterization. Not tested in production.
11) It is recommended to make the output diode conduction time longer than 0.7µs.
12) R_{CS-GND} is the resistance from the CS pin to GND. This includes the current-sense resistor from the MOSFET source to GND and the resistor from the MOSFET's source to the CS pin.
13) For different voltage levels, see Table 6 on page 30 and Table 7 on page 32.

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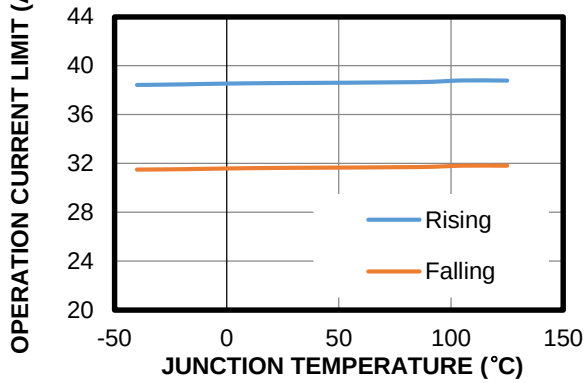
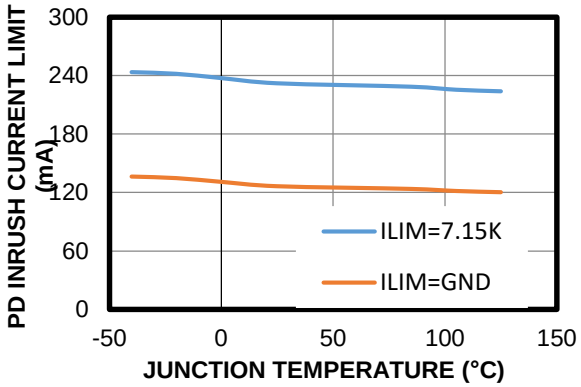
TYPICAL CHARACTERISTICS

VDD = 54V, T_A = 25°C, unless otherwise noted.

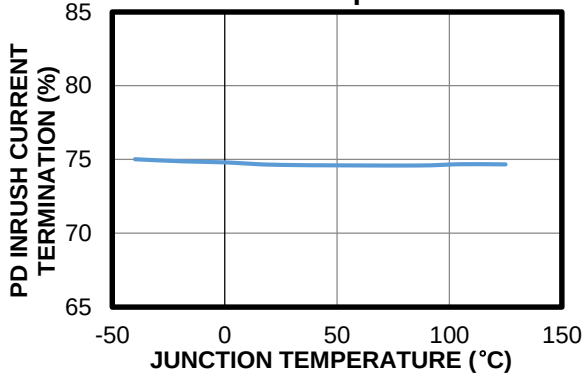
Operation Current Limit vs. Junction Temperature



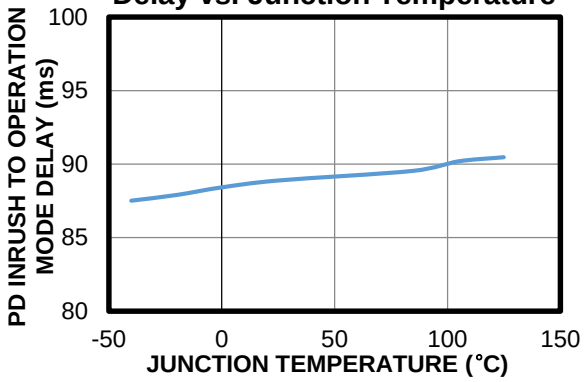
PD Inrush Current Limit vs. Junction Temperature



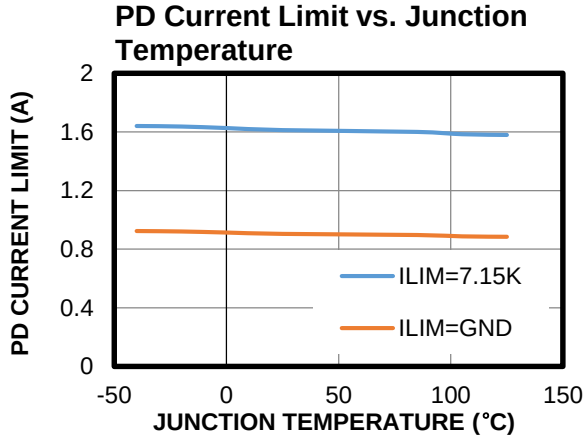
PD Inrush Current Termination vs. Junction Temperature



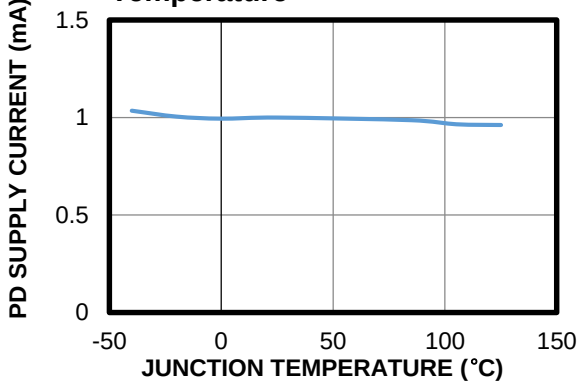
PD Inrush to Operation Mode Delay vs. Junction Temperature



PD Current Limit vs. Junction Temperature



PD Supply Current during Operation vs. Junction Temperature



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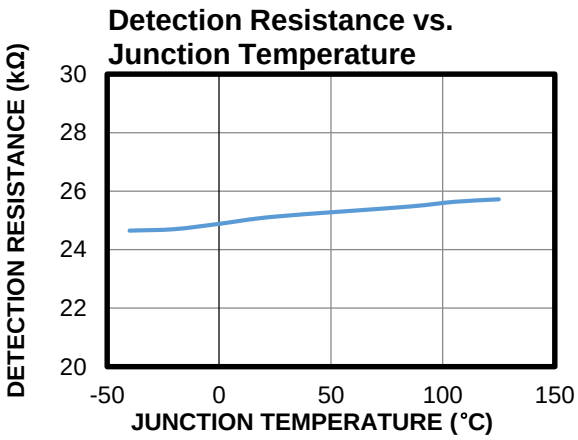
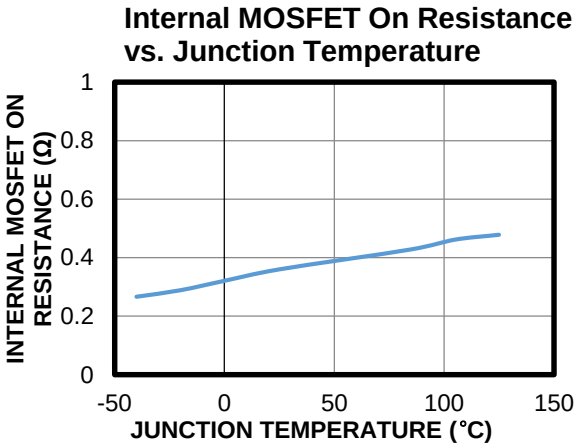
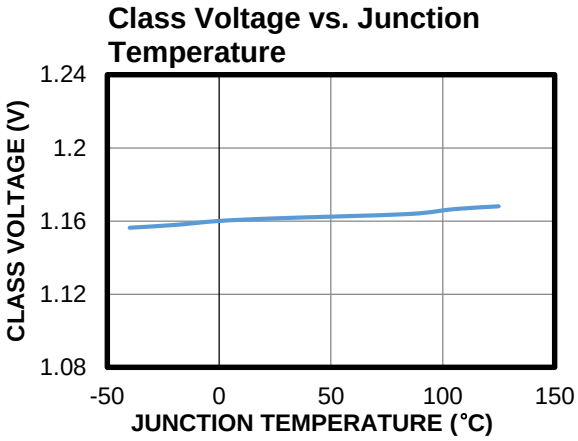
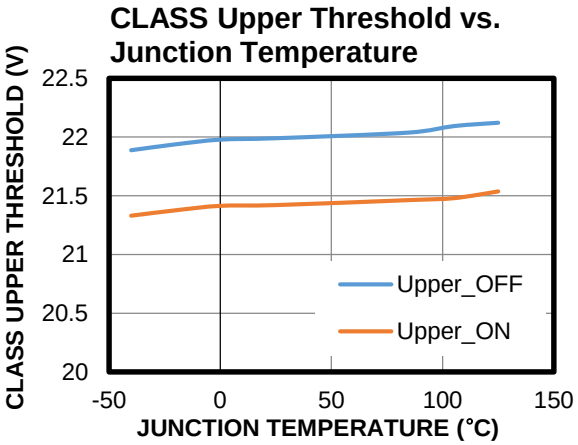
TYPICAL CHARACTERISTICS *(continued)*

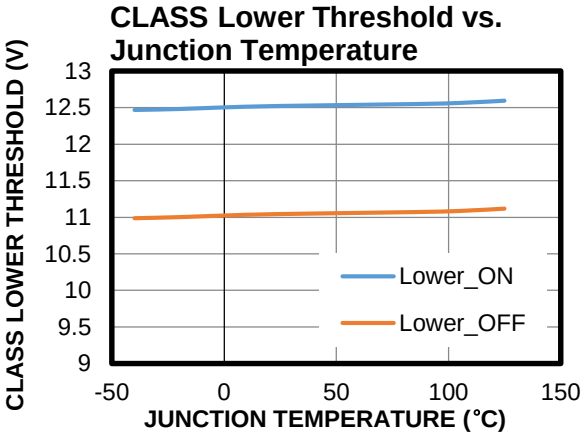
V_{DD} = 54V, T_A = 25°C, unless otherwise noted.

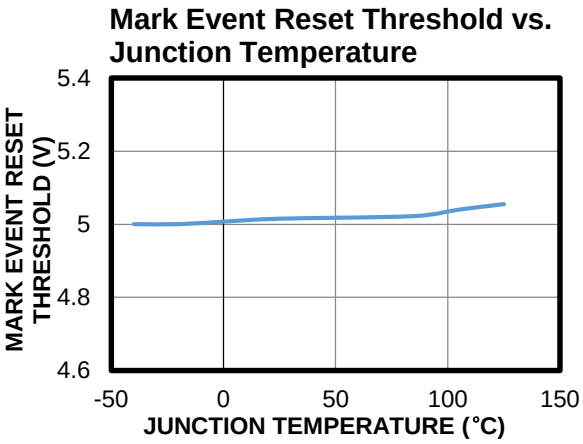












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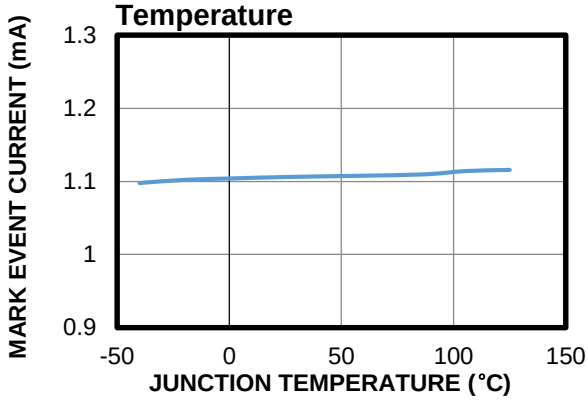
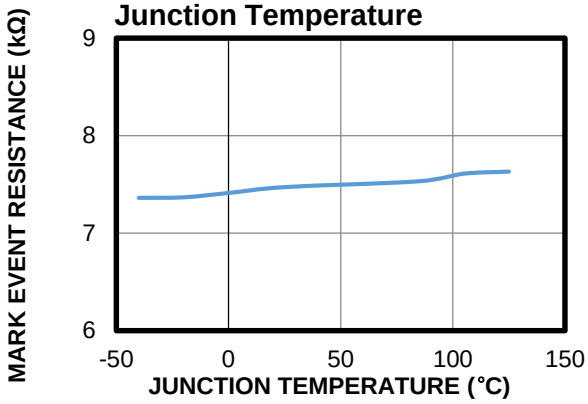
TYPICAL CHARACTERISTICS *(continued)*

V_{DD} = 54V, T_A = 25°C, unless otherwise noted.

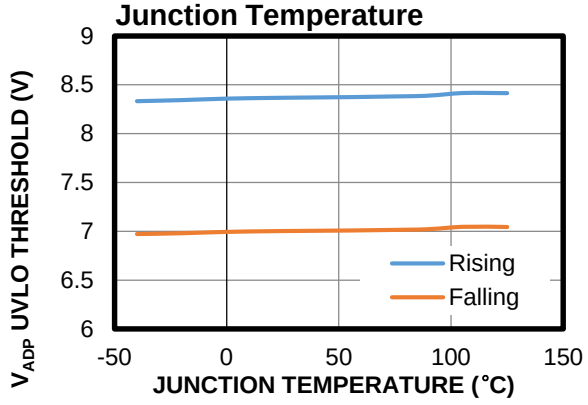
Mark Event Current vs. Junction Temperature



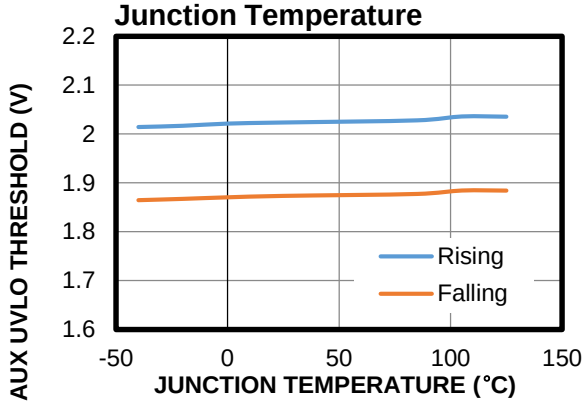
Mark Event Resistance vs. Junction Temperature



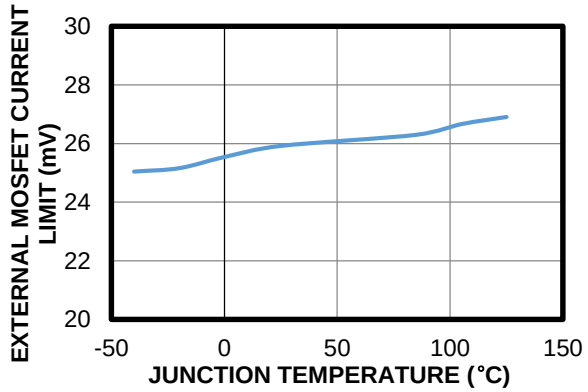
V_{ADP} UVLO Threshold vs. Junction Temperature



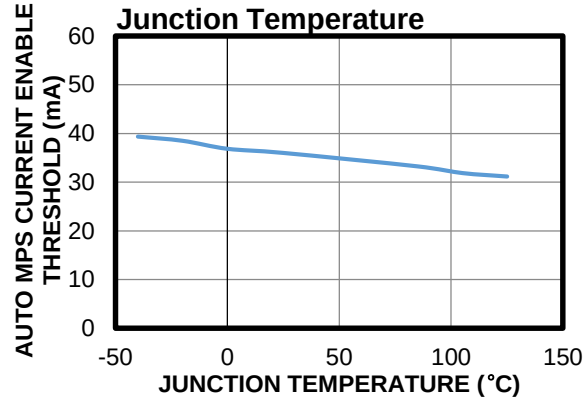
AUX UVLO Threshold vs. Junction Temperature



External MOSFET Current Limit vs. Junction Temperature



Auto Maintain Power Signature Current Enable Threshold vs. Junction Temperature



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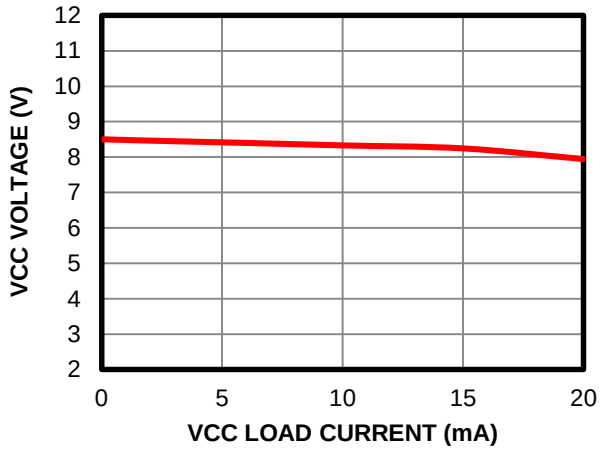
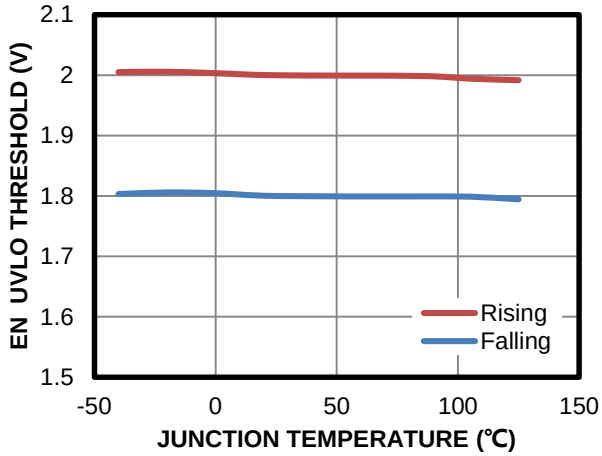
TYPICAL CHARACTERISTICS *(continued)*

V_{DD} = 54V, T_A = 25°C, unless otherwise noted.

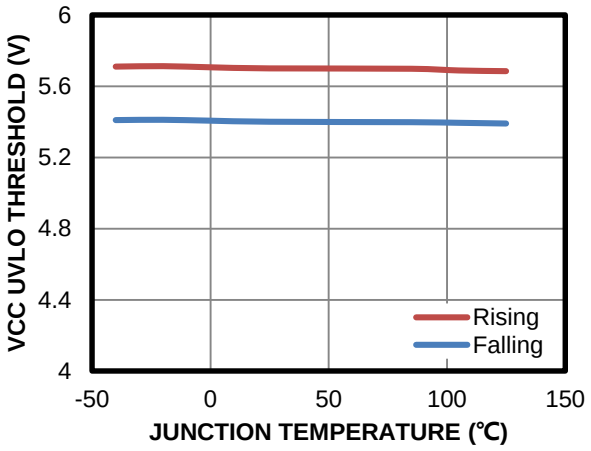
VCC Voltage vs. VCC Load Current



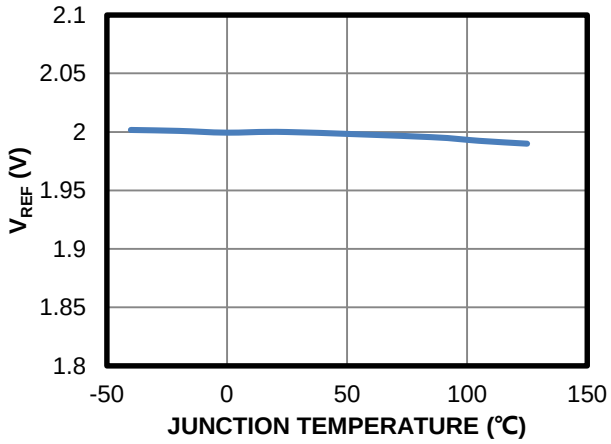
EN UVLO Threshold vs. Junction Temperature



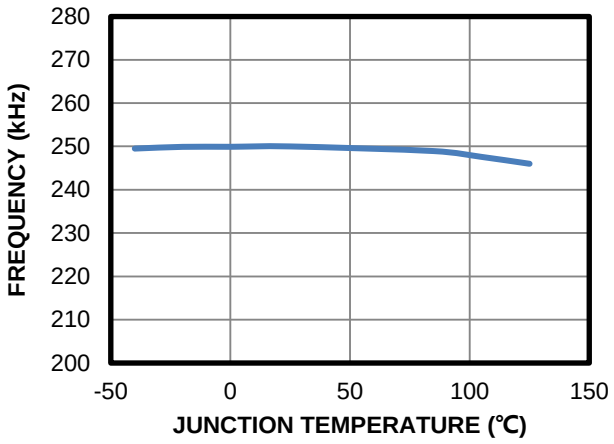
VCC UVLO vs. Junction Temperature



Reference Voltage vs. Junction Temperature

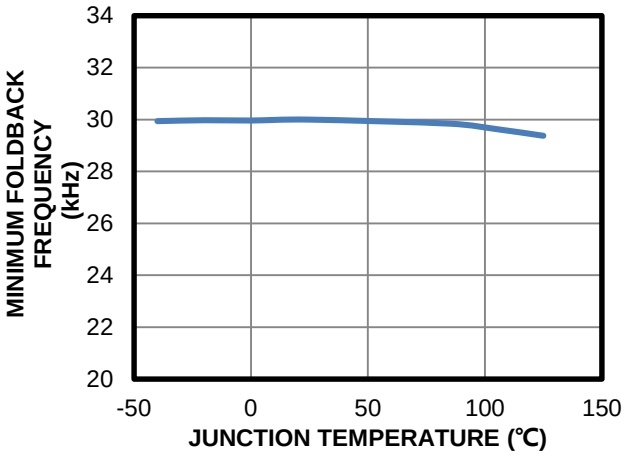


Frequency vs. Junction Temperature



Minimum Foldback Frequency vs. Junction Temperature

PSR mode



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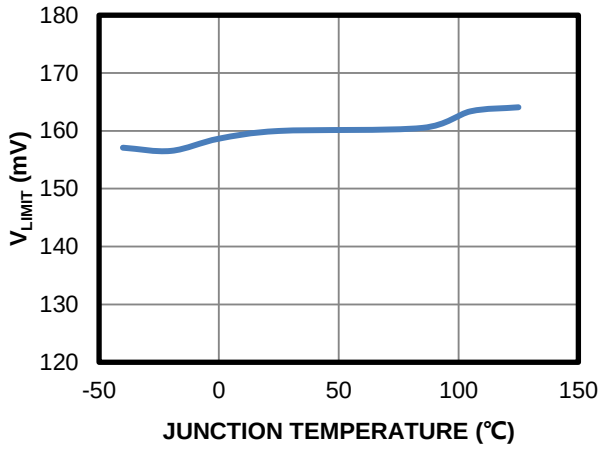
TYPICAL CHARACTERISTICS *(continued)*

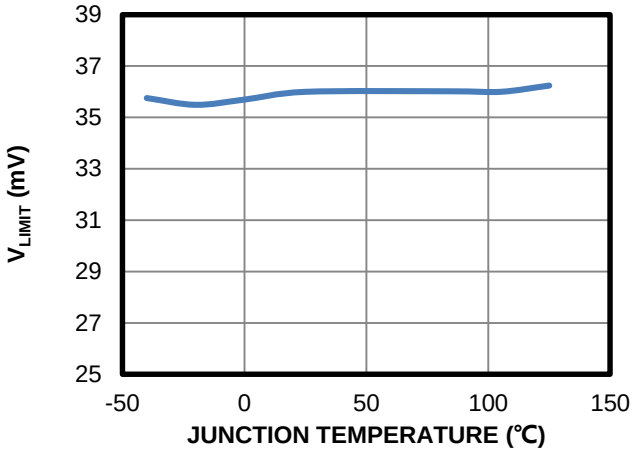
V_{DD} = 54V, T_A = 25°C, unless otherwise noted.

Current Limit vs. Junction Temperature

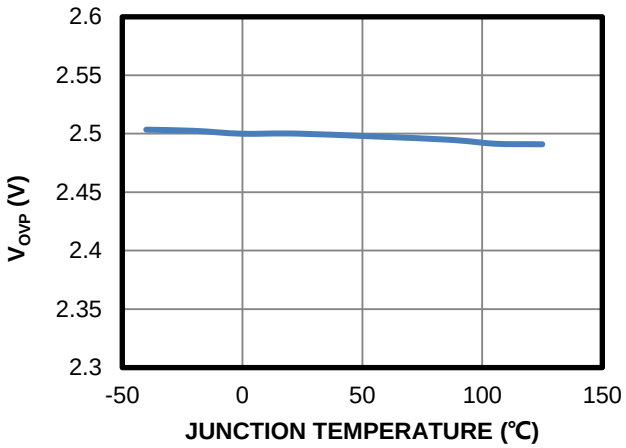


Low Threshold Current Limit vs. Junction Temperature

PSR mode



OVP Threshold vs. Junction Temperature



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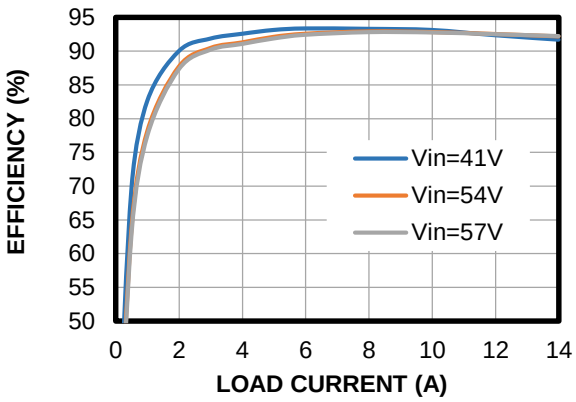
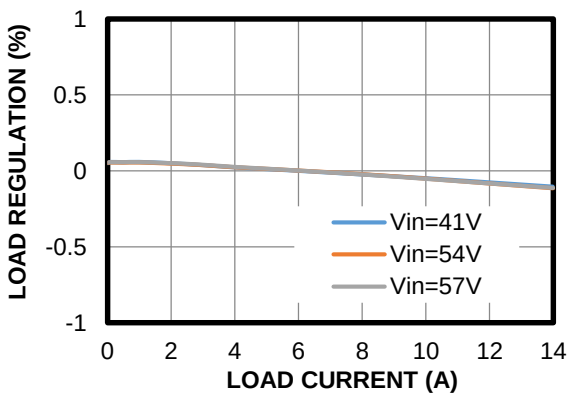
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 54V, V_{ADP} = 48V, V_{OUT} = 5V, I_{OUT} = 14A, T_A = 25°C, set in SSR forward mode, unless otherwise noted.

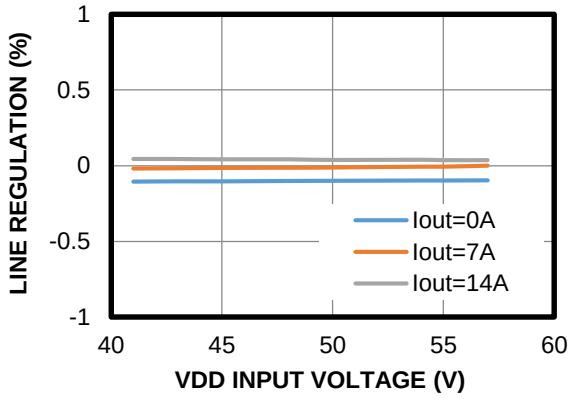
Efficiency vs. Load Current



Load Regulation



Line Regulation



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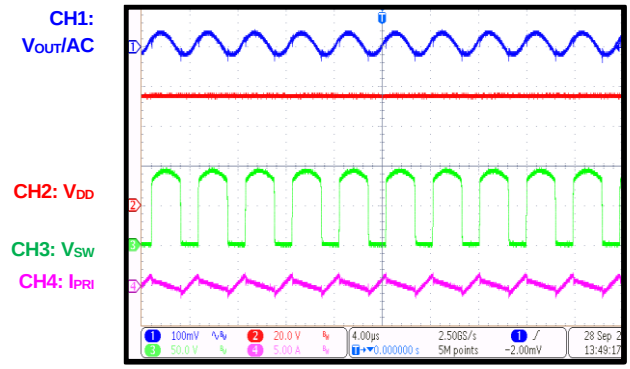
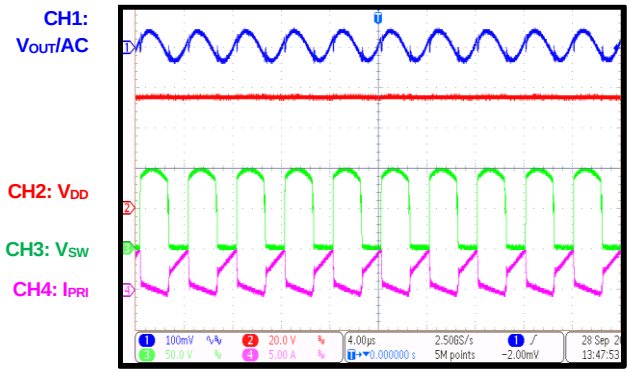
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{DD} = 54V, V_{ADP} = 48V, V_{OUT} = 5V, I_{OUT} = 14A, T_A = 25°C, set in SSR forward mode, unless otherwise noted.

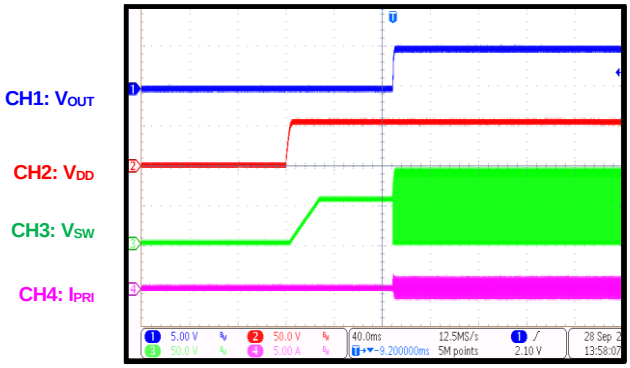
Steady State
I_{OUT} = 0A



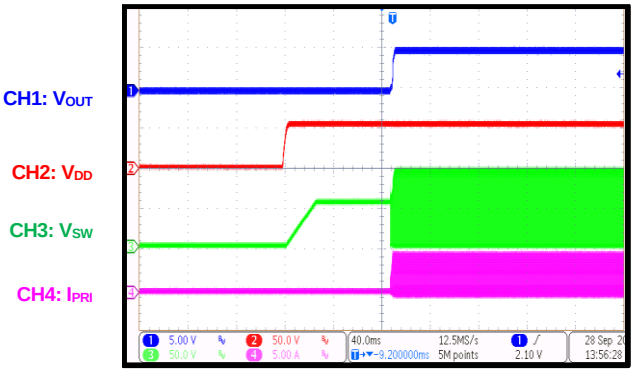
Steady State
I_{OUT} = 14A



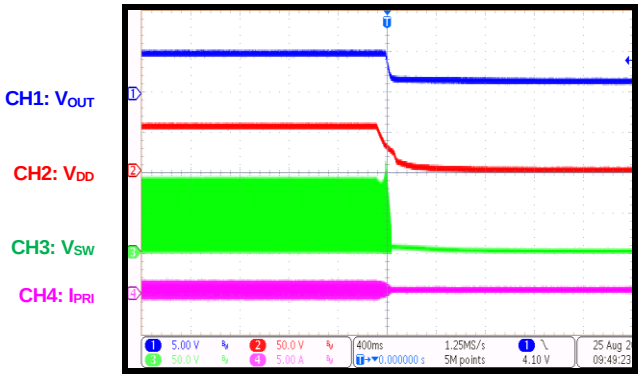
Start-Up through VDD
I_{OUT} = 0A



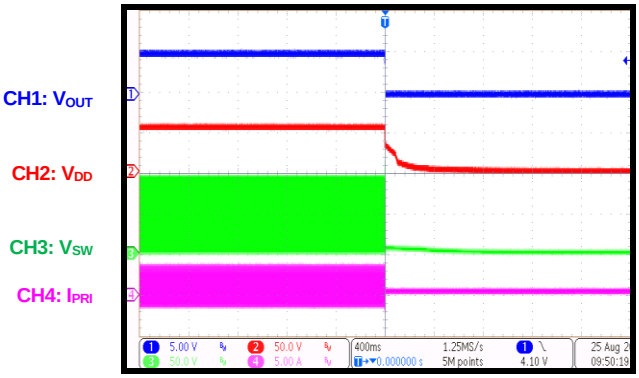
Start-Up through VDD
I_{OUT} = 14A



Shutdown through VDD
I_{OUT} = 0A



Shutdown through VDD
I_{OUT} = 14A



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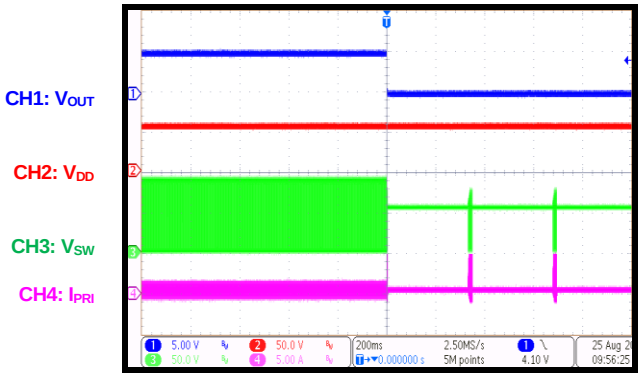
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{DD} = 54V, V_{ADP} = 48V, V_{OUT} = 5V, I_{OUT} = 14A, T_A = 25°C, set in SSR forward mode, unless otherwise noted.

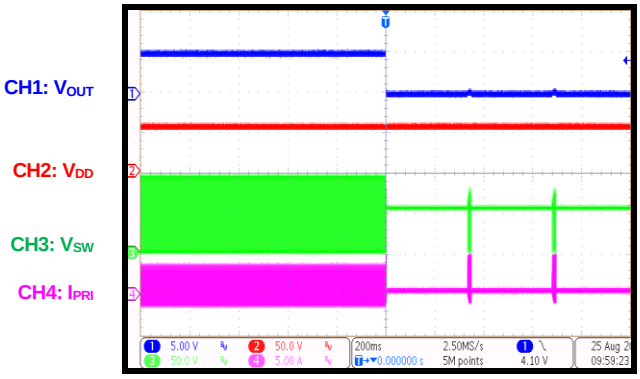
SCP Entry

I_{OUT} = 0A to short



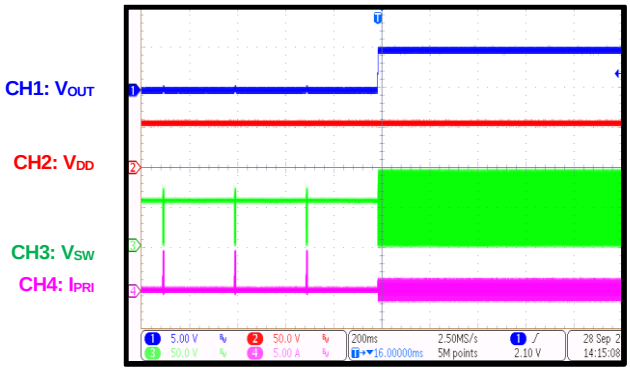
SCP Entry

I_{OUT} = 14A to short



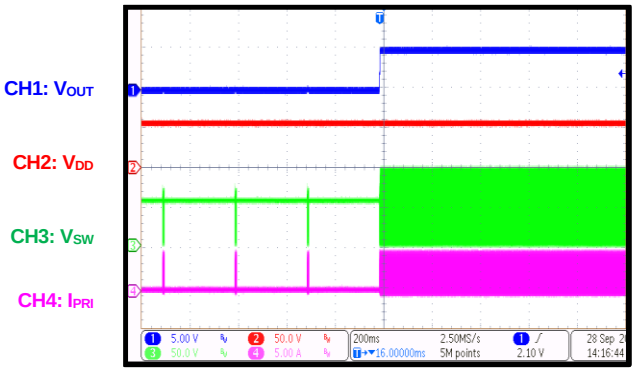
SCP Recovery

I_{OUT} = short to 0A



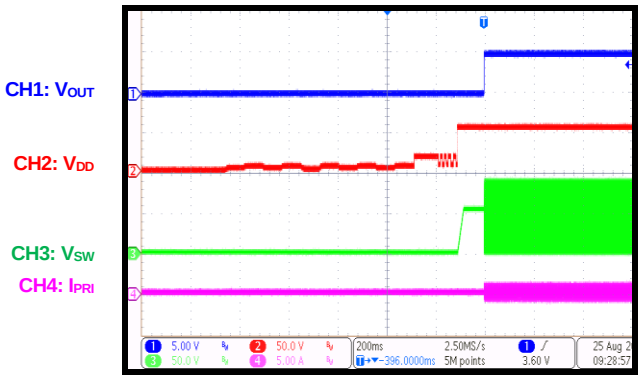
SCP Recovery

I_{OUT} = short to 14A



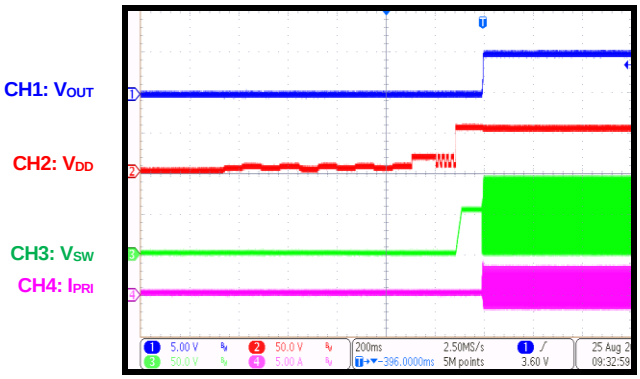
PSE Start-Up

I_{OUT} = 0A



PSE Start-Up

I_{OUT} = 14A



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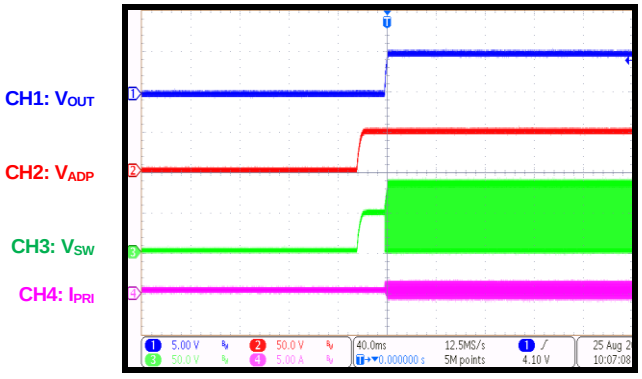
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{DD} = 54V, V_{ADP} = 48V, V_{OUT} = 5V, I_{OUT} = 14A, T_A = 25°C, set in SSR forward mode, unless otherwise noted.

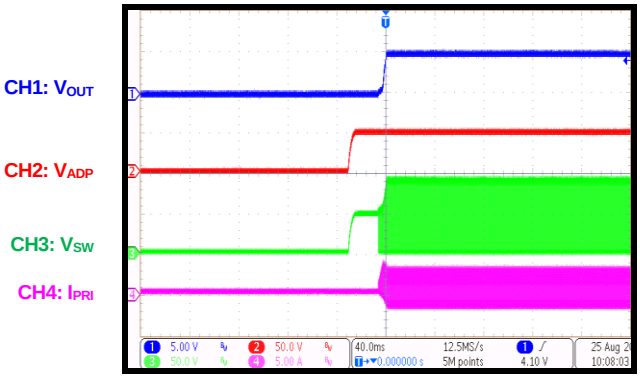
Adapter Start-Up

I_{OUT} = 0A



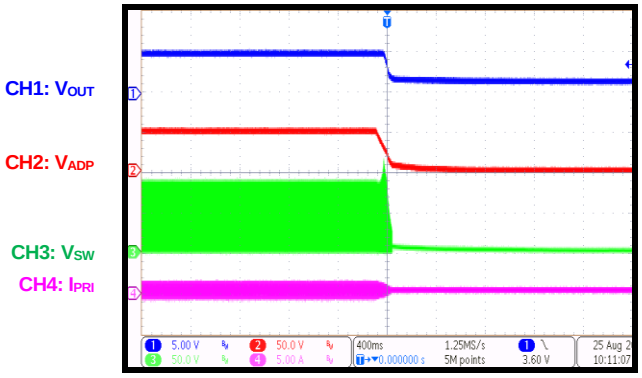
Adapter Start-Up

I_{OUT} = 14A



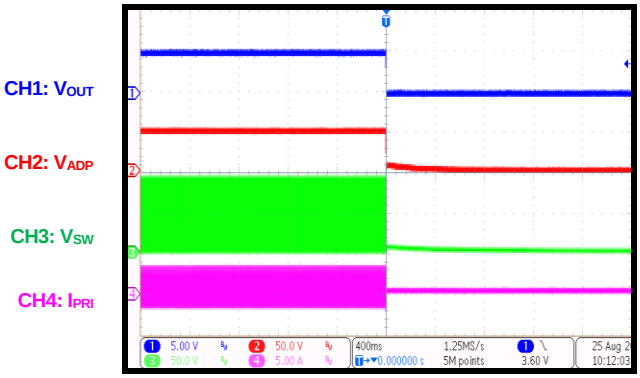
Adapter Shutdown

I_{OUT} = 0A



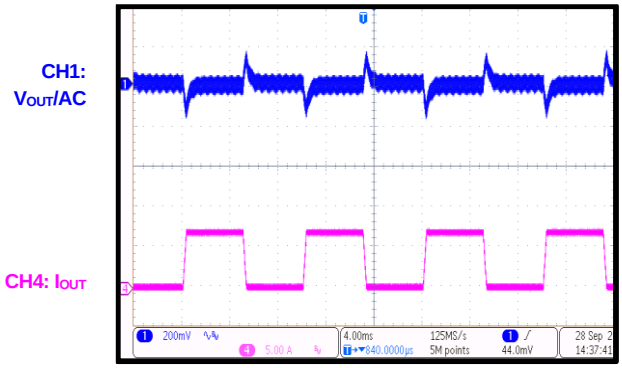
Adapter Shutdown

I_{OUT} = 14A



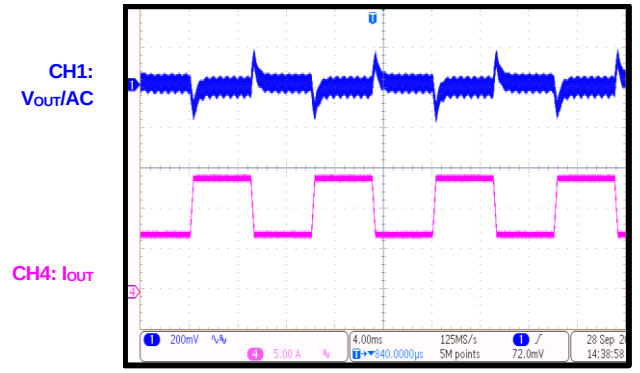
Load Transient Response

I_{OUT} = 0A to 7A, I_{RAMP} = 25mA/µs



Load Transient Response

I_{OUT} = 7A to 14A, I_{RAMP} = 25mA/µs



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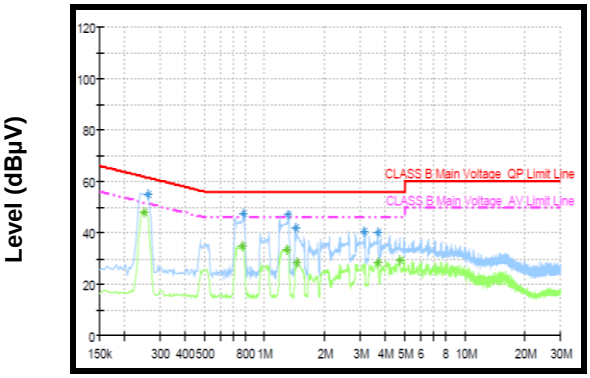
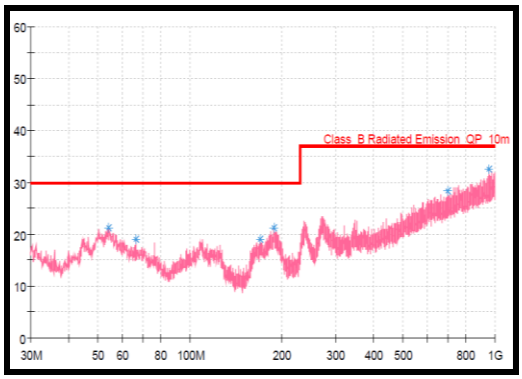
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{DD} = 54V, V_{ADP} = 48V, V_{OUT} = 5V, I_{OUT} = 14A, T_A = 25°C, set in SSR forward mode, unless otherwise noted.

Conducted Emissions Results



Radiated Emissions Results



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FUNCTIONAL BLOCK DIAGRAM

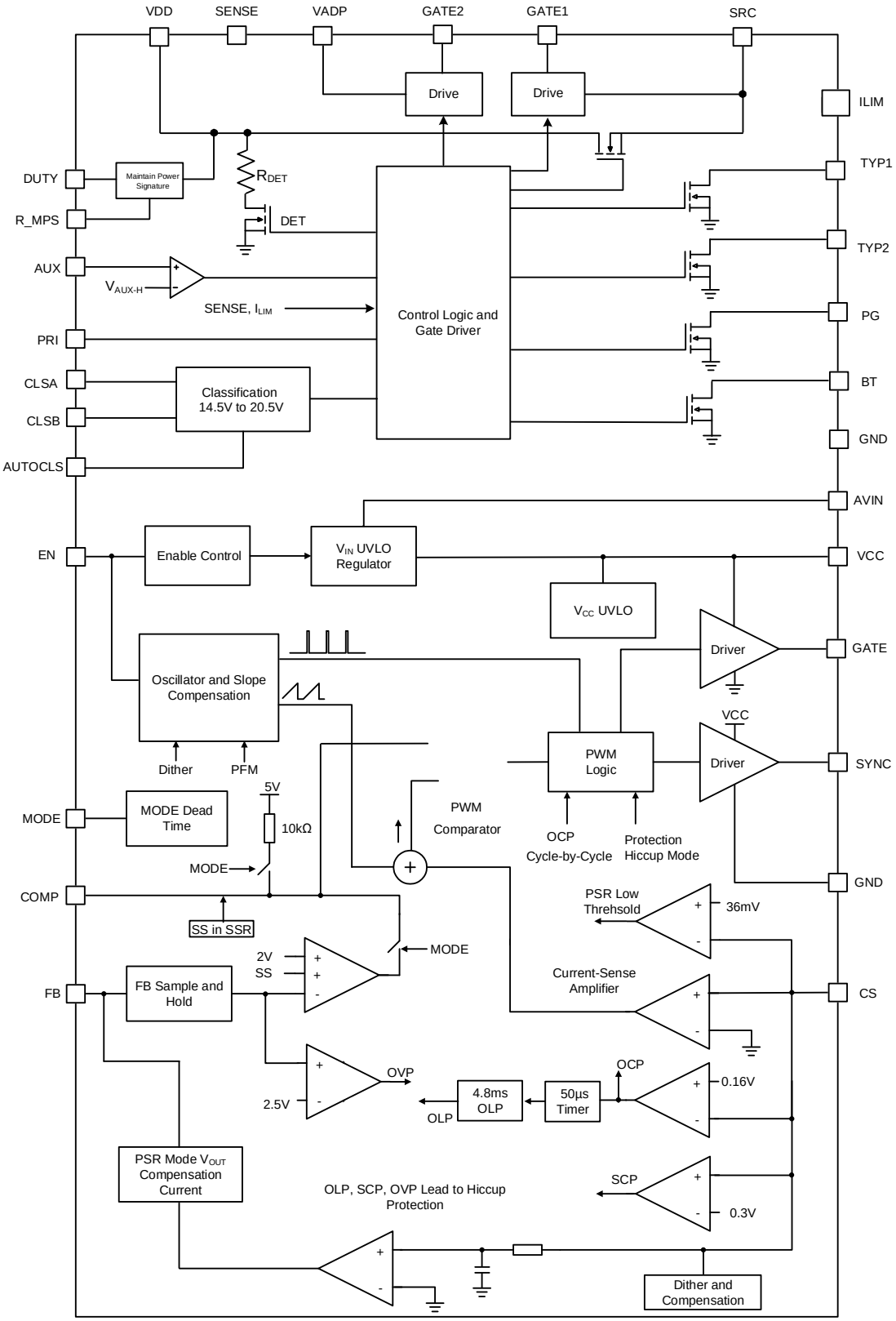

Figure 1: Functional Block Diagram

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OPERATION

The MP8030 is a fully integrated, IEEE 802.3af/at/bt-compliant, Power over Ethernet (PoE) powered device (PD) power supply converter. It includes a PD interface and high-efficiency flyback/forward controller.

PD INTERFACE

The MP8030 PD interface has all the functions of IEEE 802.3af/at/bt, including detection, classification, input current control, a 100V hot-swap MOSFET, and an automatic maintain power signature function.

Detection

The MP8030 PD integrates an internal detection resistor. When the PSE applies two safe voltages (between 2.7V and 10.1V) to the MP8030, the MP8030 PD will typically shows a 25kΩ resistance between the VDD and GND pins.

Classification

PSE distributes power to PDs based on the classification results. Classification mode is active when the input voltage is between 14.5V and 20.5V. The MP8030 PD presents different currents in classification mode (see Table 1).

Table 1: Different Classification Power Rating and Setting with PD

PD Class	Power Rating (W)	Class Cycle with Max Power	CLSA Signature	CLSB Signature	CLSA Resistor (Ω)	CLSB Resistor (Ω)
0	0.44 to 12.95	1	0	0	578	578
1	0.44 to 3.84	1	1	1	110	110
2	3.84 to 6.49	1	2	2	62	62
3	6.49 to 12.95	1	3	3	41.2	41.2
4	12.95 to 25.5	2, 3	4	4	28.7	28.7
5	25.5 to 40	4	4	0	28.7	578
6	40 to 51	4	4	1	28.7	110
7	51 to 62	5	4	2	28.7	62
8	62 to 71.3	5	4	3	28.7	41.2

IEEE802.3bt supports an 8-level class power rating, with up to 5 classification cycle operations. These classification cycles have the below functions:

- All PSEs perform one cycle classification for the class 0, class 1, class 2, and class 3 PDs.
- Type 2 PSEs perform 2-cycle classification if a class 4 signature is detected during the first class cycle.
- Type 3 and type 4 PSEs start their third cycle classification if a class 4 signature is detected during the first and second class cycle. Based on the third classification result, type 3 and type 4 PSEs follow one of the operations listed below:

  If the third classification result is a class 4 signature, classification stops and there is a class 4 PD.

  If the third classification result is a class 0 or class 1 signature, the devices continues to the fourth cycle classification.

  If the third classification result is class 2 or class 3 signature, the type 4 PSE performs a fourth and fifth cycle classification.

The MP8030 PD performs a class signature signal with the CLSA pin in the first and second class cycles. The MP8030 PD performs a class signature signal with the CLSB pin in the remaining class cycles, unless V_{DD} drops to its mark event reset threshold.

Both CLSA and CLSB use the same 1.16V output voltage for classification. The maximum output current is limited for protection.

Auto-Class Function

IEEE802.3bt also supports an auto-class function that allows the PD to communicate its effective maximum power consumption to the PSE. When MP8030 PD auto-class function is enabled (by pulling the AUTOCLS pin low), the PD switches the class current to class 0 within

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76ms to 87ms. After the first long time classification function works, this class 0 classification current lasts until the first class is complete.

The auto-class function can indicate to a type 3 or 4 PSE that it supports the auto-class function.

Under-Voltage Lockout (UVLO) and the Power Supply Voltage

The MP8030 PD integrates one under-voltage lockout (UVLO) circuit with a large hysteresis. The UVLO block ensures that the PD starts up when V_{DD} exceeds 40V and shuts down when V_{DD} drops below 30V.

The MP8030 PD also has an inrush current limit during start-up. This current is about 1/7 of the steady state current limit configured by the ILIM pin.

Hot-Swap MOSFET and Current Limit

The MP8030 PD interface integrates one 100V MOSFET for output disconnect.

When the PD voltage is powered by the PSE, and V_{DD} exceeds the rising UVLO threshold, the hot-swap MOSFET starts passing a limited current (I_{INRUSH}) to charge the DC/DC converter's input bulk capacitor. The inrush current limit function works until it drops below 75% of the inrush current limit, and then the current limit changes to the normal current limit threshold.

To meet the different power ratings, the MP8030 PD supports a configurable current limit with the ILIM pin. The ILIM pin sources a current after V_{DD} rises to the UVLO threshold. This current detects the configured current limit level. Table 2 shows the ILIM configurations.

Table 2: ILIM Configurations

ILIM to GND Resistance (kΩ)			Current Limit (A)
Min	Typ	Max	
0	0	1.4	0.9
5.76	7.15	9.09	1.6

The GATE1 pin can drive one external N-channel MOSFET, which is connected in parallel with the internal 0.35Ω MOSFET. GATE1 turns on the external MOSFET after t_{DELAY} (about 90ms) completes. If V_{DD} - V_{SRC} exceeds 10V after this delay, GATE1 does not turn on because over-current protection (OCP) is triggered. If V_{SRC} is below V_{DD} by less than 10V, GATE1 turns on to charge the bulk capacitor. The MP8030 PD turns off the external MOSFET under light-load conditions.

The internal MOSFET and external MOSFET have different current limit control loops. The internal MOSFET current limit is configured by the ILIM pin, while the external MOSFET current limit is configured by a resistor (R_{SENSE}) between the VDD and SENSE pins. To reduce additional power loss and cost, the external MOSFET current limit can be disabled by removing R_{SENSE} (connecting the SENSE pin to the VDD pin). It is recommended for R_{SENSE} to be 18mΩ. When an external R_{SENSE} is used, it is recommended to connect the ILIM pin to GND for the lowest total current limit.

Figure 2 shows the internal and external MOSFET start-up sequence.

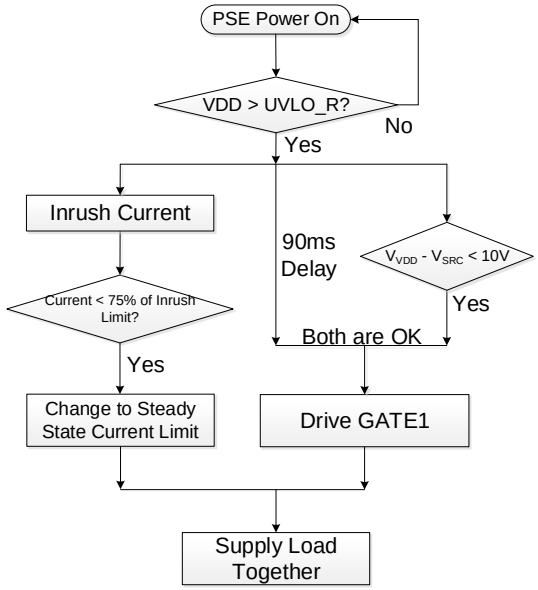

Figure 2: Internal MOSFET and External MOSFET Start-Up Sequence

The internal and external MOSFETs have fast-off current protection if there is a short-circuit event. After GATE1 turns off, the internal MOSFET recovers if V_{IN} - V_{SRC} < 10V.

If an overload event occurs when both the internal MOSFET and external MOSFET are connected, the current limit function can work in a few ways, described below:

- If the internal MOSFET triggers a current limit first, the internal current is limited, and

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additional current goes through the external MOSFET. If the external MOSFET also reaches its current limit, the external MOSFET pulls GATE1 low and V_{SRC} drops. If V_{DD} - V_{SRC} exceeds 10V for 1ms, the external MOSFET turns off, and the internal MOSFET current limit switches to the inrush limit threshold. At the same time, PG pulls low to disable the DC/DC controller, then works in a new start cycle with the inrush current limit. During this over-current condition, PG recovers without a 90ms delay after the inrush completes.

- If the external MOSFET triggers the current limit first, GATE1 pulls low. Additional current passes through the internal MOSFET and finally triggers the internal current limit. V_{SRC} drops after both current limits are triggered and finally runs into current foldback mode (inrush current limit). At the same time, PG is pulled low.
- If the internal MOSFET or external MOSFET triggers the fast-off current limit, the MP8030 PD quickly turns off the related MOSFET then restarts with a delay.

Power Good (PG) and Delay

The MP8030 PD has one PG output to enable the DC/DC controller after the inrush period finishes and the PSE is ready to provide high power. PG is an open-drain output with up to a 100V voltage rating.

PG is in high impedance when the device meets the below conditions:

- The device has changed to the steady current limit, which means that the inrush period is complete.
- The 90ms delay (t_{DELAY}) from UVLO has completed.

Then a wall power adapter is detected on AUX, and V_{ADP} exceeds its UVLO threshold (see Figure 3).

The PG signal resets when VDD UVLO_F is triggered, if over-temperature protection (OTP) occurs, or if V_{DD} - V_{SRC} > 10V for more than 1ms. The 90ms timer only works after V_{DD} UVLO is triggered.

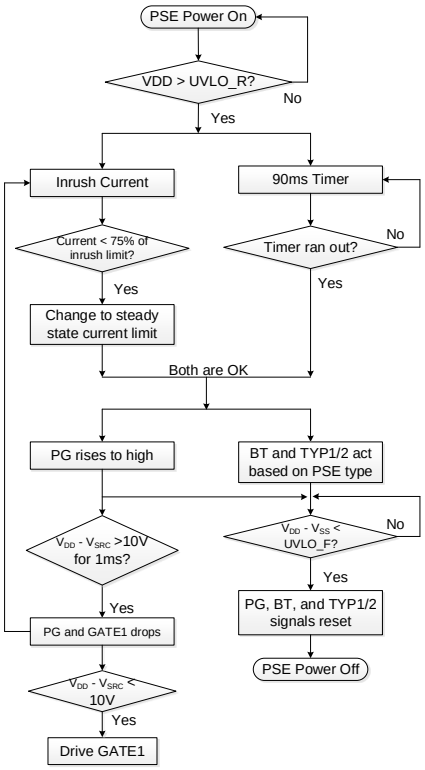

Figure 3: PG Logic

PSE and Allocated Power Indicators

IEEE802.3bt supports 4 different PSE power supplies. The BT, TYP1, and TYP2 pins indicate the PSE-allocated power type. Table 3 on page 28 lists the detailed power level indicators. Note that the indicator only shows high when it is in logic high and pulled up to a high voltage through an external pull-up resistor.

The TYP1, TYP2, and BT signals are active after t_{DELAY} (about 90ms). The outputs become inactive (high impedance) when the input voltage (V_{DD}) falls below its UVLO threshold, or if OTP is triggered. The BT, TYP1, and TYP2 signals are latched in the MP8030 PD after start-up and do not reset until V_{DD} drops to its mark event reset threshold.

The TYP1 and TPY2 pins go low if an adapter is detected. BT is high under this condition.

Table 4 on page 28 shows demotion cases.

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Table 3: PSE and Allocated Power Indicator

PSE Type	PD Class	PSE Allocated Power	Number of Class Cycles	BT	TYP1	TYP2
Type 1 Type 2	Class 0 Class 1 Class 2 Class 3	12.95W 3.84W 6.49W 12.95W	1	High	High	High
Type 2	Class 4	25.5W	2	High	High	Low
Type 3 Type 4	Class 0 Class 1 Class 2 Class 3	12.95W 3.84W 6.49W 12.95W	1	Low	High	High
	Class 4	25.5W	2, 3	Low	High	Low
	Class 5 Class 6	40W 51W	4	Low	Low	High
Type 4	Class 7 Class 8	62W 71.3W	5	Low	Low	Low

Table 4: Power Demotion Cases

PSE Type	PD Class	PSE Allocated Power	Number of Class Cycles	BT	TYP1	TYP2
Type 2	Class 4	12.95	1	High	High	High
Type 3 Type 4	Classes 4–8	12.95	1	Low	High	High
Type 3 Type 4	Classes 5–8	25.5	2, 3	Low	High	Low
Type 3 Type 4	Classes 7–8	51	4	Low	Low	High

Automatic Maintain Power Signature Function

To maintain the PSE power supply, the MP8030 supports an automatic maintain power signature and the current is configured by a resistor on the R_MPS pin.

The MP8030 also has one DUTY pin to configure the R_MPS pin's duty cycle, which can compensate the effects of the long cable and bulk bus capacitors. After V_{DD} reaches the UVLO rising threshold, the DUTY pin sources one pulse current to detect the maintain power signature function duty cycle setting. Table 5 shows the DUTY pin's configuration options. The DUTY signal resets after V_{DD} falls to its UVLO falling threshold.

Table 5: DUTY Configurations

DUTY to GND Resistance (kΩ)			R_MPS Duty Cycle (%)
Min	Typ	Max	
0	0	1.4	6
5.76	7.15	9.09	11.5
17.4	Float	Float	17

With type 1 and type 2 PSE inputs, the MP8030 generates a voltage on the R_MPS pin with a fixed 37% duty cycle.

Wall Adapter Power Supply

For applications where an auxiliary power source, such as a wall adapter, is used to power the device, the MP8030 PD features wall power adapter detection. Once the adapter voltage (V_{ADP}) exceeds about 8.3V, the MP8030 PD enables wall adapter detection.

The resistor divider connected from VADP to AUX can detect the adapter status. Once the AUX voltage exceeds the internal reference voltage, the MP8030 PD switches the power source from the PSE to the adapter if the adapter has higher priority.

GATE2 drives the external N-channel MOSFET and provides a smooth switch between the PSE and auxiliary wall adapter with less power loss compared to a traditional diode input. After the adapter supply is enabled, the PG signal is pulled high, the TYP1/TYP2 pins output low, and the BT pin stays high.

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When PRI is high, setting AUX high disables the DET, CLS, and maintain power signature functions. When PRI is low, setting AUX high cannot disable the DET, CLS, and maintain power signature functions.

If an adapter has a higher priority and replaces the PSE power supply, BT and TYP1/2 are updated once the AUX and ADP_UV signals are working. If the PSE has a higher priority and replaces the adapter supply, the MP8030 PD changes the BT and TYP1/2 statuses to Hi-Z. If PSE UVLO occurs, the statuses change to indicate the latest PSE power type after inrush is complete and the 90ms timer has finished.

Power Priority

The adapter is available when both AUX and V_{ADP} exceed their UVLO thresholds. The MP8030 PD can source a current from the adapter or PSE if both the adapter and PSE are connected. This is determined by the PRI and AUX pin settings.

The PRI pin is internally pulled up to the internal VCC. If the PRI pin is floating (the adapter has higher priority) and V_{ADP}/AUX exceed their UVLO thresholds, the MP8030 PD disables the PSE power supply, and enables the adapter power source. If AUX is below its falling threshold, the MP8030 PD supplies power via the PSE, even PRI pin is floating.

If the PRI pin is connected to GND, PSE has the higher priority. Regardless of the AUX signal, PSE outputs power, unless V_{DD} is below its UVLO threshold.

If PSE has a higher priority and the adapter is connected before PSE plug-in, a reverse block MOSFET (Q_{REV}) must be added to reversely block the power from the adapter during PoE detection and classification (see Figure 4). At the same time, the output downstream DC/DC controller should lower the power rating so that the inrush current charges the MP8030 bus capacitor (C_{BUS}). If C_{BUS} is not charged quickly, the current limit may not be met, and the device may fail to start up.

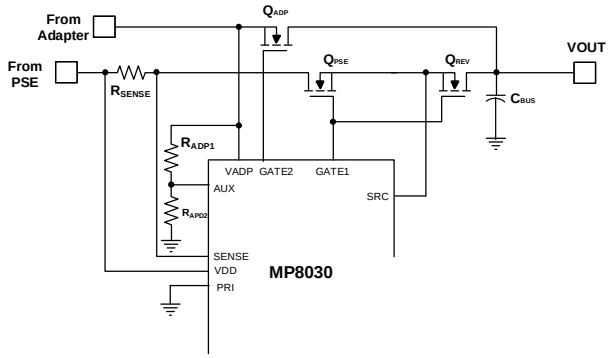

Figure 4: Reverse Block Solution

DC/DC CONTROLLER

Start-Up and Power Supply

The MP8030 DC/DC controller features a high-voltage internal start-up circuit. When the voltage between AVIN and GND exceeds 5.5V, the capacitor at VCC is charged through the internal LDO. Normally V_{CC} is regulated to 8.5V (if AVIN is high enough), and the V_{CC} UVLO threshold is typically 5.7V. In addition to V_{CC} UVLO, the DC/DC controller has an EN UVLO threshold that is typically 2V. When V_{CC} exceeds 5.7V and the EN pin is high, the DC/DC controller starts working.

V_{CC} can be powered from the transformer auxiliary winding to save IC power loss after the DC/DC controller starts switching. The auxiliary power exceeds the V_{CC} regulation voltage to override the internal LDO. There is one internal reverse blocking circuit, which means that V_{CC} can exceed AVIN if V_{CC} has biased power. The VCC power should stay below 16V due to the pin's voltage rating.

If AVIN is below 8.5V and V_{CC} cannot be regulated to 8.5V, the internal high-voltage VCC LDO has a 1.5V voltage drop. This means the DC/DC controller can work when the input is as low as 8V.

Enable (EN) Control

The EN pin enables and disables the MP8030 DC/DC controller. When the EN voltage exceeds 1V, the controller starts up some of the internal circuits. This is called micro-power mode. If the EN voltage exceeds the turn-on threshold (2V), the controller enables all functions and starts the GATE/SYNC driver signal. The GATE/SYNC signal can be disabled when the EN voltage drops to about 1.8V, but micro-power mode is disabled only after the EN

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voltage falls below 0.4V. After shutdown, the controller sinks a current (typically less than 1μA) from the input power.

One internal Zener diode on the EN pin clamps the EN voltage when the voltage divider exceeds 6.5V. Use an external pull-up resistor and ensure that the Zener diode is clamped to have a current below 0.4mA flowing into EN.

Work Mode Detection

Once enabled, the DC/DC controller outputs a 40μA current to the MODE pin to detect the resistor setting. If the MODE pin voltage exceeds 2.2V, the DC/DC controller works in primary-side regulation (PSR) mode, and the internal EA is enabled. If the MODE pin is connected to GND through a resistor, the DC/DC controller works in secondary-side regulation (SSR) mode, and the internal EA is disabled. Meanwhile, COMP is pulled up to the internal 5V power source through a 10kΩ resistor (see Table 6).

Table 6: MODE Pin Configurations

MODE to GND Resistance (kΩ)			Work Mode	Dead Time (ns)
Min	Typ (1%)	Max		
0	0	3.3	SSR	100
7.32	7.5	8.2	SSR	150
16	16.9	18.7	SSR	200
32.4	32.4	33	SSR	300
64.9	Float	Float	PSR	150

In PSR mode, the V_{OUT} feedback signal is detected by auxiliary winding from the FB pin, and the DC/DC controller reduces the frequency accordingly, but the frequency stays above 30kHz under light loads. In SSR mode, the V_{OUT} feedback signal is detected through the COMP pin, and the DC/DC controller maintains a fixed frequency. Meanwhile, the peak current can be regulated via the COMP voltage until power save mode (PSM) is triggered.

After the DC/DC controller is enabled, the device does not start switching for 500μs. The mode, dead time, dither, and V_{OUT} compensation settings can be detected by the DC/DC controller during this period.

The MODE pin can set the device to PSR or SSR mode, and it can also configure the dead time between the GATE and SYNC pins.

The MODE pin detection current lasts about 200μs. Generally, it is sufficient to place one resistor from MODE to GND. In a noisy environment, the device may require a filtering capacitor placed from MODE to GND. The capacitance should be below 100pF so that the MODE pin voltage can rise to a steady state before the DC/DC controller detects V_{MODE}.

PWM Operation

The MP8030 DC/DC controller can be set in flyback and forward topologies. In a flyback topology, the external N-channel MOSFET turns on at the beginning of each cycle, forcing the current in the transformer to increase. The current through the MOSFET can be sensed. When the sum of the current-sense (CS) signal and the slope compensation signal rises above the voltage set by the COMP pin, the external MOSFET turns off. The transformer current then transmits energy from primary-side winding to secondary-side winding, and the output capacitor is charged through the Schottky diode.

The transformer primary-side current is controlled by the COMP voltage, which itself is controlled by the output feedback voltage. Thus, the output voltage controls the transformer current to satisfy the load. In forward topologies, the energy is transferred from primary to secondary winding when the primary-side N-channel MOSFET is turned on, and the primary-side peak current is controlled by the COMP voltage. The COMP voltage is controlled by the external TL431 and optocoupler feedback.

Voltage Control

There are multiple methods to control the voltage. These methods are described in greater detail below.

Primary-Side Regulation (PSR) Mode

Unlike traditional flybacks with opto-isolator feedback, the MP8030 DC/DC controller can detect the auxiliary winding voltage from the FB pin during the secondary-side output diode conduction period.

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Assume that the secondary winding is the master, and the auxiliary winding is the slave. When the secondary-side diode conducts, the FB voltage can be calculated with Equation (1):

$$V_{FB} = \frac{N_A}{N_S} \times (V_{OUT} + V_{DOF}) \times \frac{R_{FBL}}{R_{FBH} + R_{FBL}} \quad (1)$$

Where V_{DOF} is the output diode forward-drop voltage, V_{OUT} is the output voltage, N_A and N_S are the turns of the auxiliary winding and the secondary-side output winding, respectively, and R_{FBH} and R_{FBL} are the resistor dividers for FB sampling.

Figure 5 shows the discontinuous conduction mode (DCM) condition for FB sampling.

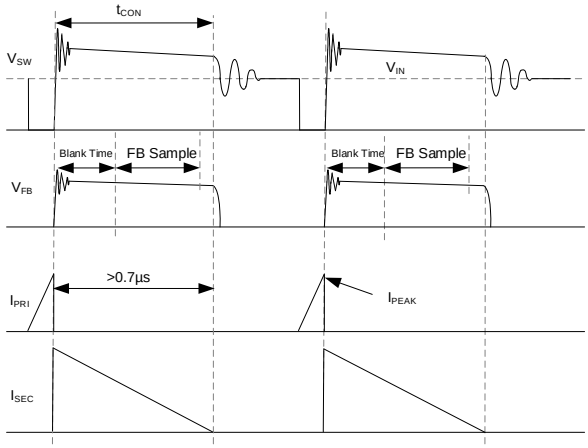

Figure 5: DCM Condition FB Sample

Figure 6 shows the continuous conduction mode (CCM) condition for FB sampling.

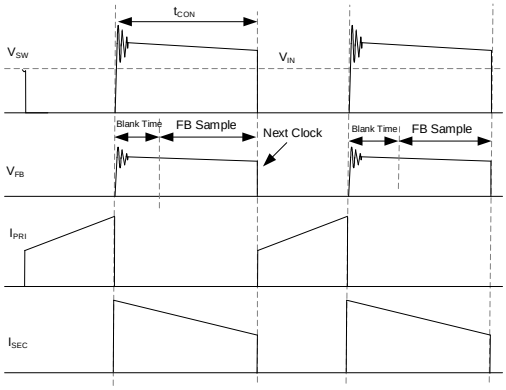

Figure 6: CCM Condition FB Sample

The DC/DC controller regulates the primary-side MOSFET switching to keep the V_{CS} current signal above 36mV (typically), and starts sampling the auxiliary winding voltage after the power MOSFET turns off. A 300ns blanking time is added to prevent spike ringing due to the leakage inductance. To guarantee that there is a sufficiently long FB sample period, the output diode current conduction time (t_{CON}) under light loads (before the diode current drops to 0A in each cycle) should be longer than 600ns. Generally, design the transformer and insure that t_{CON} is longer than 700ns and V_{CS_PK} = 33mV. The DC/DC controller GATE signal also provides a 1.2µs minimum off time, though it is limited by a maximum 70% duty cycle. This guarantees that there is a sufficient FB sample time when the DC/DC controller works with a high duty cycle.

During the FB sense period, the FB signal is sent into the negative input of the EA, and this value is held after the sense window elapses. The EA output is generated on the COMP pin and controls the transformer peak current to match the output regulation requirement.

Secondary-Side Regulation (SSR) Mode

The MP8030 DC/DC controller can also be set for traditional SSR mode. In SSR mode, the V_{OUT} signal is fed back to the COMP pin through one optocoupler. All the PSR FB voltage detection functions are disabled, and FB should be connected to GND.

Under light loads, the DC/DC controller maintains a fixed frequency. In SSR mode, the peak current drops low following the COMP voltage, until the PSM threshold is triggered. The 36mV minimum current limit does not work in SSR mode.

In SSR mode, the DC/DC controller can support both flyback and forward topologies, while the device can only support a flyback topology in PSR mode.

Output Voltage Compensation

In PSR mode, the auxiliary winding waveform reflects the secondary-side winding voltage, but output voltage (V_{OUT}) differs from the output winding voltage due to output diode voltage drop, as well as power winding resistance. The dropout voltage varies when the conducted current changes.

The resistance from the CS pin to GND can set the compensation gain of the dropout voltage when the current varies. The current-sense signal is filtered internally, and then controls the

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current sinking from the FB pin based on the average voltage from the CS pin. There are 3 types of different current gains, from the average CS voltage to the FB sinking current (see Table 7). The FB sinking current leads to a voltage drop on the FB high-side feedback resistor so that it compensates V_{OUT} (see Figure 7).

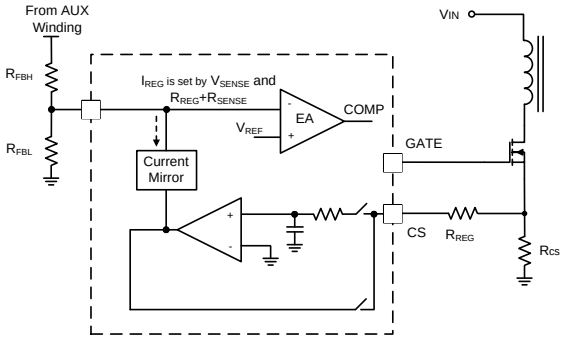

Figure 7: Output Voltage Compensation

In SSR mode, this voltage compensation function is disabled.

Frequency Dithering

The DC/DC controller integrates one frequency dithering circuit to minimize EMI emissions. During steady state, the frequency is fixed internally, but frequency dithering circuit is added to the configured frequency with 1.5kHz modulation. In PSR mode, the frequency dithering is fixed at ±6% of the switching frequency (f_{SW}). In SSR mode, the frequency dithering can be configured to be ±3%, ±6%, or ±9%, based on the resistor connected from the CS pin to GND.

Table 7 lists the dithering and V_{OUT} compensation configuration options.

Table 7: CS Pin Configurations

CS to GND Resistance (kΩ)			PSR Mode		SSR Mode
Min	Typ (1%)	Max	Dither Range (kHz)	I_{FB} / V_{CS} Ratio (uA/mV)	Dither Range (kHz)
0	0	1.3	0	0	0
3	3.3	3.6	±15	0.054	±7.5
6.2	6.8	7.5	±15	0.108	±15
12.7	12.7	13	±15	0.216	±22.5
24.9	25.5	28	±15	0	±22.5

The CS pin detection current lasts about 200µs after start-up. Generally, it is sufficient to connect a resistor between the CS and GND pins. In noisy environments, a capacitor may be required between CS and GND to provide filtering.

Current Sense and Over-Current Protection (OCP)

The MP8030 DC/DC controller is a peak current mode flyback/forward controller. The current through the external MOSFET can be sensed through a sensing resistor, which is connected in series with the MOSFET's source. The sensed voltage on the CS pin is then amplified and fed to the high-speed current comparator for current control mode. The current comparator takes this sensed voltage (plus the slope compensation) as one of its inputs, then compares it with the COMP voltage. When the amplified current signal exceeds the COMP voltage, the comparator outputs low, turning off the power MOSFET.

If the voltage on the CS pin exceeds the current limit threshold voltage (typically 160mV), the DC/DC controller turns off the GATE output for that cycle until the internal oscillator starts the next cycle and senses the current again. The DC/DC controller limits the current of the MOSFET cycle-by-cycle.

Error Amplifier (EA)

In PSR mode, the DC/DC controller senses the FB voltage during the flyback period with an FB signal pulse. Then the FB signal is held and fed to the error amplifier (EA). The EA regulates the COMP voltage based on the FB signal. The COMP voltage controls the transformer's peak current to regulate the output voltage.

In SSR mode, the internal EA is disabled, and the COMP pin is pulled up by an internal resistor. The external optocoupler can be connected to the COMP pin for the V_{OUT} signal feedback.

Light-Load Control

Under light-load conditions in PSR mode, the COMP voltage decreases to regulate the lower transformer peak current. If the sensed peak current signal is below 36mV, the DC/DC controller does not decrease the transformer current and it decreases the frequency. As a result, the transferred energy decreases and the output voltage is regulated.

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The DC/DC controller limits the minimum frequency above 30kHz under light loads in PSR mode. This can help detect V_{OUT} with a minimum frequency and prevent audible noise. This minimum frequency requires a load to maintain V_{OUT}; otherwise, V_{OUT} can rise and trigger over-voltage-protection (OVP).

Under light loads in SSR mode, the DC/DC controller maintains a fixed frequency and COMP continues to drop until it reaches the PSM threshold.

Over-Voltage Protection (OVP)

The DC/DC controller features OVP. If the voltage at FB exceeds 125% of V_{REF}, the DC/DC controller shuts off the gate driving signal and enters hiccup mode immediately. The DC/DC controller restarts after 340ms and resumes normal operation if the fault is removed.

To avoid the mistriggering due to the oscillation of the leakage inductance and the parasitic capacitance, OVP sampling has a blanking time.

OVP is supported by sensing the auxiliary winding switching voltage in flyback designs. It can be enabled by sensing V_{CC} in active-clamp forward designs (see the OVP Design for Active-Clamp Forward section on page 37 for details).

Pull the FB pin to GND to disable OVP in SSR flyback/forward topology designs.

Overload Protection (OLP)

The DC/DC controller limits the peak current cycle-by-cycle under over-current protection (OCP) conditions. If the load continues increasing after triggering OCP, V_{OUT} decreases and the peak current triggers OCP every cycle.

The DC/DC controller sets overload detection by monitoring the CS pin voltage. Once the internal soft start finishes, overload protection (OLP) is enabled. If an OCP signal is detected and lasts for longer than 4.8ms, the DC/DC controller turns off the GATE driver. After a 340ms delay, the DC/DC controller restarts with a new start-up cycle. During OLP, a one-shot timer is activated for 50µs after one OCP pulse. That means if there is one OCP pulse in a 50µs period, the DC/DC controller registers this as an OCP condition. If this condition is removed within 4.75ms, the DC/DC controller returns to normal operation.

Short-Circuit Protection (SCP)

When the output is shorted to ground, the part works in OCP mode and the current is limited cycle-by-cycle. In this scenario the part may trigger OLP.

If the peak current cannot be limited by the 160mV CS voltage in every cycle due to minimum gate on time, the current may run away and the transformer may saturate. If the monitored CS voltage reaches 300mV, the part turns off GATE and initiates hiccup protection immediately with a 340ms off time.

If the short circuit is removed, V_{OUT} recovers after the next restart cycle with a 340ms delay.

Soft Start (SS)

The DC/DC controller provides soft start (SS) by charging an internal capacitor with a current source. During soft start, the SS signal controls the voltage of the internal capacitor and ramps up slowly. The SS capacitor is discharged completely in the event of a commanded shutdown, thermal shutdown, or a protection.

In PSR mode, the SS signal clamps the FB reference voltage. The FB reference's soft-start time is typically 15ms, with a voltage between 0V and 2V.

In SSR mode, the SS signal clamps the COMP voltage until COMP rises up to match the switching current. The SS signal continuously ramps up with the same rate. Generally, COMP takes about 20ms to ramp from 1.5V to 3.5V.

Minimum On Time

The transformer parasitic capacitance and gate driver signal induce a current spike on the CS resistor when the power switch turns on. The DC/DC controller includes a 250ns leading edge blanking period to avoid falsely terminating the switching pulse. During this blanking period, the current-sense comparator is disabled, and the gate driver cannot switch off.

Gate Driver

The DC/DC controller integrates one high-current gate driver for the primary-side N-channel MOSFET. The high-current gate driver provides a strong driving capability and benefits

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for MOSFET selection. If the external MOFET's Q_G is low and the switching speed is low due to EMI, it is recommended to have a minimum 5Ω resistance.

The DC/DC controller also integrates one SYNC driver pin, which can be used to turn the second switch off when it is high, or turn the second switch on when it is low. Figure 8 shows the phase and dead time relationship between GATE and SYNC.

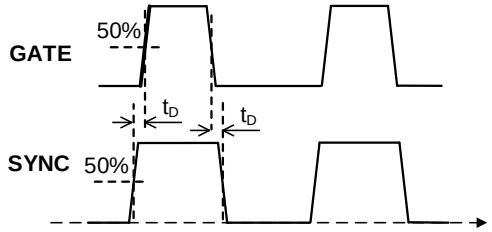

Figure 8: GATE and SYNC Driver

MOSFET selection is limited by its minimum gate charge (Q_G). Regarding information for if the MP8030 is designed as an active-clamp-forward circuit, see the OVP Design for Active-Clamp Forward section on page 37.

If the IC turns off due to UVLO or a different protection, both the GATE and SYNC pins maintain a low voltage level.

Transformer Inductance Consideration

In PSR mode, the DC/DC controller samples V_{OUT} during the flyback time. The secondary diode conduction time with a minimum peak current (controlled by a 33mV minimum CS limit) should be longer than 0.7μs. The transformer inductance should also be sufficiently high. The transformer's primary inductance can be calculated with Equation (2):

$$L_{PRI} \geq (V_{OUT} + V_{DOF}) \times \frac{N_P}{N_S} \times 0.7\mu s \times \frac{R_{SENSE}}{33mV} \quad (2)$$

Where V_{DOF} is the output rectifier diode's forward-drop voltage.

In SSR mode, there is no limit for inductance, but it is recommended to set the peak current high enough to avoid triggering PSM logic if the device is designed for CCM mode. This is because PSM may result in a higher output voltage ripple, especially in sync mode forward topologies.

Over-Temperature Protection (OTP)

Thermal shutdown is implemented to prevent the chip from thermal runaway. The MP8030 has a separate temperature monitoring circuit for the PD and DC/DC power controller. The two thermal protections do not affect one other. Once the temperature drops below its recovery threshold, the thermal shutdown condition is removed, and the MP8030 is enabled.

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APPLICATION INFORMATION

Selecting a TVS Diode

To limit the input transient voltage within the absolute maximum ratings, a TVS diode should be placed across the rectified voltage (between VDD and GND). It is recommended to use a SMAJ58A or a diode with an equivalent protection voltage for general indoor applications. The outdoor transient levels (or special applications) require additional protection.

Selecting the PD Input Capacitor

A 0.05μF to 0.12μF input bypass capacitor must be placed from VDD to GND for IEEE 802.3bt standard specifications. A 0.1μF, 100V ceramic capacitor is recommended.

Selecting the Classification Resistors (R_{CLSA} and R_{CLSB})

Connect a resistor from CLSA and CLSB to GND to configure the classification current according to the IEEE 802.3bt standard. The assigned class power should correspond to the maximum average power drawn by the PD during operation. To select R_{CLSA} and R_{CLSB}, see Table 1 on page 25.

Wall Power Adapter Detection Circuit

The MP8030 PD features wall power adapter detection. Once the input voltage (between VADP and GND) exceeds about 8.3V, the PD enables wall adapter detection. Then the resistor divider from VADP to the AUX pin can configure the threshold to switch from the PoE to an adapter (see Figure 9).

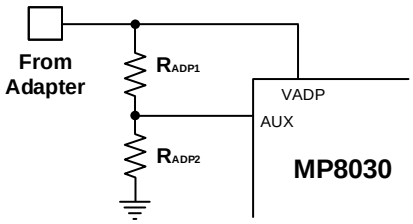

Figure 9: Wall Adapter Threshold Setting

PG Pin Setting

The PG pin is an active high, open-drain output that requires an external pull-up resistor. The PG pin's maximum sinking current should be limited below 3mA, so a 20kΩ to 100kΩ pull-up resistor should be place between SRC and PG. Connect PG to the DC/DC controller's downstream EN pin to enable the downstream DC/DC converter.

PG is in high impedance if all of the following conditions are met:

- The steady current limit changes, which means the inrush period is complete.
- t_{DELAY} (about 90ms) from UVLO is complete.

Then wall power adapter is detected on AUX, and V_{ADP} exceeds its UVLO threshold.

BT, TYP1, TYP2 Indicator Connection

The BT, TYP1, and TYP2 pins are active low, open-drain outputs that indicate the PSE type or the presence of a wall adapter. Optocouplers can interface these pins to circuitry on the secondary side of the converter. Design the optocoupler interface for the BT, TYP1, and TYP2 signals (see Figure 10).

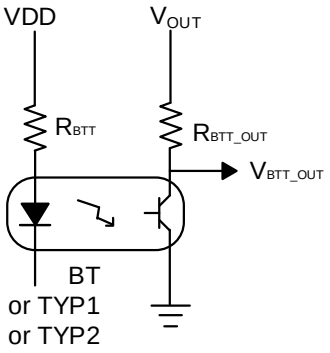

Figure 10: BT, TYP1, and TYP2 Interface

BT, TYP1, and TYP2 should have maximum sinking currents at 3mA, and R_{BTT} should exceed 20kΩ to match the maximum 57V input.

The BT, TYP1, and TYP2 devices each light separate LEDs. These three LEDs indicate the PSE type. When lighting an LED from VDD to BT/TYP1/TYP2, the resistance can be higher to match the LED's maximum current and reduce power loss.

Configurable Current Limit

After the MP8030's V_{DD} exceeds its UVLO threshold, the ILIM pin sources a current that detects the configurable current limit. By connecting ILIM to GND through a resistor (or shorting ILIM to GND), the MP8030's current limit can be configured (see Table 2 on page 26).

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The MP8030 PD also has an inrush current limit function after start-up. This limit is about 1/7 of the steady state current limit.

Selecting the PoE Power MOSFET

The MP8030 PD internal hot-swap MOSFET has a maximum 1.6A current limit. For type 1–3 PDs (≤51W), the internal hot-swap MOSFET can support the application. For type 4 PDs (>51W), an external MOSFET must be placed in parallel with the internal hot-swap MOSFET. The GATE1 pin can drive one external N-channel MOSFET. The MOSFET should be selected to meet the following specifications:

- The voltage rating should be 100V at minimum for high-voltage surge environments.
- On resistance ($R_{DS(ON)}$): $R_{DS(ON)}$ should be below 200mΩ for power dissipation considerations and for light-load shutdown functions. A 100mΩ $R_{DS(ON)}$ is recommended.
- Gate charge (Q_G): Q_G is recommended to be as small as possible to satisfy faster response times under overload conditions. It is recommended for Q_G to be below 15nC (V_{GATE} = 4.5V).
- The gate threshold voltage should be below 4V to fully drive the GATE1 and GATE2 voltages.

SENSE Pin Setting

The external parallel MOSFET current limit is configured by a resistor (R_{SENSE}) between the VDD and SENSE pins. It is recommended for R_{SENSE} to be 18mΩ. The total current limit can be calculated with Equation (3):

$$I_{IN_LIM} = I_{INNER} + \frac{26mV}{R_{SENSE}} \quad (3)$$

Where I_{IN_LIM} is the MP8030 PD total current limit, and I_{INNER} is the MP8030 PD internal hot-swap MOSFET current limit. When the external MOSFET is connected, it is recommended to set I_{INNER} to 0.9A.

Selecting the Adapter's MOSFET

The MP8030 PD's GATE2 pin is designed to drive one external N-channel MOSFET for the adapter supply. Select the adapter MOSFET using the same guidelines for the PSE MOSFET.

Output Voltage Setting

For the MP8030 DC/DC controller, there are two feedback modes (PSR and SSR).

In PSR mode, the converter detects the auxiliary winding voltage from the FB pin. R_{FBH} and R_{FBL} comprise the resistor divider used for feedback sampling (see Figure 11).

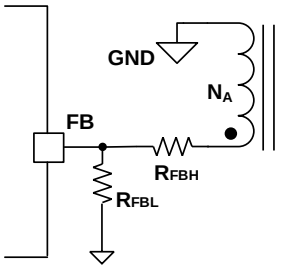

Figure 11: Feedback in PSR mode

When the primary-side power MOSFET turns off, the auxiliary winding voltage is proportional to the output winding. V_{OUT} can be estimated with Equation (4):

$$V_{OUT} = \frac{V_{REF} \times (R_{FBH} + R_{FBL})}{R_{FBL}} \times \frac{N_S}{N_A} - V_{DOF} \quad (4)$$

Where N_S is transformer's secondary-side winding turns, N_A is transformer's auxiliary winding turns, V_{DOF} is the output rectifier diode's forward-drop voltage, and V_{REF} is the reference voltage on the FB pin.

When the main power MOSFET turns on, the auxiliary winding voltage is negative, and the FB voltage is limited at about -0.7V. The current flowing out of the FB pin can be estimated with Equation (5):

$$I_{FB} = \frac{1}{R_{FBH}} \times (\frac{V_{IN} \times N_A}{N_P} - 0.7) \quad (5)$$

R_{FBH} should be high enough to limit the FB negative current below 1mA. However, due to FB parasitic capacitance, R_{FBH} should be not too high. It is recommended for R_{FBH} to be between 49.9kΩ and 100kΩ.

In SSR mode, the output voltage is set by an external TL431 regulator. If the TL431's reference voltage is 2.5V, and the expected output voltage is 12V, then the upper and lower

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resistor divider ratio is 3.8. Then TL431 generates an amplified signal and controls the MP8030 DC/DC controller's COMP pin through an optocoupler, such as PC357. COMP controls the current, and then V_{OUT} is regulated based on the feedback signal.

Work Mode Setting

Once enabled, the MP8030 DC/DC controller outputs a 40μA current to the MODE pin to detect the MODE resistance. If the MODE pin's voltage exceeds 2.2V, the MP8030 DC/DC controller works in PSR mode or SSR mode. The MODE pin can also configure the dead time between the GATE and SYNC pins (see Table 6 on page 30).

VCC Power Supply Setting

The VCC voltage is regulated by the internal LDO from AVIN. V_{CC} is typically regulated to 8.5V. It is recommended to place a decoupling capacitor between VCC and GND

In flyback mode, the VCC capacitor is recommended to be 1μF at minimum. V_{CC} can also be powered from transformer auxiliary winding to reduce high-voltage LDO power loss (se Figure 12).

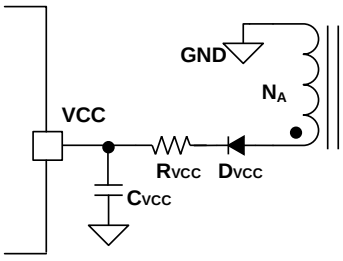

Figure 12: Flyback V_{CC} from N_A Winding

The auxiliary winding supply voltage can be calculated with Equation (6):

$$V_{CC} = \frac{N_A}{N_S} \times (V_{OUT} + V_{DOF}) - V_{DVCCF} \quad (6)$$

Where V_{DVCCF} is the diode (D_{VCC}) voltage drop from auxiliary winding.

In forward mode, the VCC capacitor is recommend to be 4.7μF at minimum. V_{CC} can also be powered from transformer auxiliary winding (see Figure 13).

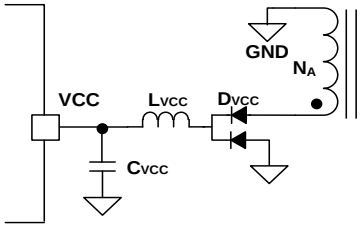

Figure 13: Forward V_{CC} from N_A Winding

The auxiliary winding supply voltage can be calculated with Equation (7):

$$V_{CC} = \frac{N_A}{N_S} \times V_{OUT} \quad (7)$$

V_{CC} should be below 16V.

OVP Design for Active-Clamp Forward

In active-clamp forward, the FB pin cannot directly sense a V_{OUT} OVP event unless an isolated sense circuit is added. The FB pin supports V_{OUT} OVP by monitoring V_{CC}, which is proportional to V_{OUT} based on the transformer turns ratio; this indirect V_{OUT} OVP sensing can serve as supplemental protection in the event of V_{OUT} optocoupler feedback failure.

In active-clamp forward, V_{CC} is supplied by a non-synchronous rectifier circuit (see Figure 13). V_{CC} is charged through a diode (D_{VCC}) and inductor (L_{VCC}) (see Figure 14). The V_{CC} consumption current should be high enough to keep V_{CC} in regulation, because the inductor current (I_L) is always in the direction of V_{CC} with the diode rectifier, and the MP8030 switches with a fixed frequency. If the V_{CC} consumption current falls below the minimum V_{CC} load requirement, V_{CC} is charged high cycle by cycle, which may trigger OVP even if V_{OUT} is still within regulation.

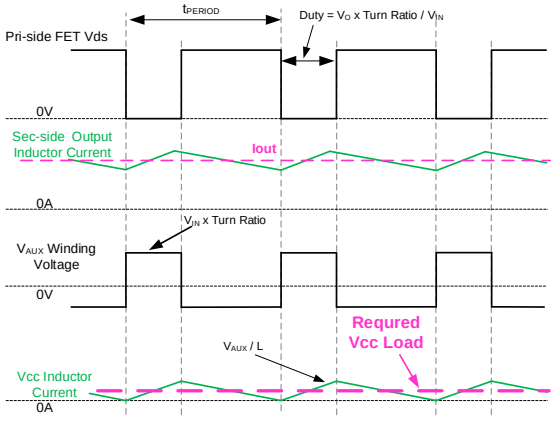

Figure 14: V_{CC} Minimum Load Requirement

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To design an appropriate OVP circuit, consider the following:

1. The transformer turns ratio determines the nominal V_{CC}.
2. For the OVP resistor divider, the OVP threshold should be set with margin from the nominal V_{CC} to the OVP threshold. It should be ≥125% the nominal V_{CC}, a ≤16V OVP threshold is recommended.
3. For the V_{CC} rail inductance, the average inductor current (I_L) in boundary CCM determines the minimum V_{CC} load requirement to keep V_{CC} in regulation.
4. The lowest value between the f_{SW} tolerance and V_{CC} inductance is used as the highest V_{CC} supplied current and the highest V_{CC} load is required in design.
5. When selecting the MOSFET Q_G, Q_G adds driving current from V_{CC} based on Q_G x f_{SW}. The minimum Q_G should be limited to balance the load current compared to the charge current from the V_{CC} inductor. An N-channel MOSFET with a minimum >17.5nC Q_G and a P-channel MOSFET with a >5nC Q_G may be necessary (see Table 8).

The V_{CC} consumption current includes the Q_G driving current, OVP resistor divider bleed current, and a 1.1mA CCM operation current. An additional resistor dummy load on V_{CC} is required if the V_{CC} consumption current is lower than the minimum V_{CC} load requirement (see Figure 14 on page 37).

Table 8 shows one design example for OVP and its components selection.

Table 8: Active-Clamp Forward OVP Design and Component Selection Example (14)

Max PoE Input	57V
V_{OUT} Regulation Voltage	12V
Transformer Turns Ratio (primary-side winding:secondary-side winding:V_{CC} winding)	20:10:8
OVP Resistor Divider	100kΩ + 20kΩ
V_{CC} Inductor	1mH ±10%
Q_G Limit for Main N-Channel MOSFET	>17.5nC (e.g. FDMS86250)
Q_G Limit for Clamp P-Channel MOSFET	>5nC (e.g. Si2325)

Note:

14) All MOSFET Q_G values in Table 8 are based on V_{GS} = 10V and V_{DS} = 75V (or -75V) with tolerance consideration.

If considering changes for circuit design and components selection while V_{CC} OVP is enabled, contact an MPS FAE.

V_{OUT} Compensation and Frequency Dithering Setting

The CS pin can be used to set V_{OUT} compensation as well as the frequency dithering function. Once enabled, the MP8030 DC/DC controller outputs a 100μA current to the CS pin to detect the CS resistance. The MP8030 DC/DC controller determines the compensation type and the frequency dithering type based on the resistance (see Table 7 on page 32).

The V_{OUT} compensation function is only enabled in PSR mode.

Current-Sense Resistor Setting

The MP8030 DC/DC controller is a peak current mode flyback/forward controller. The current through the external MOSFET can be sensed through a current-sense resistor. If the sensed voltage on the CS pin exceeds the current limit threshold voltage (typically 160mV), the MP8030 DC/DC controller turns off the GATE output for that cycle.

To avoid reaching the current limit, the voltage across the current-sense resistor (R_{CS}) should be less than 80% of the current limit voltage (about 160mV). R_{CS} can be estimated with Equation (8):

$$R_{CS} = \frac{0.8 \times 160mV}{I_{PEAK}} \quad (8)$$

Where I_{PEAK} is the primary-side peak current.

Selecting the Power MOSFET

The MP8030 DC/DC controller is capable of driving a wide variety of N-channel power MOSFETS. The critical parameters when selecting a MOSFET are the maximum drain-to-source voltage ($V_{DS(MAX)}$), maximum current ($I_{D(MAX)}$), on resistance ($R_{DS(ON)}$), total gate charge (Q_G), and turn-on threshold (V_{TH}).

In flyback applications, the off-state voltage across the MOSFET (which determines when

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the MOSFET shuts down) can be calculated with Equation (9):

$$V_{MOSFET} = V_{IN} + N \times V_{OUT} \quad (9)$$

Considering the voltage spike when the device turns off, $V_{DS(MAX)}$ should be greater than 1.5 times V_{MOSFET}.

In forward applications, the off-state voltage across the MOSFET is calculated with:

$$V_{MOSFET} = \frac{D \times V_{IN}}{1-D} + V_{IN} \quad (10)$$

Where D is the duty cycle. Generally, the maximum duty cycle is limited at 70%.

The maximum current through the power MOSFET occurs when the input voltage is at its minimum and the output power is at its maximum. The current rating of the MOSFET should be greater than 1.5 times I_{RMS}.

The on resistance of the MOSFET determines the conduction loss. This resistance should be low.

Q_G determines the commutation time. A high Q_G leads to high switching loss, while a low Q_G may cause a fast turn-on/off speed that affects the spike and kick.

In an active-clamp-forward application, the primary-side switching MOSFET's minimum Q_G should be high enough to sink the current from the non-synchronous V_{CC} inductor current. The minimum Q_G limits MOSFET selection (see the OVP Design for Active-Clamp Forward section on page 37 for details).

Consider the turn-on threshold voltage (V_{TH}). GATE is powered by V_{CC}, so V_{TH} must be below V_{CC}.

Selecting the Flyback Transformer

The transformer in a flyback converter determines the converter's duty cycle, peak current, efficiency, MOSFET, and output diode rating. A good transformer should consider the winding ratio, primary-side inductance, saturation current, leakage inductance, current rating, and core selection.

The transformer winding ratio determines the duty cycle. Calculate the duty cycle with Equation (11):

$$D = \frac{N \times V_{OUT}}{N \times V_{OUT} + V_{IN}} \quad (11)$$

Where N is the transformer primary winding to output winding ratio, and D is the duty cycle. Typically, a duty cycle of about 45% is recommended for most applications.

The primary-side inductance affects the input current ripple ratio factor. A high inductance results in a large transformer size and high cost; a low inductance results in high switching peak current and RMS current, which reduces efficiency. Choose a primary-side inductance to make the current ripple ratio factor about 30% to 50% of the input current. Estimate the primary-side inductance with Equation (12):

$$L_P = \frac{V_{IN} \times D^2}{2 \times n \times I_{IN} \times f_{SW}} \quad (12)$$

Where n is the current ripple ratio, I_{IN} is the input current, and L_P is the primary inductance. Calculate L_P based on the minimum input voltage condition.

The transformer should have a high saturation current to support the switching peak current; otherwise, the transformer inductance decreases sharply. The CS resistor can be used to limit the switching peak current.

The energy stored in the leakage inductance cannot couple to the secondary side, causing a high spike when the MOSFET turns off. This decreases efficiency and increases MOSFET stress. Normally, the transformer leakage inductance can be controlled below 3% of the transformer inductance.

The current rating counts the maximum RMS current, which flows through each winding. The current density should be controlled; otherwise, it can cause a high resistive power loss.

Diode Conduction Time Setting (For PSR Flyback)

In PSR mode, the MP8030 DC/DC controller starts sampling the auxiliary winding voltage after the primary power MOSFET turns off.

A blanking time is added in the MP8030 DC/DC controller to prevent spike ringing due to the leakage inductance. To guarantee a sufficiently long FB sample period, the output diode current

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conduction time (t_{CON}) under light loads should be longer than 600ns. Design the transformer and ensure that t_{CON} is longer than 700ns when V_{CS_PK} = 33mV. This relationship can be calculated with Equation (13):

$$\frac{33mV \times L_P \times N_S}{R_{CS} \times N_P \times (V_{OUT} + V_{DOF})} \geq 700ns \quad (13)$$

Where V_{DOF} is the output diode's forward-drop voltage.

Selecting the RCD Snubber for Flyback Applications

The transformer leakage inductance causes spikes and excessive ringing on the MOSFET drain's voltage waveform. An RCD snubber circuit limits the MOSFET voltage spike (see Figure 15).

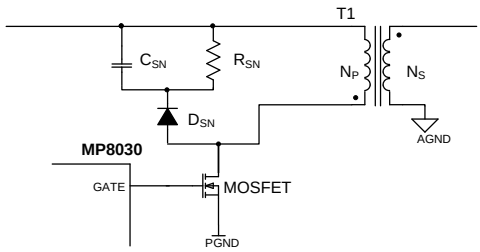

Figure 15: RCD Snubber Circuit

The power dissipation in the snubber circuit can be estimated with Equation (14):

$$P_{SN} = \frac{1}{2} \times L_K \times I_{PEAK}^2 \times f_{SW} \quad (14)$$

Where L_K is the leakage inductance and I_{PEAK} is the peak switching current. Since R_{SN} consumes the leakage inductance power loss, R_{SN} can be calculated with Equation (15):

$$R_{SN} = \frac{V_{SN}^2}{P_{SN}} \quad (15)$$

Where V_{SN} is the expected snubber voltage on the snubber capacitor (C_{SN}).

C_{SN} can be designed to achieve an appropriate voltage ripple on the snubber, estimated with Equation (16):

$$\Delta V_{SN} = \frac{V_{SN}}{R_{SN} \times C_{SN} \times f_{SW}} \quad (16)$$

Generally, a 15% ripple is recommended.

Selecting Output Diode for Flyback Applications

The flyback output rectifier diode supplies current to the output capacitor when the primary-side MOSFET is off. A Schottky diode reduces losses due to the diode's forward voltage and recovery time. The diode should be rated for a reverse voltage 1.5 times greater than V_{DIODE}. V_{DIODE} can be calculated with Equation (17):

$$V_{DIODE} = \frac{V_{IN}}{N} + V_{OUT} \quad (17)$$

The average current rating must exceed the maximum expected load current, and the peak current rating must exceed the output winding peak current.

It is recommended to use an RC snubber circuit for the output diode.

Selecting the Forward Transformer

The forward transformer transfers energy to output when the power MOSFET turns on. This transformer's key parameters are the winding ratio, primary winding turns, current rating, and core selection.

The transformer winding ratio determines the duty cycle (D). D can be estimated with Equation (18):

$$D = \frac{V_{OUT} \times N}{V_{IN}} \quad (18)$$

Where N is the transformer's primary winding to output winding ratio. A duty cycle of about 45% is recommended for most applications.

The transformer winding ratio affects OVP design with different MOSFET Q_G values. If forward OVP is enabled, the minimum MOSFET Q_G is limited. See the OVP Design for Active-Clamp Forward section on page 37 for details.

When the power MOSFET turns on, the transformer transfers energy to the output. At the same time, the input voltage generates a primary-side current in the transformer. There should be sufficient primary winding to ensure that the transformer does not saturate. The peak exciting current is calculated with Equation (19):

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$$I_{EXC} = \frac{V_{OUT} \times N}{2 \times L_P \times f_{SW}} \quad (19)$$

Where I_{EXC} is the peak primary-side current, and L_P is the primary inductance. Use I_{EXC} to calculate the primary winding. There should be sufficient margins for extreme conditions, such as load transient response and OCP.

The current rating is based on the maximum RMS current, which flows through each winding. The current density should be controlled; otherwise, it can cause a high resistive power loss.

Selecting the Forward SYNC MOSFET

The MP8030 DC/DC controller supports active-clamp forward applications. The active clamp P-channel MOSFET must have same maximum voltage as the main switch power MOSFET, and its maximum current should exceed the peak primary-side current and RMS current.

If V_{CC} OVP monitoring is enabled in the forward circuit, the P-channel MOSFET selection is limited by its minimum Q_G (see the OVP Design for Active-Clamp Forward section on page 37 for details).

Selecting the Forward Output MOSFET

The forward output MOSFET requires two diodes to conduct the current. If higher efficiency is required, the diodes must be replaced by MOSFETs (see Figure 16).

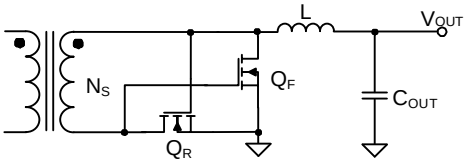

Figure 16: Forward Output MOSFET

The MOSFET voltage rating should exceed the maximum V_{DS} voltage. The maximum V_{DS} voltage for Q_R (V_R) can be calculated with Equation (20):

$$V_R = \frac{D \times V_{IN}}{N \times (1-D)} \quad (20)$$

Where N is the transformer primary winding to output winding ratio, and D is the primary MOSFET duty cycle. A margin is typically required.

The maximum V_{DS} voltage for Q_F (V_F) can be estimated with Equation (21):

$$V_F = \frac{V_{IN}}{N} \quad (21)$$

The MOSFET current rating should exceed its maximum RMS current and peak current. The Q_R RMS current can be estimated with Equation (22)

$$I_R = I_{OUT} \times \sqrt{D} \times \sqrt{1 + \frac{1}{3} \times (\frac{I_{PP}}{I_{OUT}})^2} \quad (22)$$

Where I_{PP} is the L peak-to-peak current.

The Q_F RMS current can be calculated with Equation (23):

$$I_F = I_{OUT} \times \sqrt{1-D} \times \sqrt{1 + \frac{1}{3} \times (\frac{I_{PP}}{I_{OUT}})^2} \quad (23)$$

The Q_R MOSFET's gate driving voltage is equal to V_F, and the Q_F MOSFET's gate driving voltage is equal to V_R. If the driving voltage exceeds the MOSFETs' maximum gate voltage, a clamp circuit is required. The MOSFET's turn-on resistance determines the conduction loss, while Q_G determines the driver circuit loss. These values should be low enough to increase efficiency with a lower rising temperature.

Selecting the Forward Output Inductor

MPL Optimized Performance with MPS Inductor MPL-AY Series

A forward output inductor is required to supply constant current to the output load while the main power MOSFET turns on. A larger-value inductor results in less ripple current and a lower output voltage ripple. However, a larger-value inductor has a larger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance is to allow the peak-to-peak ripple current in the inductor to be approximately 30% to 50% of the maximum output current. The inductance value can be estimated with Equation (24):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT} \times N}{V_{IN}}) \quad (24)$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, f_{SW} is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple

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current. Choose an inductor that does not saturate under the maximum inductor peak current.

MPS inductors are optimized and tested for use with our complete line of integrated circuits.

Table 9 lists our power inductor recommendations. Select a part number based on your design requirements.

Table 9: Power Inductor Selection

Part Number	Inductor Value	Manufacturer
MPL-AY	1µH to 10µH	MPS
MPL-AY1265-2R2	2.2µH	MPS

Visit MonolithicPower.com under Products > Inductors for more information.

Selecting the Input Capacitor

An input capacitor is required to supply the AC ripple current to the inductor while limiting noise at the input source. A low-ESR capacitor is required to minimize the noise at the IC. Ceramic capacitors are recommended, though tantalum or low-ESR electrolytic capacitors are sufficient. For ceramic capacitors, the capacitance dominates the input voltage ripple at the switching frequency.

In flyback mode, the input voltage ripple can be calculated with Equation (25):

$$\Delta V_{IN} = I_{IN} \times \frac{V_{IN}}{f_{SW} \times C_{IN} \times (N \times V_{OUT} + V_{IN})} \quad (25)$$

Where ΔV_{IN} is the input voltage ripple, I_{IN} is the input current, and C_{IN} is the input capacitor.

In forward mode, the input voltage ripple can be estimated with Equation (26):

$$\Delta V_{IN} = \frac{I_{IN}}{f_{SW} \times C_{IN}} \times (1 - \frac{V_{OUT} \times N}{V_{IN}}) \quad (26)$$

Note that this equation ignores the primary-side current, which makes current ripple smaller.

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. For the best results, use ceramic capacitors or low-ESR capacitors to minimize the output voltage ripple. For ceramic capacitors, the capacitance dominates the output voltage ripple at the switching frequency.

In flyback mode, the output voltage ripple can be calculated with Equation (27):

$$\Delta V_{OUT} = \frac{N \times V_{OUT}}{(V_{IN} + N \times V_{OUT}) \times f_{SW}} \times \frac{I_{OUT}}{C_{OUT}} \quad (27)$$

If the output voltage ripple is too high, a π filter is required. Choose the inductor to be between 0.1µH to 0.47µH to achieve an optimal output voltage ripple and system stability.

In forward mode, the output voltage ripple can be estimated with Equation (28):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT} \times N}{V_{IN}}) \quad (28)$$

Design Example

Table 10 is a forward design example following the application guidelines for the specifications below.

Table 10: Forward Design Example

PoE Input	41V to 57V
V_{OUT}	5V
I_{OUT}	14A

The detailed application schematic is shown in Figure 20 on page 45. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section on page 19. For more device applications, refer to the related evaluation board datasheet.

Table 11 is a flyback design example following the application guidelines for the specifications below.

Table 11: Flyback Design Example

PoE Input	41V to 57V
V_{OUT}	12V
I_{OUT}	6A

The detailed application schematic is shown in Figure 21 on page 45. For more device applications, refer to the related evaluation board datasheet.

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PCB Layout Guidelines

An efficient PCB layout for the PoE front-end and high-frequency switching power supply are critical for stable operation. A suboptimal layout may result in reduced performance, excessive EMI, resistive loss, and system instability. For the best results, refer to Figure 17, Figure 18 and Figure 19 on page 44, and follow the guidelines below.

The PD Interface Circuit

All component placements must follow the power flow from RJ-45, the Ethernet transformer, the diode bridges, the TVS diode to 0.1μF capacitor, and the DC/DC converter's input bulk capacitor.

1. Ensure that all power connections are as short as possible with wide traces.
2. Place the current-sense resistor (R_{SENSE}) as close to VDD pin as possible.
3. Use a Kelvin connection between R_{SENSE} and the SENSE pin for an accurate current limit.
4. Place the PoE input capacitor as close to the VDD pin as possible.
5. Place the adapter's input capacitor as close to the VADP pin as possible.
6. Place the SRC capacitor as close to the SRC pin as possible.
7. Place a wide copper plane and vias under the MP8030, PoE power MOSFET and adapter MOSFET to improve thermal performance.

Forward Toplogy

1. Keep the input loop between the input capacitor, transformer, MOSFET, CS resistor, and GND plane as short as possible for minimal noise and ringing.
2. Keep the active-clamp loop between the input capacitor, transformer, C5, and Q3 as short as possible for minimal noise and ringing.
3. Keep the output high-frequency current loop between the transformers, Q_4, and Q_5 as short as possible.
4. The VCC capacitor must be placed close to the VCC and GND pins for the best decoupling.
5. Route the COMP feedback trace far away from noisy sources, such as the switching node.
6. Use a single-point connection between power GND and signal GND.

Figure 17 shows the recommended forward layout, which is based on the Typical Application section on page 2. For more details, refer to the related evaluation board datasheet.

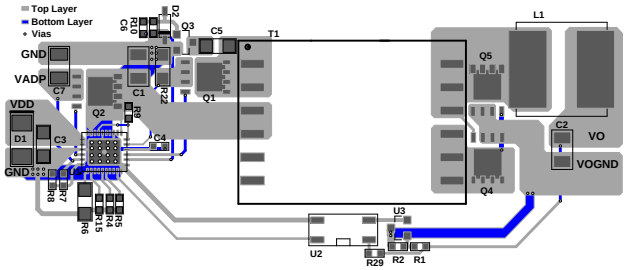

Figure 17: Recommended PCB Layout for Forward Topology

Flyback Topology

1. Keep the input loop between the input bulk capacitor, transformer, MOSFET, CS resistor, and GND plane as short as possible for minimal noise and ringing.
2. Keep the output loop between the rectifier MOSFET, output capacitor, and transformer as short as possible.
3. The clamp loop circuit between D_{SN}, C_{SN}, and the transformer should be as small as possible.
4. The VCC capacitor must be placed close to the VCC and GND pin for the best decoupling.
5. Route the feedback trace far away from noisy sources, such as the switching node.
6. Place the COMP components close to the COMP pin.
7. Use a single-point connection between power GND and signal GND.

Figure 18 on page 44 shows a recommended flyback layout. For more details, refer to the related evaluation board datasheet.

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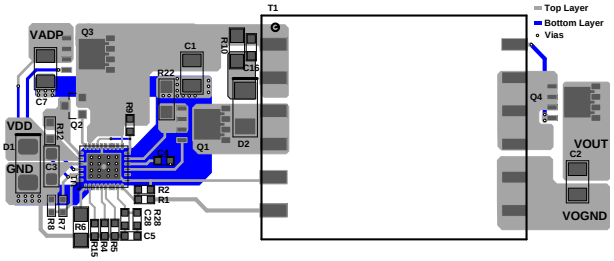

Figure 18: Recommended PCB Layout for Flyback Topology

Figure 19 shows the recommended schematic for a flyback layout.

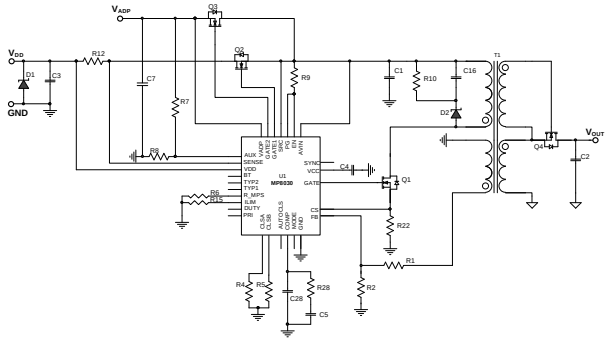

Figure 19: Recommended Flyback Layout

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TYPICAL APPLICATION CIRCUITS

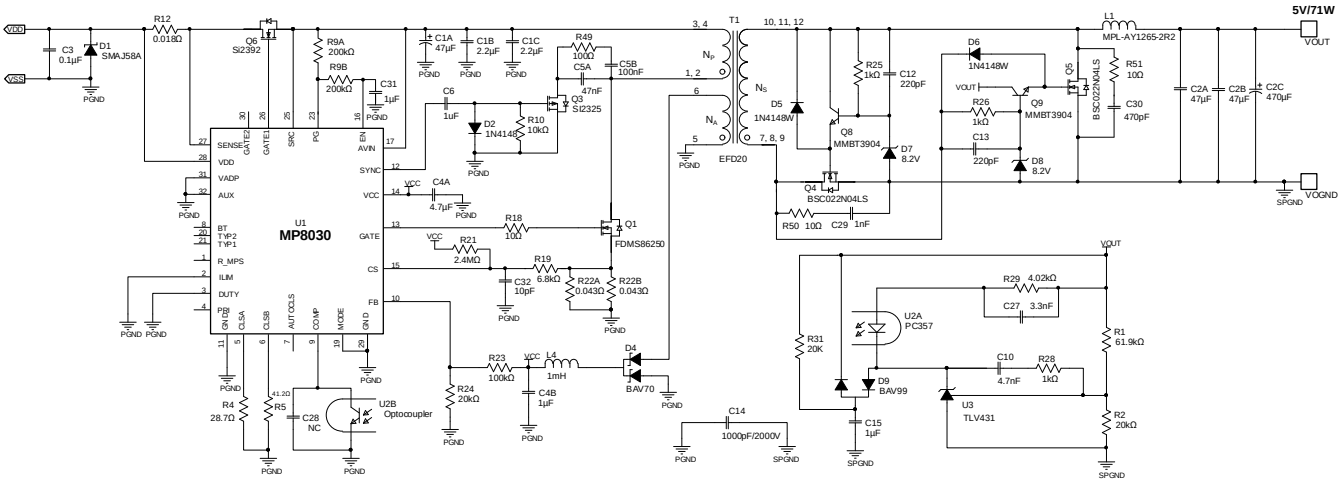

Figure 20: Typical SSR Forward Application Circuit (V_{IN} = 41V to 57V, V_{OUT} = 5V, I_{OUT} = 14A)

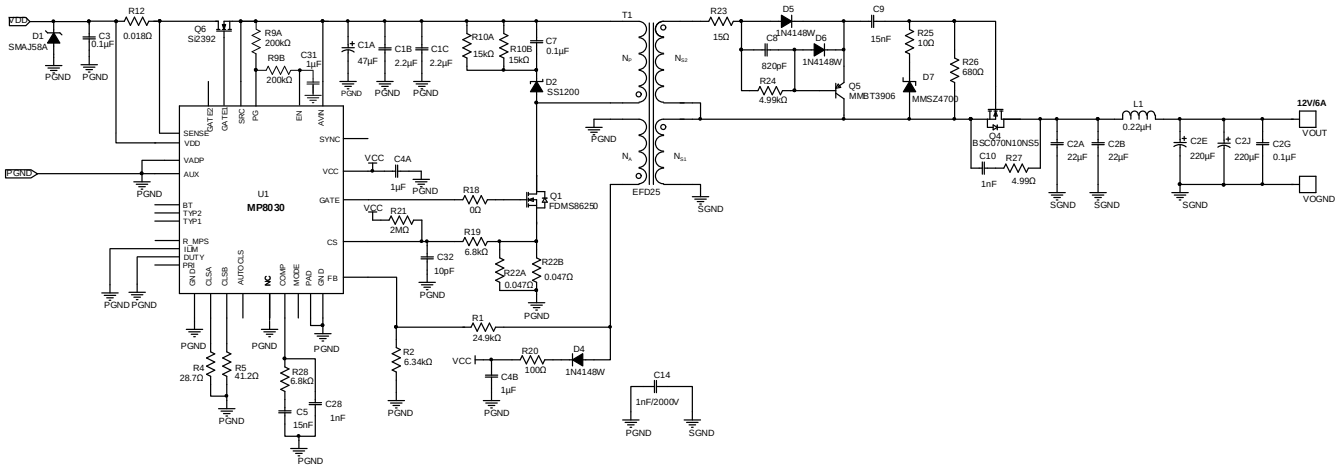

Figure 21: Typical PSR Flyback Application Circuit (V_{IN} = 41V to 57V, V_{OUT} = 12V, I_{OUT} = 6A)

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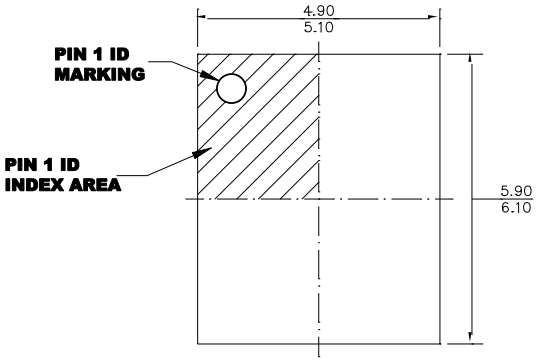
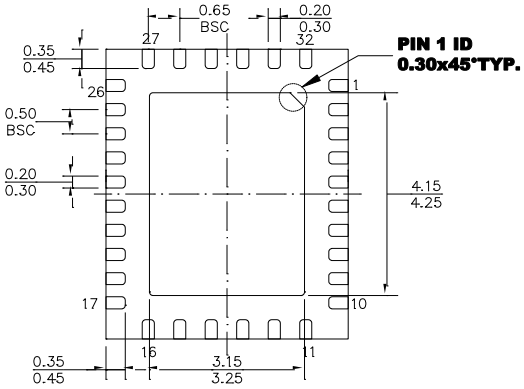
PACKAGE INFORMATION

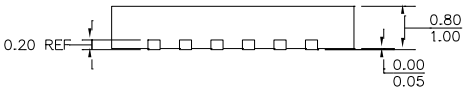
QFN-32 (5mmx6mm)



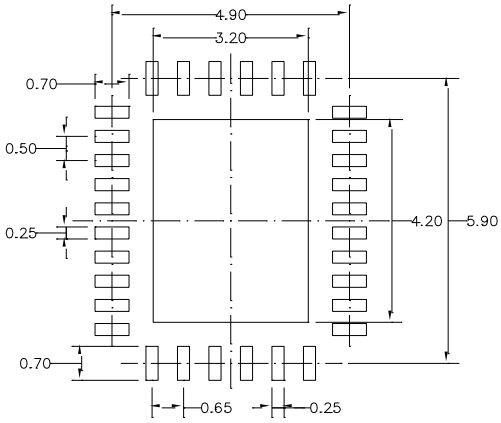
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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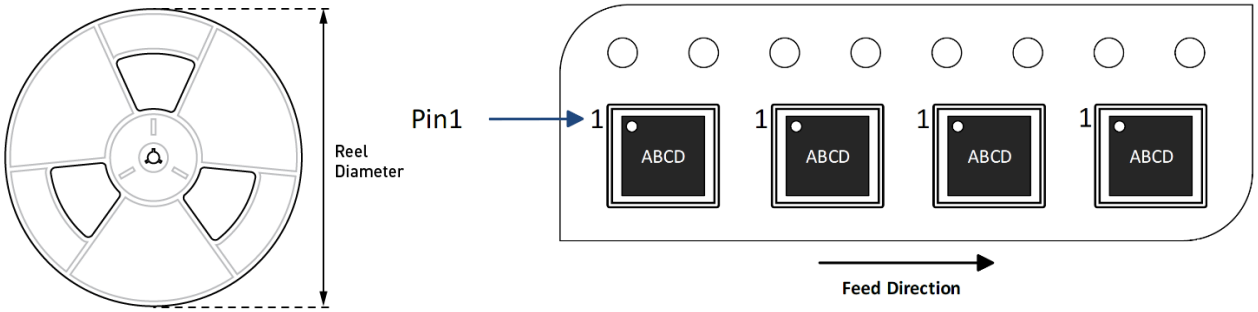
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP8030GQJ-Z	QFN-32 (5mmx6mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	1/31/2022	Initial Release	-
1.1	4/30/2025	Added “Accurate Over-Voltage Protection (OVP) for Active-Clamp Forward without Isolated Sensing Based on the Appropriate MOSFET Q_G Selection” to the Features section; added note 1.	1
		Updated descriptions for pins 9, 10, 12, and 13 in the Pin Functions section.	4
		Moved descriptions for pins 18-22, 24 in the Pin Functions section to page 5.	5
		Updated all note numbers.	6–13
		Added conditions information for the FB OVP threshold parameter in the Electrical Characteristics section.	11
		Minor grammatical updates in the Frequency Dithering section.	32
		Added additional description to the Over-Voltage Protection (OVP) section.	33
		Added additional description to the Gate Driver section; minor formatting updates.	34
		Correct any page references that need to be updated due to the added content	34, 43, 45
		Added new OVP Design for Active-Clamp Forward section, Figure 14, Table 8, and note 14.	37–38
		Added additional description to the Selecting the Power MOSFET section; minor formatting updates.	39
		Added additional description to the Selecting the Forward Transformer section; minor formatting updates.	40
		Updated figure numbers for Figures 15, 16, 17, 18, 19, 20, 21.	40–45
		Added additional description to the Selecting the Forward SYNC MOSFET” section; minor formatting updates.	41
		Updated table numbers for Tables 9, 10.	42

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