MP7758

18V, 2 x 15W Stereo BTL, Fixed-Frequency, Inductorless Class-D Audio Amplifier

DESCRIPTION

The MP7758 is an inductorless, analog input class-D audio amplifier that drives stereo speakers in a bridge-tied load configuration. The device is a fully integrated audio amplifier, which reduces solution size dramatically. It integrates 240mΩ power MOSFETs and short-circuit protection circuits.

The MP7758 features start-up/shutdown pop elimination, as well as advanced EMI performance. The device can pass EMC tests without an inductor.

The device utilizes a stereo BTL structure capable of delivering 15W per channel into 8Ω speakers with a 16V power supply. MPS class-D audio amplifiers exhibit the high fidelity of class-AB amplifiers, with high efficiency.

The MP7758 includes an internal circuit that allows the system to automatically shut down after the absence of an audio signal is detected. This feature is well-suited for energy-using products and battery-operated applications.

The device offers an adjustable power limit (PLIMIT) function. The PLIMIT circuit sets a limit on the output peak-to-peak voltage. This is done by limiting the duty cycle to a fixed maximum value. This limit functions as a virtual voltage rail, and is lower than the supply connected to PVCC.

The MP7758 is available in a TSSOP-28 EP package.

FEATURES

- 5V to 18V Operation from a Single Supply
- ±5A Peak Current Output
- Output Power:
  - 9.5W/Channel at 12V, 8Ω Load, 10% THD
  - 15W/Channel at 16V, 8Ω Load, 10% THD
- 90% Efficiency with 8Ω Load, 10% THD, 1kHz, 12V Supply Voltage
- 240mΩ Power MOSFETs
- Start-Up/Shutdown Pop Elimination
- Short-Circuit Protection Circuits
- Inductorless Topology
- Advanced EMI Performance
- All Switches Current Limited
- Internal Under-Voltage Protection (UVP)
- Internal Thermal Protection
- Adjustable Power Limit
- Automatic Shutdown with Zero Input Signal Detection
- Fault Output Flag
- Available in a TSSOP-28 EP Package

APPLICATIONS

- Wireless/Portable Speakers
- TVs
- DVD Receivers
- Active Speakers

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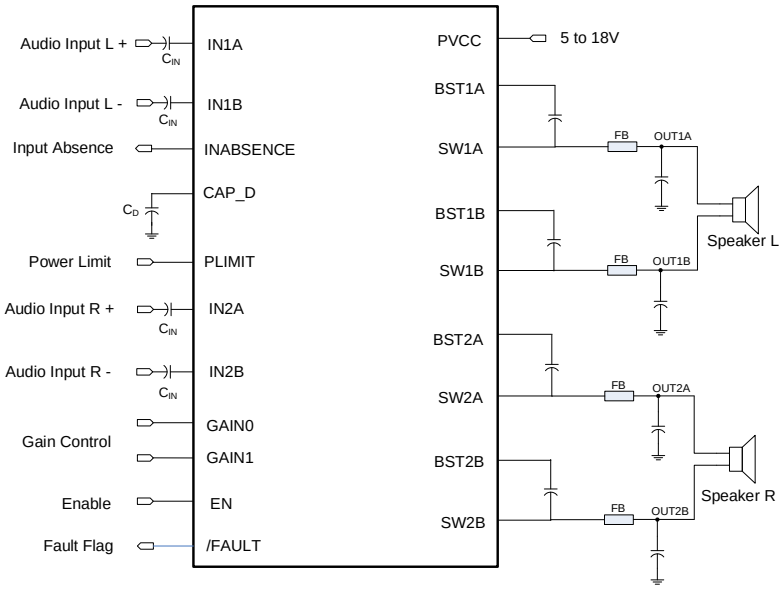
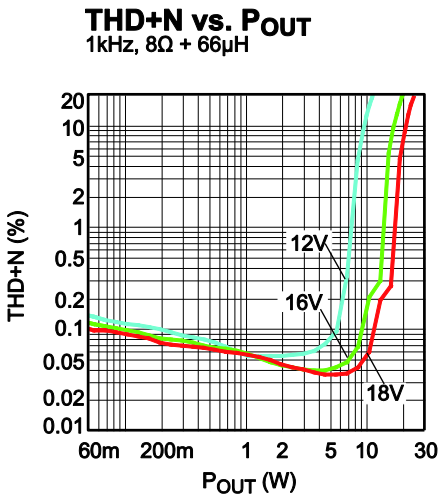
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP7758GF	TSSOP-28 EP	*See Below*	2a

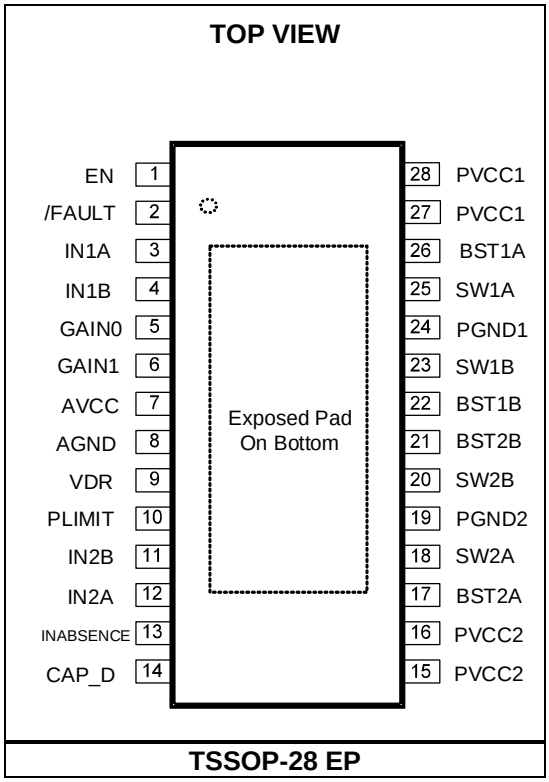
* For Tape & Reel, add suffix –Z (e.g. MP7758GF–Z).

TOP MARKING

MPSYYWW
MP7758
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP7758: Part number
LLLLLLLLL: Lot number

PACKAGE REFERENCE



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PIN FUNCTIONS

Pin #	Name	Description
1	EN	**Enable input.** Drive the EN pin high to turn the four amplifiers on (1A, 1B, 2A, and 2B); drive EN low to turn them off.
2	/FAULT	**Fault output.** A low output at the /FAULT pin indicates that the IC has detected an over-temperature or over-current condition. This output is open drain.
3	IN1A	**Positive audio input for channel 1.** Biased at 2.5V.
4	IN1B	**Negative audio input for channel 1.** Biased at 2.5V.
5	GAIN0	**Gain selection bit.**
6	GAIN1	**Gain selection bit.**
7	AVCC	**Internal analog reference.** This pin has a 5.5V output. Connect a bypass capacitor from AVCC to AGND.
8	AGND	**Analog ground.**
9	VDR	**Gate drive supply bypass.** VDR powers the internal circuitry and the internal MOSFET gate driver. Bypass VDR to AGND with a 0.1μF to 10μF capacitor.
10	PLIMIT	**Power limiting and anti-clipping feature control.** Connect a resistor divider from AVCC to GND to set the power limit. Connect a resistor divider directly to AVCC for no power limit.
11	IN2B	**Negative audio input for channel 2.** Biased at 2.5V.
12	IN2A	**Positive audio input for channel 2.** Biased at 2.5V.
13	INABSENCE	**Open-drain output used to report the input signal absence.**
14	CAP_D	**Delay time control for input signal absence report function.** The holding time can be adjusted with an external capacitor. Connect this pin to AGND to disable automatic shutdown if an input signal cannot be detected.
15, 16	PVCC2	**Power supply input for channel 2.** Bypass PVCC2 to PGND2 with a 1μF X7R capacitor (in addition to the main bulk capacitor), placed close to the PVCC2 and PGND2 pins.
17	BST2A	**High-side MOSFET bootstrap input for amplifier 2A.** A capacitor connected from BST2A to SW2A supplies the gate drive current to the internal high-side MOSFET.
18	SW2A	**Switched power output for amplifier 2A (the positive output of channel 2).**
19	PGND2	**Power ground for amplifier 2A and 2B.**
20	SW2B	**Switched power output for amplifier 2B (the negative output of channel 2).**
21	BST2B	**High-side MOSFET bootstrap input for amplifier 2B.** A capacitor from BST2B to SW2B supplies the gate drive current to the internal high-side MOSFET.
22	BST1B	**High-side MOSFET bootstrap input for amplifier 1B.** A capacitor from BST1B to SW1B supplies the gate drive current to the internal high-side MOSFET.
23	SW1B	**Switched power output for amplifier 1B (the negative output of channel 1).**
24	PGND1	**Power ground for amplifier 1A and 1B.**
25	SW1A	**Switched power output for amplifier 1A (the positive output of channel 1).**
26	BST1A	**High-side MOSFET bootstrap input for amplifier 1A.** Connect a capacitor from BST1A to SW1A to supply the gate drive current to the internal high-side MOSFET.
27, 28	PVCC1	**Power supply input for channel 1.** Bypass PVCC1 to PGND1 with a 1μF X7R capacitor (in addition to the main bulk capacitor), placed close to the PVCC1 and PGND1 pins.

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{CC}) .....-0.3V to +20V
V_{SW}.....-1V to V_{CC} + 1V
V_{EN}, $V_{/FAULT}$, V_{GAIN}, $V_{INABSENCE}$.....
..... - 0.3V to V_{CC} + 0.3V
BS Voltage V_{BST} .....V_{SW} - 0.3V to V_{SW} + 6V
V_{PLIMIT} .....-0.3V to V_{AVCC} + 0.3V
V_{INXX} .....-0.3V to +6.5V
AGND to PGND .....-0.3V to +0.3V
Continuous power dissipation (T_A = 25°C) (2)
.....3.9W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged device model (CDM) ..... ±1.5kV

Recommended Operating Conditions (3)

Supply voltage (V_{CC}) .....5V to 18V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TSSOP-28 EP	32	6 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS (5) (6)

V_{CC} = 18V, V_{EN} = 5V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Standby current	I_{QSTBY}	V_{EN} = 0V		130	200	µA
Quiescent current	I_Q	V_{EN} = 5V, no load, no LC filter		20	40	mA
		V_{EN} = 5V, input signal = 0, T_J = -40°C to +85°C		5.5	10	mA
Output offset voltage	V_{OS}	V_I = 0V, gain = 36dB, T_J = 25°C		20	65	mV
SW on resistance	$R_{DS(ON)}$	I_{OUT} = 500mA, T_J = 25°C		0.24		Ω
Short circuit current		Source and sink, T_J = 25°C	4	5	6	A
Closed loop gain	G	GAIN0 = low, GAIN1 = low	19	20	21	dB
		GAIN0 = high, GAIN1 = low	25	26	27	
		GAIN0 = low, GAIN1 = high	31	32	33	
		GAIN0 = high, GAIN1 = high	35	36	37	
EN enable threshold voltage		V_{EN} rising		1.3	2.0	V
		V_{EN} falling	0.4	0.9		V
EN enable input current		V_{EN} = 5V		12	25	µA
Under-voltage protection		V_{UVP} rising		4.6	5	V
		V_{UVP} falling	4	4.3		V
AVCC operating voltage			5	5.5	6	V
VDR operating voltage			5	5.5	6	V
$V_{INN/INP}$ common mode voltage			2.3	2.5	2.7	V
GAIN0/GAIN1 threshold		V_{GAIN} rising		1.6	2	V
		V_{GAIN} falling	0.6	1.1		V
Turn-on time	t_{ON}			13		ms
Turn-off time	t_{OFF}			0.2		µs
Switching frequency			260	325	360	kHz
Input signal absence sensitivity			2	5	8	mV
Thermal shutdown trip point		T_J rising		150		°C
Thermal shutdown hysteresis				20		°C

Notes:

5) The device is not guaranteed to function outside its operating rating.
6) The electrical characteristics are for the IC only, with no external components except for the bypass capacitors.

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OPERATING SPECIFICATIONS (7)

V_{CC} = 18V, gain = 20dB, V_{EN} = 5V, R_{LOAD} = 8Ω + 66μH, T_A = 25°C, unless otherwise noted. For more details, see Figure 7 on page 19.

Parameters	Symbol	Condition		Min	Typ	Max	Units
Power output		f = 1kHz, THD+N = 10%, V_{CC} = 18V			20		W
		f = 1kHz, THD+N = 10%, V_{CC} = 16V			15		
		f = 1kHz, THD+N = 10%, V_{CC} = 12V			9.5		
THD+noise		P_{OUT} = 5W, f = 1kHz, V_{CC} = 12V			0.5		%
		P_{OUT} = 15W, f = 1kHz, V_{CC} = 18V			0.5		%
Efficiency		P_{OUT} = 9.5W + 9.5W, THD+N = 10%, V_{CC} = 12V, 1kHz, R_{LOAD} = 8Ω			90		%
Dead time		I_O=0.5A			40		ns
Cross talk		V_O = 1Vrms, f = 217Hz			-110		dB
Noise floor		A-Weighted, 22 Hz to 22 kHz			115		μV
Signal-to-noise ratio		f = 1kHz, THD+N = 1%, A-Weighted			100		dB
Power supply rejection		V_{RIPPLE} = 300mV_{PP}, Inputs AC-coupled to AGND	f = 1kHz		-60		dB
			f = 217Hz		-70		dB

Note:

7) The operating specifications are for the IC set-up in the Typical Application Circuit on page 19. Not production tested.

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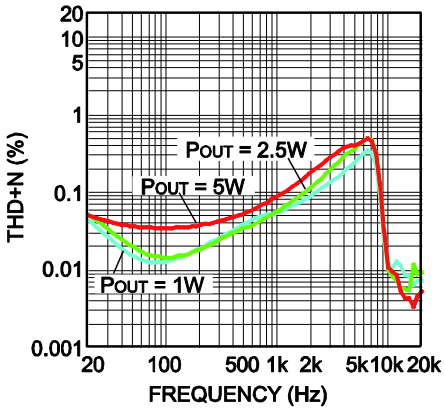
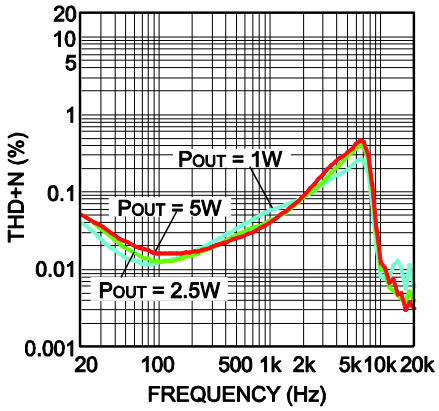
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 12V, gain = 20dB, f = 1kHz, T_A = 25°C, unless otherwise noted.

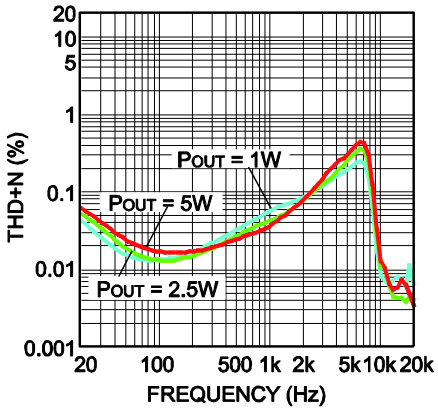
THD+N vs. Frequency
12V, 8Ω + 66μH



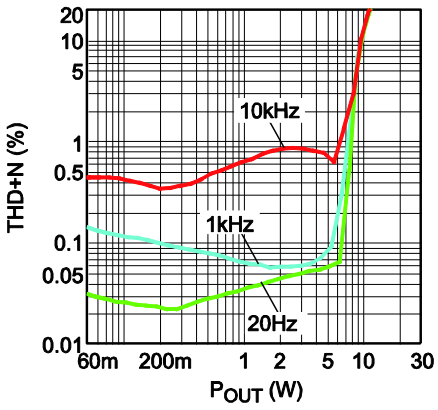
THD+N vs. Frequency
16V, 8Ω + 66μH



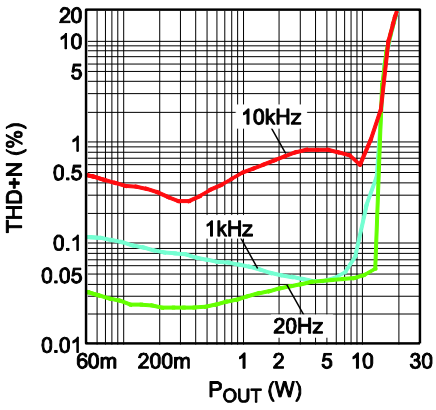
THD+N vs. Frequency
18V, 8Ω + 66μH



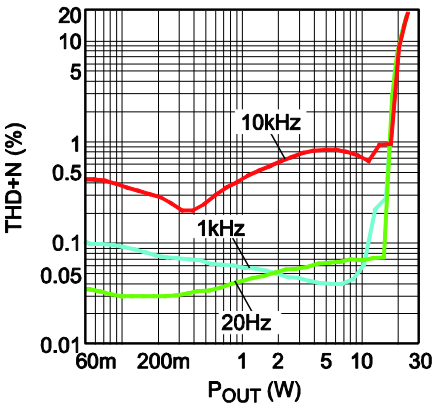
THD+N vs. P_{OUT}
12V, 8Ω + 66μH



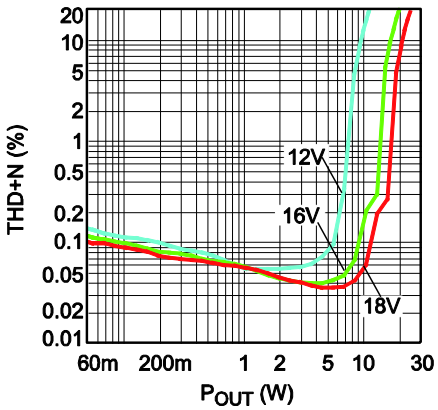
THD+N vs. P_{OUT}
16V, 8Ω + 66μH



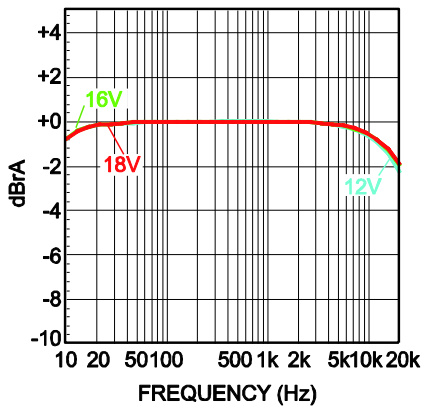
THD+N vs. P_{OUT}
18V, 8Ω + 66μH



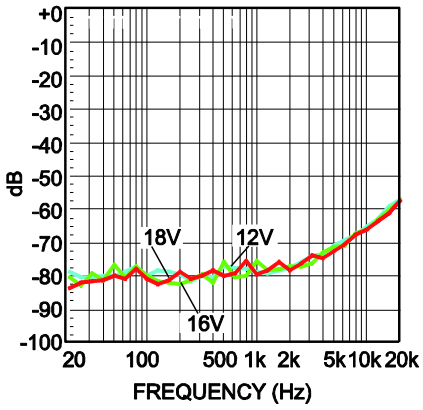
THD+N vs. P_{OUT}
1kHz, 8Ω + 66μH



Frequency Response
1W, 8Ω + 66μH



PSRR Test
8Ω + 66μH, Gain = 20dB,
V_{AC_RIPPLE} = 300mV_{PP}



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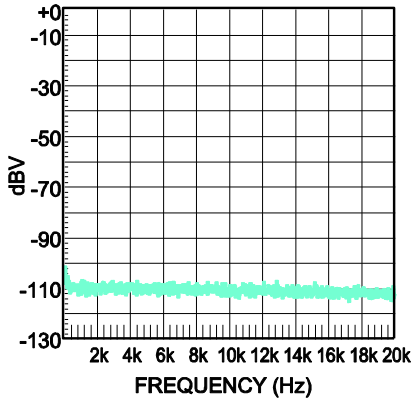
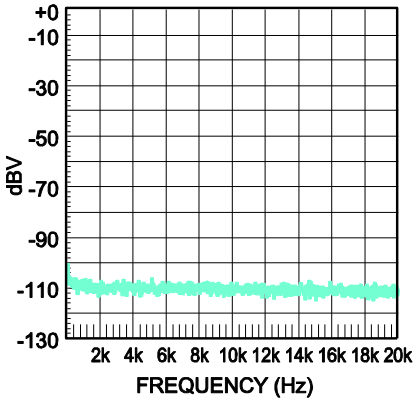
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{CC} = 12V, gain = 20dB, f = 1kHz, T_A = 25°C, unless otherwise noted.

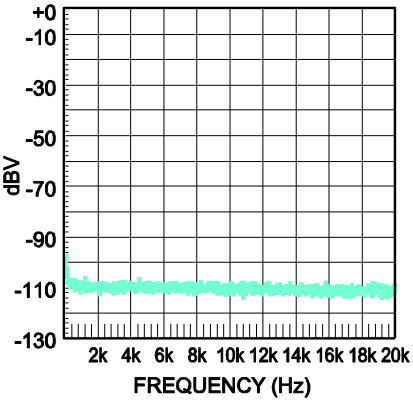
FFT Noise Floor Test
12V, 8Ω + 66μH



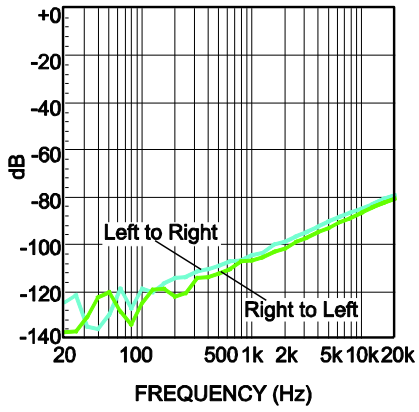
FFT Noise Floor Test
16V, 8Ω + 66μH



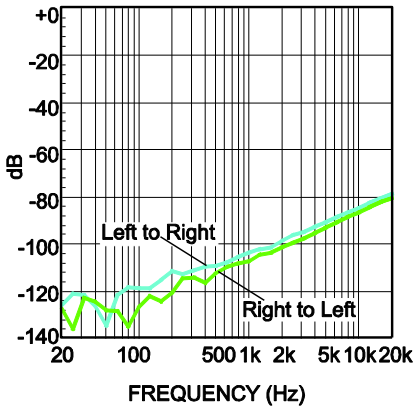
FFT Noise Floor Test
18V, 8Ω + 66μH



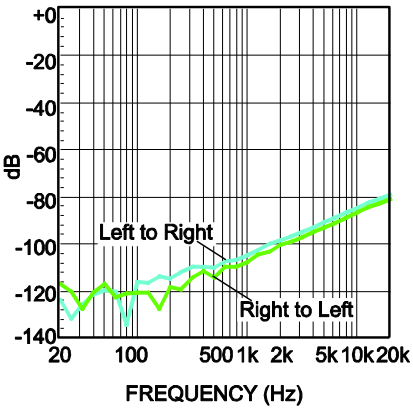
Cross Talk
12V, 8Ω + 66μH, P_{OUT} = 5W



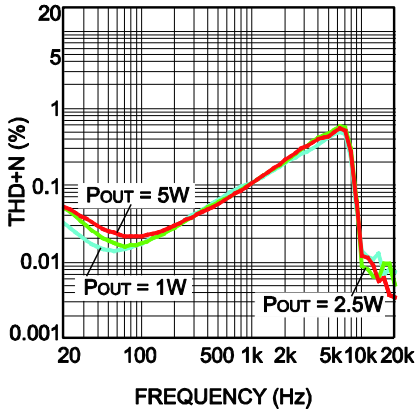
Cross Talk
16V, 8Ω + 66μH, P_{OUT} = 5W



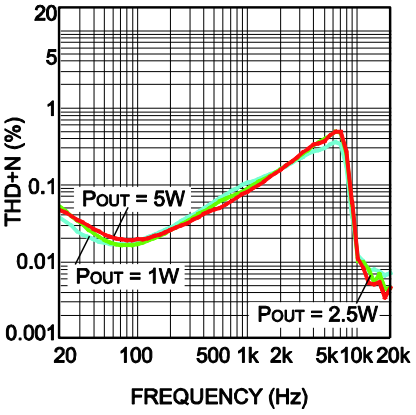
Cross Talk
18V, 8Ω + 66μH, P_{OUT} = 5W



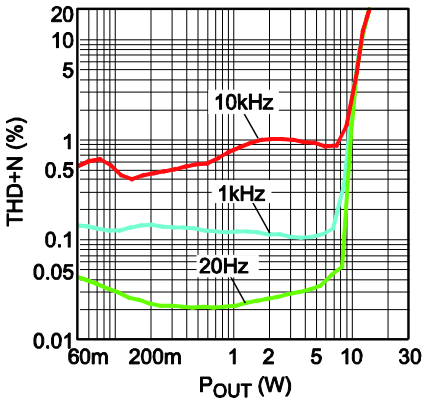
THD+N vs. Frequency
12V, 6Ω + 44μH



THD+N vs. Frequency
16V, 6Ω + 44μH



THD+N vs. P_{OUT}
12V, 6Ω + 44μH



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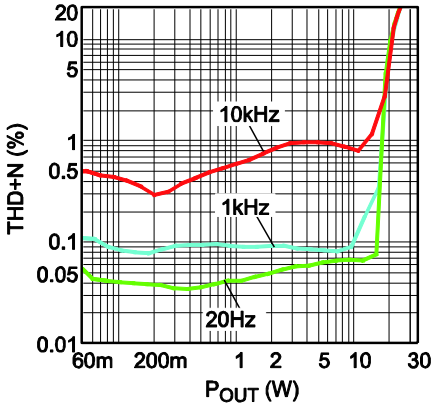
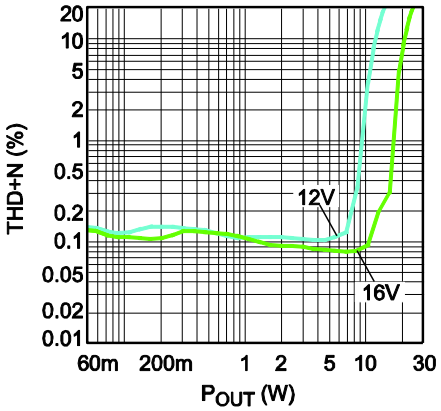
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{CC} = 12V, gain = 20dB, f = 1kHz, T_A = 25°C, unless otherwise noted.

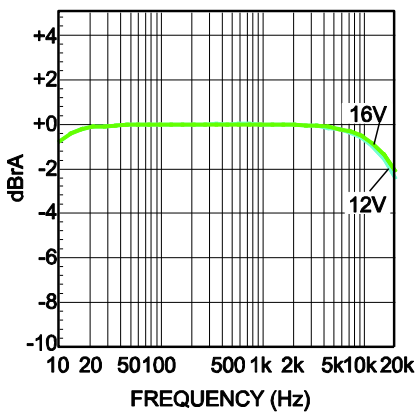
THD+N vs. P_{OUT}
16V, 6Ω + 44μH



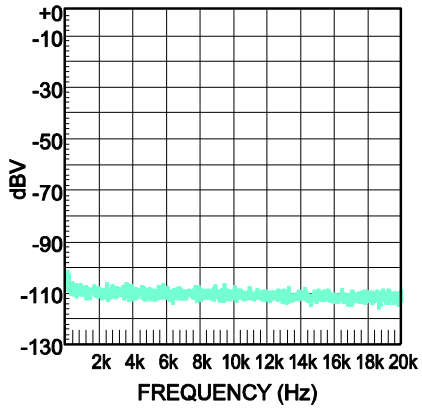
THD+N vs. P_{OUT}
1kHz, 6Ω + 44μH



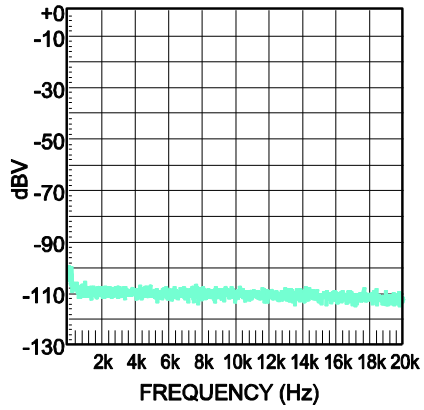
Frequency Response
1W, 6Ω + 44μH



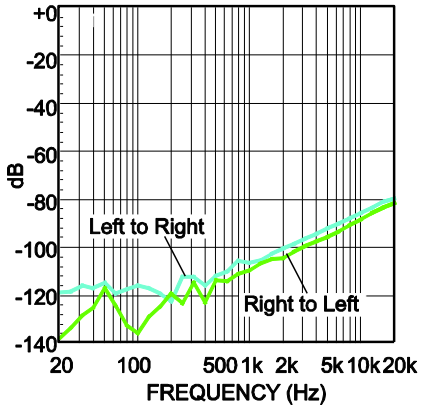
FFT Noise Floor Test
12V, 6Ω + 44μH



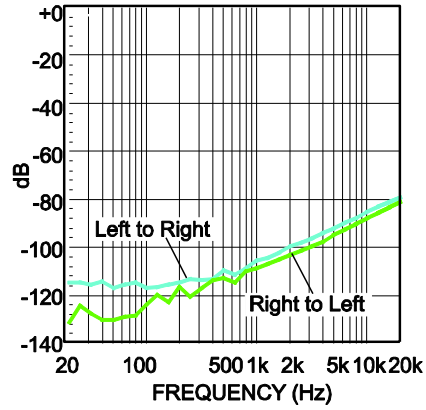
FFT Noise Floor Test
16V, 6Ω + 44μH



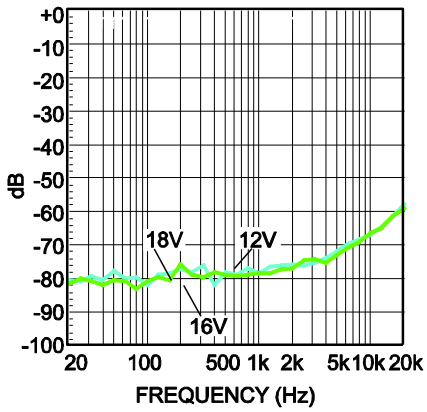
Cross Talk Test
12V, 6Ω + 44μH, P_{OUT} = 5W



Cross Talk Test
16V, 6Ω + 44μH, P_{OUT} = 5W



PSRR Test
6Ω + 44μH, Gain = 20dB,
V_{AC_RIPPLE} = 300mV_{PP}



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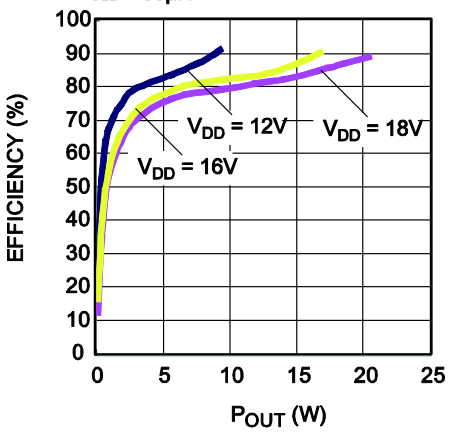
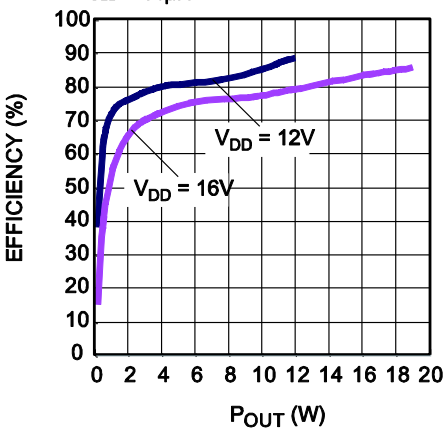
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{CC} = 12V, gain = 20dB, f = 1kHz, T_A = 25°C, unless otherwise noted.

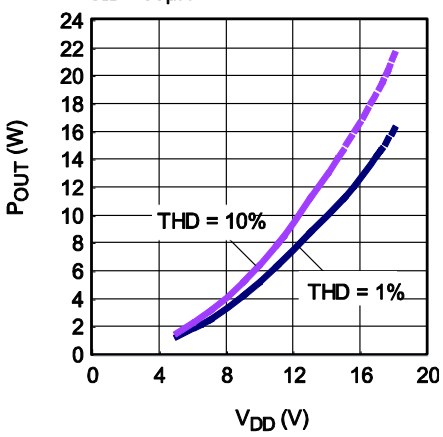
Efficiency vs. P_{OUT}
8Ω + 66µH



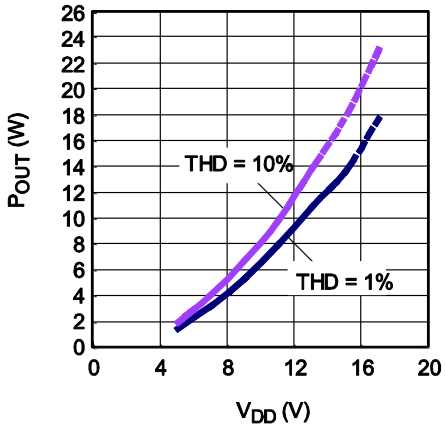
Efficiency vs. P_{OUT}
6Ω + 44µH



V_{DD} vs. P_{OUT}
8Ω + 66µH



V_{DD} vs. P_{OUT}
6Ω + 44µH



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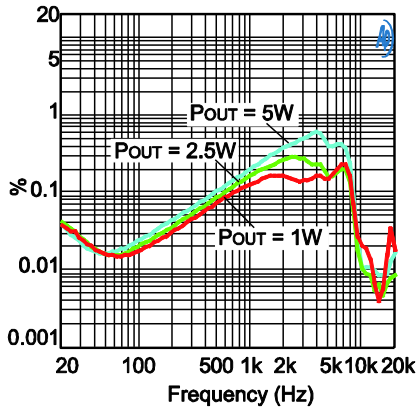
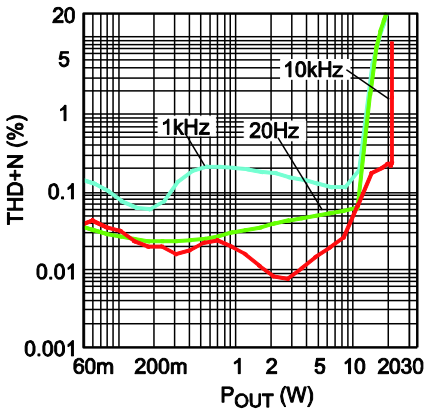
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{CC} = 12V, gain = 20dB, f = 1kHz, T_A = 25°C, unless otherwise noted.

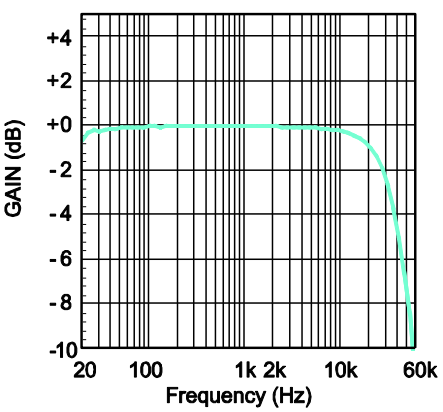
THD+N vs. Frequency
12V, 4Ω + 33μH



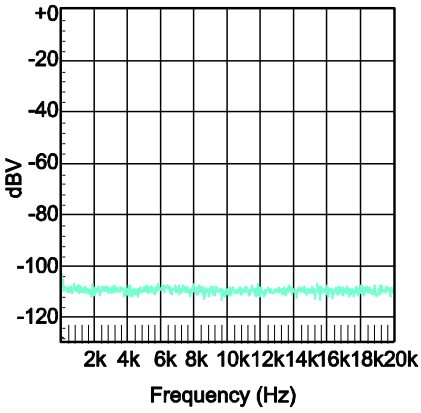
THD+N vs. P_{OUT}
12V, 4Ω + 33μH



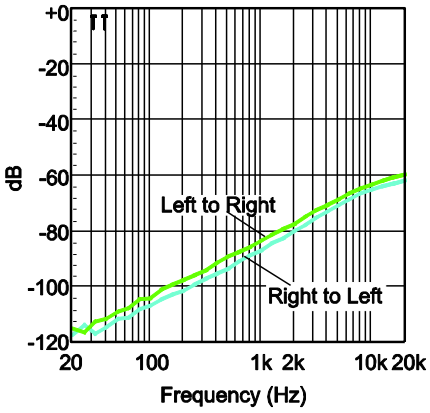
Frequency Response
12V, 4Ω + 33μH, 1W



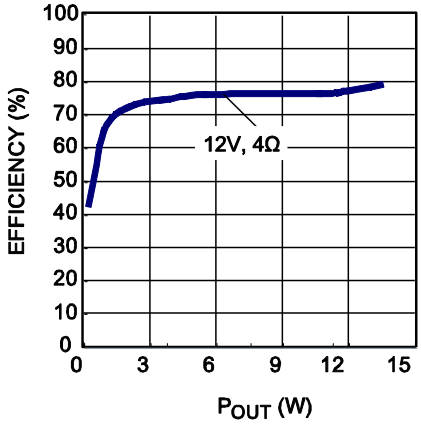
FFT Noise Floor Test
12V, 4Ω + 33μH



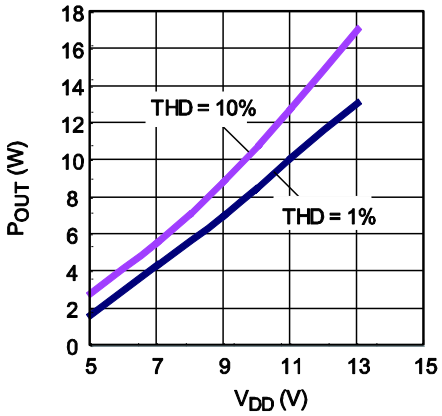
Cross Talk
12V, 4Ω + 33μH, P_{OUT} = 5W



Efficiency vs. P_{OUT}
4Ω + 33μH



V_{DD} vs. P_{OUT}
4Ω + 33μH



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FUNCTIONAL BLOCK DIAGRAM

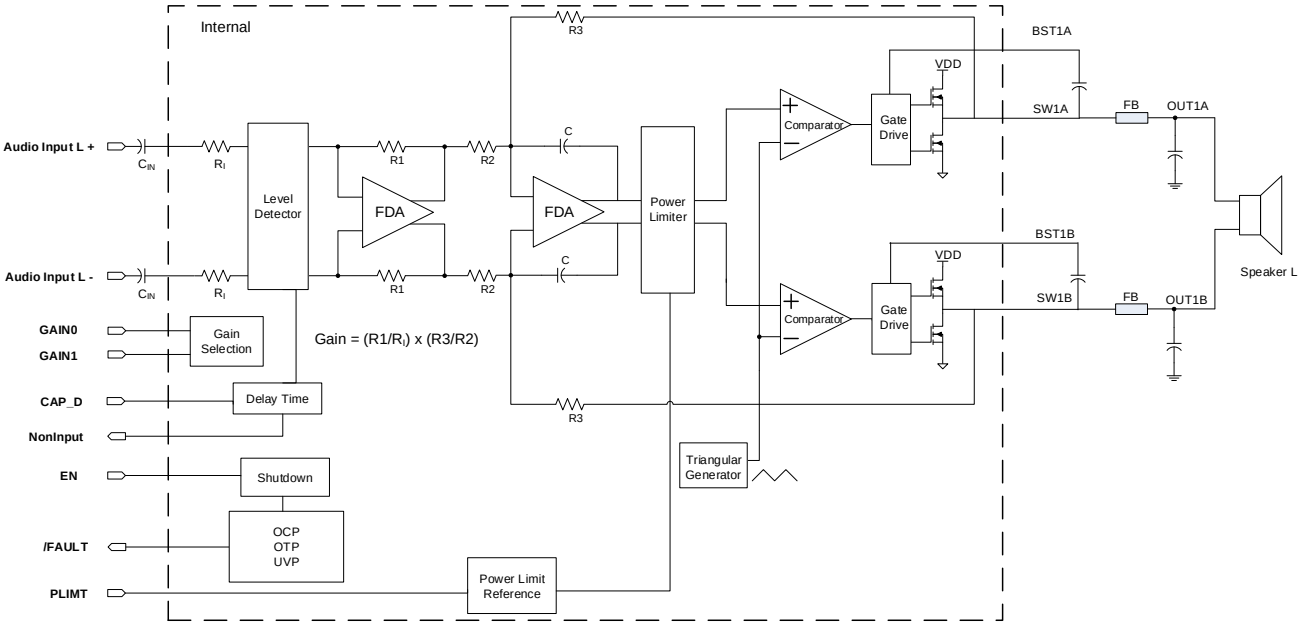

Figure 1: Functional Block Diagram (One Channel)

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OPERATION

The MP7758 is a fully integrated class-D stereo BTL audio amplifier. The switching class-D output stage provides reduced power dissipation when compared to class-A, class-B or class-A/B amplifiers, while maintaining high fidelity and low distortion.

The amplifier has fully differential outputs and inputs. The differential input minimizes common mode noise (any noise that appears on both input lines of the channel). The MP7758 can also be used with a single-ended input.

The MP7758 includes eight high-power MOSFETs. For each half-bridge channel, the output driver stage uses two N-channel MOSFETs to deliver the pulses to the magnetic bead and capacitor output filter. This process drives the load.

To fully enhance the high-side MOSFET (HS-FET), the gate is driven to a voltage above the source via the bootstrap capacitor placed between the OUTxx and BSTxx pins. While the output is driven low, the bootstrap capacitor is charged from a power supply through an internal circuit.

The gate of the HS-FET is driven high from the voltage at the bootstrap supply, forcing the MOSFET gate to a voltage above the power supply voltage. This allows the MOSFET to fully turn on, reducing power loss in the amplifier.

The gain of the MP7758 is set by the input terminals (GAIN0 and GAIN1). The actual gain settings are controlled by the ratios of the input and feedback resistors

Enable (EN) Function

The MP7758 EN input is an active high enable control pin. To enable the MP7758, drive the EN pin to 2.0V or higher. To disable the amplifier, drive EN below 0.4V. While the MP7758 is disabled, the PVCC operating current is about 250μA, and the output driver MOSFETs are turned off.

Absent Input Signal Detection

The MP7758 includes an internal circuit that automatically shuts down the system after detecting the absence of an audio signal. This feature is used for energy-using products and battery-operated applications.

The MP7758 includes a delay circuit that allows the IC to hold the flag after the absence of the audio signal. This holding time can be adjusted with an external capacitor. Two absent input scenarios are described in further detail below:

- The input absence flag is initially high at start-up. After the device is enabled, the internal circuit starts to detect the input signal. The MP7758 holds the output report and normal operation for a delay time. This time can be adjusted by the CAP_D capacitor. Then the MP7758 turns off all the MOSFETs. The input absence output is pulled low until the input signal is detected again (see Figure 2).

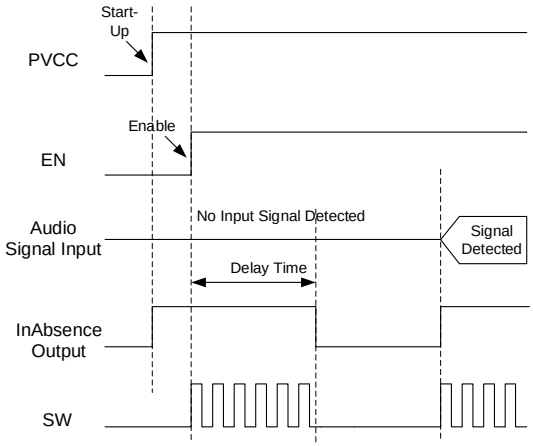

Figure 2: Enable On (No Signal Detected)

- The input absence flag output stays high or is pulled high when an input signal is detected. The delay circuit is only activated when the input signal is absent. The MP7758 holds the output report for a delay time that can be adjusted by the CAP_D capacitor. Then the MP7758 turns off the all MOSFETs. The input absence output is pulled low until the input signal is detected again (see Figure 3).

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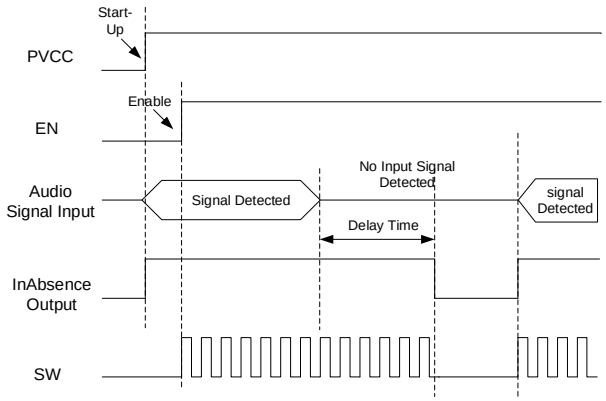

Figure 3: Enable On (Audio Signal Present)

Adjustable Power Limit

The MP7758 features power limiting and anti-clipping control. The voltage on the PLIMIT pin can limit the power below levels that would be possible based on the supply rail.

Connect a resistor divider from AVCC to GND to set the power limit. Connect the resistor divider directly to AVCC to remove the power limit.

An external reference may also be used if tighter tolerance is required. In this scenario, place a 1µF capacitor from PLIMIT to ground.

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. The is accomplished by limiting the duty cycle to fixed maximum value. This limit acts as a virtual voltage rail that is lower than the supply connected to PVCC. This virtual rail is 9 times the voltage at the PLIMIT pin. The output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance (see Figure 4).

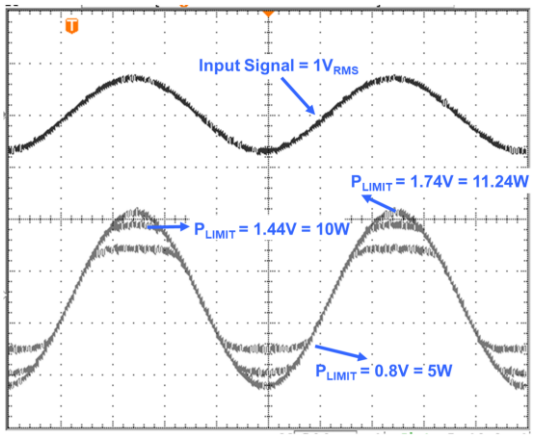

Figure 4: PLIMT Circuit Operation

For unclipped power, the output power can be calculated with Equation (1):

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L} \quad (1)$$

Where R_S is the total output series resistance (including $R_{DS(ON)}$ and the resistance of the output filter), R_L is the load resistance, and V_P is the peak amplifier of the output voltage.

If the PLIMIT voltage times 8 is below the PVCC voltage, V_P can be estimated with Equation (2):

$$V_P = 9 \text{ x PLIMIT Voltage} \quad (2)$$

The value for clipped output power can be calculated with Equation (3):

$$P_{OUT}@10\%THD \approx 1.25 \times \text{unclipped } P_{OUT} \quad (3)$$

Table 2 lists typical power limit values.

Table 2: Typical Power Limit Operation

Test Conditions	PLIMIT Voltage	Output Voltage (V_{PP})	Output Power (10% THD)
VDD = 12V, V_{IN} = 1V_{RMS}, load = 8Ω, gain = 20dB	0.80V	14.9	5.0W
VDD = 16V, V_{IN} = 1V_{RMS}, load = 8Ω, gain = 20dB	0.80V	14.9	5.0W
VDD = 16V, V_{IN} = 1V_{RMS}, load = 8Ω, gain = 20dB	1.44V	23.6	10.0W
VDD = 18V, V_{IN} = 1V_{RMS}, load = 8Ω, gain = 20dB	1.44V	23.6	10.0W

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Gain Setting

The MP7758's gain is set by the input terminals GAIN0 and GAIN1. The actual gain settings are controlled by the ratios of the internal input and feedback resistors (see Table 2).

Table 2: Gain Setting

GAIN0	GAIN1	Typical Gain (dB)	Typical Input Impedance (kΩ)
0	0	20	75
1	0	26	50
0	1	32	30
1	1	36	20

Over-Temperature Shutdown

The MP7758 monitors the temperature. If the die temperature rises above 150°C, all switches turn off. The temperature must fall below 130°C before normal operation resumes. The device uses the same start-up sequence to prevent popping noise.

Short-Circuit Protection (SCP)

The MP7758 has internal overload and short-circuit protection (SCP). The currents in both the high-side and low-side MOSFETs are measured. If a short circuit is detected, all MOSFETs of the full bride that detected the over-current condition go into high impedance for a fixed duration before resuming normal operation. If the short circuit condition is removed after the fixed duration, the MP7758 restarts. The device uses the same start-up sequence to prevent popping noise.

Fault Output

The MP7758 includes an open drain, active low fault indicator output on the /FAULT pin. A fault triggers if either the current limit or thermal shutdown threshold is tripped.

A fault on any channel causes the /FAULT pin to pull low. A fault on either channel causes the all outputs to go into high impedance. When the fault condition is removed, the MP7758 resumes normal operation (see Figure 5).

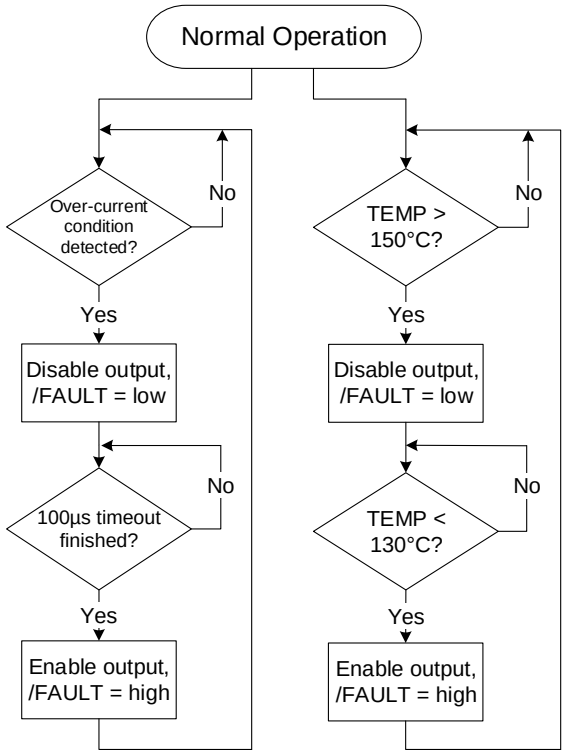

Figure 5: Fault Timing Chart

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APPLICATION INFORMATION

COMPONENT SELECTION

Delay Time for Input Signal Absence Reporting

The delay time can be calculated with Equation (4):

$$t_{DELAY} = 1.6 \times 10^8 \times C_R [sec] \quad (4)$$

Selecting the Output EMI Filter

The magnetic bead capacitor filter converts the pulses at SW to the output voltage that drives the speaker. Both the PVCC line and output current flow require magnetic beads to prevent large radiation from the high slew rate pulses. Magnetic beads with a higher impedance result in improved EMI performance.

Selecting the Input Coupling Capacitor

The input coupling capacitor transmits the AC signal from the source to the MP7758 while blocking the DC voltage. Choose an input coupling capacitor such that the corner frequency (f_{IN}) is below the passband frequency. The corner frequency can be estimated with Equation (5):

$$f_{IN} = \frac{1}{2 \times \pi \times R_{IN} \times C_{IN}} \quad (5)$$

The impedance of the input resistor changes with the gain setting. At the same gain setting, the input impedance between different parts may shift by ±20% due to shifts in the actual resistance of the input resistors. However, the gain variation between parts is minimal.

For design purposes, the input network should be designed assuming an input impedance of 16kΩ (the MP7758's absolute minimum input impedance). At lower gain settings, the input impedance can be as high as 90kΩ.

Setting the Power Source

For maximum output power, the amplifier circuit requires a regulated external power source. A high power supply voltage can deliver more power to a given load resistance, but a power source voltage that exceeds the maximum voltage (about 18V) can damage the MP7758.

The MP7758's power supply rejection is excellent. However, power supply noise can pass to the output, so considerations must be made to minimize power supply noise within the passband frequencies. Bypass the power supply with a large capacitor (typically aluminum electrolytic) along with two smaller 1μF and 1nF ceramic capacitors at the VCC supply pins.

Electromagnetic Interference (EMI) Considerations

Due to the switching nature of class-D amplifiers, care must be taken to minimize the effects of electromagnetic interference from the amplifier. Optimal component selection and careful attention to the circuit layout can minimize the effects of EMI due to the amplifier switching.

The magnetic beads block radiated emissions from the SW nodes. For the best EMI performance, use high-current and high-impedance magnetic beads. Murata's NFZ2M series Class-D EMI filter is well-suited to work with the PVCC and four SW outputs.

Minimize the size of the high-current loops that carry rapidly changing currents. Ensure that the VCC bypass capacitors are as close to the MP7758 as possible.

Nodes that carry rapidly changing voltage (e.g. the SW node) must be as small as possible. If sensitive traces run near a trace connected to SW, place a ground shield between the traces.

The MP7758's evaluation board passed CISPR22 Class B standard with stereo full power output (see Figure 6).

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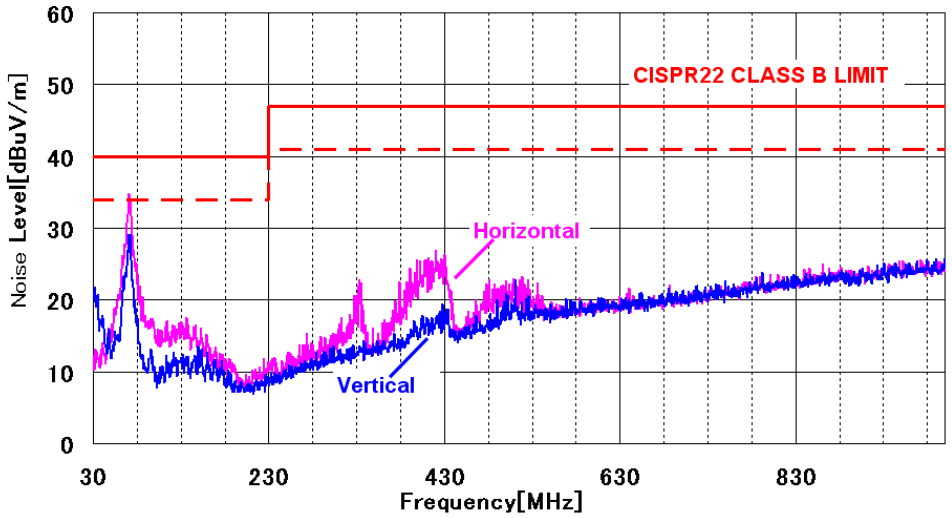

Figure 6: EMI Test Data of the MP7758 Evaluation Board (8)

Note:

8) Testing conditions: 10 meter EMI chamber, 1.2 meter twist speaker cable, MP7758 evaluation board stereo test. VDD = 12V, Load = 8Ω + 66µH, P_{OUT} = 9.5W x 2, 1kHz signal.

PCB Layout Guidelines

Circuit layout is critical for optimal performance, low output distortion, and noise. For the best results, duplicate the evaluation board layout, refer to Figure 7, and follow the guidelines below:

1. Place the bootstrap capacitor (C_{BS}) as close to the BST and SW pins as possible. The capacitor supplies the gate drive current to the internal high-side MOSFET (HS-FET).
2. Place the power supply bypass capacitor (C_{BYP}) as close to the PVCC pins as possible to prevent excessive output noise and avoid overstressing the MP7758. The capacitors carry the transient current for the switching power stage.
3. Keep the magnetic bead capacitor filter close to the magnetic bead. The filter converts the pulse train at SW to the output voltage that drives the speaker.
4. Ensure that any traces carrying the switch node (SW) voltages are routed far from any input signal traces. If the trace must run near the SW trace near the input, shield the input with a ground plane between the traces. Physically separate each channel to prevent crosstalk.
5. Route each power supply from the source to each channel individually, and not serially. This prevents channel-to-channel coupling through the power supply input.

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TYPICAL APPLICATION CIRCUIT

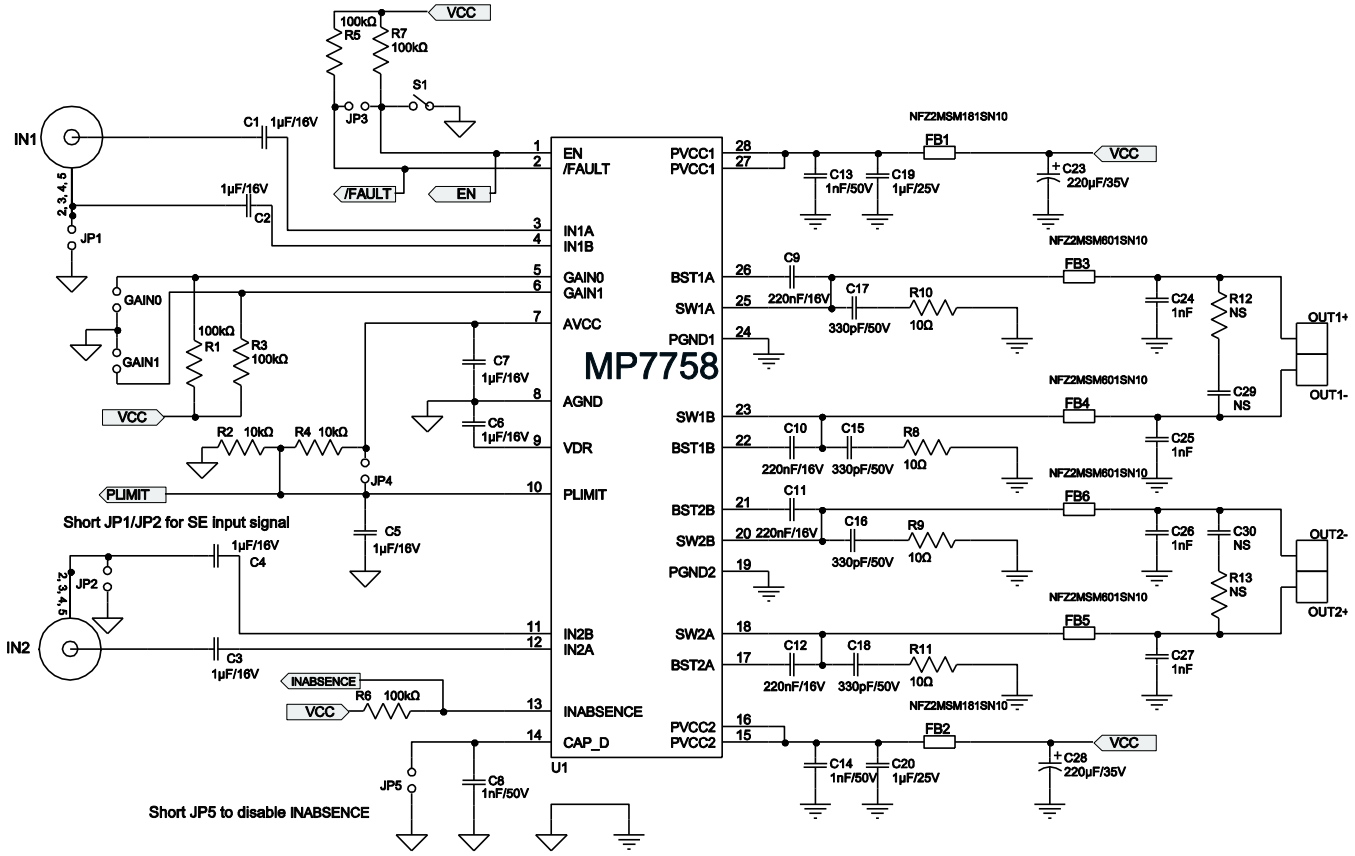

Figure 7: Typical Application Circuit

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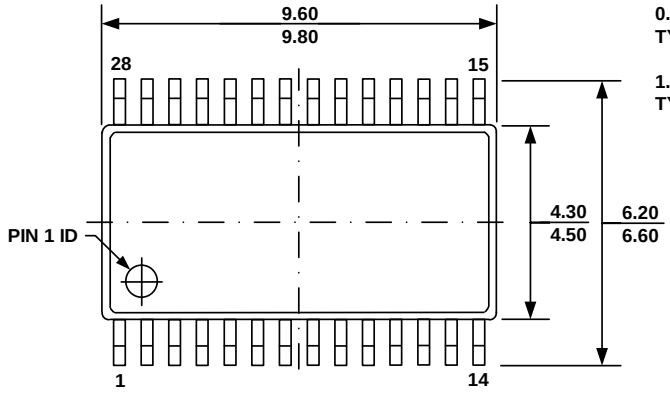
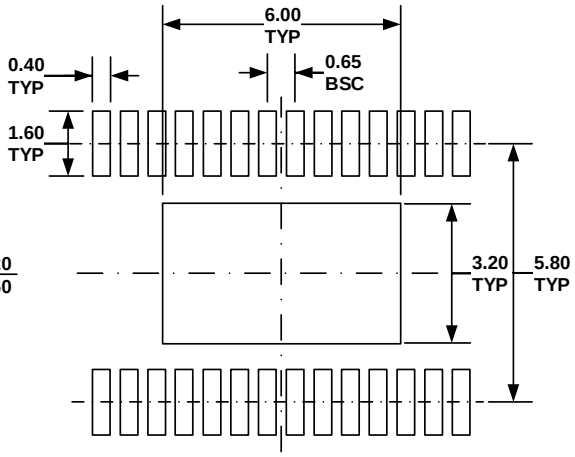
PACKAGE INFORMATION

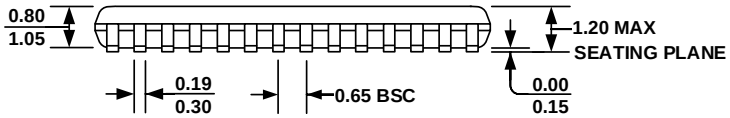
TSSOP-28 EP



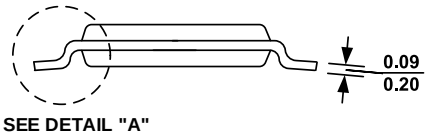
TOP VIEW



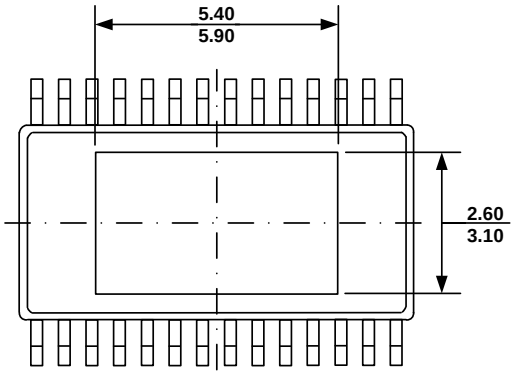
RECOMMENDED LAND PATTERN



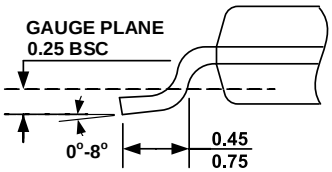
FRONT VIEW



SIDE VIEW



BOTTOM VIEW



DETAIL “A”

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION AET.
6) DRAWING IS NOT TO SCALE.

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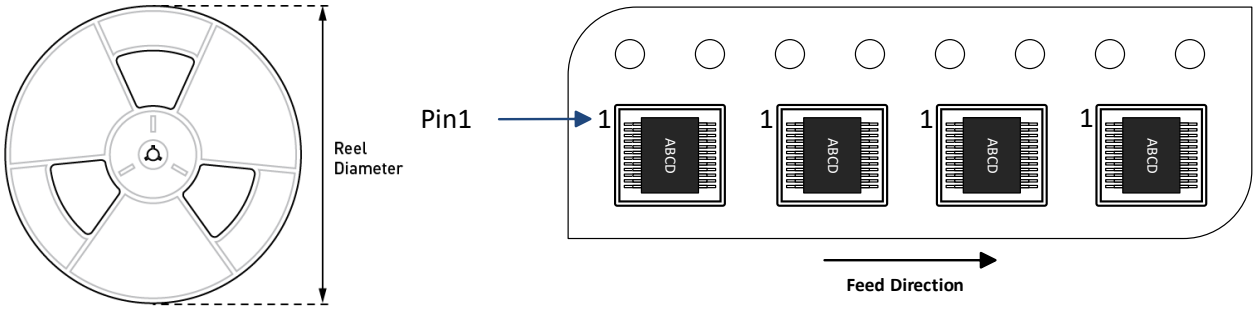
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP7758GF–Z	TSSOP-28 EP	2500	50	N/A	13in	16mm	8mm

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Revision History

Revision #	Revision Date	Description	Pages Updated
1.0	12/3/2020	Initial Release	-

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