MP7731

5W - 30W Class D Mono Bridged Audio Amplifier

The Future of Analog IC Technology

DESCRIPTION

The MP7731 is a mono, 5W - 30W Class D Audio Amplifier. It is one of MPS' second generation of fully integrated audio amplifiers which dramatically reduces solution size by integrating the following:

- Start Up / Shut Down Pop Elimination
- Short Circuit Protection Circuits
- 180mΩ Power MOSFETs
- Mute / Standby Mode

The MP7731 utilizes a full bridge output structure capable of delivering 5W - 30W into 4Ω speakers. As in all other MPS Class D Audio Amplifiers, this device exhibits the high fidelity of a Class AB amplifier with an efficiency of 90%. The circuit is based on the MPS' proprietary variable frequency topology Analog Adaptive Modulation (AAM™, Patent No. 6,420,930; other patents pending) that delivers excellent PSRR, fast response time and operates on a single power supply.

EVALUATION BOARD REFERENCE

Board Number	Dimensions
EV0045	4.8cm x 3.0cm x 1.5cm

FEATURES

- 30W into 4Ω with V_{DD} = 16.5V
- 90% Efficiency at 5W
- Amplifies Full Audio Range with Low THD+N
  - Typical = 0.1%
- 9.5V to 18V Supply Voltage Operation
- Full Bridge Output Drive
- 4 Integrated 180mΩ Switches
- Turn On / Turn Off Click and Pop Suppression
- Integrated Short Circuit Protection
- Integrated Thermal shutdown
- Mute / Standby Mode

APPLICATIONS

- Flat Panel LCD and PDP Displays
- Notebook and Multimedia Computers
- Televisions
- Home Stereos
- DVD and VCD Players
- Game Devices and Systems
- Monitors

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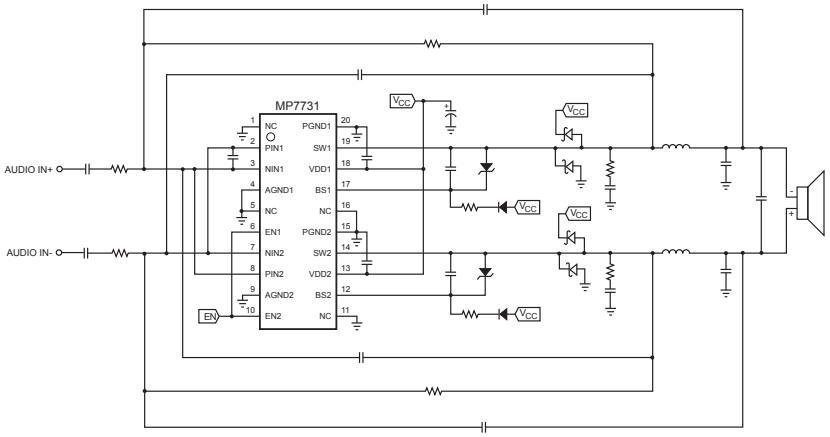
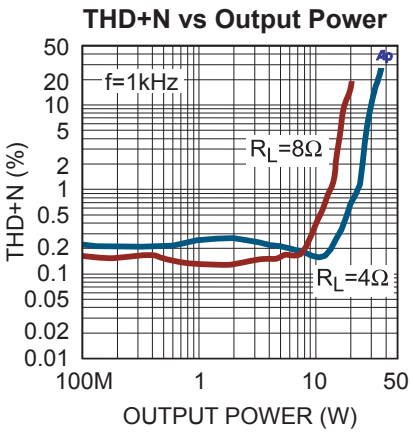
TYPICAL APPLICATION





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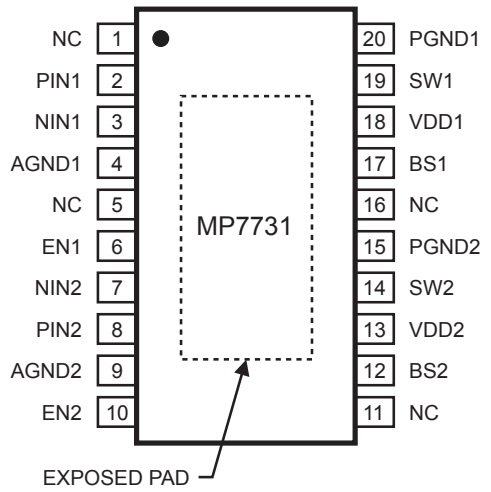
PACKAGE REFERENCE



Part Number*	Package	Temperature
MP7731DF	TSSOP20	–40°C to +85°C

* For Tape & Reel, add suffix –Z (eg. MP7731DF–Z)
For RoHS compliant packaging, add suffix –LF (eg. MP7731DF–LF–Z)

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{DD} 26V
BS Voltage ..... V_{SW}-0.3V to V_{SW}+6.5V
Enable Voltage V_{EN} ..... -0.3V to 6V
V_{SW}, V_{PIN}, V_{NIN} ..... -1V to V_{DD}+1V
AGND to PGND ..... -0.3V to 0.3V
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... -65°C to 150°C

Recommended Operating Conditions (2)

Supply Voltage V_{DD} ..... 9.5V to 18V
Operating Temperature T_A ..... -40°C to 85°C

Thermal Resistance (3)

	θ_{JA}	θ_{JC}	
TSSOP20	40	6	°C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) Measured on approximately 1" square of 1 oz copper.

ELECTRICAL CHARACTERISTICS (4, 5)

V_{DD} = 16.5V, V_{EN} = 5V, R_L = 4Ω, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Standby Current		V_{EN} = 0V		2	10	μA
Quiescent Current				3	6	mA
SW On Resistance		Sourcing and Sinking		0.18		Ω
Short Circuit Current		Sourcing and Sinking		5.0		A
PIN, NIN Input Common Mode Voltage Range			0	V_{DD}/2	V_{DD}-1.5	V
PIN, NIN Input Current		V_{PIN}=V_{NIN}=8V		1	5	μA
EN Enable Threshold Voltage		V_{EN} Rising		1.4	2.0	V
		V_{EN} Falling	0.4	1.2		V
EN Enable Input Current		V_{EN} = 5V		1		μA
Thermal Shutdown Trip Point		T_J Rising		150		°C
Thermal Shutdown Hysteresis				30		°C

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OPERATING SPECIFICATIONS (6)

Circuit of Figure 1, V_{DD} = 16.5V, V_{EN} = 5V, R_L = 4Ω, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Standby Current		V_{EN} = 0V		700		μA
Quiescent Current				28		mA
Power Output		f=1KHz, THD+N=10%		30		W
		f=1KHz, THD+N=10%, R_L=8Ω		17		W
THD+ Noise		P_{OUT}=1W, f=1KHz		0.2		%
		P_{OUT}=1W, f=1KHz, R_L=8Ω		0.1		%
Efficiency		f=1KHz, P_{OUT}=10W		85		%
		f=1KHz, P_{OUT}=10W, R_L=8Ω		88		%
Maximum Power Bandwidth				20		KHz
Dynamic Range				90		dB
Noise Floor		A-Weighted		370		μV
Power Supply Rejection		f=1KHz		60		dB

Note:

4) The device is not guaranteed to function outside its operating rating.
5) Electrical Characteristics are for the IC only with no external components except bypass capacitors.
6) Operating Specifications are for the IC in Typical Application circuit (Figure 1).

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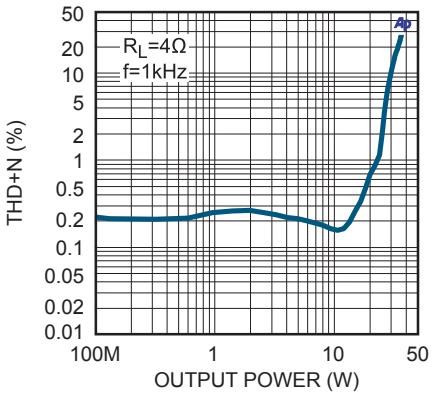
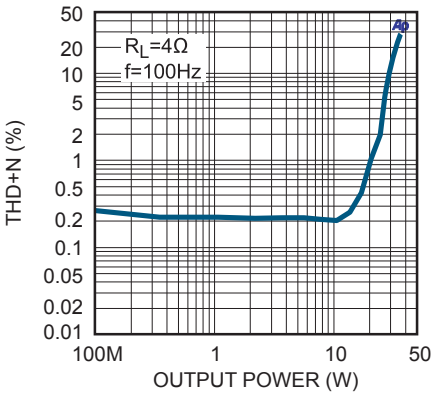
TYPICAL PERFORMANCE CHARACTERISTICS

Circuit of Figure 1, V_{DD}=16.5V, T_A=25°C, unless otherwise noted.

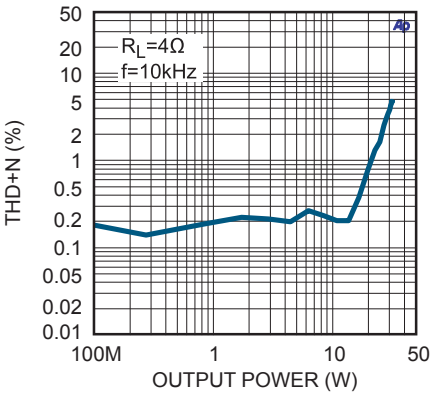
THD+N vs Output Power



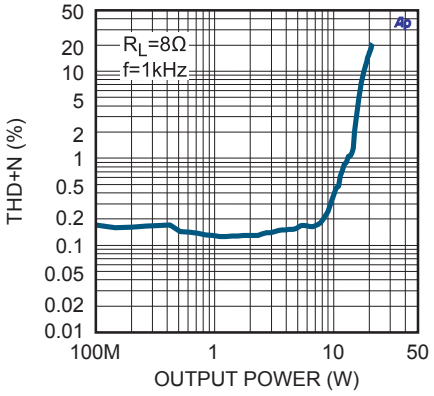
THD+N vs Output Power



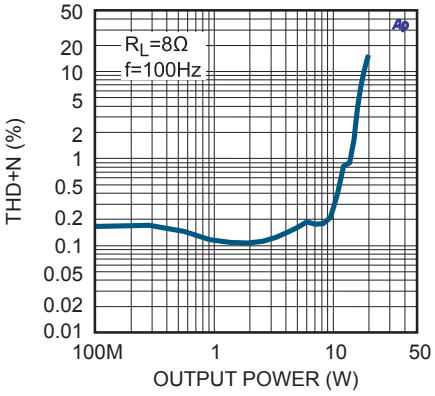
THD+N vs Output Power



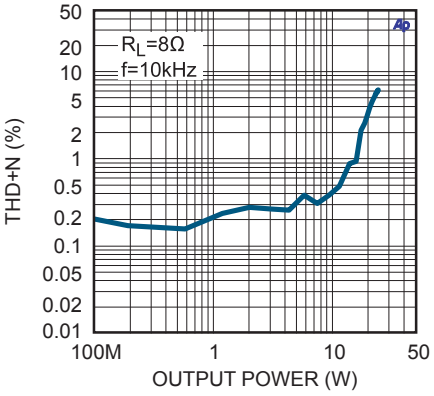
THD+N vs Output Power



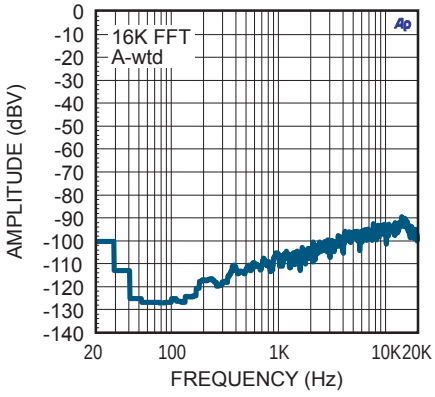
THD+N vs Output Power



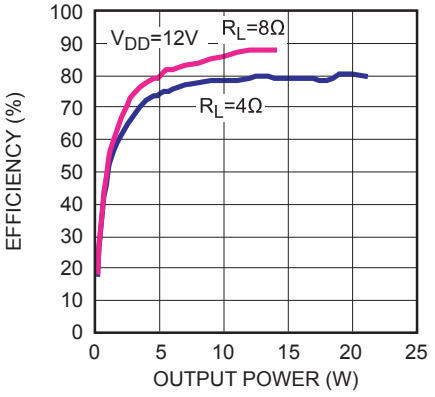
THD+N vs Output Power



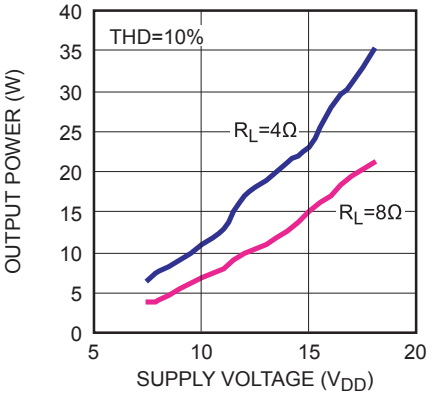
FFT Noise Floor



Efficiency vs Output Power



Output Power vs Supply Voltage



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PIN FUNCTIONS

Pin #	Name	Description
1, 5, 11, 16	NC	No Connect – Not internally connected
2	PIN1	Amplifier 1 Positive Input. PIN1 is the positive side of the differential input to Amplifier 1. See Figure 1.
3	NIN1	Amplifier 1 Negative Input. NIN1 is the negative side of the differential input to Amplifier 1. See Figure 1.
4	AGND1	Analog Ground 1. Connect AGND1 to AGND2.
6	EN1	Enable Input 1. EN1 must be connected to EN2. Drive high to enable MP7731, drive low to disable.
7	NIN2	Amplifier 2 Negative Input. NIN2 is the negative side of the differential input to Amplifier 2. See Figure 1.
8	PIN2	Amplifier 2 Positive Input. PIN2 is the positive side of the differential input to Amplifier 2. See Figure 1.
9	AGND2	Analog Ground 2. Connect AGND2 to AGND1.
10	EN2	Enable Input 2. EN2 must be connected to EN1. Drive high to enable MP7731, drive low to disable.
12	BS2	High-Side MOSFET Bootstrap Input for Amplifier 2. A capacitor from BS2 to SW2 supplies the gate drive current to the internal high-side MOSFET. Connect a 1μF capacitor from SW2 to BS2. See Figure 1.
13	VDD2	Power Supply Input. Bypass VDD2 to PGND2 with a 1μF X7R capacitor (in addition to the main bulk capacitor), placed close to the IC PIN13 and PIN15.
14	SW2	Switched Power Output. SW2 is the output of Amplifier 2. Connect the LC filter to this pin. See Figure 1.
15	PGND2	Power Ground for Amplifier 2. Connect PGND2 to PGND1. See Figure 1.
17	BS1	High-Side MOSFET Bootstrap Input for Amplifier 1. A capacitor from BS1 to SW1 supplies the gate drive current to the internal high-side MOSFET. Connect a 1μF capacitor from SW1 to BS1. See Figure 1.
18	VDD1	Power Supply Input. Bypass VDD1 to PGND1 with a 1μF X7R capacitor (in addition to the main bulk capacitor), placed close to the IC PIN18 and PIN20.
19	SW1	Switched Power Output. SW1 is the output of Amplifier 1. Connect the LC filter to this pin. See Figure 1.
20	PGND1	Power Ground for Amplifier 1. Connect PGND1 to PGND2. See Figure 1.

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APPLICATION INFORMATION

COMPONENT SELECTION

The MP7731 uses a minimum number of external components to complete a fully bridged Class D audio amplifier. The circuit in Figure 1 shows a typical application. Use the following sections to customize the amplifier for your particular application.

Setting the Voltage Gain

The voltage gain sets the output voltage swing for a given input voltage swing and is set by the following equation:

$$A_V = 2\left(\frac{R_1}{R_4}\right)$$

Where:

- R1 = R8
- R4 = R6

The maximum output voltage swing is limited by the power supply. The MP7731 is a bridged amplifier and the output load is driven differentially. Each side of the load is limited to a maximum peak-to-peak voltage swing of approximately V_{DD}. To achieve the maximum output power of the MP7731 amplifier, set the amplifier gain such that the maximum peak-to-peak input signal results in at least the maximum peak-to-peak output voltage swing.

Setting the Switching Frequency

The idle switching frequency (the switching frequency with no audio input signal) is a function of the supply voltage, V_{DD}, the capacitors C4, C6 and C10 and resistors R1 and R8. Lower switching frequencies result in more inductor ripple, causing more quiescent output voltage ripple, increasing the output noise.. Higher switching frequencies result in more power loss. The optimum quiescent switching frequency is approximately 400KHz-600KHz. C6 and C14 are typically 1pF to 2.2pF. C10 is used to program the idle switching frequency.

Choosing the LC Filter

Two identical LC filters are required in the typical application. The inductor-capacitor (LC) filter is a second order filter that converts the pulse train at SW (Pins 14, 19) to the output differential signal that drives the speaker. Typical values for the LC filters are shown in Figure 1. The characteristic frequency of the LC filter needs to be high enough to allow high frequency audio to reach the output, yet needs to be low enough to filter out high frequency contents of the pulses from SW.

The characteristic frequency of the LC filter is:

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

Where:

- L = L1 + L2, L1 = L2
- $C = C9 + \left(\frac{C2 \times C17}{C2 + C17}\right)$, C2 = C17

The quality factor (Q) of the LC filter is important. If this is too low, output noise will increase. If the Q factor is too high, then peaking may occur at high signal frequencies reducing the pass-band flatness.

The Q is calculated as:

$$Q = \frac{R}{\sqrt{\frac{L}{C}}}$$

Where R is the load (speaker) resistance.

Use an LC filter with a Q between 0.7 and 2.0. The actual output ripple and noise is greatly affected by the type of inductor and capacitor used in the LC filter. Use a film capacitor and an inductor with sufficient power handling capability to supply the output current to the load. The inductor should exhibit soft saturation characteristics. If the inductor exhibits hard saturation, it should operate well below the saturation current. Gapped ferrite, MPP, Powdered Iron, or similar type toroidal cores are recommended. If open or shielded bobbin

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ferrite cores are used, make sure that the start windings of each inductor line up (all starts going toward SW pin, or all starts going toward the output) to prevent crosstalk or other channel-to-channel interference.

Input Coupling Capacitor

The input coupling capacitors, C7 and C12, are used to pass only the AC audio signal to the input of the amplifier. In a typical system application, the source input signal is typically centered around the circuit ground, while the MP7731 input is at half the power supply voltage (V_{DD}/2). The input coupling capacitor transmits the AC signal from the source to the MP7731 while blocking the DC voltage. This input coupling capacitor creates a low-pass filter with the input resistor of the MP7731. Choose an input coupling capacitor such that the corner frequency (f_{IN}) is less than the desired pass-band frequency.

The formula for the corner frequency is:

$$f_{IN} = \frac{1}{(2\pi RC)}$$

Where:

- R = R4 = R6
- C = C7 = C12

Where f_{IN} is the -3db cutoff frequency, R4 and R6 are the input resistors and C7 and C12 are the input AC coupling capacitors.

Power Source

For maximum output power, the amplifier circuit requires a regulated external power source to supply the power to the amplifier. The higher the power supply voltage, the more power can be delivered to a given load resistance. However, if the power source voltage exceeds the maximum operating voltage of 18V, the MP7731 may sustain damage. The power supply rejection of the MP7731 is excellent. However, noise at the power supply can get to the output, so care must be taken to minimize power supply noise within the pass-band frequencies. Bypass the power supply pins with a large electrolytic capacitor (typically aluminum electrolytic) along with smaller 1μF ceramic capacitors at the MP7731 V_{DD} supply pins.

Circuit Layout

Proper circuit layout is critical for optimum performance and low output distortion and noise. Place the following components as close to the MP7731 as possible:

1. **Power Supply Bypass, C5, C11**.
   C5 and C11 carry the transient current for the switching power stage. Place a 1uF power supply bypass capacitor as close to Pin 18 (VDD1) and Pin 20 (PGND1) as possible. Also place a 1uF power supply bypass capacitor as close to Pin 13 (VDD2) and Pin 15 (PGND2) as possible.
2. **Output Catch Diodes, D2, D3, D5, and D6**.
   These diodes carry the current over the dead-time while both MOSFET switches are off. Place D3 between Pin 19 (SW1) and Pin 20 (PGND1) to prevent the voltage at SW1 from swinging excessively below ground, and place D2 between SW1 and pin 18 (V_{DD1}) to prevent the voltage at SW1 from swinging excessively about V_{DD}. Place D6 and D5 similarly to minimize the under-shoot and over-shoot of SW2 node.
3. **Input Modulator Capacitor, C10**.
   C10 is used to set the amplifier switching frequency. Place C10 as close to the differential inputs, Pin 2 and Pin 3, as possible to reduce distortion and noise.

Electro-Magnetic Interference (EMI)

Due to the switching nature of the Class-D amplifier, care must be taken to minimize the effects of electromagnetic interference from the amplifier. However, with proper component selection and careful attention to circuit layout, the effects of the EMI due to the amplifier switching can be minimized. The power inductors are a potential source of radiated emissions. For the best EMI performance, use shielded inductors, since the magnetic field is well contained inside the core. On the system printed circuit board, trace loops that carry rapidly changing currents need to be minimized. V_{DD} bypass capacitors (C5 and C11) must be placed as close to the MP7731 as possible. Nodes that carry rapidly changing voltage, such as SW1 and SW2, must be made as small as possible. If sensitive traces run near SW1 or SW2, place a ground shield between the traces.

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TYPICAL APPLICATION CIRCUIT

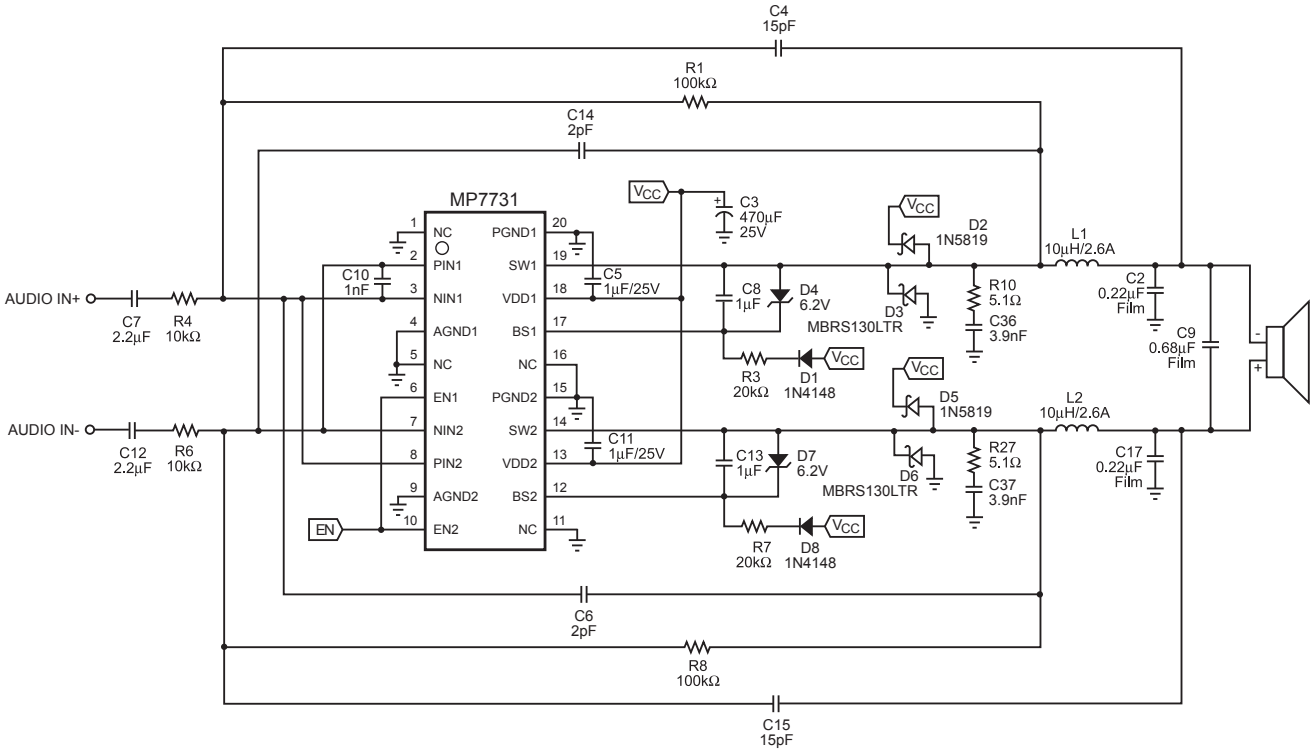

Figure 1— Mono Full Bridged Circuit

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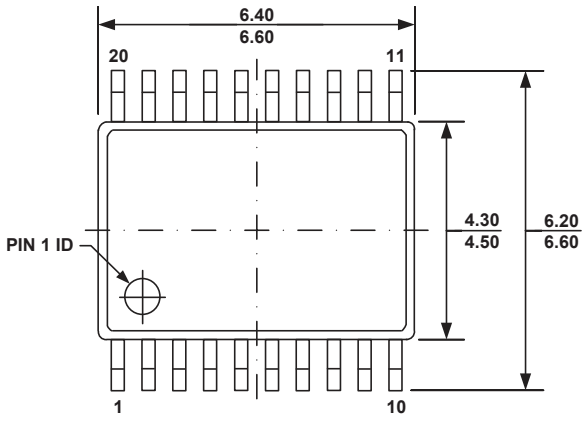
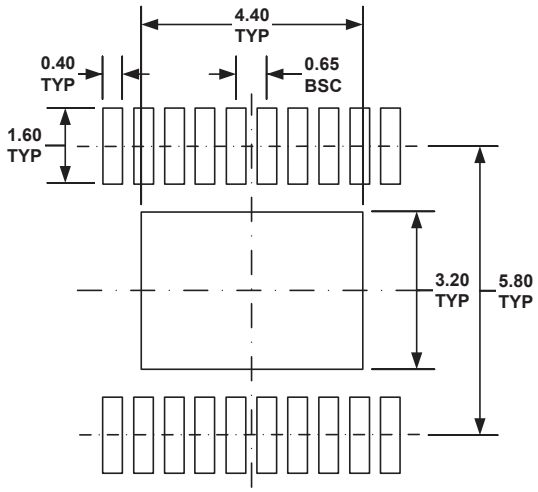
PACKAGE INFORMATION

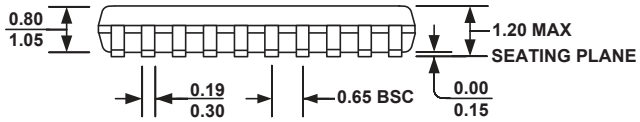
TSSOP20F
(Exposed Paddle)



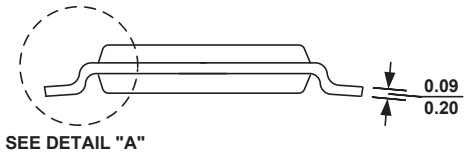
TOP VIEW



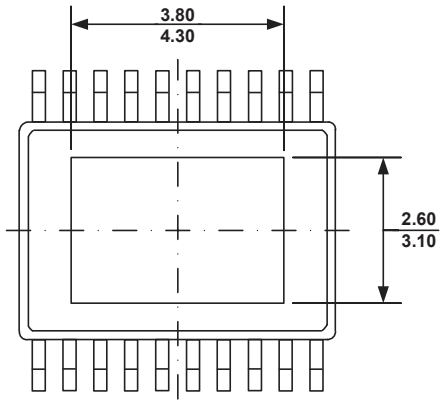
RECOMMENDED LAND PATTERN



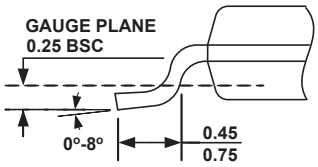
FRONT VIEW



SIDE VIEW



BOTTOM VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION ACT.
6) DRAWING IS NOT TO SCALE.

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