MP7200

42V, 1.2A Buck-Boost or 3A Buck Synchronous LED Driver

DESCRIPTION

The MP7200 is a high-frequency, constant-current, buck-boost LED driver with integrated power MOSFETs. It offers a very compact solution to achieve up to 1.2A of continuous output current, with excellent load and line regulation across a wide input supply range. The MP7200 can also be configured to buck mode to provide up to 3A of constant load current.

Constant frequency hysteretic control mode provides extremely fast transient response without loop compensation. The switching frequency goes up to a fixed 2.3MHz in buck mode to reduce the current ripple and improve EMI, and down to 1.15MHz in buck-boost mode to optimize efficiency and thermal performance.

Full protection features include over-current protection (OCP), output over-voltage (OV) and under-voltage (UV), thermal derating (TD), and thermal shutdown (TSD). The fault indicator outputs an active logic low signal if a fault condition occurs.

The MP7200 requires a minimal number of readily available, standard external components, and is available in a space-saving QFN-19 (3mmx4mm) package.

FEATURES

- Wide 6V to 42V Operating Input Range
- 44mΩ/40mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- High-Efficiency Synchronous Mode Operation
- Configurable 1.2A Buck-Boost or 3A Buck Mode
- Configurable LED Current without Current-Sense Resistor
- Default 2.3MHz Switching Frequency for Buck Mode and 1.15MHz Switching Frequency for Buck-Boost Mode with Spread Spectrum
- PWM Dimming (Dimming Frequency from 100Hz to 2kHz)
- Internal 500Hz Two-Step Dimming with Configurable Duty Cycle
- Fault Indication for LED Short (to GND and Battery) and Open, Output Over-Voltage, and Thermal Shutdown
- Over-Current Protection (OCP) with Latch-Off Mode
- Configurable Thermal Derating via NTC Remote Temperature Sense
- EMI Reduction Technique
- Available in a QFN-19 (3mmx4mm) Package with Wettable Flanks

APPLICATIONS

- Turn Indicator Lights
- Daytime Running Lights (DRLs)
- Fog Lights
- Rear Lights

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TYPICAL APPLICATIONS

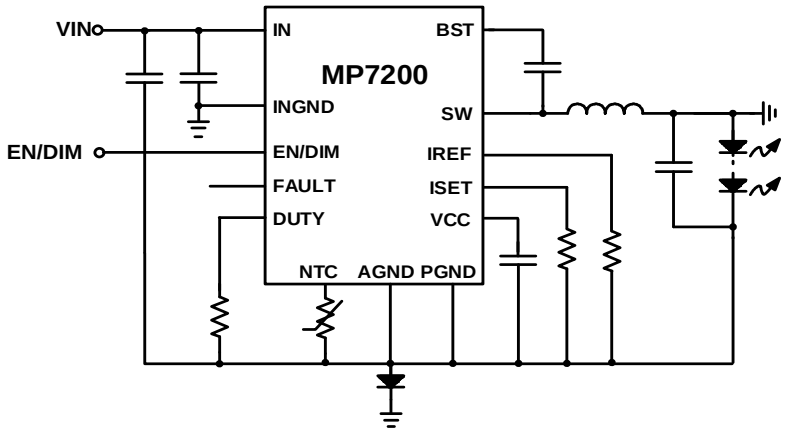

Figure 1: Buck-Boost Topology (≤9.09kΩ R_{IREF})

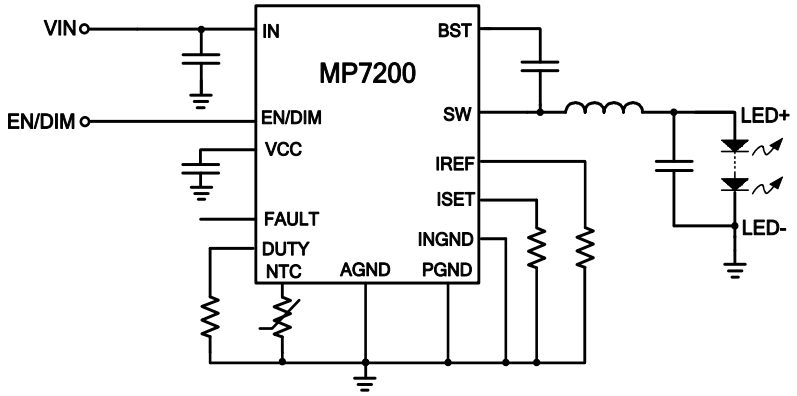

Figure 2: Buck Topology (≥14.7kΩ R_{IREF})

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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MP7200GLE***	QFN-19 (3mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix –Z (e.g. MP7200GLE–Z).

** Moisture Sensitivity Level Rating.

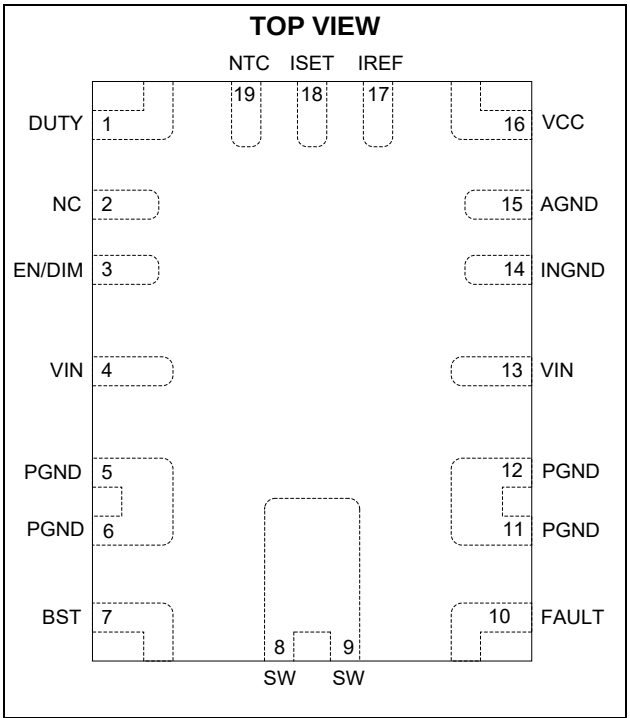
*** Wettable Flank.

TOP MARKING

MPYW
7200
LLL
E

MP: MPS prefix
Y: Year code
W: Week code
7200: First four digits of the part number
LLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



QFN-19 (3mmx4mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	DUTY	**Two-step dimming duty setting.** Connect a resistor (R_{DUTY}) between DUTY and AGND to disable two-step dimming or set the two-step dimming duty cycle. The two-step dimming duty cycle can be set between 5% and 15%, with 1% a step. For more details on the relationship between duty cycle and R_{DUTY}, see the Two-Step Dimming section on page 43. If the DUTY pin is shorted to ground or an open fault is detected before start-up, the part latches off and FAULT is asserted.
2	NC	**Not connection.** Leave this pin floating.
3	EN/DIM	**Enable/dimming control.** Pull EN high to enable the chip. The part starts to sense the pin's configuration at the first positive edge. Once the configuration is completed, apply a 100Hz to 2kHz external clock to the EN/DIM pin for PWM dimming (R_{DUTY} = 4.87KΩ). EN/DIM can be connected to VIN through a maximum 100kΩ resistor. In two-step dimming mode, EN is off and the PWM dimming function is deactivated. Pull this pin high for 100% dimming duty, and pull this pin low to set the dimming duty via R_{DUTY}.
4, 13	VIN	**Supply voltage.** The MP7200 operates from a 6V to 42V input rail. VIN requires an input capacitor (C_{IN}) to decouple the input rail. Connect VIN to the input rail using a wide PCB trace.
5, 6, 11, 12	PGND	**Power ground.** PGND is the power device reference ground, including the configuration pins (e.g. NTC), so it requires additional considerations while designing the PCB layout. PGND is also used to dissipate the thermal heat.
7	BST	**Bootstrap.** Place a capacitor between the SW and BST pins to form a floating supply across the high-side MOSFET driver. Place an optional resistor between the SW and BST capacitors to reduce SW voltage spikes and improve EMI performance.
8,9	SW	**Switch output.** SW is the middle point between the high-side and low-side MOSFETs. When designing the PCB layout, it is recommended to make the SW node as small as possible with a wide trace. This reduces noise coupling and improves EMI.
10	FAULT	**Fault indicator.** FAULT is an open-drain output with an internal 300kΩ pull-up resistor connected to VIN, and a 4MΩ pull-down resistor connected to INGND. FAULT is pulled low if any of the following occurs: LED short or open, over-temperature protection (OTP), false mode detection, or over-current protection (OCP). FAULT can be continuously connected to VIN with a pull-up resistor.
14	INGND	**VIN, EN/DIM, and FAULT ground for buck-boost topology.** For a buck topology, connect INGND to PGND and AGND.
15	AGND	**Analog ground.** Reference ground of the logic circuit. Connect AGND to PGND using an external trace.
16	VCC	**Internal bias supply.** VCC supplies power to the internal control circuit and gate drivers. Connect a ≥3µF decoupling capacitor to VCC and ground. A 10µF/10V or 16V, X7R capacitor is strongly recommend due to capacitance derating.
17	IREF	**Mode selection and NTC reference current setting.** Connect a ≤9.09kΩ resistor at IREF to select buck-boost mode, or a ≥14.7kΩ resistor to select buck mode. The voltage of IREF is 0.57V. Connect a resistor (R_{IREF}) from IREF to GND to get a reference current (0.57V / R_{IREF}). If the IREF pin is shorted to ground or an open fault is detected, the part is latched off and asserts FAULT. The NTC pin current is 50 (buck mode) or 5 (buck-boost mode) times that of the IREF reference current.
18	ISET	**LED current setting.** Connect an external resistor from ISET to ground to set the LED average current. If the ISET pin is shorted to ground or an open fault is detected, the part is latched off and asserts FAULT.
19	NTC	**Remote temperature sense.** Connect NTC to a resistor network to configure the temperature derating starting point. There are protections if NTC is shorted to PGND, AGND, INGND, or the battery.

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ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} - $V_{PGND/AGND}$ ..... -0.3V to +50V
V_{IN} - V_{INGND} ..... -0.3V to +50V
V_{INGND} - $V_{PGND/AGND}$ ..... -0.3V to +50V
V_{FAULT} - V_{INGND} ..... -0.3V to +50V
$V_{EN/DIM}$ - V_{INGND} ..... -0.3V to +5.5V
V_{SW} - $V_{PGND/AGND}$ -0.3V to V_{IN} - $V_{PGND/AGND}$ + 0.3V
V_{BST} ..... V_{SW} + 5.5V
V_{NTC} - $V_{PGND/AGND}$ ..... -0.3V to +50V
All other pins - $V_{PGND/AGND}$ ..... -0.3V to +5.5V
Continuous power dissipation (T_A = 25°C) (2) (4)
QFN-19 (3mmx4mm) 3.9W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged device model (CDM) ..... ±750V

Recommended Operating Conditions

Supply voltage (V_{IN} - V_{PGND}) ..... 6V to 42V
LED current (I_{LED}) in buck-boost mode……..
……..Up to 1.2A
LED current (I_{LED}) in buck mode ..... Up to 3A
Operating junction temp (T_J)….-40°C to +125°C

Thermal Resistance	θ_{JA}	θ_{JC}	
QFN-19 (3mmx4mm)			
JESD51-7 (3)	48	11	°C/W
EVQ7200-L-00A (4)	32	6	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Measured on JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.
4) Measured on MPS standard EVB of MP7200, 2oz, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 13.5V, V_{EN} = 2V, T_J = -40°C to +125°C (5), typical values are at T_J = 25°C, buck mode, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Shutdown supply current	I_{IN}	V_{EN} = 0V		30	80	μA
Quiescent supply current	I_Q	V_{EN} = 2V, no switching, I_{REF} floating (exclude I_{REF} and NTC current)		1.2	2	mA
		FAULT latch			2	mA
HS-FET on resistance	$HS_{RDS(ON)}$	V_{BST-SW} = 5V, R_{ISET} = 13.3kΩ		44	75	mΩ
		V_{BST-SW} = 5V, R_{ISET} = 40.2kΩ		85	150	mΩ
LS-FET on resistance	$LS_{RDS(ON)}$	V_{CC} = 5.2V, R_{ISET} = 13.3kΩ		40	70	mΩ
		V_{CC} = 5.2V, R_{ISET} = 40.2kΩ		80	140	mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} =13.5V, T_J = 25°C			1	μA
		V_{EN} = 0V, V_{SW} = 13.5V			5	μA
Peak current limit (6)	I_{LIMIT_PEAK}	R_{ISET} = 40.2kΩ	2.65	3.15	3.65	A
		R_{ISET} = 13.3kΩ	5.3	6.3	7.3	A
Zero-current detection (6)				50		mA
Oscillator frequency	f_{SW}		2000	2300	2600	kHz
Minimum on time (6)	t_{ON_MIN}			55	80	ns
Minimum off time (6)	t_{OFF_MIN}			75	100	ns
Maximum duty cycle (6)	D_{MAX}	Low dropout	95	98		%
Frequency spread spectrum (6)				15		kHz
Frequency spread spectrum range (6)				±10% x f_{SW}		kHz
LED current	I_{LED}	R_{ISET} = 13.3kΩ, T_J = 25°C to 100°C	-5%	1.2	+5%	A
		R_{ISET} = 13.3kΩ	-15%		+15%	
LED current threshold for MOSFET cutoff	I_{LED_CUT}			600	700	mA
ISET voltage	V_{ISET}	I_{ISET} = 45μA	0.578	0.592	0.606	V
ISET current threshold for pin short		I_{LED} < I_{LED_CUT}	80	120	160	μA
		I_{LED} > I_{LED_CUT}	180	220	260	μA
ISET current threshold for pin open			0.5	1.4	5	μA
EN rising threshold	V_{EN_RISING}	V_{EN} - V_{INGND}	1.2	1.67	2.5	V
EN falling threshold	$V_{EN_FALLING}$	V_{EN} - V_{INGND}	1	1.58	2.2	V
EN threshold hysteresis	V_{EN_HYS}	V_{EN} - V_{INGND}		100		mV
EN input current	I_{EN}	V_{EN} - V_{INGND} = 2V		2	8	μA
		V_{EN} - V_{INGND} = 0V		0	0.2	μA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 13.5V, V_{EN} = 2V, T_J = -40°C to +125°C (5), typical values are at T_J = 25°C, buck mode, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
EN turn-off delay	$t_{EN-TD-OFF}$		10	25	45	ms
VIN under-voltage lockout (UVLO) rising threshold	$INUV_{VTH_R}$	V_{IN} - V_{INGND}	5.75	6	6.25	V
VIN UVLO falling threshold	$INUV_{VTH_F}$	V_{IN} - V_{INGND}	4.5	4.9	5.2	V
VIN UVLO threshold hysteresis	$INUV_{HYS}$	V_{IN} - V_{INGND}		1.1		V
VCC UVLO rising threshold	V_{CC_VTH}	V_{CC} - V_{AGND}	4.4	4.7	5	V
VCC UVLO falling threshold		V_{CC} - V_{AGND}	3.4	4.05	4.7	V
VCC UVLO threshold hysteresis	V_{CC_HYS}	V_{CC} - V_{AGND}		650		mV
VCC regulator	V_{CC}	I_{CC} = 0mA	4.9	5.1	5.3	V
VCC load regulation		I_{CC} = 20mA	4.7			V
VCC maximum current ability		V_{CC} = V_{CC_UVLO} + 100mV, no switching	50	80	120	mA
VCC source current ability (6)		V_{CC} = V_{CC_UVLO} + 100mV, switching		25		mA
DUTY source current	I_{DUTY}	I_{DUTY1}	40	45	50	µA
		I_{DUTY2}	550	600	650	µA
V_{DUTY} threshold maximum		I_{DUTY1} and I_{DUTY2}	3.287	3.355	3.422	V
V_{DUTY} threshold minimum (6)		I_{DUTY1} and I_{DUTY2}	0.28	0.302	0.33	V
Two-step dimming frequency (6)				500		Hz
Output over-voltage (OV) threshold	OV_{VTH}		16.5	18	19	V
Output under-voltage (UV) threshold	UV_{VTH}		0.6	1.1	1.7	V
LED low-current threshold		$I_{LED_SETTING}$ < I_{LED_CUT}	45	60	75	mA
		$I_{LED_SETTING}$ > I_{LED_CUT}	100	120	150	mA
FAULT assertion delay time during start-up	t_{FT-D_START}		25	35	40	ms
FAULT assertion deglitch time after start-up (6)	t_{FT-D}			20		µs
FAULT assertion low sink current ability	I_{FAULT_SINK}	V_{FAULT} = 12V	10	30	50	mA
		V_{FAULT} = 0.2V	5	12		mA
FAULT pull-up resistor			100	300	500	kΩ
FAULT pull-down resistor			2000	4000	6000	kΩ
IREF current for mode detection			200	240	280	µA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 13.5V, V_{EN} = 2V, T_J = -40°C to +125°C [5], typical values are at T_J = 25°C, buck mode, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{IREF} threshold for mode detection			2.6	2.7	2.8	V
IREF voltage	V_{IREF}	I_{REF} = 20μA	0.50	0.57	0.63	V
IREF current threshold for pin short detection			60	90	120	μA
IREF current threshold for pin open detection				3	6	μA
NTC source current	I_{NTC1}		4.5	7.6	10	μA
	I_{NTC2}	V_{NTC} = 1.25V, I_{REF} = 20μA	980	1020	1060	μA
NTC voltage for current derating		I_{LED} = 98% of the nominal voltage	-2.5%	1.25	+2,5%	V
		I_{LED} = 58% of the nominal voltage	-2.5%	0.65	+2.5%	V
VNTC OV threshold		V_{NTC1}	1.8	2	2.2	V
VNTC threshold for over-temperature protection (OTP)		V_{NTC2}	0.2	0.38	0.48	V
VNTC deglitch time for OTP		V_{NTC} = 0.3V	180	256	320	μs
VNTC UV threshold		V_{NTC2}	0.14	0.18	0.22	V
Thermal shutdown [6]			155	170	185	°C

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 13.5V, V_{EN} = 2V, T_J = -40°C to +125°C (5), typical values are at T_J = 25°C, buck-boost mode, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Shutdown supply current	I_{IN}	V_{EN} = 0V		30	80	μA
Quiescent supply current	I_Q	V_{EN} = 2V, no switching, I_{REF} float (exclude I_{REF} and NTC current)		1.2	2	mA
		FAULT latch			2	mA
HS-FET on resistance	$HS_{RDS(ON)}$	V_{BST-SW} = 5V, R_{ISET} = 13.3kΩ		44	75	mΩ
LS-FET on resistance	$LS_{RDS(ON)}$	V_{CC} = 5.2V, R_{ISET} = 13.3kΩ		40	70	mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 13.5V, T_J = 25°C			1	μA
		V_{EN} = 0V, V_{SW} = 13.5V			5	μA
Peak current limit (6)	I_{LIMIT_PEAK}		5.3	6.3	7.3	A
Zero-current detection (ZCD) (5)				50		mA
Oscillator frequency	f_{SW}		920	1150	1380	kHz
Minimum on time (6)	t_{ON_MIN}			55	80	ns
Minimum off time (6)	t_{OFF_MIN}			75	100	ns
Maximum duty cycle (6)	D_{MAX}	Low dropout	95	98		%
Frequency spread spectrum (6)				15		kHz
Frequency spread spectrum range (6)				±10% x f_{SW}		kHz
LED current	I_{LED}	R_{ISET} = 21.5kΩ, T_J = 25°C to 100°C	-7%	0.75	+7%	A
		R_{ISET} = 21.5kΩ	-15%		+15%	
		R_{ISET} = 13.3kΩ, T_J = 25°C to 100°C	-5%	1.2	+5%	A
		R_{ISET} = 13.3kΩ	-15%		+15%	
ISET voltage	V_{ISET}	I_{ISET} = 45μA	0.578	0.592	0.606	V
Power derating ratio		V_{IN} = 6.6V, V_{ISET} with respect to the nominal voltage	91.5	95	98.5	%
		V_{IN} = 5.3V, V_{ISET} with respect to the nominal voltage	72.5	76	79.5	%
ISET current threshold for pin short			90	110	130	μA
ISET current threshold for pin open			0.5	1.4	5	μA
EN rising threshold	V_{EN_RISING}	V_{EN} - V_{INGND}	1.2	1.67	2.5	V
EN falling threshold	$V_{EN_FALLING}$	V_{EN} - V_{INGND}	1.0	1.58	2.2	V
EN threshold hysteresis	V_{EN_HYS}	V_{EN} - V_{INGND}		100		mV

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 13.5V, V_{EN} = 2V, T_J = -40°C to +125°C (5), typical values are at T_J = 25°C, buck-boost mode, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
EN input current	I_{EN}	V_{EN} = 2V		2	8	μA
		V_{EN} = 0V		0	0.2	μA
EN turn-off delay	$t_{EN-TD-OFF}$		10	25	45	ms
VIN UVLO rising threshold	$INUV_{VTH_R}$	V_{IN} - V_{INGND}	5.75	6	6.25	V
VIN UVLO falling threshold	$INUV_{VTH_F}$	V_{IN} - V_{INGND}	4.5	4.9	5.2	V
VIN UVLO threshold hysteresis	$INUV_{HYS}$	V_{IN} - V_{INGND}		1.1		V
VCC UVLO rising threshold	V_{CC_VTH}	V_{CC} - V_{AGND}	4.4	4.7	5	V
VCC UVLO falling threshold		V_{CC} - V_{AGND}	3.4	4.05	4.7	V
VCC UVLO threshold hysteresis	V_{CC_HYS}	V_{CC} - V_{AGND}		650		mV
VCC regulator	V_{CC}	I_{CC} = 0mA	4.9	5.1	5.3	V
VCC load regulation		I_{CC} = 20mA	4.7			V
VCC maximum current ability		V_{CC} = V_{CC_UVLO} + 100mV, no switching	50	80	120	mA
VCC source current ability (6)		V_{CC} = V_{CC_UVLO} + 100mV, switching		25		mA
DUTY source current	I_{DUTY}	I_{DUTY1}	40	45	50	μA
		I_{DUTY2}	550	600	650	μA
VDUTY threshold maximum		I_{DUTY1} and I_{DUTY2}	3.287	3.355	3.422	V
VDUTY threshold minimum (6)		I_{DUTY1} and I_{DUTY2}	0.28	0.302	0.33	V
Two-step dimming frequency (6)				500		Hz
Output OV threshold	OV_{VTH}	V_{INGND} - V_{AGND}	17	18	19	V
Output UV threshold	UV_{VTH}	V_{INGND} - V_{AGND}	1	1.35	1.7	V
VIN load dump protection threshold			38	40	42	V
VIN load dump protection falling threshold			37	39	41	V
VIN load dump protection hysteresis				1		V
Output discharge current for load dump protection		V_{INGND} - V_{PGND} > 5V	40	100	180	mA
		V_{INGND} - V_{PGND} = 1V	20	45	90	mA
FAULT assertion delay time when during start-up	t_{FT-D_START}		25	35	40	ms
FAULT assertion deglitch time after start-up	t_{FT-D}			20		μs

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 13.5V, V_{EN} = 2V, T_J = -40°C to +125°C (5), typical values are at T_J = 25°C, buck-boost mode, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
FAULT assertion low sink current ability	I_{FAULT_SINK}	V_{FAULT} = 12V	10	30	50	mA
		V_{FAULT} = 0.2V	5	12		mA
FAULT pull-up resistor			100	300	500	kΩ
FAULT pull-down resistor			2000	4000	6000	kΩ
IREF current for mode detection			200	240	280	μA
VIREF threshold for mode detection			2.6	2.7	2.8	V
IREF voltage	V_{IREF}	I_{REF} = 20μA	0.50	0.57	0.63	V
IREF current threshold for pin short detection			600	900	1200	μA
IREF current threshold for pin open detection				40	70	μA
NTC source current	I_{NTC1}		4.5	7.6	10	μA
	I_{NTC2}	V_{NTC} = 1.25V, I_{REF} = 200μA	980	1020	1060	μA
NTC voltage for current derating		I_{LED} = 98% of the nominal voltage	-2.5%	1.25	+2.5%	V
		I_{LED} = 58% of the nominal voltage	-2.5%	0.65	+2.5%	V
V_{NTC} OV threshold		V_{NTC1}	1.8	2	2.2	V
V_{NTC} threshold for OTP		V_{NTC2}	0.2	0.38	0.48	V
V_{NTC} deglitch time for OTP		V_{NTC} = 0.3V	180	256	320	μs
V_{NTC} UV threshold		V_{NTC2}	0.14	0.18	0.22	V
Thermal shutdown (6)			155	170	185	°C

Notes:

5) Not tested in production. Guaranteed by over-temperature correlation.
6) Not tested in production. Guaranteed by design and characterization.

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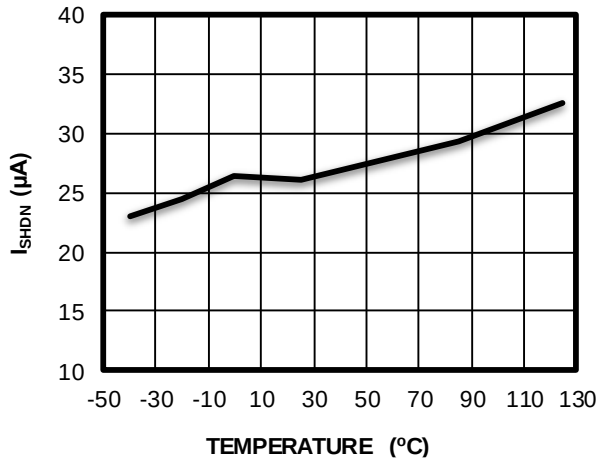
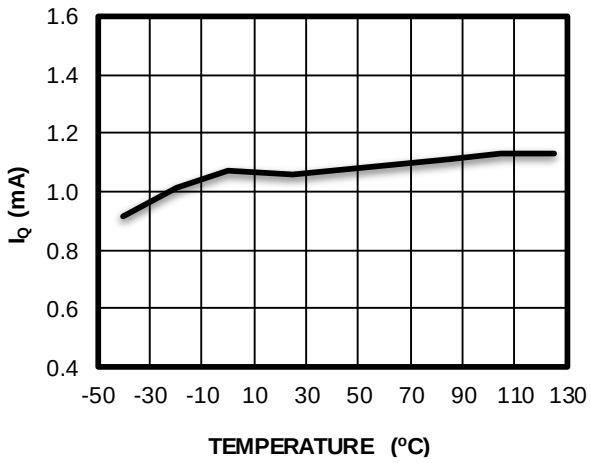
TYPICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

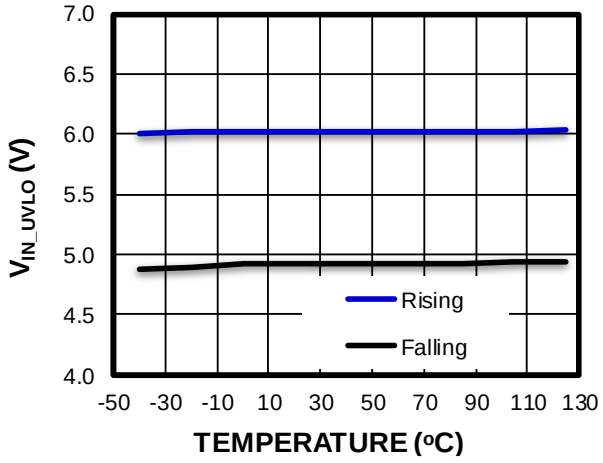
Shutdown Current vs. Temperature



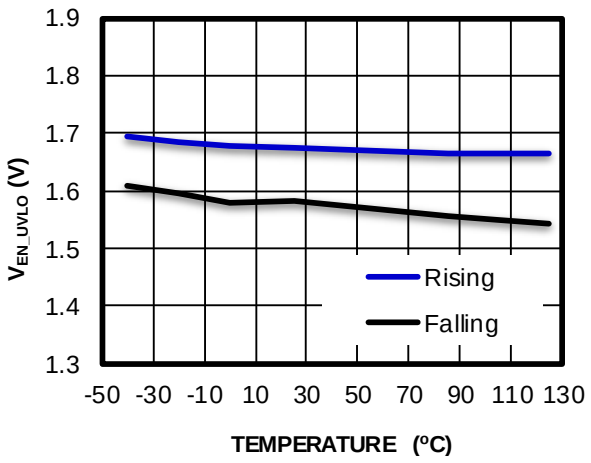
Quiescent Current vs. Temperature



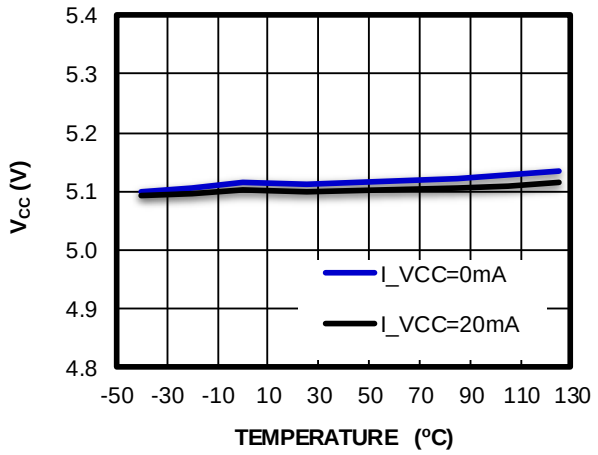
VIN UVLO Threshold vs. Temperature



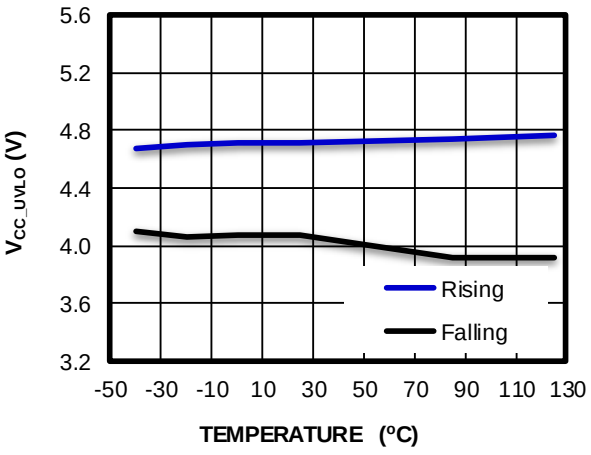
EN UVLO Threshold vs. Temperature



VCC Voltage vs. Temperature



VCC UVLO Threshold vs. Temperature



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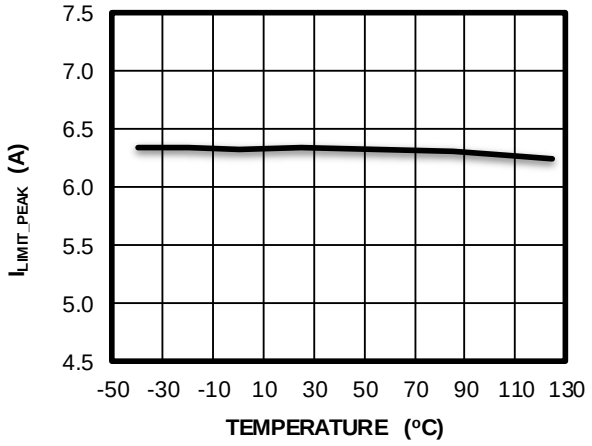
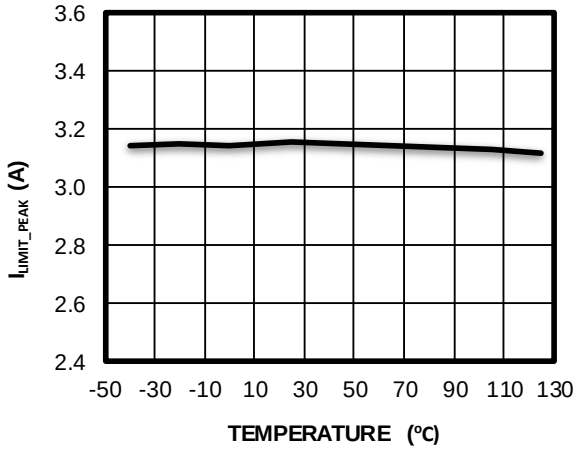
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

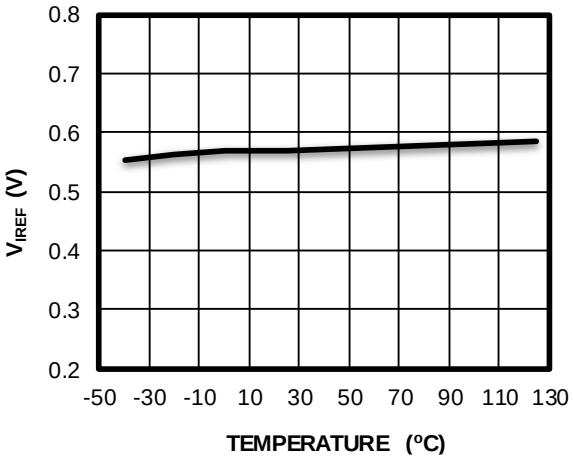
Current Limit with MOSFETs Fully On vs. Temperature



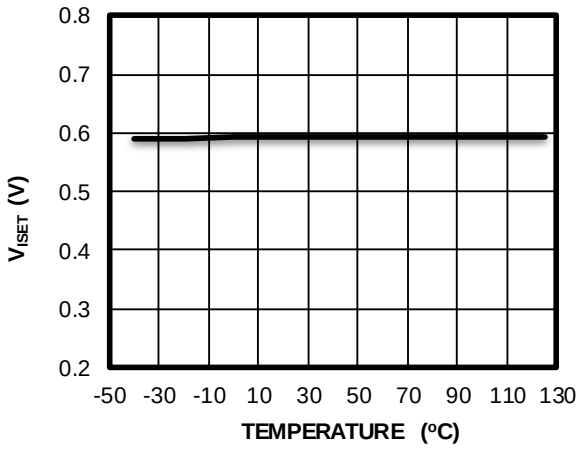
Current Limit with MOSFETs Half On vs. Temperature



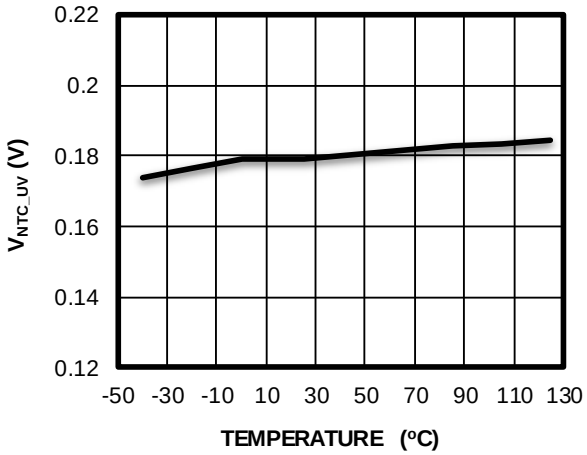
V_{IREF} vs. Temperature



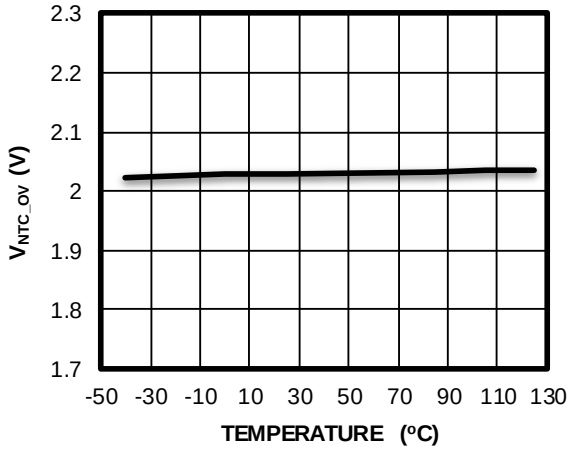
V_{ISET} vs. Temperature



V_{NTC} UV Threshold vs. Temperature



V_{NTC} OV Threshold vs. Temperature



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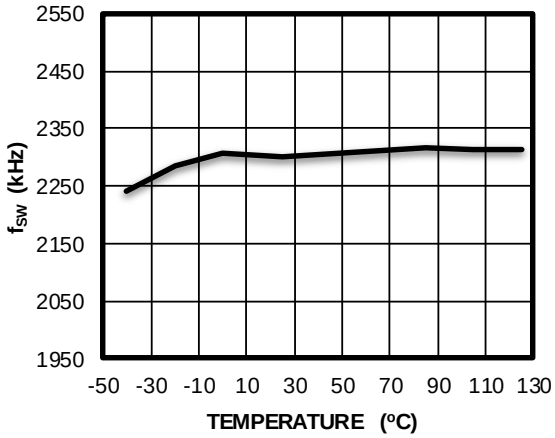
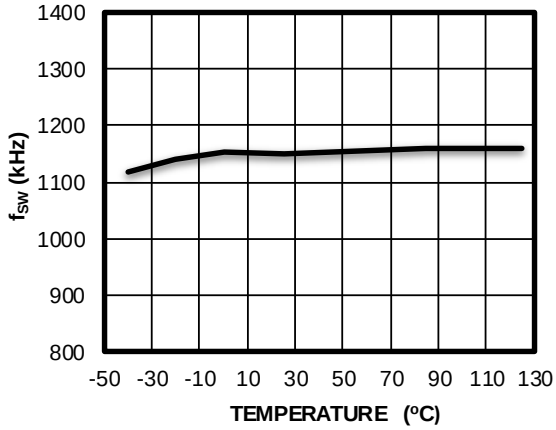
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

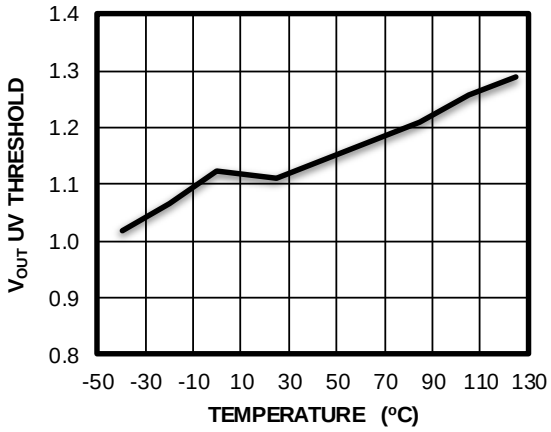
Switching Frequency vs. Temperature
Buck mode



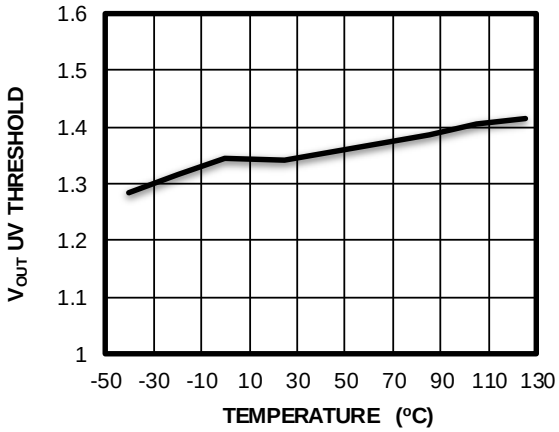
Switching Frequency vs. Temperature
Buck-boost mode



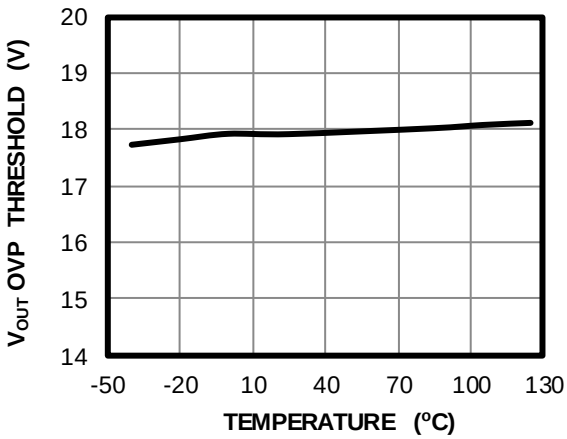
V_{OUT} UV Threshold vs. Temperature
Buck mode



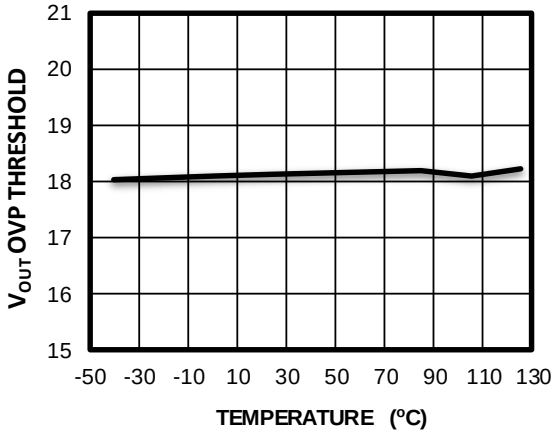
V_{OUT} UV Threshold vs. Temperature
Buck-boost mode



V_{OUT} OVP Threshold vs. Temperature
Buck mode



V_{OUT} OVP Threshold vs. Temperature
Buck-boost mode



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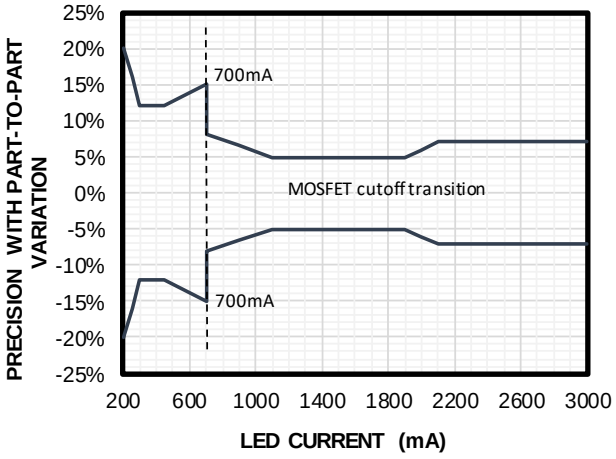
TYPICAL PERFORMANCE CHARACTERISTICS

Buck mode, 2 LEDs (V_{LED} = 6V), V_{IN} = 13.5V, f_{SW} = 2.3MHz, L = 4.7µH, T_A = 25°C, unless otherwise noted.

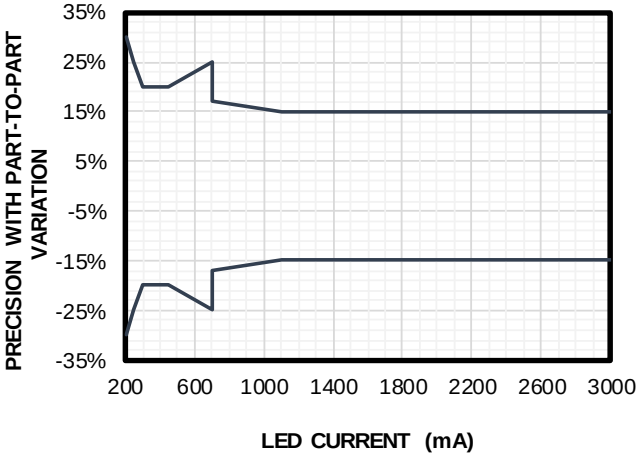
I_{LED} Part-to-Part Variation

T_J = 25°C to 100°C



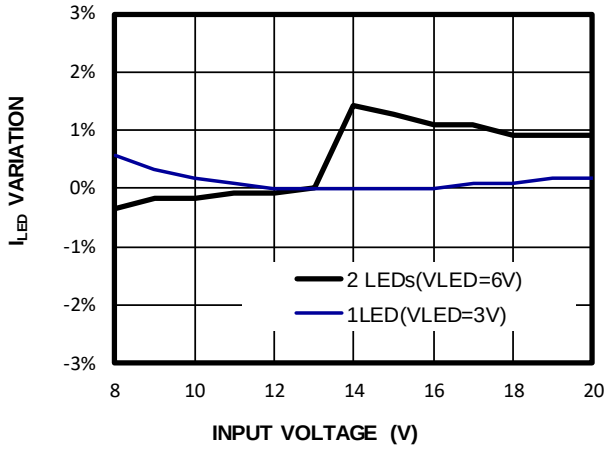
I_{LED} Part-to-Part Variation

T_J = -40°C to +150°C



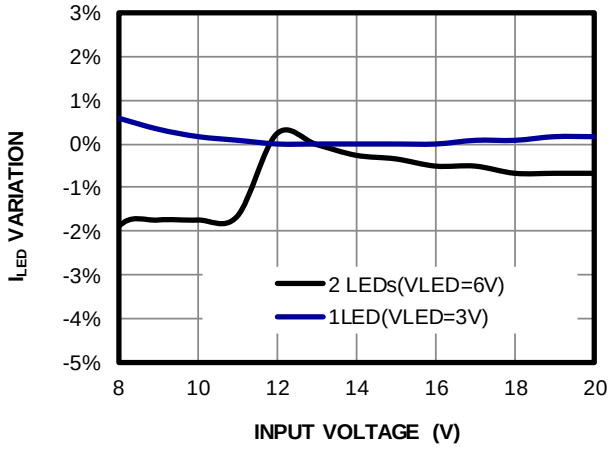
I_{LED} Precision vs. Input Voltage

L = 4.7µH, I_{LED} = 1.2A, V_{IN} ramping up



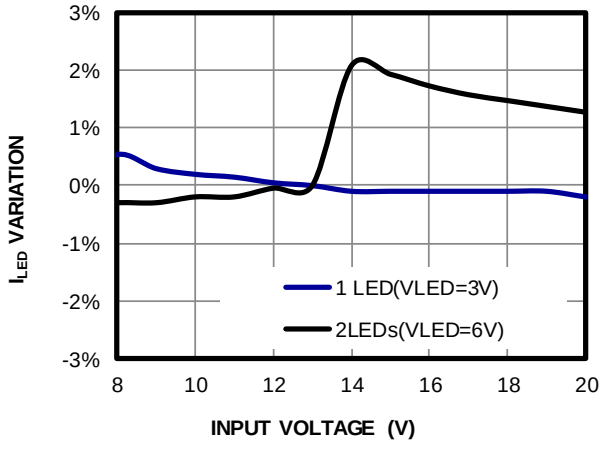
I_{LED} Precision vs. Input Voltage

L = 4.7µH, I_{LED} = 1.2A, V_{IN} ramping down



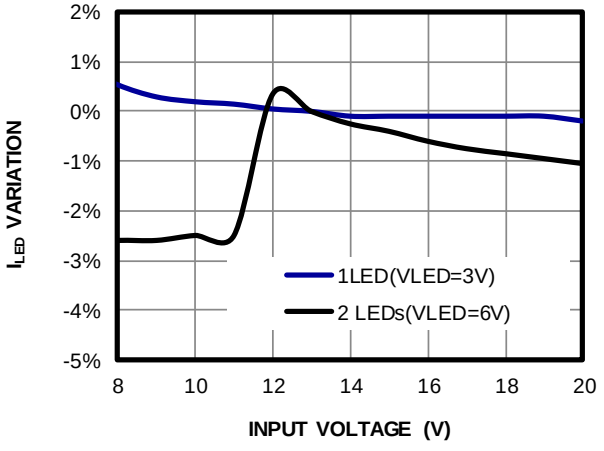
I_{LED} Precision vs. Input Voltage

L = 3.3µH, I_{LED} = 2A, V_{IN} ramping up



I_{LED} Precision vs. Input Voltage

L = 3.3µH, I_{LED} = 2A, V_{IN} ramping down



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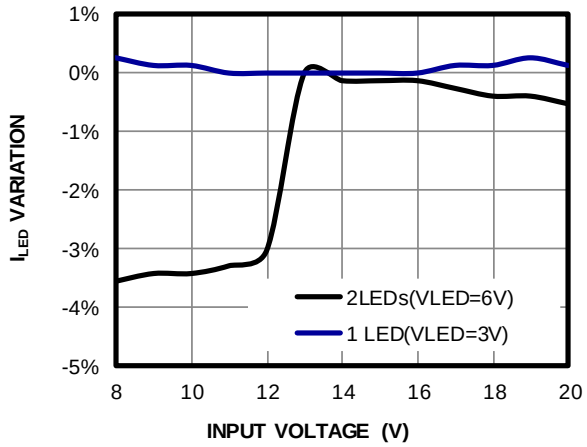
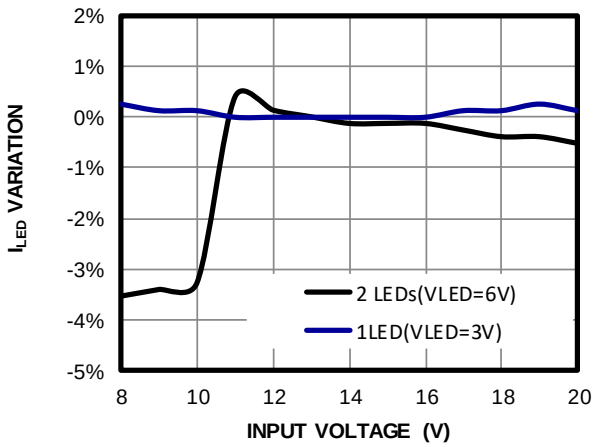
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck mode, 2 LEDs (V_{LED} = 6V), V_{IN} = 13.5V, f_{SW} = 2.3MHz, L = 4.7µH, T_A = 25°C, unless otherwise noted.

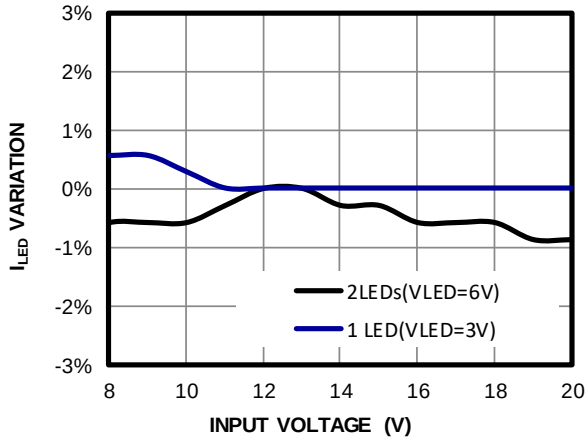
I_{LED} Variation vs. V_{IN}
L = 6.8µH, I_{LED} = 0.75A, V_{IN} ramping up



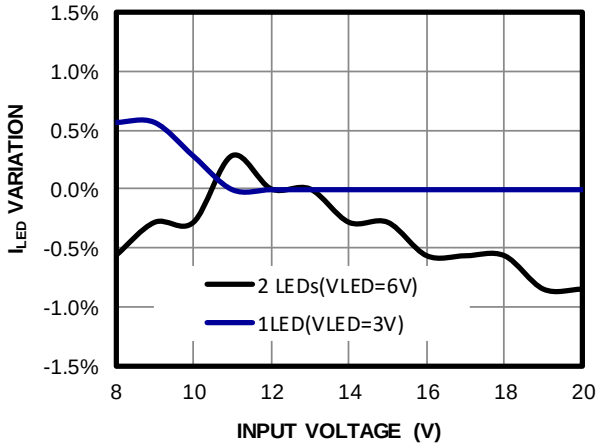
I_{LED} Variation vs. V_{IN}
L = 6.8µH, I_{LED} = 0.75A, V_{IN} ramping down



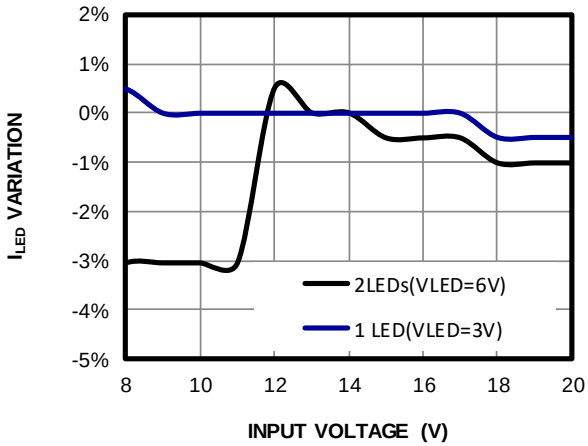
I_{LED} Variation vs. V_{IN}
L = 10µH, I_{LED} = 0.35A, V_{IN} ramping up



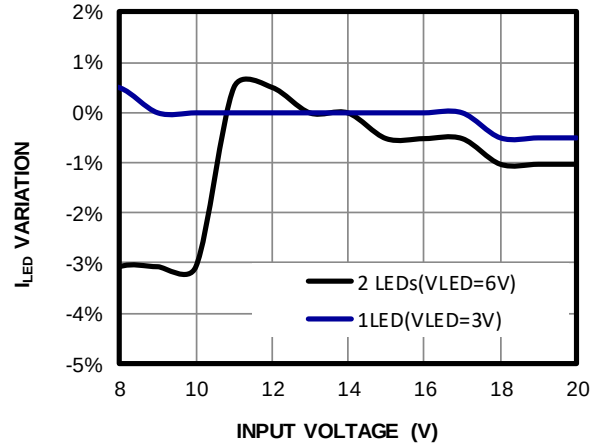
I_{LED} Variation vs. V_{IN}
L = 10µH, I_{LED} = 0.35A, V_{IN} ramping down



I_{LED} Variation vs. V_{IN}
L = 15µH, I_{LED} = 0.2A, V_{IN} ramping up



I_{LED} Variation vs. V_{IN}
L = 15µH, I_{LED} = 0.2A, V_{IN} ramping down



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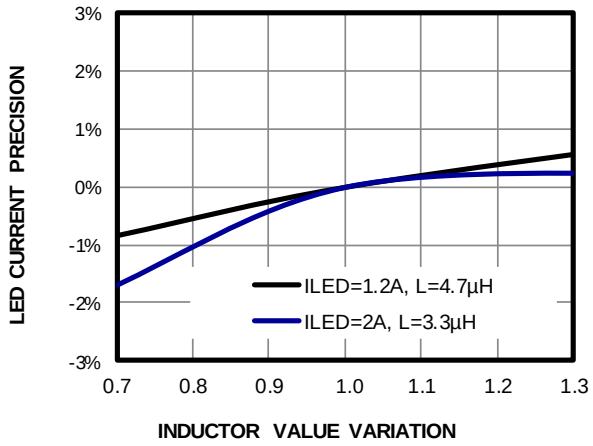
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck mode, 2 LEDs (V_{LED} = 6V), V_{IN} = 13.5V, f_{SW} = 2.3MHz, L = 4.7µH, T_A = 25°C, unless otherwise noted.

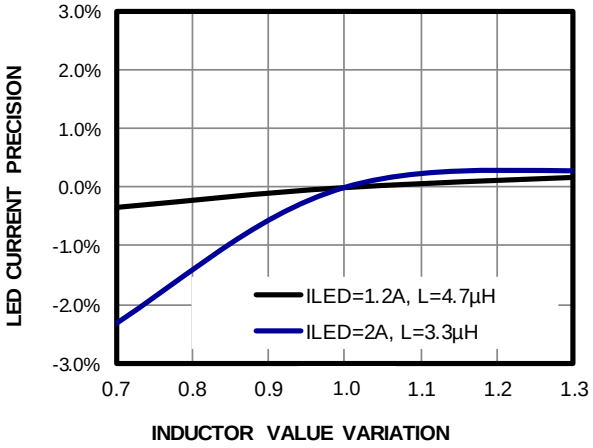
I_{LED} Precision vs. Inductor Value Variation

V_{IN} = 13.5V, 2 LEDs (V_{LED} = 6V)



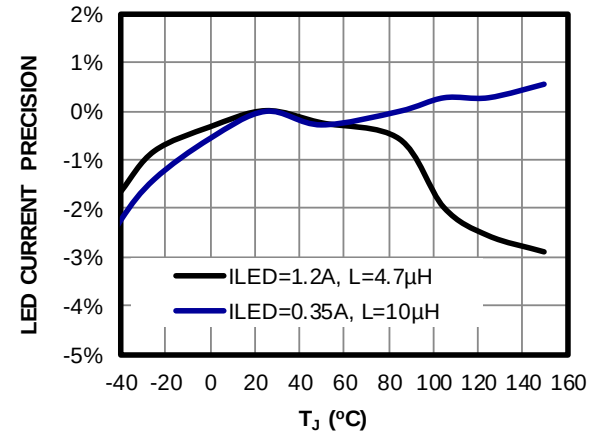
I_{LED} Precision vs. Inductor Value Variation

V_{IN} = 13.5V, 1 LED (V_{LED} = 3V)



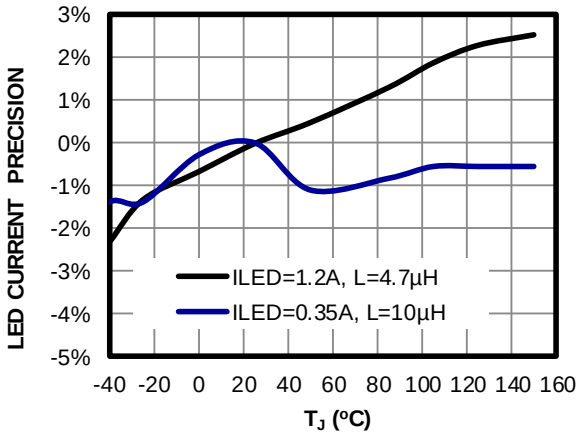
I_{LED} Precision vs. HS-FET Temperature Sense

2 LEDS (V_{LED} = 6V)



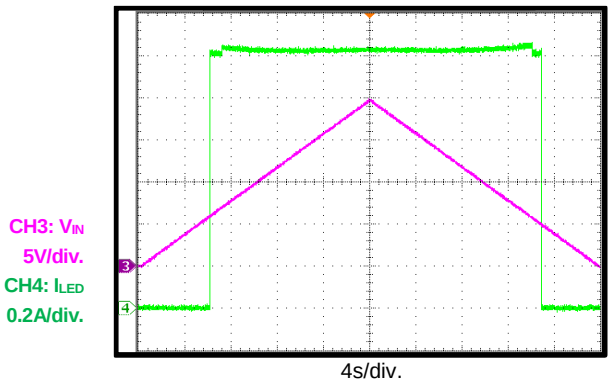
I_{LED} Precision vs. LS-FET Temperature Sense

2 LEDs (V_{LED} = 6V)



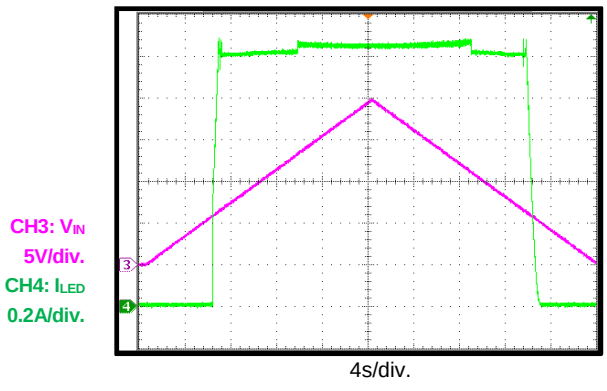
V_{IN} Slow Ramp Up and Down

2 LEDs (V_{LED} = 6V), I_{LED} = 1.2A,
V_{IN} = 0V to 20V, 0.001V/ms



V_{IN} Slow Ramp Up and Down

1 LED (V_{LED} = 3V), I_{LED} = 1.2A,
V_{IN} = 0V to 20V, 0.001V/ms



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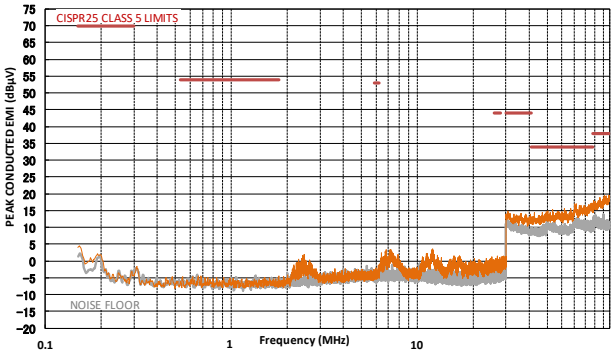
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck mode, V_{IN} = 12V, 2 LEDs in series (V_{LED} = 6V) when I_{LED} = 3A, L = 4.7µH, f_{SW} = 2.3MHz, with EMI filters, T_A = 25°C, unless otherwise noted. (7)

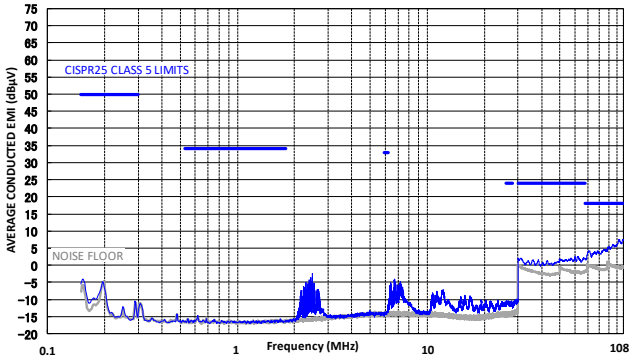
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



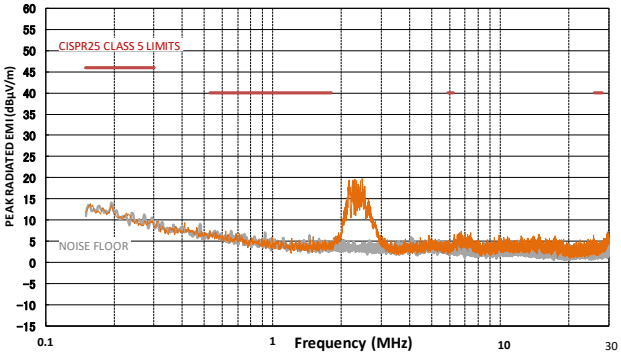
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



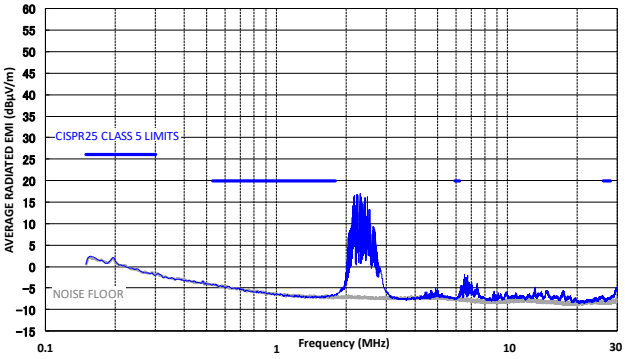
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



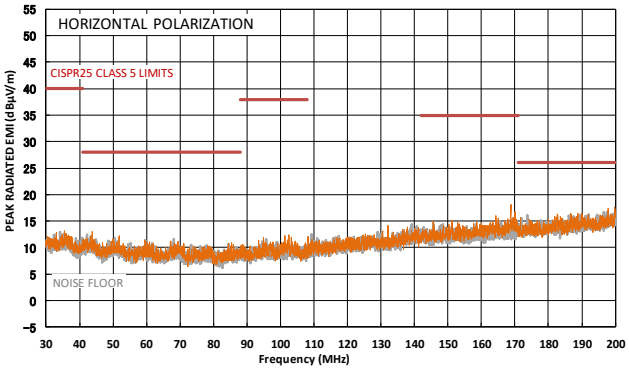
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



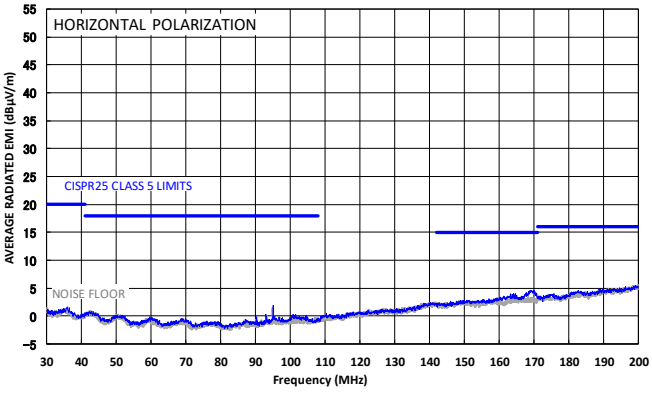
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 200MHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 200MHz



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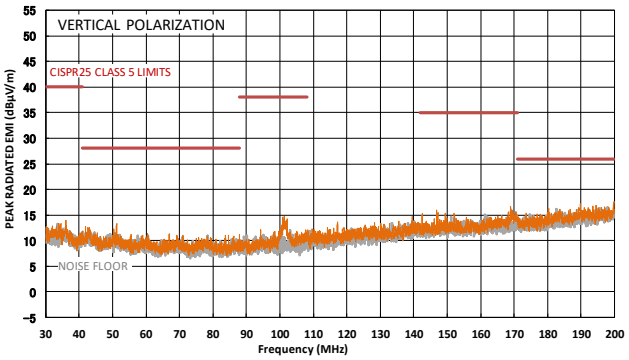
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck mode, V_{IN} = 12V, 2 LEDs in series (V_{LED} = 6V) when I_{LED} = 3A, L = 4.7µH, f_{SW} = 2.3MHz, with EMI filters, T_A = 25°C, unless otherwise noted. (7)

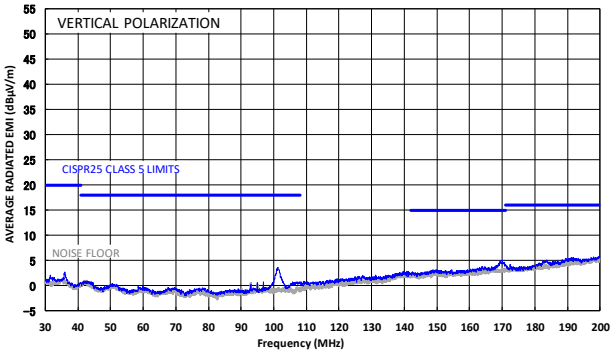
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 200MHz



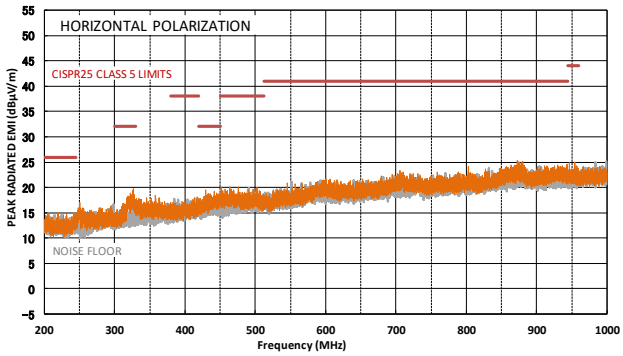
CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 200MHz



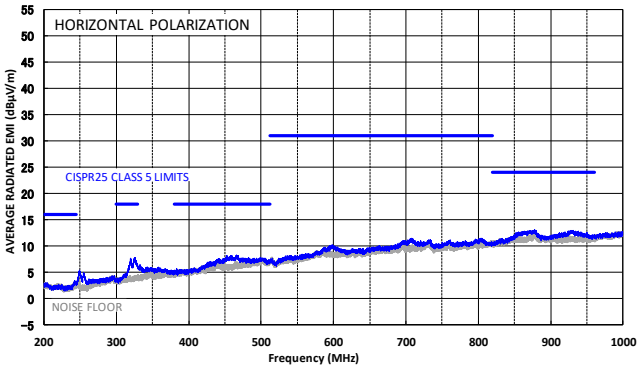
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 200MHz to 1GHz



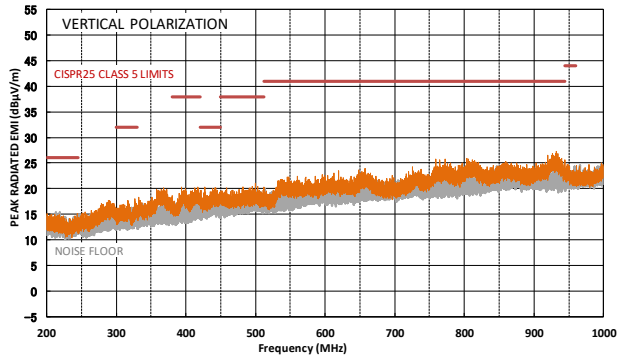
CISPR25 Class 5 Average Radiated Emissions

Horizontal, 200MHz to 1GHz



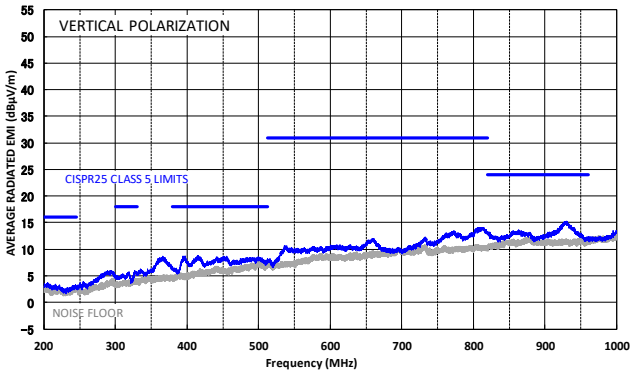
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 200MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 200MHz to 1GHz



Note:

7) Buck mode EMC test results are based on the application circuit with EMI filters (see Figure 11 on page 54).

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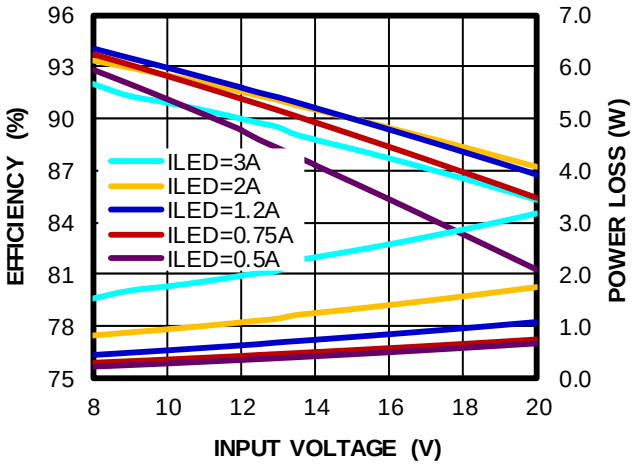
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck mode, 2 LEDs in series (V_{LED} = 6V), V_{IN} = 13.5V, f_{SW} = 2.3MHz, L = 4.7µH, T_A = 25°C, unless otherwise noted.

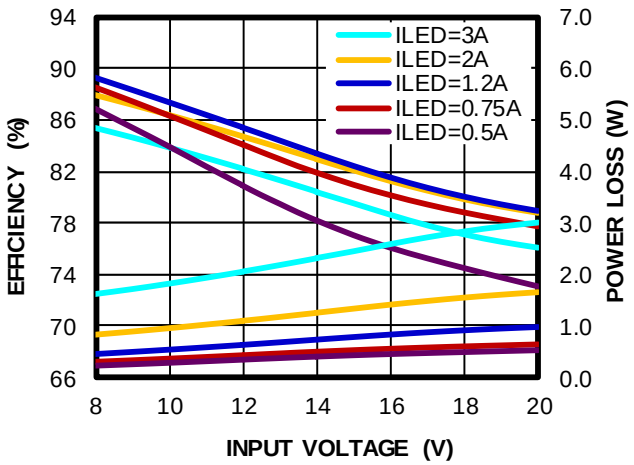
Efficiency vs. Input Voltage

2 LEDs (V_{LED} = 6V) , MOSFET Cut-Off when I_{LED} = 0.5A



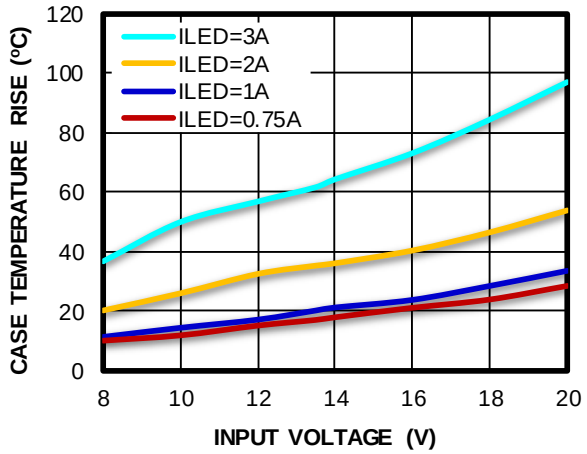
Efficiency vs. Input Voltage

1 LED (V_{LED} = 3V) , MOSFET Cut-Off when I_{LED} = 0.5A



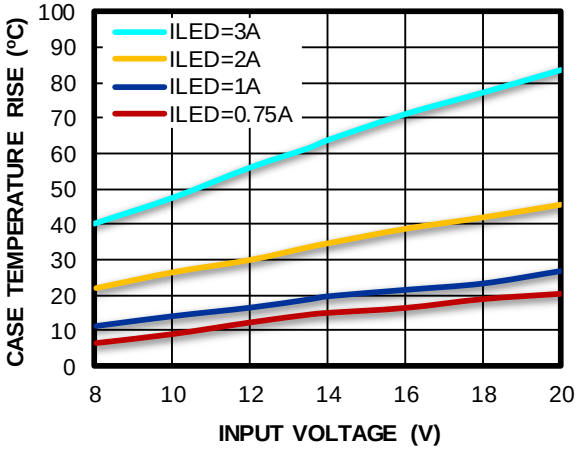
Case Temperature Rise vs. Input Voltage

2 LEDs (V_{LED} = 6V)



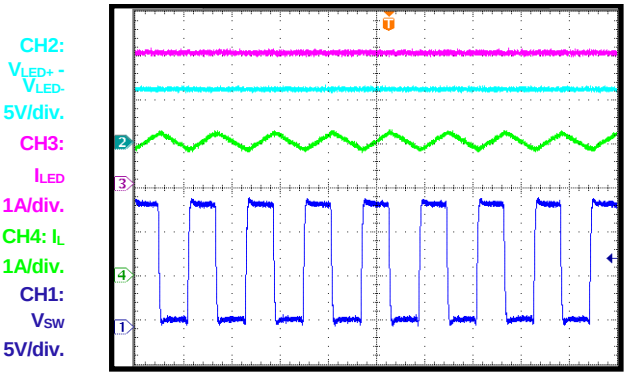
Case Temperature Rise with 1 LED

V_{LED} = 3V, MOSFET cut off when I_{LED} = 0.5A



Steady State

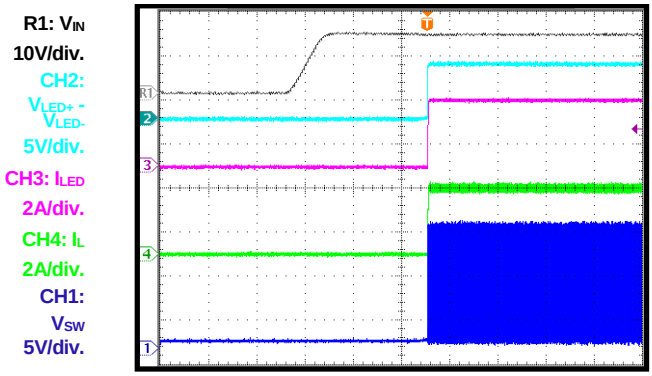
I_{LED} = 3A



400ns/div.

Start-Up through VIN

I_{LED} = 3A



2ms/div.

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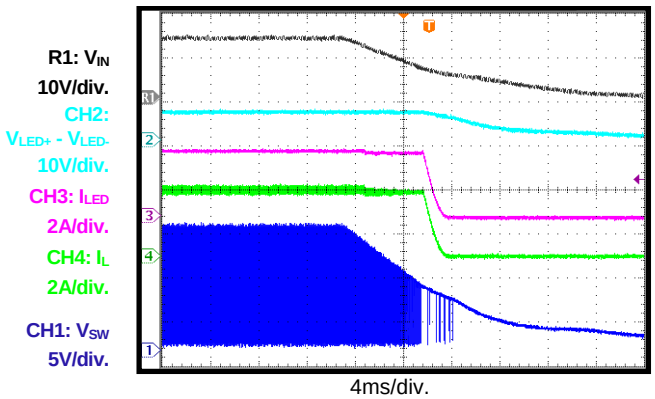
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck mode, 2 LEDs (V_{LED} = 6V), V_{IN} = 13.5V, f_{SW} = 2.3MHz, L = 4.7µH, T_A = 25°C, unless otherwise noted.

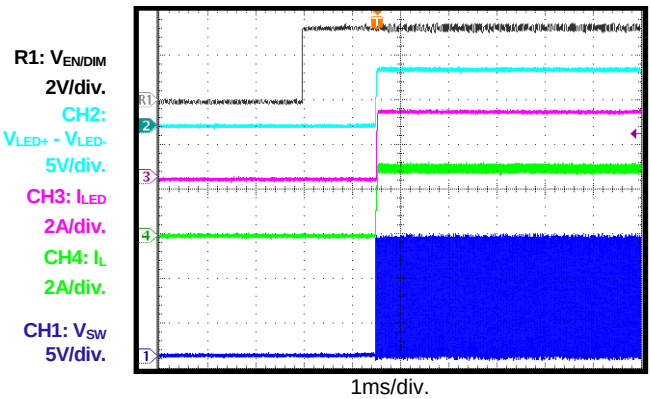
Shutdown through VIN

I_{LED} = 3A



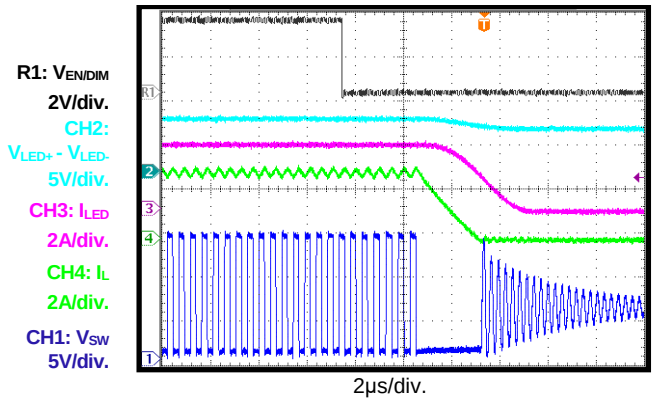
Start-Up through EN/DIM

I_{LED} = 3A



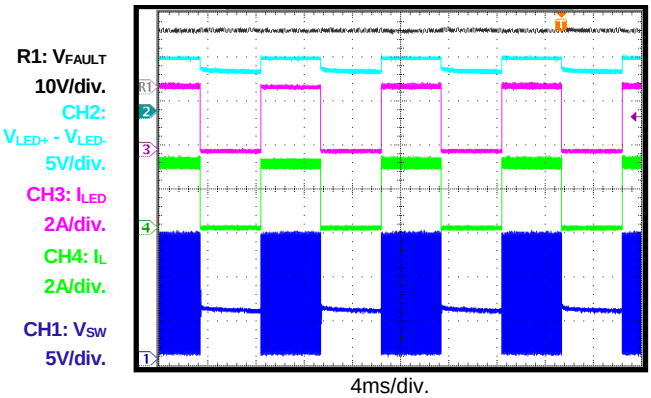
Shutdown through EN/DIM

I_{LED} = 3A



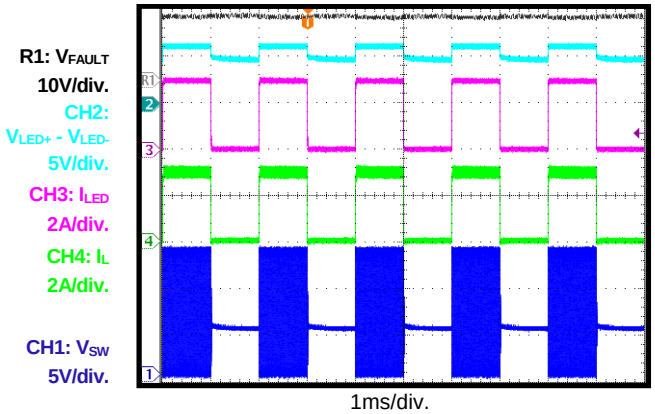
PWM Dimming Steady State

Dimming frequency = 100Hz



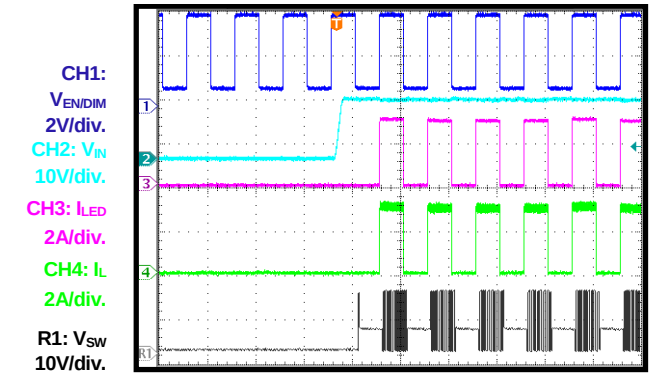
PWM Dimming Steady State

Dimming frequency = 500Hz



PWM Dimming

Start-up through VIN



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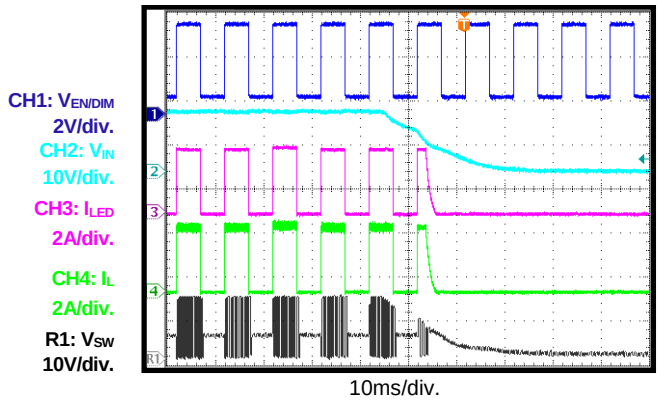
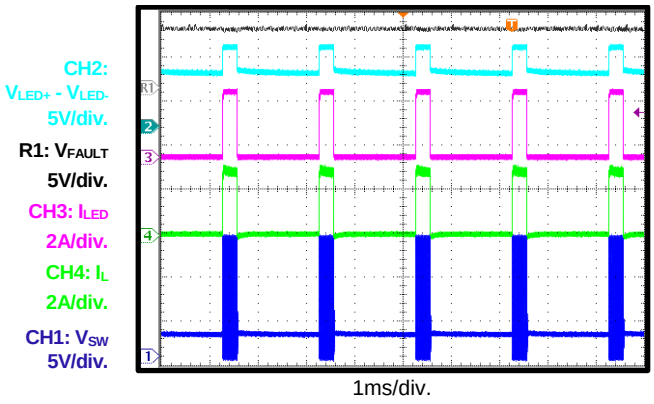
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck mode, 2 LEDs (V_{LED} = 6V), V_{IN} = 13.5V, f_{SW} = 2.3MHz, L = 4.7µH, T_A = 25°C, unless otherwise noted.

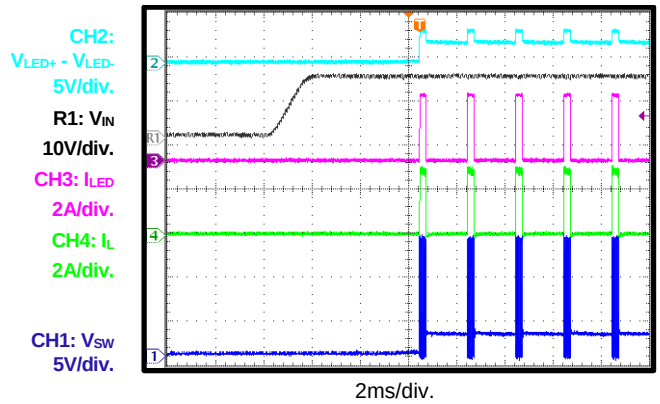
PWM Dimming
Shutdown through VIN



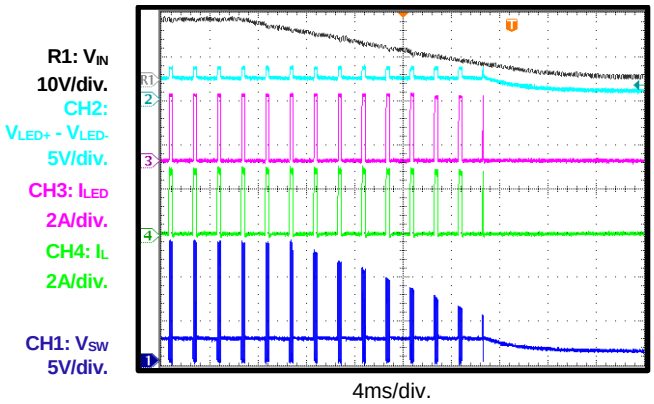
Two-Step Dimming
Steady state



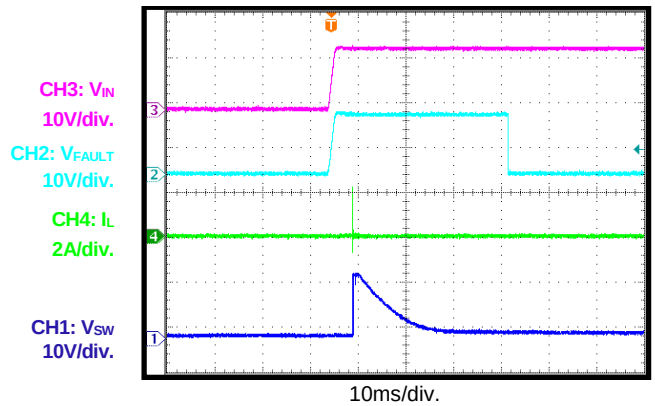
Two-Step Dimming
Start-up through VIN



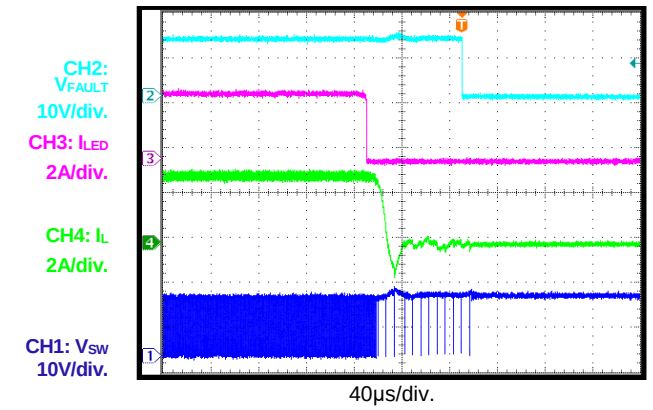
Two-Step Dimming
Shutdown through VIN



No Dimming
LED open start-up



No Dimming
LED open entry



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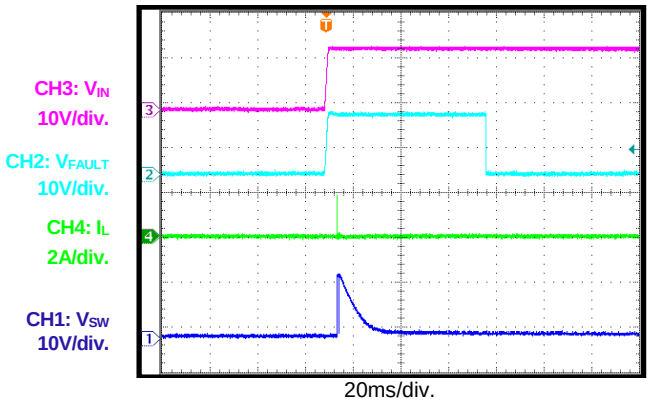
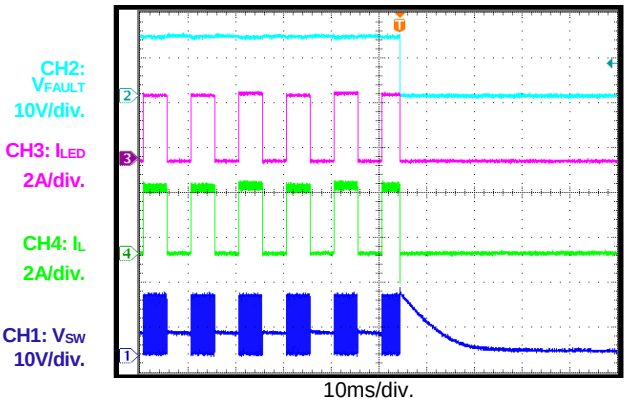
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck mode, 2 LEDs (V_{LED} = 6V), V_{IN} = 13.5V, f_{SW} = 2.3MHz, L = 4.7µH, T_A = 25°C, unless otherwise noted.

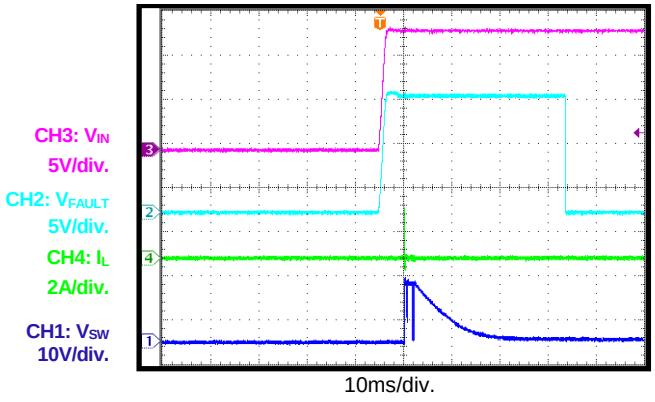
PWM Dimming
LED open start-up



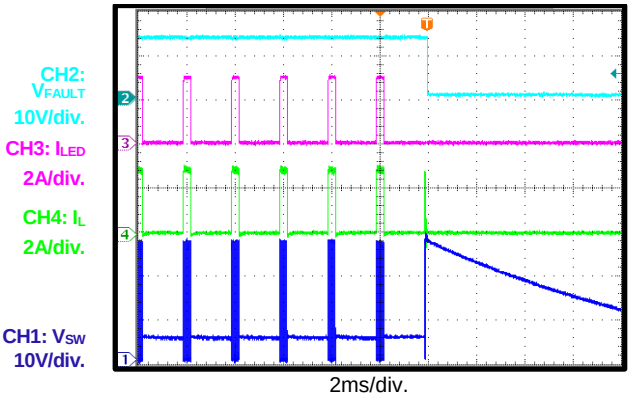
PWM Dimming
LED open entry



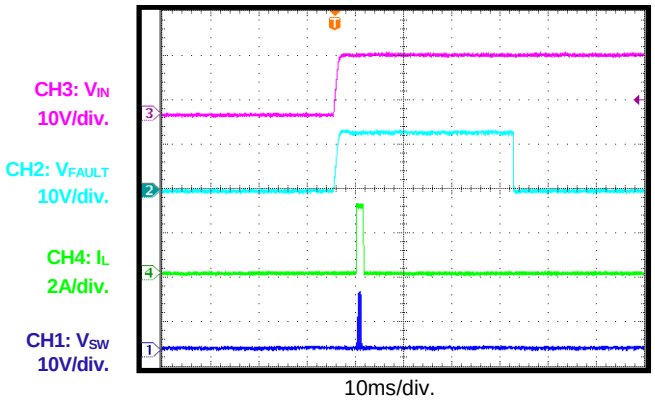
Two-Step Dimming
LED open start-up



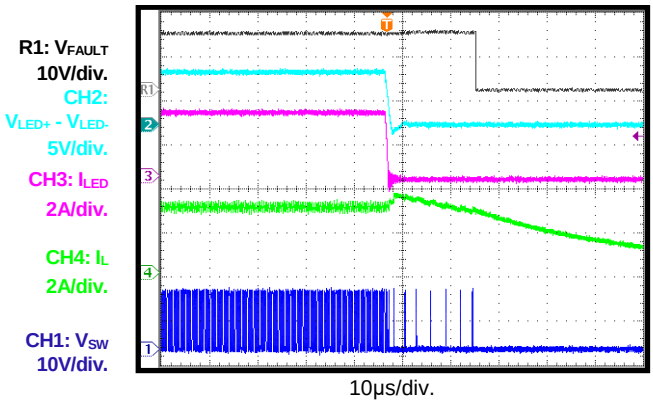
Two-Step Dimming
LED open entry



No Dimming
LED+ short to LED- start-up



No Dimming
LED+ short to LED- entry



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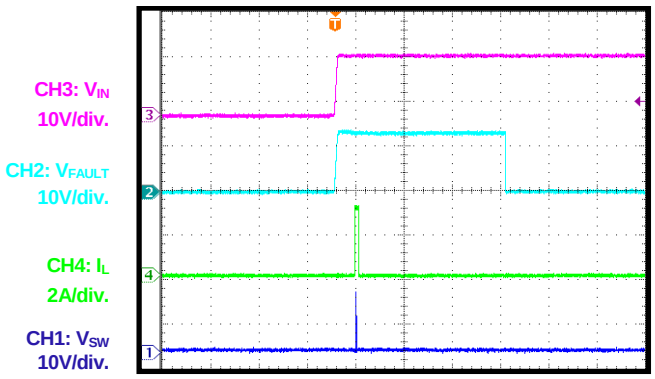
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

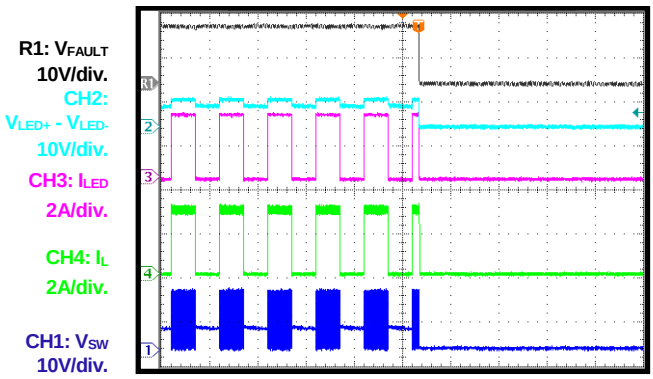
Buck mode, 2 LEDs (V_{LED} = 6V), V_{IN} = 13.5V, f_{SW} = 2.3MHz, L = 4.7µH, T_A = 25°C, unless otherwise noted.

PWM Dimming
LED+ short to LED- start-up



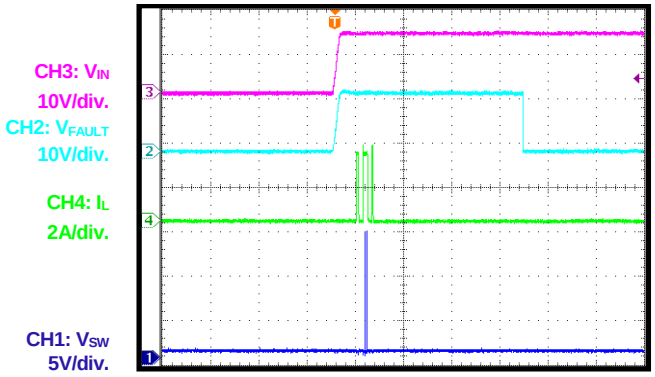
20ms/div.

PWM Dimming
LED+ short to LED- entry



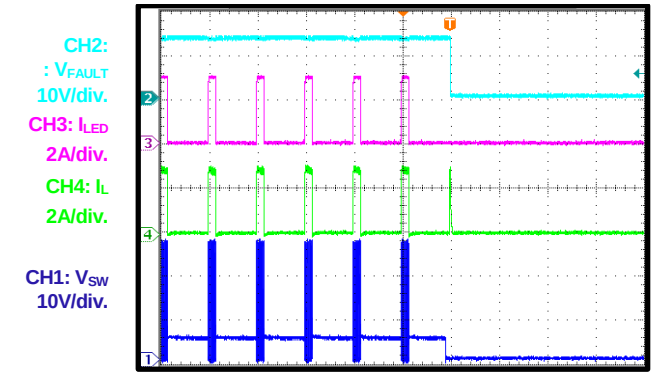
10ms/div.

Two-Step Dimming
LED+ short to LED- start-up



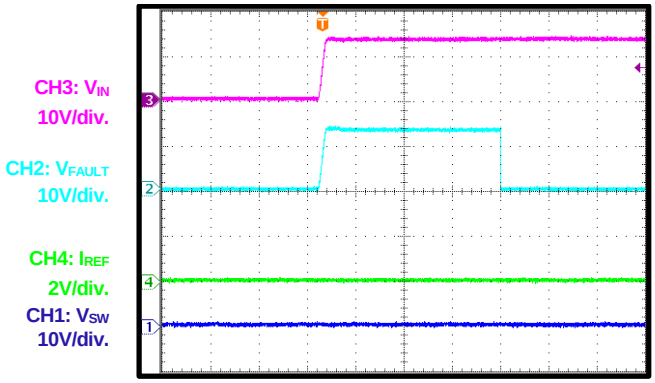
10ms/div.

Two-Step Dimming
LED+ short to LED- entry



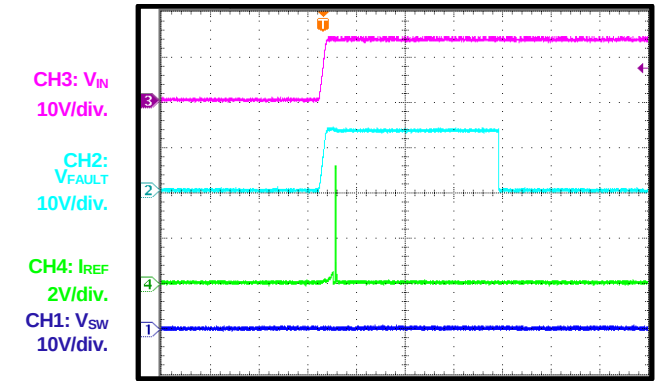
2ms/div.

IREF Short Before IC Starts Up



10ms/div.

IREF Open Before IC Starts Up



10ms/div.

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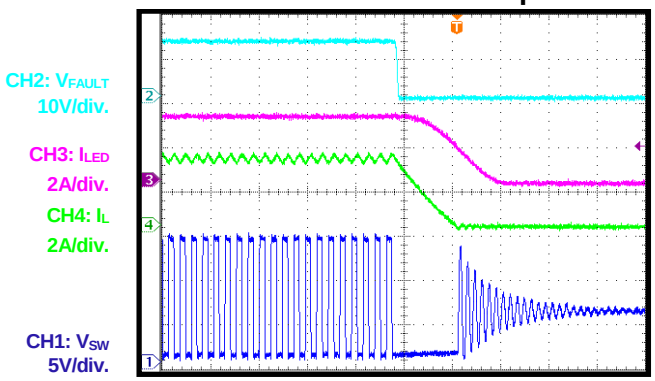
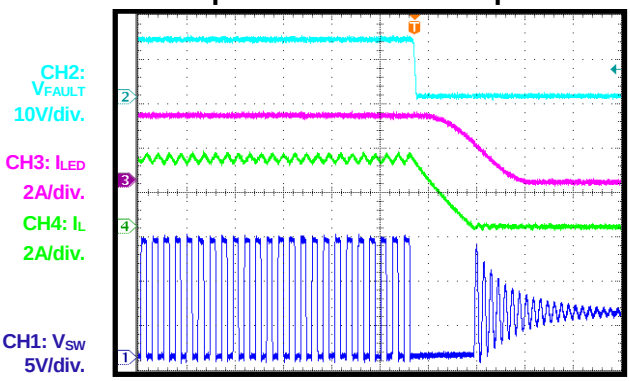
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck mode, 2 LEDs (V_{LED} = 6V), V_{IN} = 13.5V, f_{SW} = 2.3MHz, L = 4.7µH, T_A = 25°C, unless otherwise noted.

IREF Short after IC Starts Up

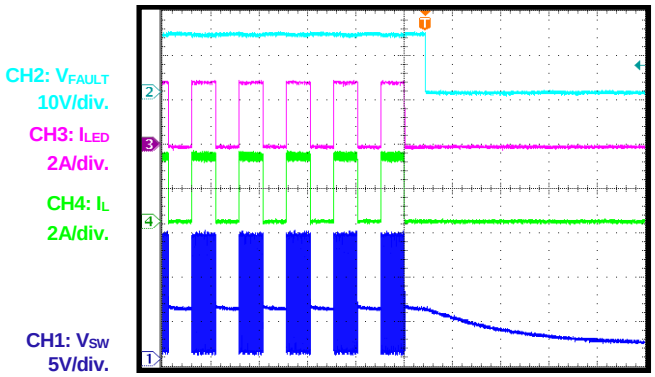


IREF Open after IC Starts Up



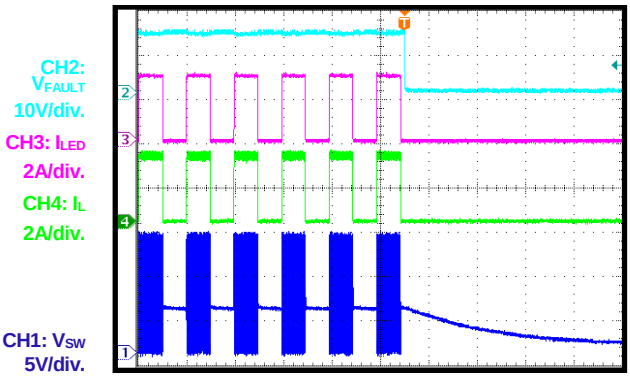
IREF Short after IC Starts Up

PWM dimming



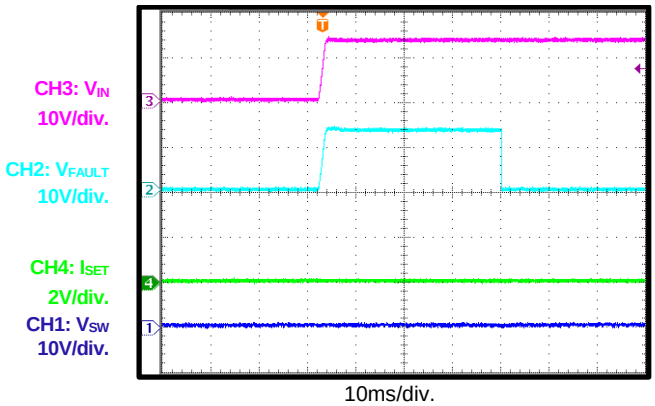
IREF Open after IC Starts Up

PWM dimming



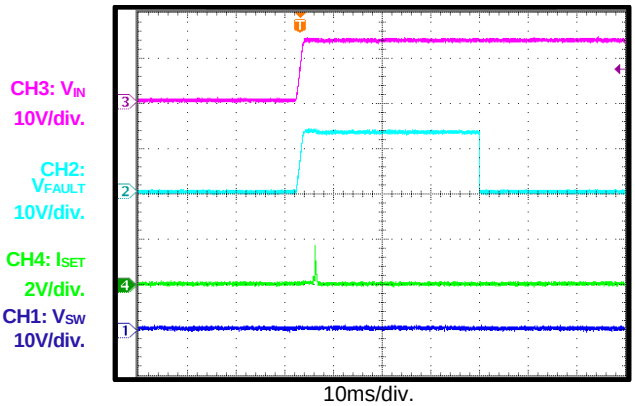
ISET Short Before IC Starts Up

PWM dimming



ISET Open Before IC Starts Up

PWM dimming



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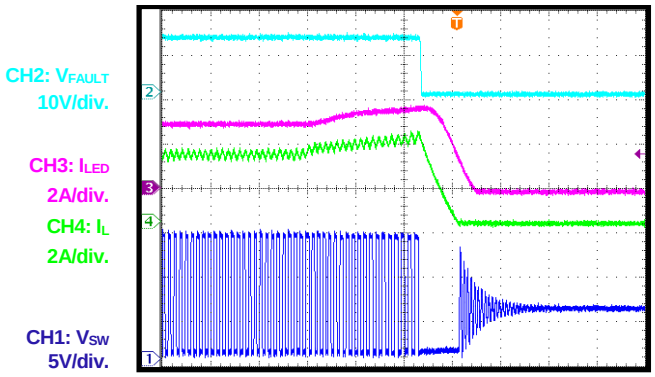
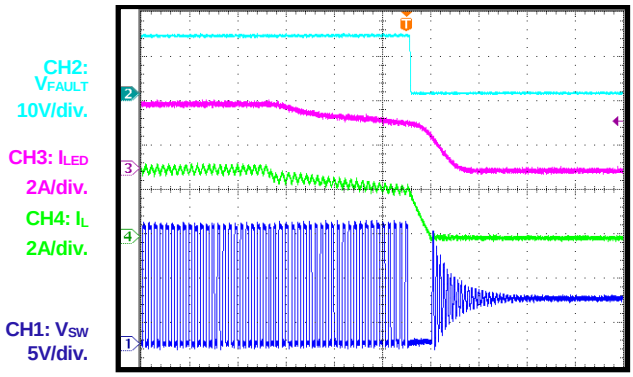
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck mode, 2 LEDs (V_{LED} = 6V), V_{IN} = 13.5V, f_{SW} = 2.3MHz, L = 4.7µH, T_A = 25°C, unless otherwise noted.

ISET Short after IC Starts Up

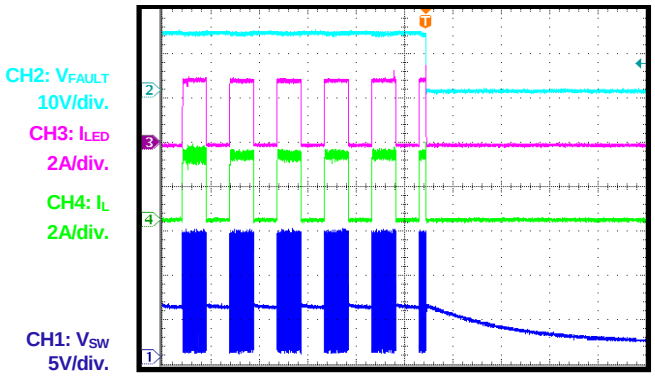


ISET Open after IC Starts Up



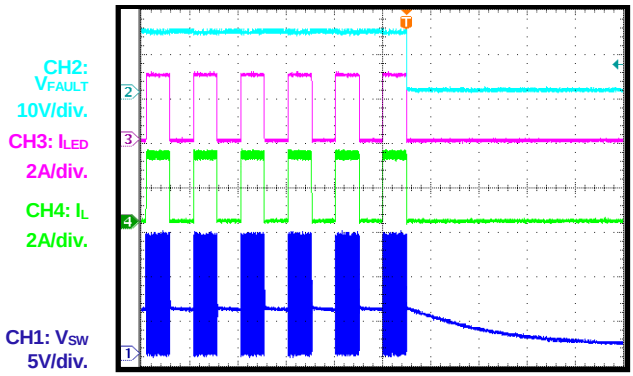
ISET Short after IC Starts Up

PWM dimming

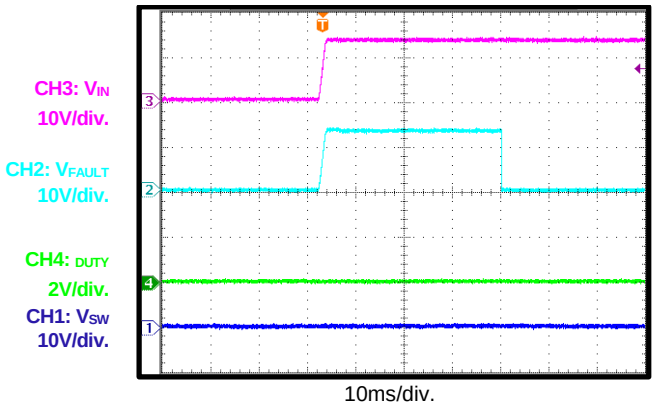


ISET Open after IC Starts Up

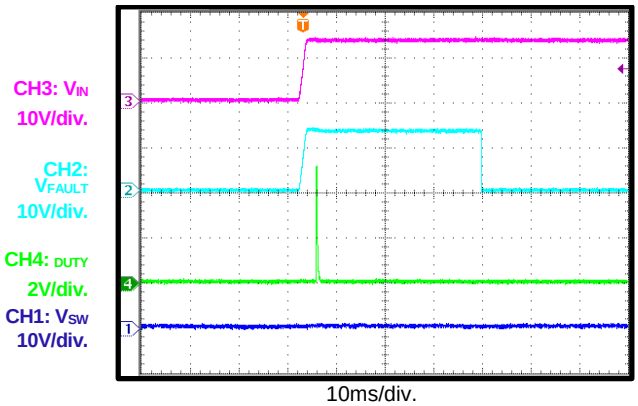
PWM dimming



DUTY Short before IC Starts Up



DUTY Open before IC Starts Up



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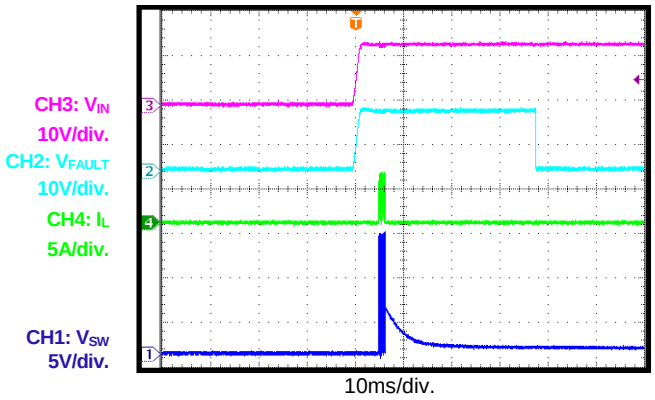
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck mode, 2 LEDs (V_{LED} = 6V), V_{IN} = 13.5V, f_{SW} = 2.3MHz, L = 4.7µH, T_A = 25°C, unless otherwise noted.

False Mode Detection during VIN Start-Up



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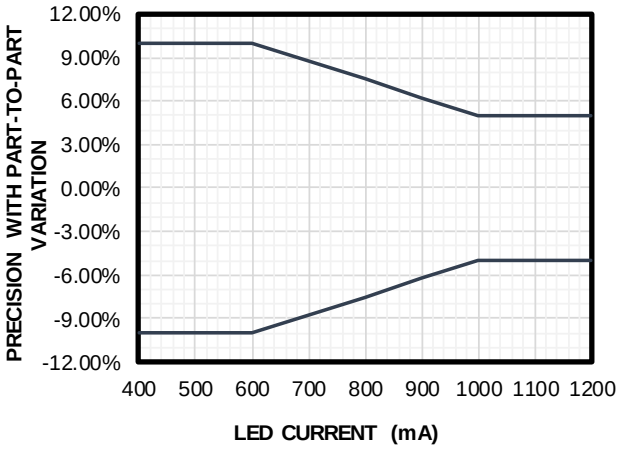
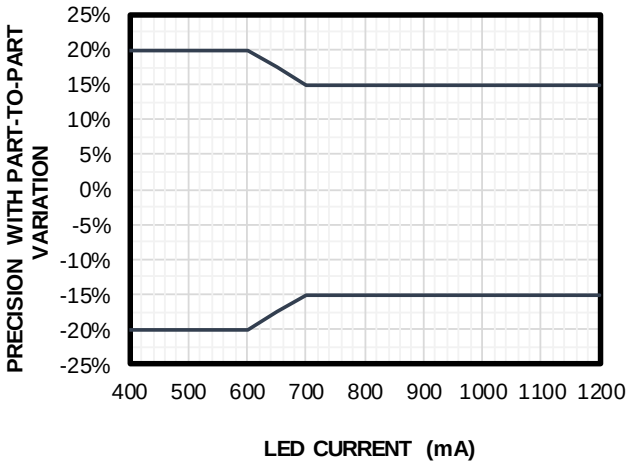
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck-boost mode, 4 LEDs (V_{LED} = 12V), V_{IN} = 13.5V, f_{SW} = 1.15MHz, L = 4.7µH, T_A = 25°C, unless otherwise noted.

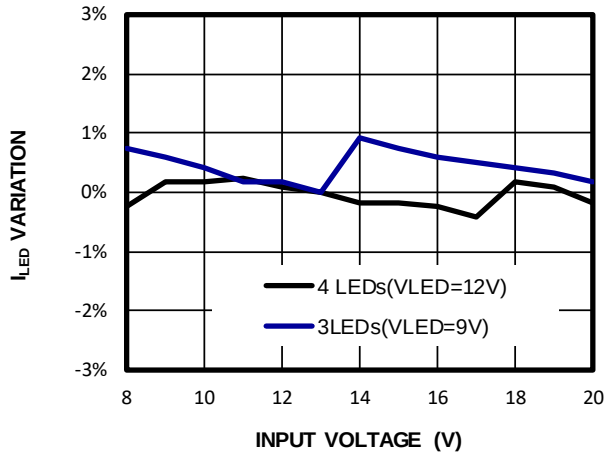
I_{LED} Part-to-Part Variation
T_J = 25°C to 100°C



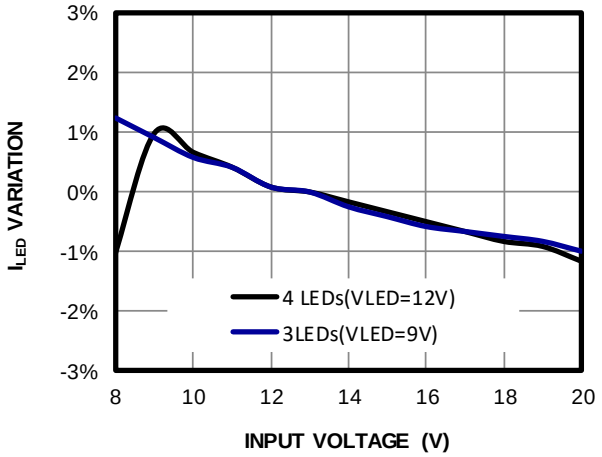
I_{LED} Part-to-Part Variation
T_J = -40°C to +150°C



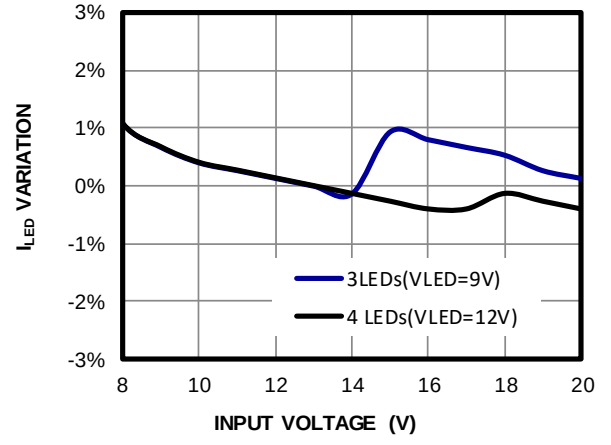
I_{LED} Variation vs. V_{IN}
L = 3.3µH, I_{LED} = 1.2A, V_{IN} ramping up



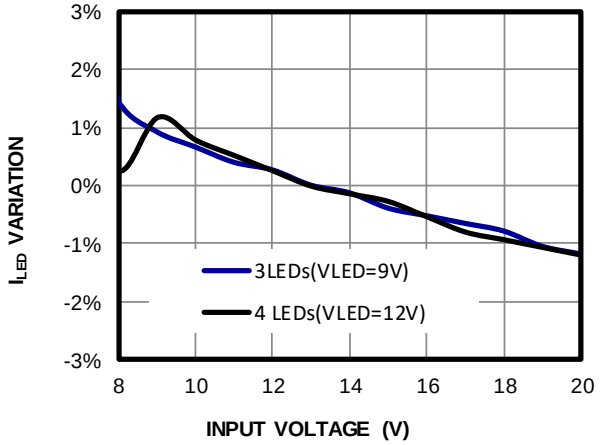
I_{LED} Variation vs. V_{IN}
L = 3.3µH, I_{LED} = 1.2A, V_{IN} ramping down



I_{LED} Variation vs. V_{IN}
L = 6.8µH, I_{LED} = 0.75A, V_{IN} ramping up



I_{LED} Variation vs. V_{IN}
L = 6.8µH, I_{LED} = 0.75A, V_{IN} ramping down



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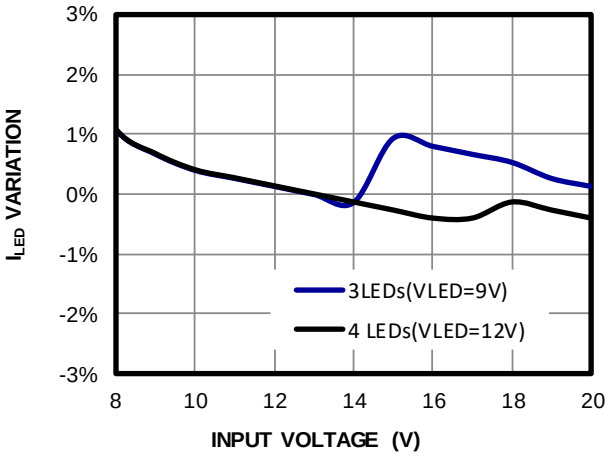
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck-boost mode, 4 LEDs (V_{LED} = 12V), V_{IN} = 13.5V, f_{SW} = 1.15MHz, L = 4.7µH, T_A = 25°C, unless otherwise noted.

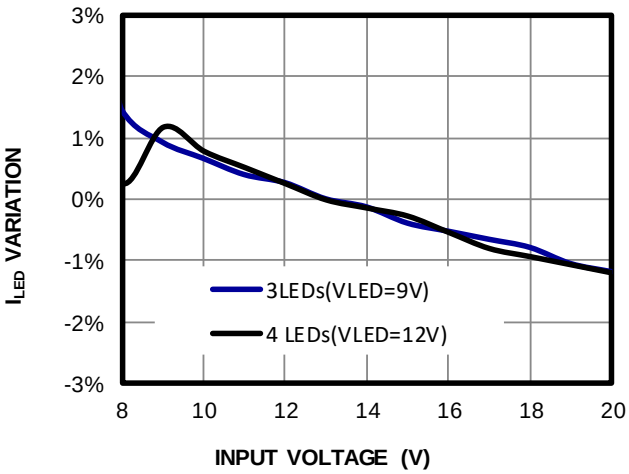
I_{LED} Variation vs. V_{IN}

L = 4.7µH, I_{LED} = 1A, V_{IN} ramping up



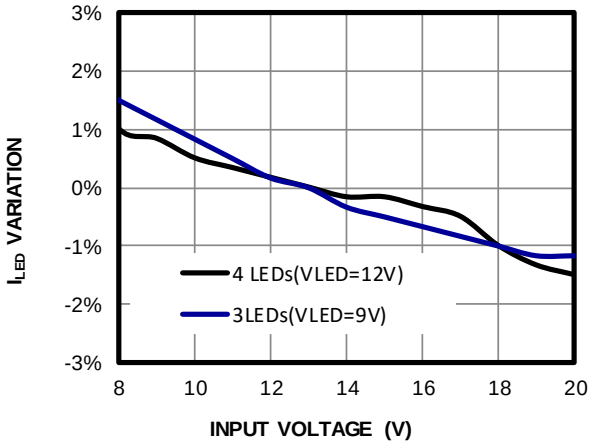
I_{LED} Variation vs. V_{IN}

L = 4.7µH, I_{LED} = 1A, V_{IN} ramping down



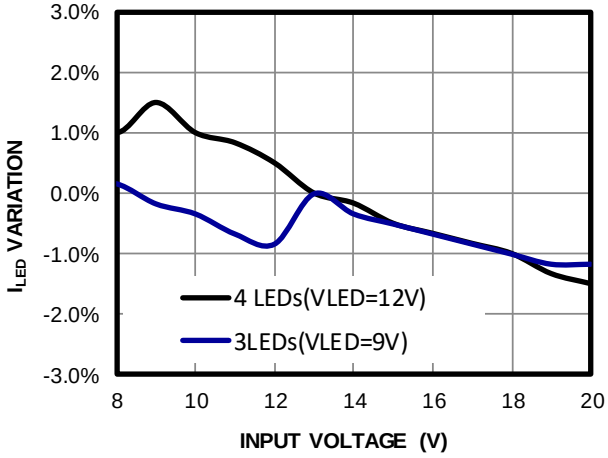
I_{LED} Variation vs. V_{IN}

L = 6.8µH, I_{LED} = 0.6A, V_{IN} ramping up



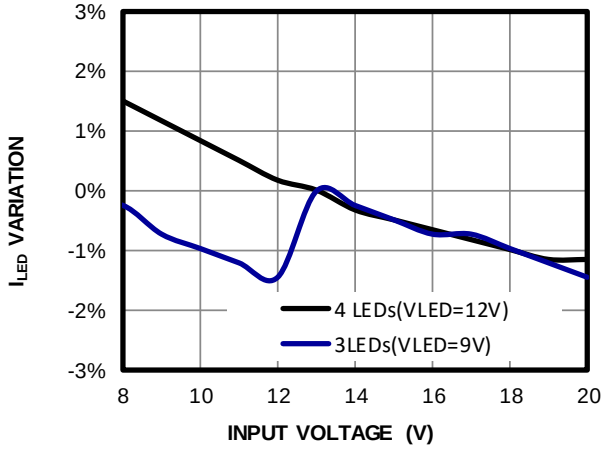
I_{LED} Variation vs. V_{IN}

L = 6.8µH, I_{LED} = 0.6A, V_{IN} ramping down



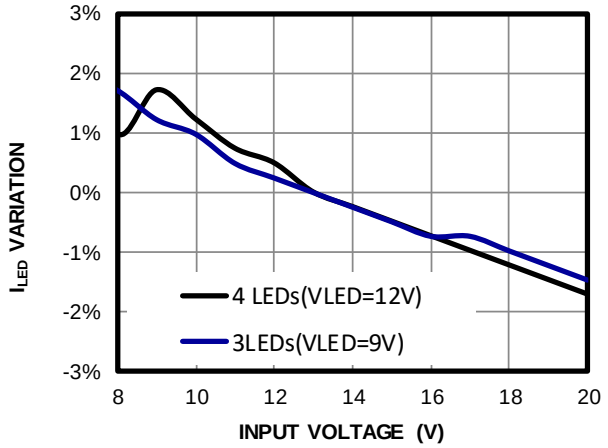
I_{LED} Variation vs. V_{IN}

L = 10µH, I_{LED} = 0.4A, V_{IN} ramping up



I_{LED} Variation vs. V_{IN}

L = 10µH, I_{LED} = 0.4A, V_{IN} ramping down



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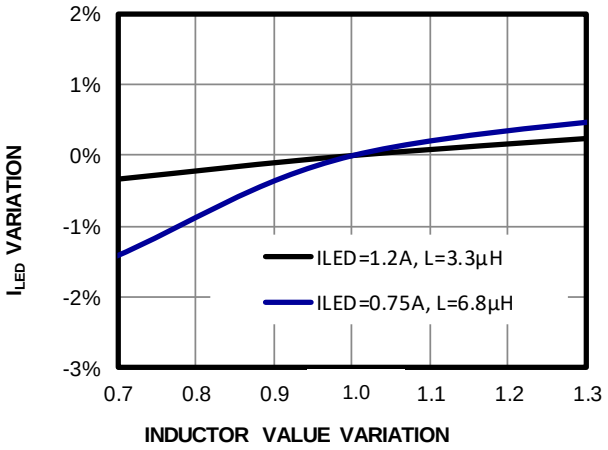
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck-boost mode, 4 LEDs (V_{LED} = 12V), V_{IN} = 13.5V, f_{SW} = 1.15MHz, L = 4.7µH, T_A = 25°C, unless otherwise noted.

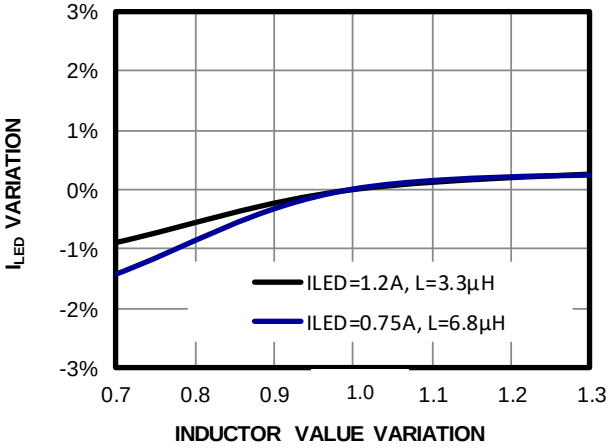
LED Current Precision vs. Inductor Value Variation

V_{IN} = 13.5V, 4 LEDs (V_{LED} = 12V)



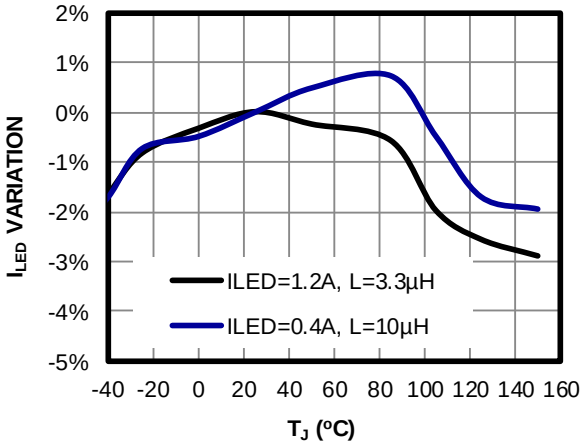
LED Current Precision vs. Inductor Value Variation

V_{IN} = 13.5V, 3 LEDs (V_{LED} = 9V)



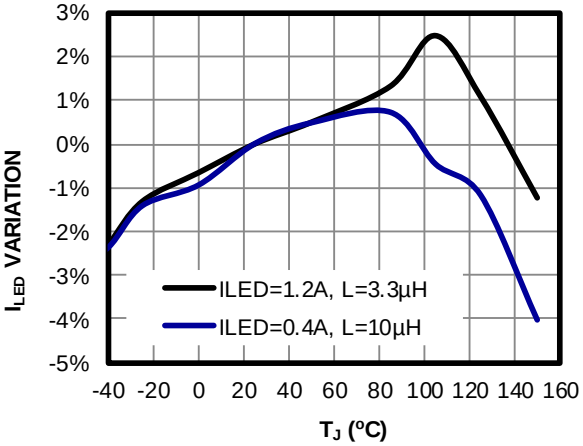
I_{LED} Precision vs. Temperature HS-FET Sense

4 LEDs (V_{LED} = 12V)



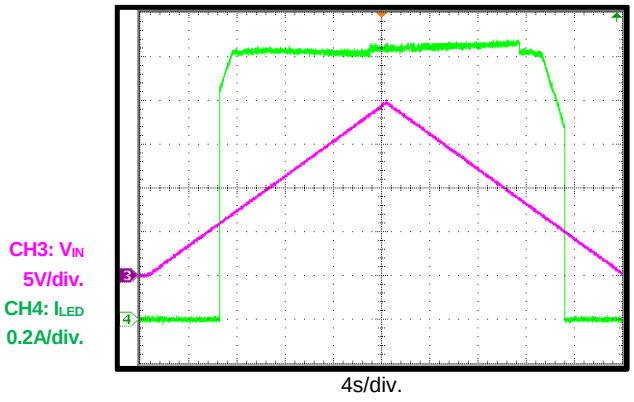
I_{LED} Precision vs. Temperature LS-FET Sense

4 LEDs (V_{LED} = 12V)



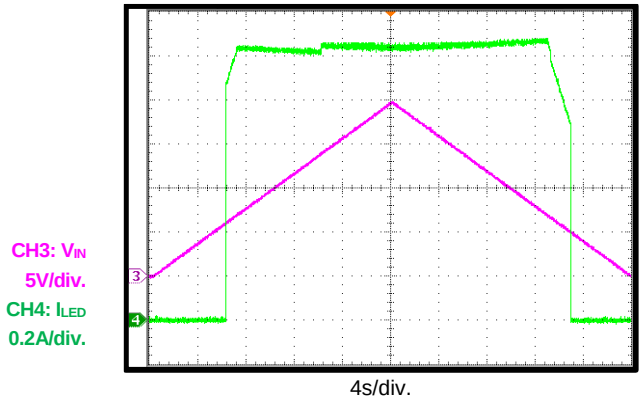
V_{IN} Slow Ramp Up and Down

4 LEDs (V_{LED} = 12V), I_{LED} = 1.2A,
V_{IN} = 0V to 20V, 0.001V/ms



V_{IN} Slow Ramp Up and Down

3 LEDs (V_{LED} = 9V), I_{LED} = 1.2A,
V_{IN} = 0V to 20V, 0.001V/ms



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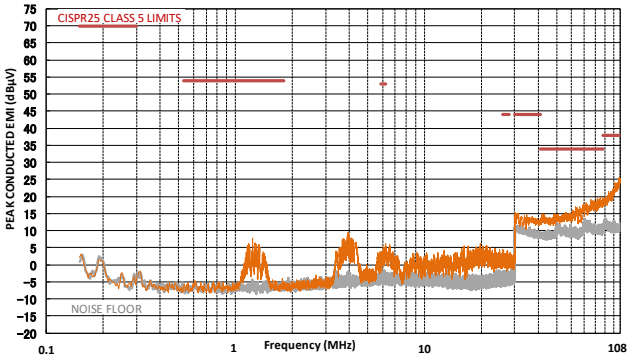
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck-boost mode, V_{IN} = 12V, 4 LEDs in series (V_{LED} = 12V) when I_{LED} = 1.2A, L = 4.7µH, f_{SW} = 1.15MHz, with EMI filters, T_A = 25°C, unless otherwise noted. (8)

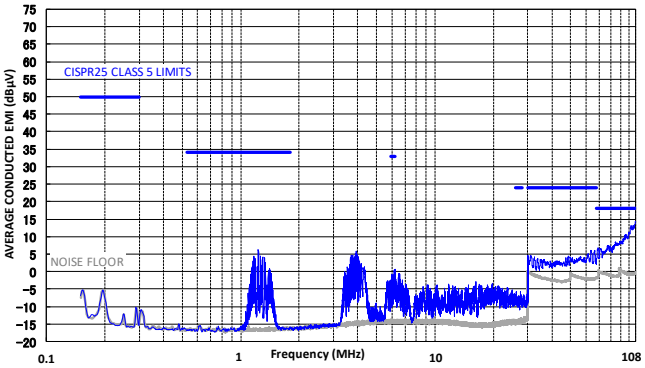
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



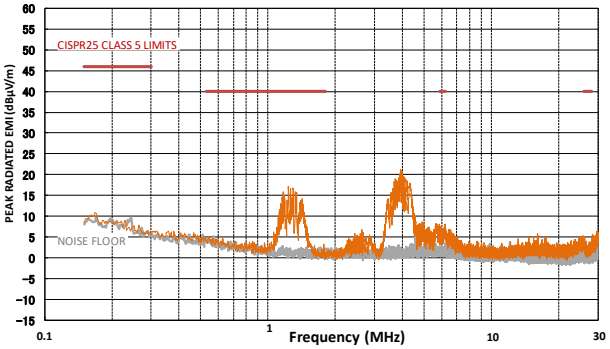
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



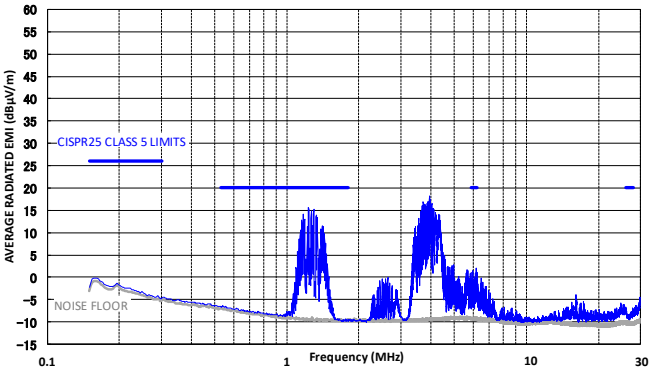
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



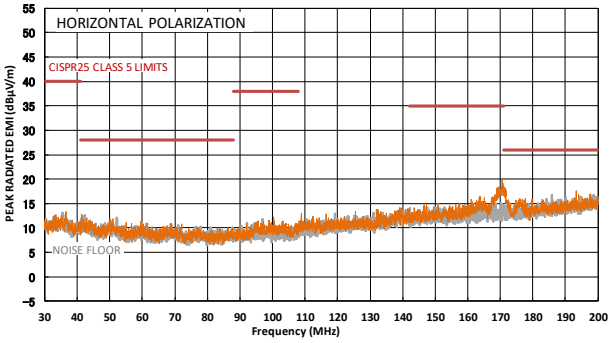
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



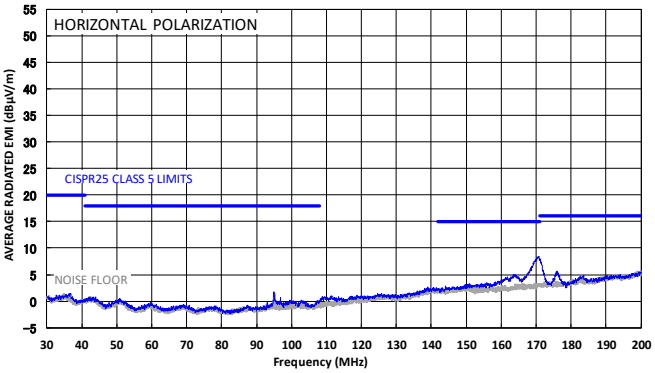
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 200MHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 200MHz



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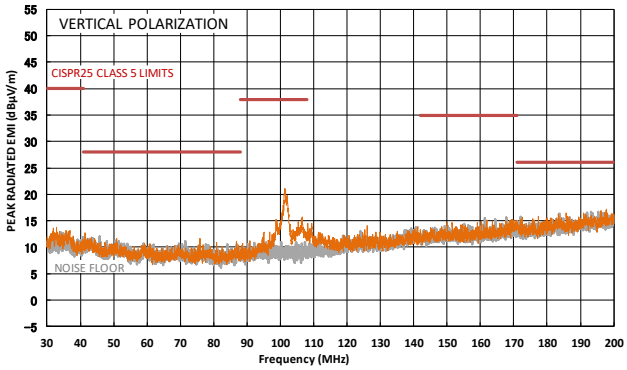
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck-boost mode, V_{IN} = 12V, 4 LEDs in series (V_{LED} = 12V) when I_{LED} = 1.2A, L = 4.7µH, f_{SW} = 1.15MHz, with EMI filters, T_A = 25°C, unless otherwise noted. (8)

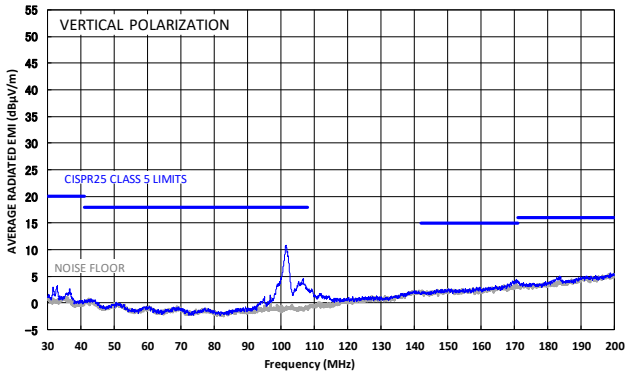
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 200MHz



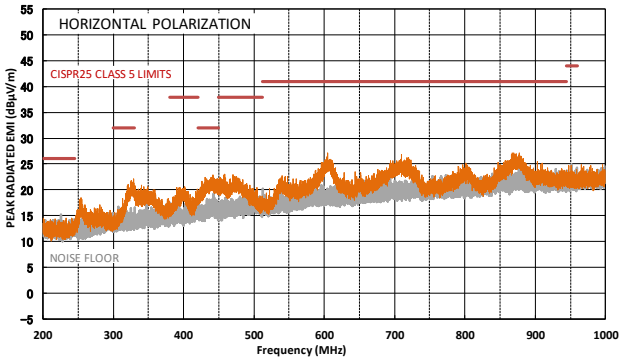
CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 200MHz



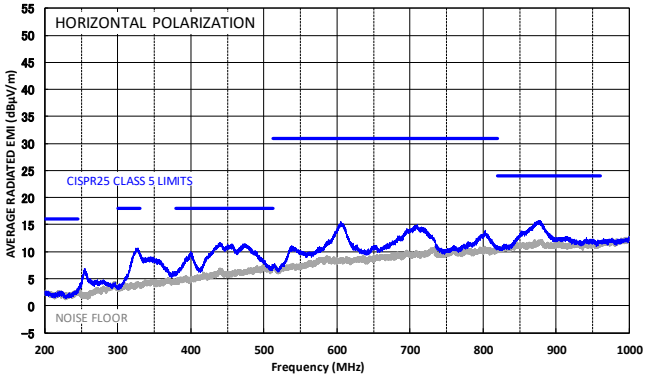
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 200MHz to 1GHz



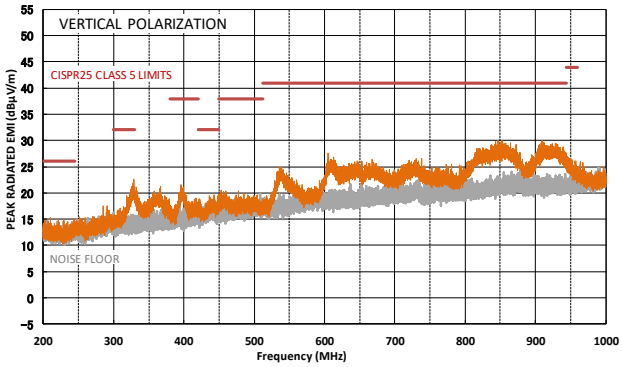
CISPR25 Class 5 Average Radiated Emissions

Horizontal, 200MHz to 1GHz



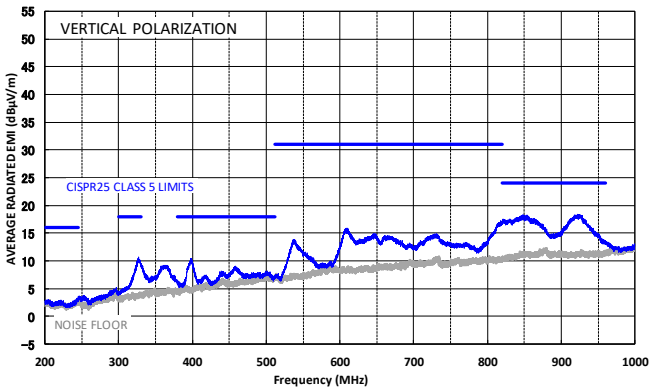
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 200MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 200MHz to 1GHz



Note:

8) The MP7200 buck-boost mode EMC test results are based on the application circuit with EMI filters (see Figure 12 on page 54).

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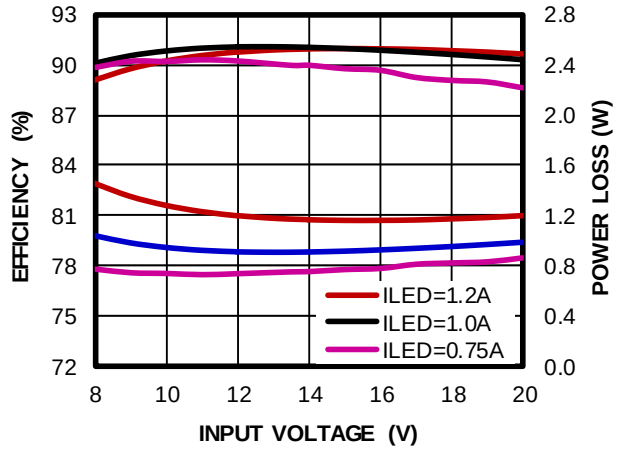
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck-boost mode, 4 LEDs (V_{LED} = 12V), V_{IN} = 13.5V, f_{SW} = 1.15MHz, L = 4.7µH, T_A = 25°C, unless otherwise noted.

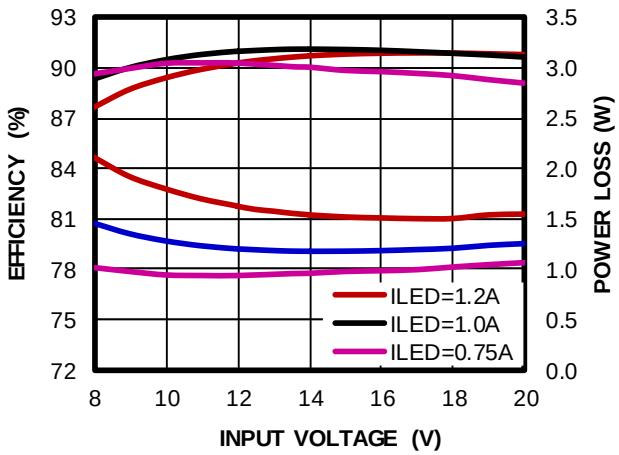
Efficiency vs. Input Voltage

3 LEDs (V_{LED} = 9V)



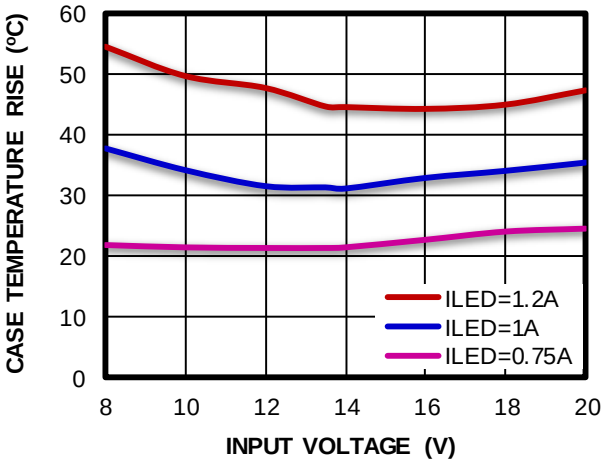
Efficiency vs. Input Voltage

4 LEDs (V_{LED} = 12V)



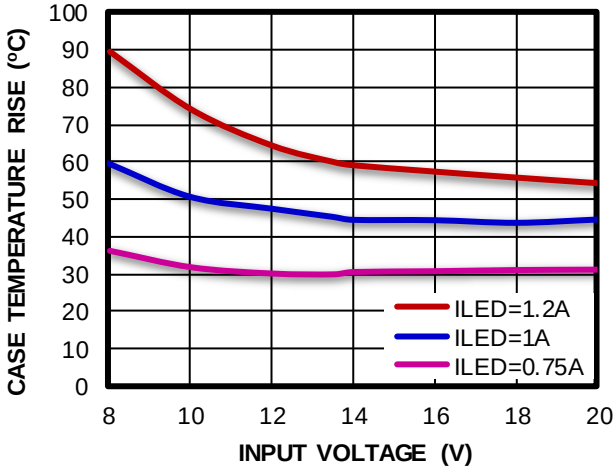
Case Temperature Rise vs. Input Voltage

3 LEDs (V_{LED} = 9V)



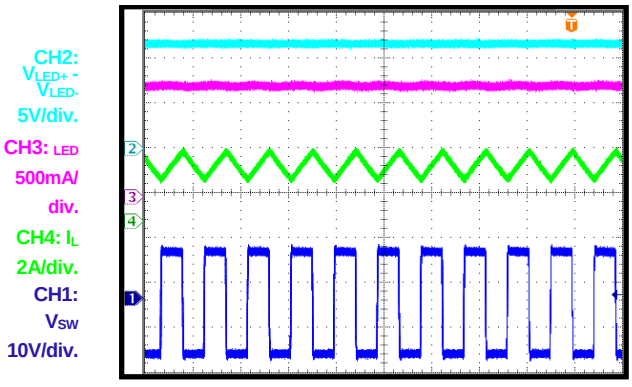
Case Temperature Rise vs. Input Voltage

4 LEDs (V_{LED} = 12V)



Steady State

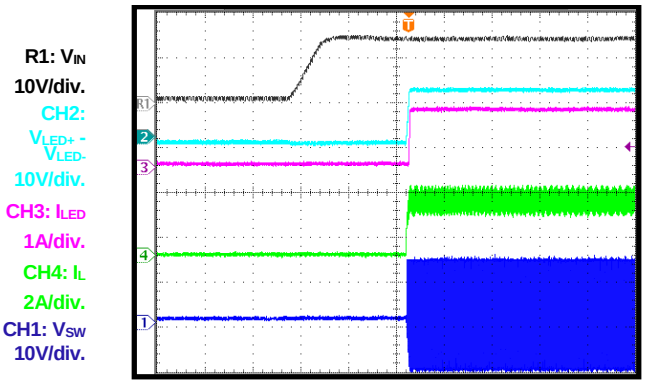
I_{LED} = 1.2A



1µs/div.

Start-Up through VIN

I_{LED} = 1.2A



2ms/div.

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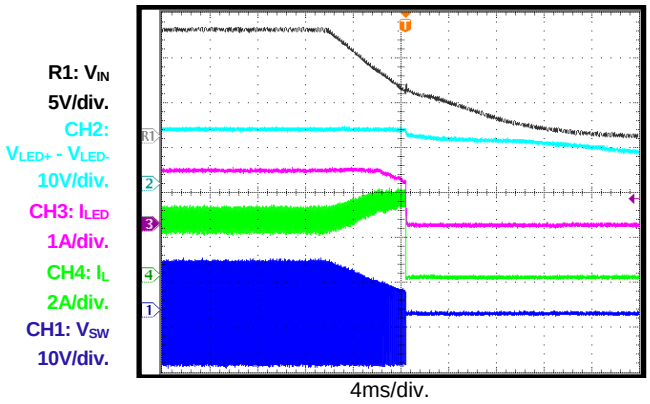
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck-boost mode, 4 LEDs (V_{LED} = 12V), V_{IN} = 13.5V, f_{SW} = 1.15MHz, L = 4.7µH, T_A = 25°C, unless otherwise noted.

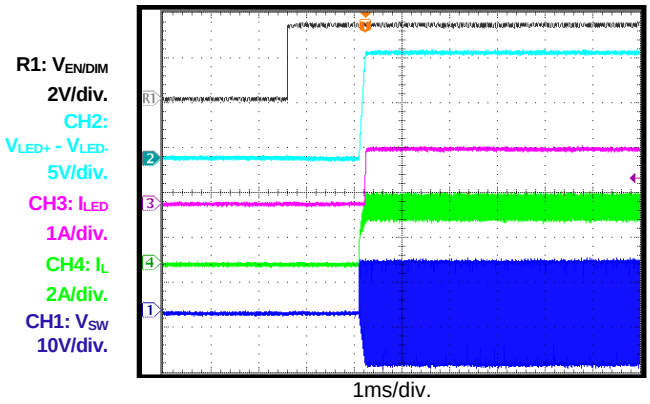
Shutdown through VIN

I_{LED} = 1.2A



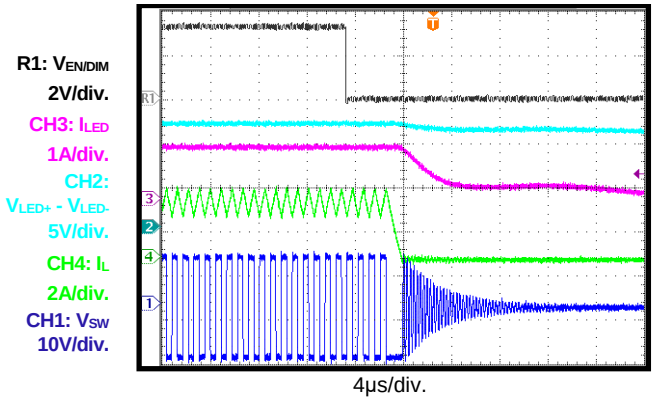
Start-Up through EN/DIM

I_{LED} = 1.2A



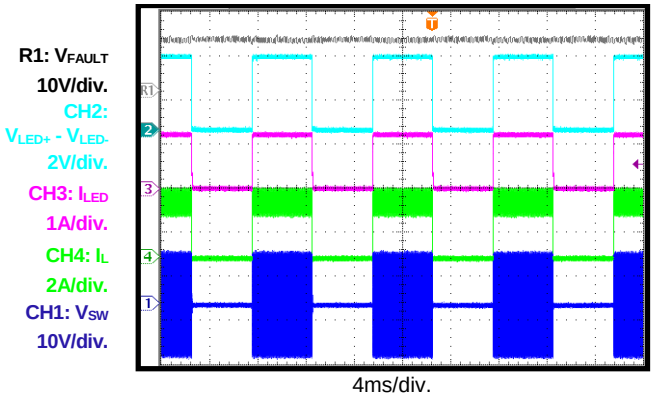
Shutdown through EN/DIM

I_{LED} = 1.2A



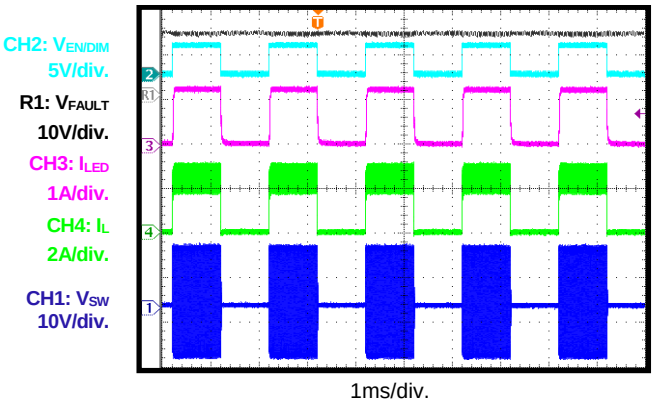
PWM Dimming Steady State

Dimming frequency = 100Hz



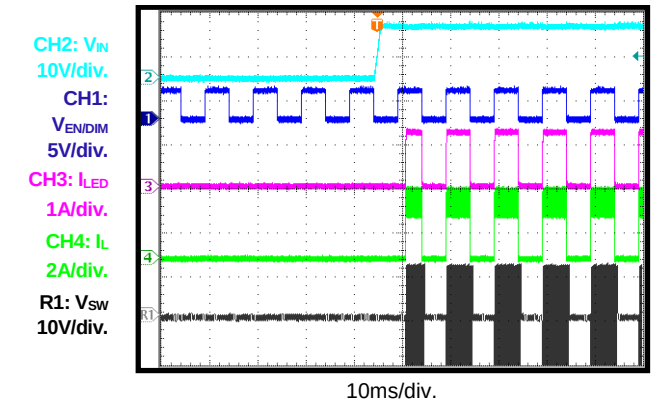
PWM Dimming Steady State

Dimming frequency = 500Hz



PWM Dimming

Start-up through VIN



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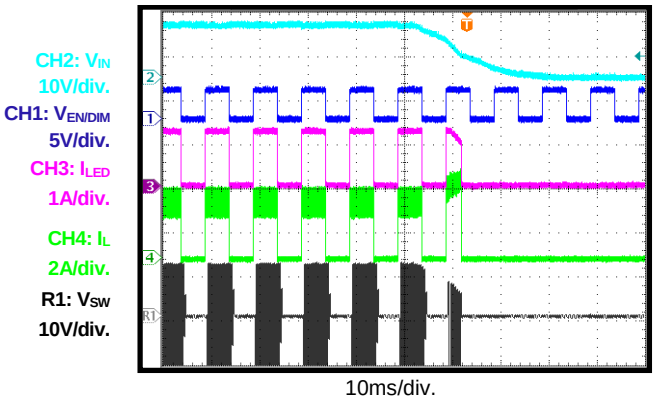
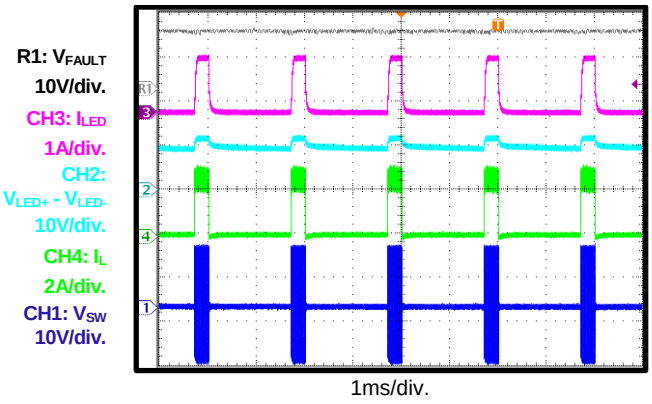
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck-boost mode, 4 LEDs (V_{LED} = 12V), V_{IN} = 13.5V, f_{SW} = 1.15MHz, L = 4.7µH, T_A = 25°C, unless otherwise noted.

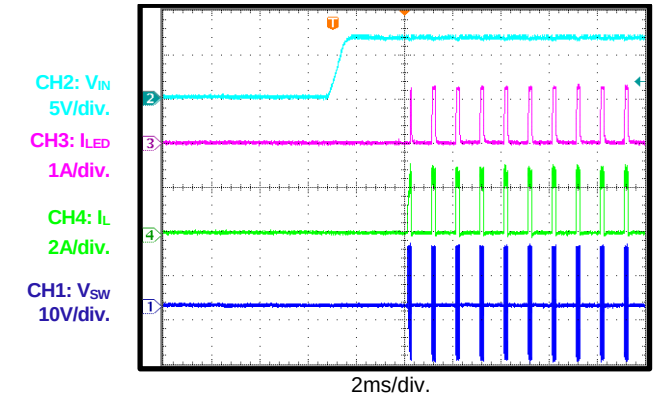
PWM Dimming
Shutdown through VIN



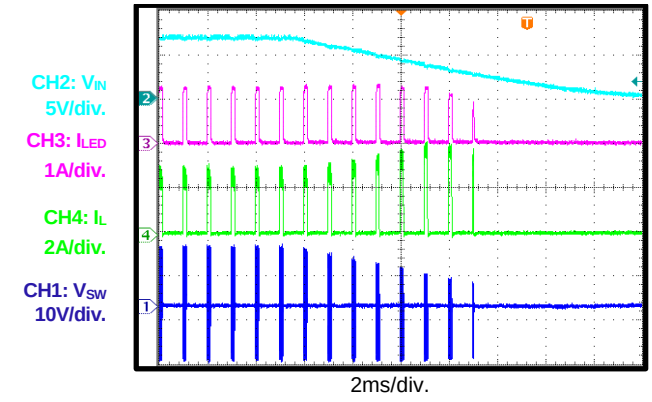
Two-Step Dimming
Steady state



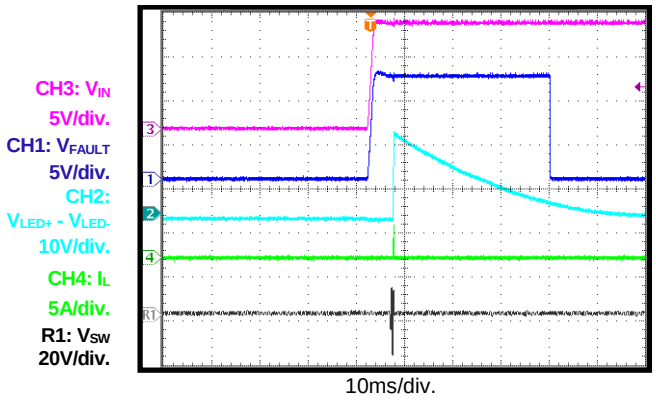
Two-Step Dimming
Start-up through VIN



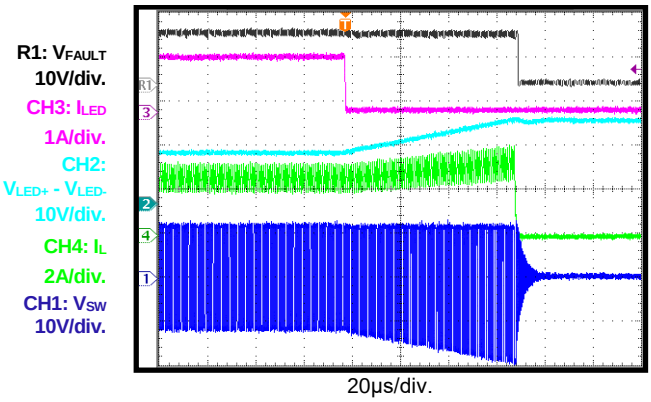
Two-Step Dimming
Shutdown through VIN



No Dimming
LED open, start-up through VIN



No Dimming
LED open entry



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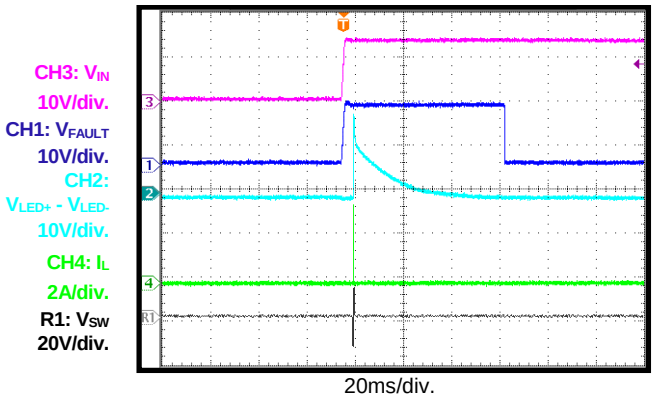
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

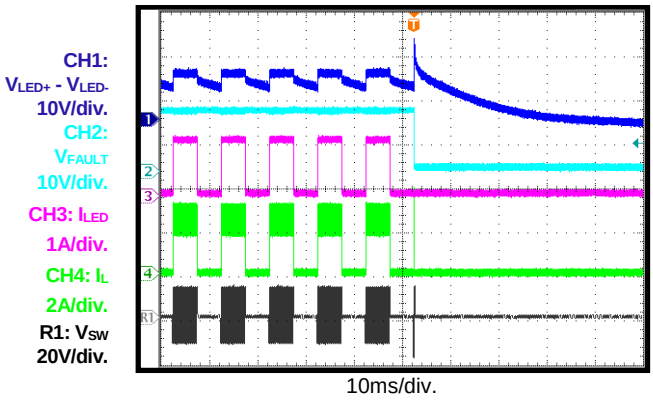
Buck-boost mode, 4 LEDs (V_{LED} = 12V), V_{IN} = 13.5V, f_{SW} = 1.15MHz, L = 4.7µH, T_A = 25°C, unless otherwise noted.

PWM Dimming
LED open during VIN start-up



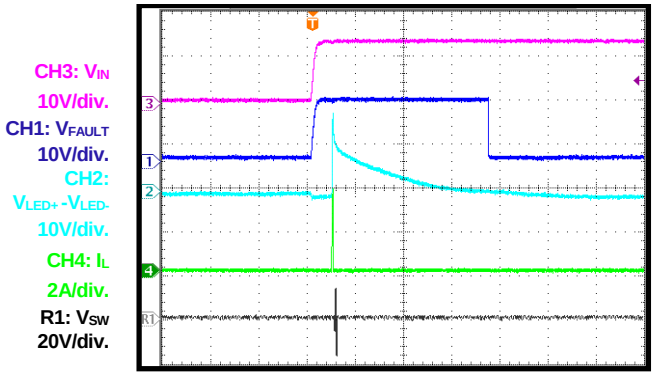
20ms/div.

PWM Dimming
LED open entry



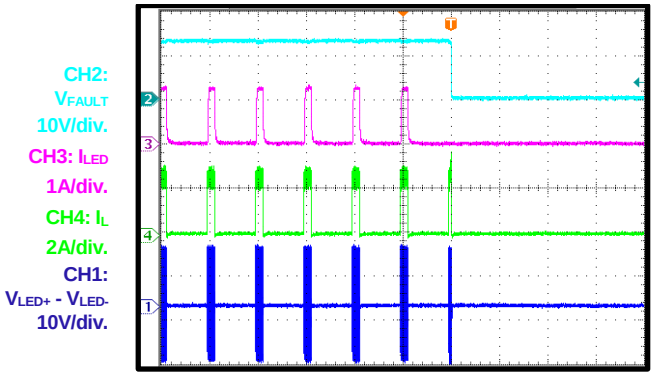
10ms/div.

Two-Step Dimming
LED open during VIN start-up



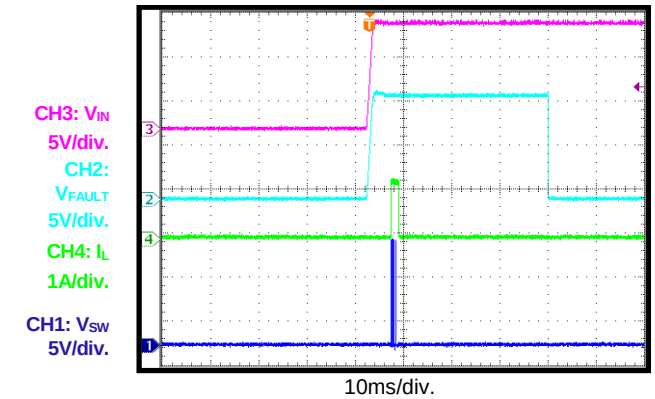
10ms/div.

Two-Step Dimming
LED open entry



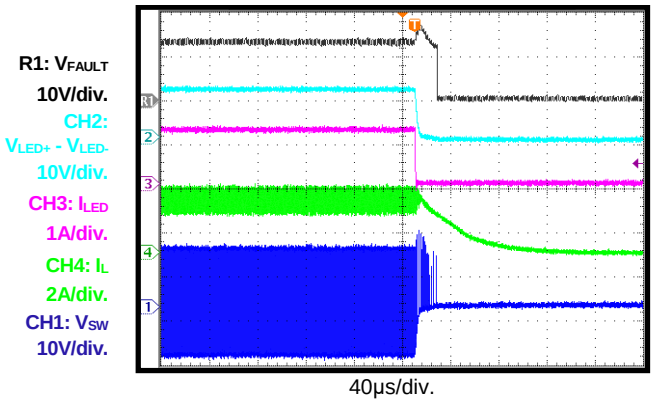
2ms/div.

No Dimming
LED+ short to LED- during VIN start-up



10ms/div.

No Dimming
LED+ short to LED- entry



40µs/div.

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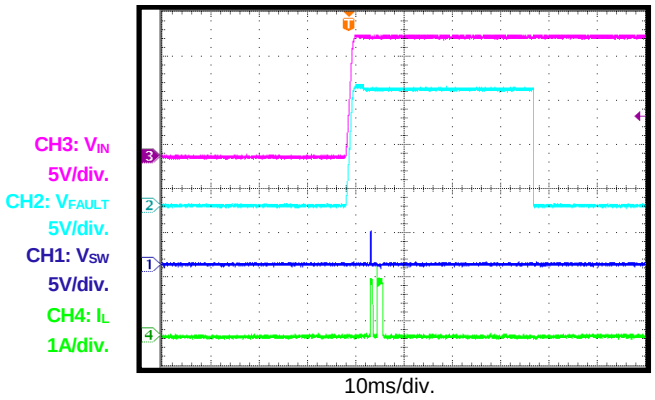
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck-boost mode, 4 LEDs (V_{LED} = 12V), V_{IN} = 13.5V, f_{SW} = 1.15MHz, L = 4.7µH, T_A = 25°C, unless otherwise noted.

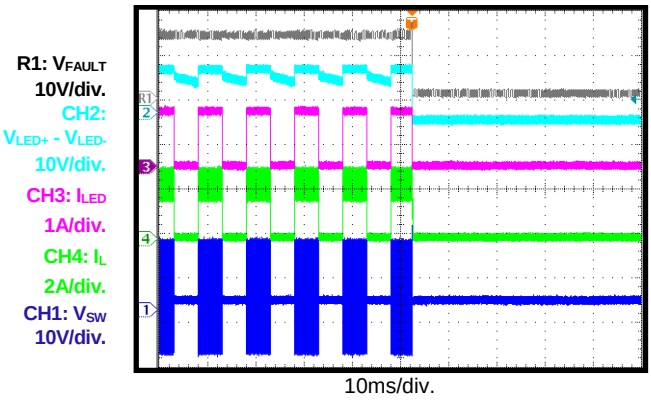
PWM Dimming

LED+ short to LED- during VIN start-up



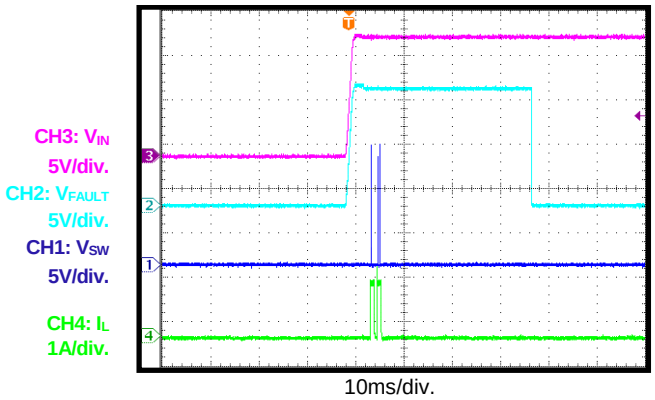
PWM Dimming

LED+ short to LED- entry



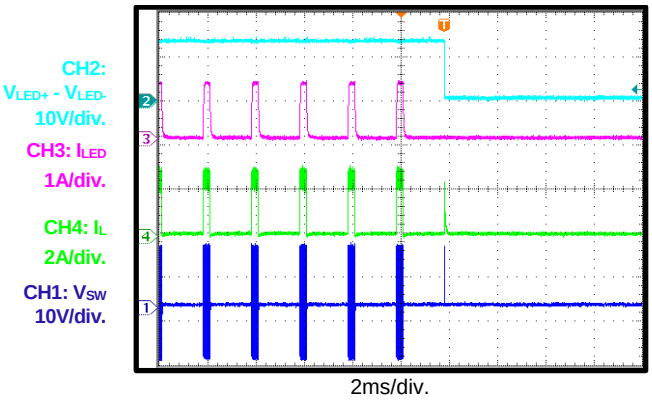
Two-Step Dimming

LED+ short to LED- during VIN start-up

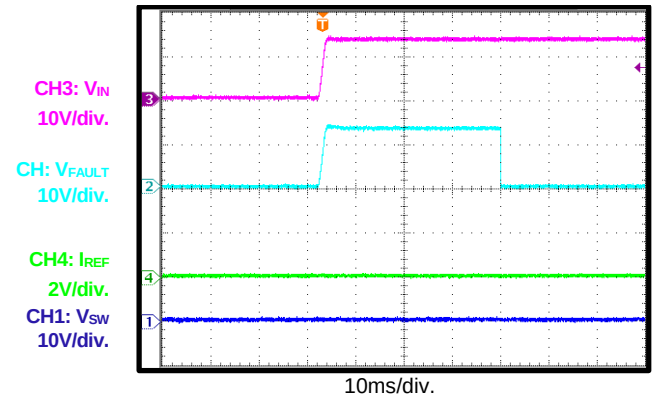


Two-Step Dimming

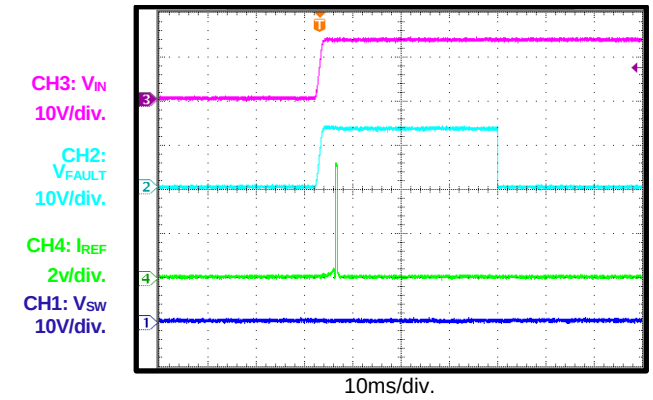
LED+ short to LED- entry



IREF Short before VIN Start-Up



IREF Open before VIN Start-Up



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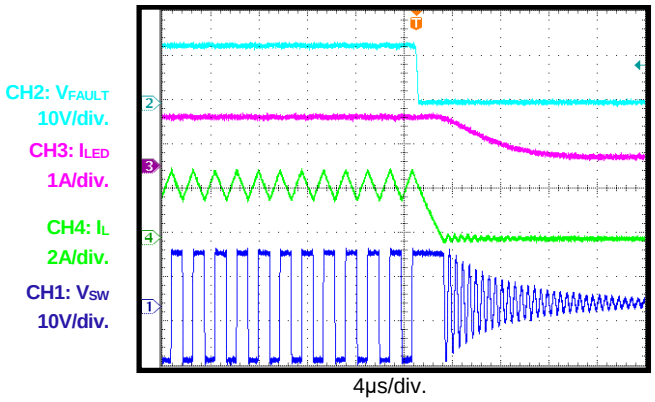
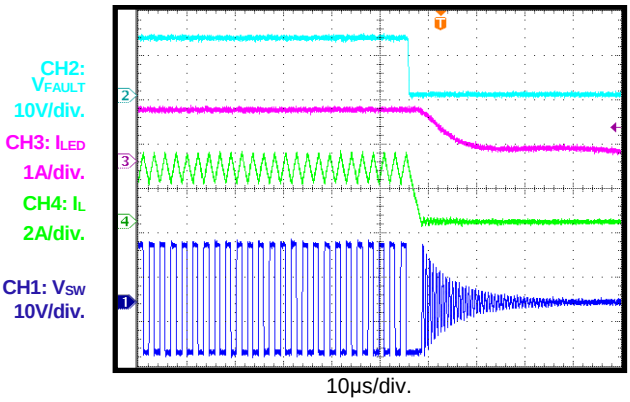
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck-boost mode, 4 LEDs (V_{LED} = 12V), V_{IN} = 13.5V, f_{SW} = 1.15MHz, L = 4.7µH, T_A = 25°C, unless otherwise noted.

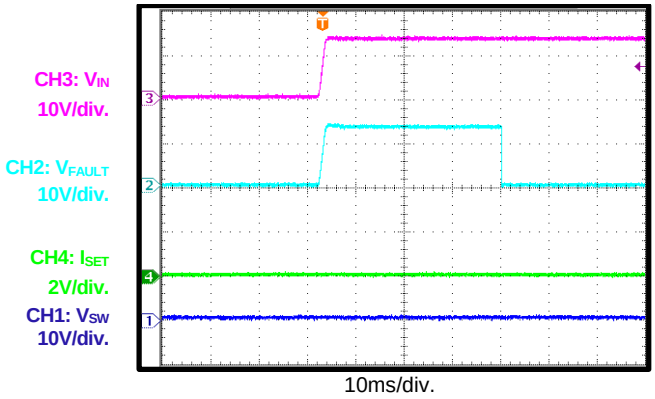
IREF Short after VIN Start-Up



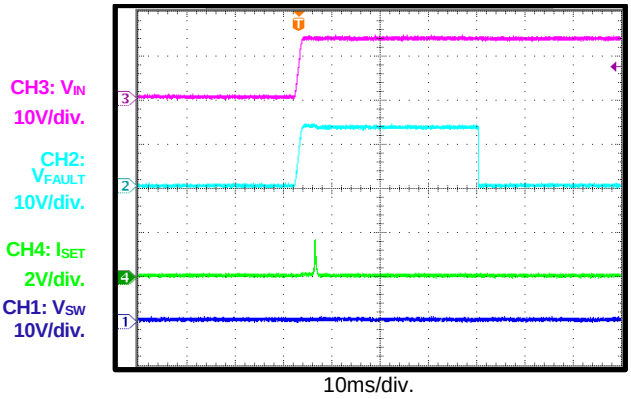
IREF Open after VIN Start-Up



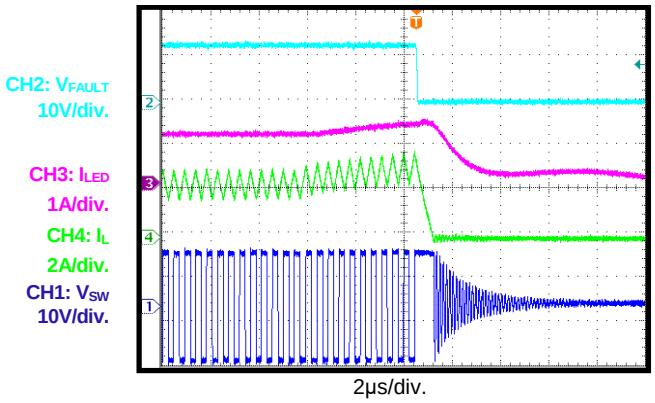
ISET Short before VIN Start-Up



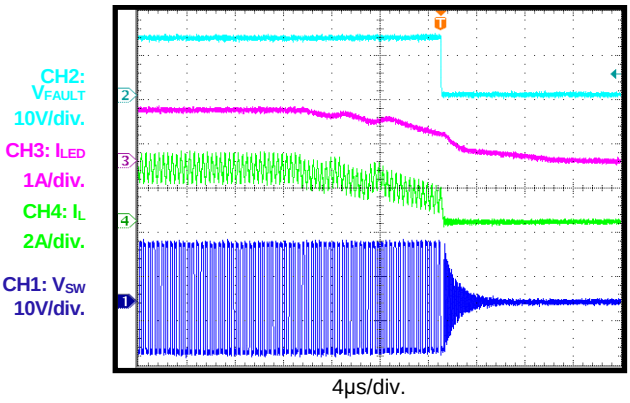
ISET Open before VIN Start-Up



ISET Short after VIN Start-Up



ISET Open after VIN Start-Up



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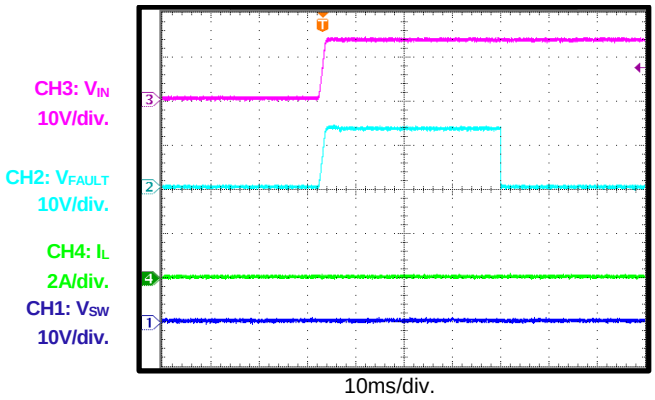
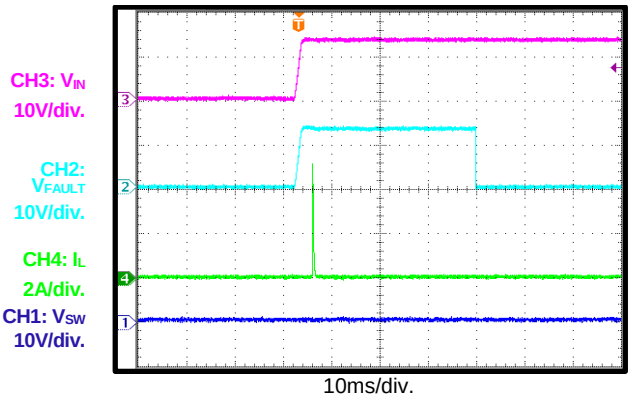
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck-boost mode, 4 LEDs (V_{LED} = 12V), V_{IN} = 13.5V, f_{SW} = 1.15MHz, L = 4.7µH, T_A = 25°C, unless otherwise noted.

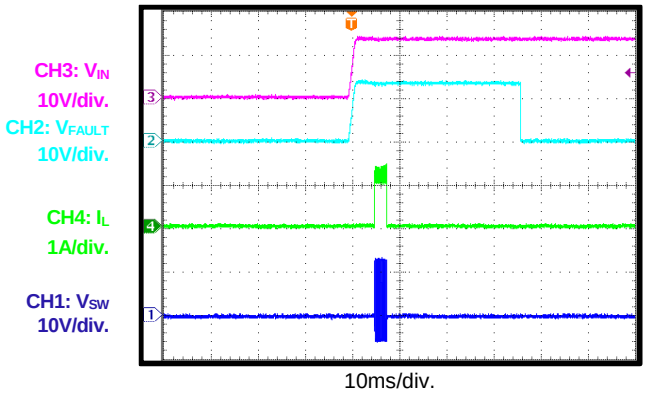
IDUTY Short before VIN Start-Up



IDUTY Open before VIN Start-Up



False Mode Detection during VIN Start-Up



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FUNCTIONAL BLOCK DIAGRAM

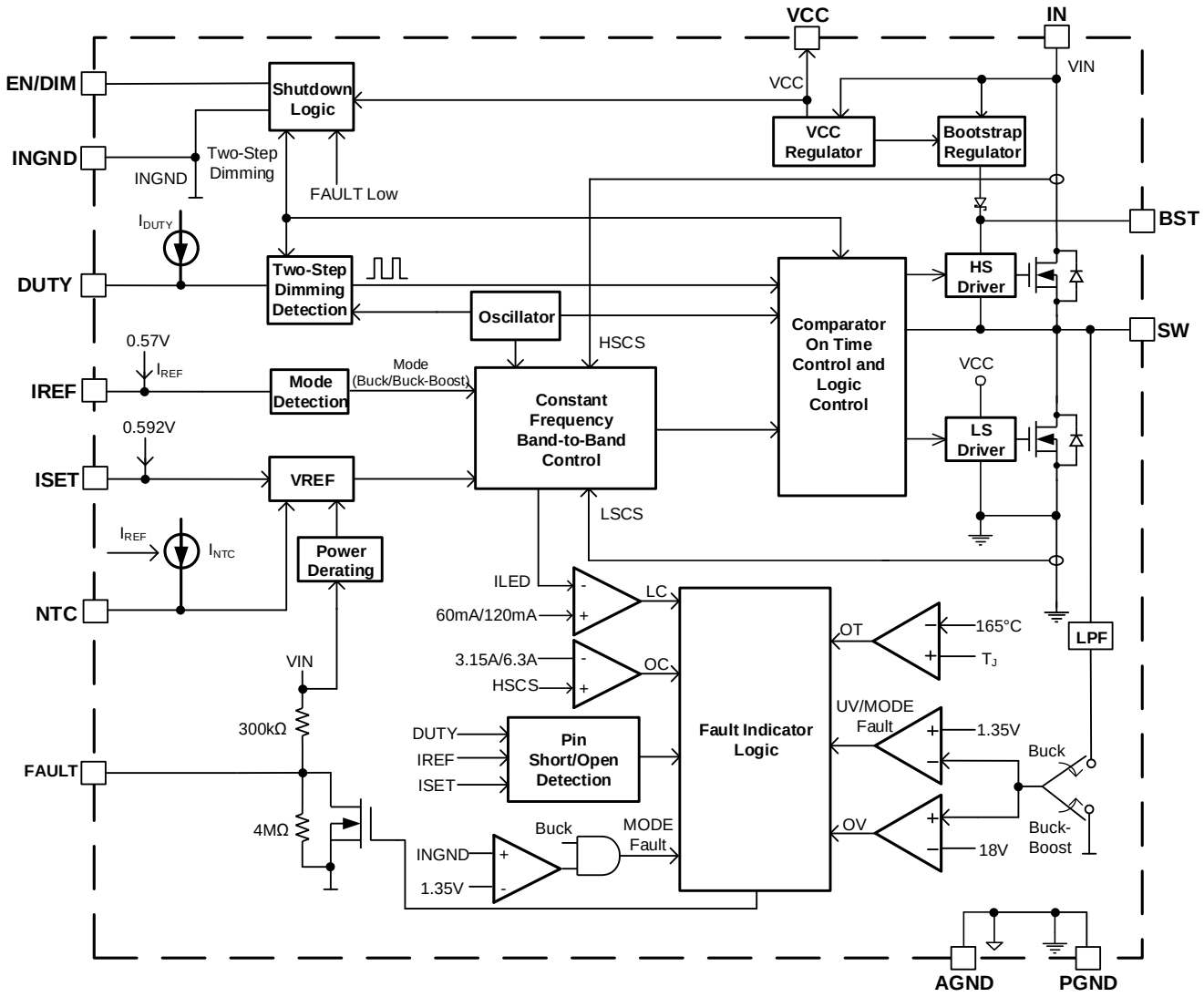

Figure 3: Functional Block Diagram

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OPERATION

The MP7200 is a high-frequency, synchronous, rectified, buck-boost or buck switch-mode LED driver with built-in power MOSFETs. It offers a very compact solution to achieve up to 1.2A of continuous output current in a buck-boost topology (or 3A in a buck topology), with excellent load and line regulation across a 6V to 42V input supply range.

Fixed-Frequency Band-to-Band Control

The MP7200 uses fixed-frequency band-to-band control, plus spread spectrum, to reduce electromagnetic interference (EMI) noise. Compared to fixed-frequency PWM control, band-to-band control offers a simpler control loop and faster transient response. The loop is stable without an output capacitor. Band-to-band control compares the inductor current to the internal thresholds ($I_{BANDPEAK}$ and $I_{BANDVALLEY}$).

When the inductor current (I_L) exceeds $I_{BANDPEAK}$, the high-side MOSFET (HS-FET) turns off. When I_L drops below $I_{BANDVALLEY}$, the HS-FET turns on. ($I_{BANDPEAK}$ + $I_{BANDVALLEY}$) / 2 is controlled by a PID loop to regulate the LED current. $I_{BANDPEAK}$ - $I_{BANDVALLEY}$ is controlled by a PLL loop to regulate the switching frequency to be 2.3MHz in buck mode, and 1.15MHz in buck-boost mode. If the minimum on time (t_{ON_MIN}) or minimum off time (t_{OFF_MIN}) is triggered, the switching frequency is extended. The real switching frequency is (D / t_{ON_MIN}) or (1 - D) / t_{OFF_MIN}, where D is the required duty cycle, and t_{ON_MIN} and t_{OFF_MIN} are both 80ns maximum.

The spread spectrum function uses a 15kHz modulation frequency with a triangular profile to spread the internal oscillator frequency across a ±10% nominal switching frequency window (1.15MHz in buck mode, and 2.3MHz in buck-boost mode).

Middle-Point Inductor Current Sense

The MP7200 senses the LED current by sensing the inductor current middle point (I_{LMID}). I_{LMID} is sensed through the sensing FET. I_{LMID} is sensed through the HS-FET when the duty cycle exceeds D_{TH_H} (55% in buck mode or 60% in buck-boost mode), and is sensed through the LS-FET when the duty cycle is below D_{TH_L} (45% in buck mode or 40% in buck-boost mode).

A duty cycle hysteresis (D_{TH_HYS}) (10% in buck mode and 20% in buck-boost mode) is used to prevent frequent current-sense switches between the HS-FET and LS-FET at the critical duty cycle (see Figure 4).

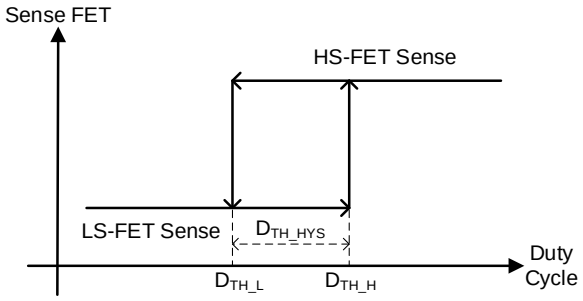

Figure 4: Current-Sense MOSFET vs. Duty Cycle

In buck mode, the LED current is equal to I_{LMID}. In buck-boost mode, it is equal to I_{LMID} x V_{IN} / (V_{IN} + V_{OUT}).

Buck and Buck-Boost Mode Selection

The MP7200 can be configured to buck or buck-boost mode by connecting a different resistor (R_{IREF}) at the IREF pin.

Mode detection starts when VCC reaches its under-voltage lockout (UVLO) threshold of about 4.7V. There is a 240µA current source (I_{REF_DET}) flowing out of the IREF pin to detect the resistor voltage value at the pin during start-up. If the voltage generated by I_{REF_DET} x R_{IREF} is below 2.6V, buck-boost mode is selected. If I_{REF_DET} x R_{IREF} exceeds 2.8V, buck mode is selected. The corresponding R_{IREF} is ≤9.09kΩ for buck-boost mode, and ≥14.7kΩ for buck mode.

Certain resistors are recommended to avoid an IREF short fault in buck-boost mode, and an IREF open fault in buck mode. In buck mode, R_{IREF} should be set between 1.05kΩ and 9.09kΩ. In buck-boost mode, R_{IREF} should be set between 14.7kΩ and 80.6kΩ. Once the resistor has been detected, the mode is latched and I_{REF} becomes 0.57V / R_{IREF}, which is the reference for the NTC pin current. The latched mode signal is reset by VCC UVLO; it cannot be reset by pulling EN/DIM low.

An internal 1MHz filter works with a 250µs deglitch time to protect the part from false mode detection caused by noise coupling at the pin. To ensure that the detected mode is consistent with the real topology connection, V_{INGND} - V_{PGND} is

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monitored. If buck mode is detected when (V_{INGND} - V_{PGND}) > 1.35V, or buck-boost mode is detected when (V_{INGND} - V_{PGND}) < 1.35V (detected as output under-voltage [UV] condition), the part latches off and asserts FAULT low.

Internal Regulator

The 5.1V internal regulator (VCC) powers most of the internal circuitries. VCC rises once V_{IN} reaches its rising UVLO threshold, regardless of whether EN is high or low. VCC is a reference to PGND and AGND, but not INGND. This means that in buck-boost mode, VCC cannot have the same ground level as INGND. In buck-boost mode, the regulator uses either V_{IN} or V_{INGND} as the input: When (V_{INGND} - V_{PGND}) < 5.1V, VCC is powered from VIN. When (V_{INGND} - V_{PGND}) > 5.1V, the VCC regulator input switches to V_{INGND} to reduce power loss. Once this switch occurs, VIN does not power VCC until V_{INGND} - V_{PGND} drops below 4.8V.

A smaller-value VCC capacitor can cause VCC voltage ringing and can makes the switch unstable. A ≥3µF decoupling ceramic capacitor is needed at the VCC pin. When selecting a VCC capacitor, consider the capacitance derating to ensure that the real capacitance ≥3µF. A 10µF, X7R capacitor with a ≥10V DC rated voltage is recommended. VCC has its own UVLO with a 4.7V rising threshold and a 4.05V falling threshold. In addition to powering internal circuitries, VCC also powers external circuitries in the system, with a current capability of 25mA.

CCM Operation and DCM Operation

The MP7200 uses continuous conduction mode (CCM) to ensure that the part works with fixed frequency across the full load range. The advantage of CCM is the controllable frequency and lower output ripple at light loads. When $I_{BANDVALLEY}$ = 0A, the MP7200 enters discontinuous conduction mode (DCM), in which the LS-FET acts as an ideal diode. Use an inductor that can ensure that the part does not enter DCM, even during a power or thermal derating. Otherwise, LED current precision cannot be guaranteed.

Enable Control (EN)

When the two-step dimming function is not active (see the Two-Step Dimming section on page 43), EN/DIM is a control pin that turns the LED driver on and off. Drive $V_{EN/DIM}$ - V_{INGND} above 1.67V to turn the part on. Drive $V_{EN/DIM}$ - V_{INGND} below 1.58V for longer than 25ms to turn the part off and reset FAULT. When two-step dimming is active, the part automatically turns on while VIN and VCC exceed their UVLO thresholds, and EN is configured to be the two-step dimming control pin. Drive EN/DIM high to select a 100% dimming duty. Drive EN/DIM low to select the dimming duty via the DUTY pin. EN cannot reset FAULT in two-step dimming mode.

Connect EN/DIM to VIN through a resistor in both buck and buck-boost mode (it can also be connected to VCC in buck mode) if the EN/DIM pin is not used to control whether the part is on or off. In this scenario, the part always delivers the full configured current (no dimming). If two-step dimming is deactivated, connect an internal 1MΩ resistor from EN/DIM to INGND to float EN/DIM and shut down the chip. Place an integrated Zener diode in parallel with the EN/DIM pin to clamp $V_{EN/DIM}$ - V_{INGND} to about 7V. This internal Zener diode can handle a 1mA current for a load dump voltage up to 100V when a 100kΩ resistor is connected between VIN and EN/DIM.

ISET

The LED average current can be configured by connecting a resistor (R_{ISET}) at the ISET pin. The LED current can be calculated with Equation (1):

$$I_{LED}\ (A) = 16 / R_{ISET}\ (k\Omega) \quad (1)$$

The ISET pin nominal voltage (V_{ISET}) is 0.592V. V_{ISET} can be set below 0.592V to decrease the LED current in the event of power derating or thermal derating.

During the mode detection period during start-up while the device is in buck mode, the ISET current is monitored to detect if the LED current is set above or below 600mA. If I_{ISET} > 22.2µA during this period, then the LED current setting is detected as >600mA and the MOSFETs turn fully on.

If the LED current setting is detected to be <600mA, half of the HS-FETs and LS-FETs are cut off to improve current-sense accuracy. After

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this cutoff, the current limit drops from 6.3A to 3.15A. The signal to indicate whether the LED current is above or below 600mA is latched once detection finishes, and only can be reset by VCC UVLO. After LED current detection, the MOSFET's $R_{DS(ON)}$ does not change, even if the current setting exceeds or falls below 600mA.

During normal operation, the ISET pin is continuously monitored to detect the occurrence of an open or short to GND condition. If the ISET current is above its specific value, the device detects a pin short to ground. In buck-boost mode, the MOSFET is always on, regardless of the current.

If the LED current (I_{LED}) is set below 600mA, the ISET current threshold for short detection is 120μA (with the 4.9kΩ resistor, or 3.24A I_{LED}). If I_{LED} is set above 600mA, the threshold is 220μA (with a 2.7kΩ resistor, or 5.9A I_{LED}). When the ISET current is below 1.4μA (with a 428kΩ resistor, or 37.3mA I_{LED}), a pin open fault is detected.

The part latches off if the ISET pin detects a short or open fault, regardless of whether FAULT is asserted. If there is an ISET pin short or open fault after start-up, FAULT is pulled low immediately. There is a 25ms to 40ms delay for FAULT assertion if a short or open fault is detected during start-up.

IREF

The IREF pin configures the device to buck or buck-boost mode. Afterward, it sets the current in the external NTC. After mode detection finishes, the IREF pin voltage (V_{IREF}) is set to 0.57V with a 10.5% tolerance. Connect a resistor (R_{IREF}) between IREF and AGND to get a current (I_{REF}) equal to 0.57V / R_{IREF}. This current is used as a reference current for the NTC's current source. The NTC current is 50 times that of I_{REF} in buck mode, and 5 times that of I_{REF} in buck-boost mode. The IREF current is continuously monitored to detect if the IREF pin open and short to GND conditions occur.

If the IREF current exceeds 90μA in buck mode (with a 6.3kΩ resistor) or 900μA in buck-boost mode (with a 0.63kΩ resistor), a short-to-GND fault is detected. If the IREF current drops below 3μA in buck mode (with a 190kΩ resistor) or below 40μA in buck-boost mode (with a 14.3kΩ resistor), an open fault is detected.

The part latches off if a short or open fault is detected on IREF, regardless of whether FAULT asserts. If there is an IREF pin short or open fault after start-up, FAULT is pulled low immediately. There is a 25ms to 40ms delay for FAULT assertion if a short or open fault is detected during start-up.

PWM Dimming

When two-step dimming is inactive (R_{DUTY} = 4.87kΩ), an external 100Hz to 2kHz PWM waveform can be applied to the EN/DIM pin. In external PWM dimming mode, the part stops switching when EN/DIM drops below 1.58V and I_{LED} is 0A. The part resumes normal operation with the nominal LED current, and when EN/DIM exceeds 1.67V. The average LED current is proportional to the PWM duty, and its accuracy can be up to ±15% when V_{IN} = 13.5V ± 0.5V and T_J is between 25°C and 100°C.

Note that the EN/DIM high-voltage period should always be longer than 100μs. Otherwise, the part can stop switching, and an LED open fault may not be detected. To prevent the part from shutting down, the EN/DIM low-voltage period should not be longer than 10ms (EN turn-off delay).

Two-Step Dimming

When VCC reaches its UVLO rising threshold (4.7V), two-step dimming detection is activated on the DUTY pin. A 45μA current source (I_{DUTY1}) with a ±11% tolerance flows through the resistor between the DUTY pin and GND.

If the generated voltage (V_{DUTY}) exceeds 3.347V, an open fault is detected, the part latches off, and FAULT asserts. If 0.302V < V_{DUTY} < 3.347V, the two-step dimming function is activated and the two-step dimming duty cycle is selected using Table 1. If V_{DUTY} is below 0.302V, the DUTY current source rises to 600μA (I_{DUTY2}) with a ±8.75% tolerance to detect V_{DUTY} again.

If V_{DUTY} > 2.235V at this point, two-step dimming is disabled. Then the part can be turned on/off through EN/DIM, or can work in normal PWM dimming by applying a dimming signal at EN/DIM. If V_{DUTY} < 0.302V, a short fault is detected, the part latches off, and FAULT

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asserts. If 0.302V < V_{DUTY} < 2.235V, two-step dimming is reactivated and the two-step dimming duty cycle is determined by V_{DUTY}. After this detection, the duty is not affected by changing V_{DUTY}, even if the DUTY pin is opened or shorted to GND.

Once two-step dimming is activated, PWM dimming is deactivated. The EN/DIM pin is used as the input pin to select no dimming or low dimming. When the EN/DIM pin is high, a 100% dimming duty cycle is selected. When EN/DIM is low, the dimming duty cycle is determined by I_{DUTY} and V_{DUTY}. The part can switch between dimming values in less than 20ms.

Configurable dimming is implemented as PWM dimming, but not analog dimming. When two-step dimming is activated at I_{DUTY1}, the dimming duty can be set between 15% and 10% with a 1% step. The corresponding typical V_{DUTY} is between 3.347V and 0.302V, with a 33% decrement for each step. When two-step dimming is activated at I_{DUTY2}, the dimming duty can be set between 9% and 5% with a 1% step. The corresponding V_{DUTY} is between 2.235V and 0.302V, with a 33% decrement for each step. Table 1 shows the relationship between the two-step dimming duty and V_{DUTY} window when considering different V_{DUTY} threshold tolerances.

Table 1: Two-Step Dimming Duty vs. V_{DUTY} Window

Two-Step Dimming Duty		Corresponding V_{DUTY} Window					
		V_{DUTY_H}			V_{DUTY_L}		
I_{DUTY1}	I_{DUTY2}	Min	Typ	Max	Min	Typ	Max
Latch	No two-step dim.	4.018	4.100	4.182	3.280	3.347	3.414
15%		3.280	3.347	3.414	2.190	2.235	2.279
14%	9%	2.190	2.235	2.279	1.460	1.489	1.519
13%	8%	1.460	1.489	1.519	0.969	0.989	1.009
12%	7%	0.969	0.989	1.009	0.634	0.653	0.673
11%	6%	0.634	0.653	0.673	0.407	0.428	0.449
10%	5%	0.407	0.428	0.449	0.28	0.302	0.33
To I_{DUTY2}	Latch	0.28	0.302	0.33	-		

To prevent errors while selecting the two-step dimming duty, ensure that the V_{DUTY} window is between the minimum V_{DUTY_H} and maximum V_{DUTY_L} values when selecting R_{DUTY}. An E96 series resistor is recommend to select precise dimming values. Table 2 shows the proposed R_{DUTY} in E96 series for different two-step dimming duties, while considering the I_{DUTY} tolerance and a ±3% resistor tolerance

If V_{CC} drops below 4.05V before two-step dimming detection finishes, two-step dimming detection stops and does not restart until V_{CC} returns to 4.7V. The two-step dimming signal, together with the two-step dimming duty, is latched once detection finishes. It only can be reset by VCC UVLO, and not an EN shutdown.

The two-step dimming frequency is typically 500Hz, within ±50Hz.

Table 2: Two-Step Dimming Duty vs. R_{DUTY}

Two-Step Dimming Duty	R_{DUTY} (Ω)
15%	61900
14%	41200
13%	27400
12%	18200
11%	12100
10%	7870
PWM dimming (two-step dimming inactivated)	4870
9%	3090
8%	2050
7%	1370
6%	887
5%	576

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Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. Both (V_{IN} - V_{INGND}) and V_{CC} have UVLO thresholds. The V_{IN} - V_{INGND} UVLO rising threshold is 6V, with a 1.1V hysteresis. The V_{CC} UVLO rising threshold is 4.7V, with a 0.65V hysteresis. Neither of these UVLOs triggers a fault.

Fault Detection and Indication

The MP7200 has fault indication. The FAULT pin is the open drain of a MOSFET. FAULT is internally pulled up to VIN through a 300kΩ resistor, and pulled down with a 4MΩ resistor connected to INGND. The FAULT pin is pulled high during normal operation. It pulls low to indicate a fault status if any of the following events occur:

- An LED short or open fault
- Thermal shutdown
- False mode detection
- Over-current protection (OCP)

An ISET or IREF pin short/open fault during (or after) start-up can assert FAULT. An IDUTY pin short/open fault can only assert FAULT if it is detected before start-up. The MP7200 senses the output by monitoring the average SW voltage in buck mode, or the INGND voltage in buck-boost mode. If LED+ shorts to LED- or PGND, V_{OUT} drops below its under-voltage (UV) threshold, a short-circuit is detected, and FAULT asserts. If an LED open or output over-voltage (OV) fault is detected in buck-boost mode, or the high-side MOSFET current is detected in buck mode, then FAULT asserts. The low-current threshold is 60mA when the LED current is set below 600mA, or 120mA when the LED current is set above 600mA.

To prevent the part from latching due to cold crank conditions while in buck mode, low-current detection is disabled when V_{IN} drops below 7.5V. If LED+ (INGND) shorts to the battery, V_{IN} - V_{INGND} falls below its UV threshold in buck-boost mode, and FAULT cannot assert. If LED- (PGND) shorts to INGND, V_{INGND} drops below its UV threshold and FAULT asserts. If an LED open fault occurs, V_{INGND} exceeds its OV threshold and FAULT asserts.

At high temperatures, the part operates with a reduced current level. The device only stops if the internal temperature reaches the 170°C over-temperature (OTP) threshold and FAULT asserts. If any fault occurs, the part stops switching, the FAULT output asserts in 20µs, and then the part latches. While latched, V_{CC} is still present, and the part's consumption current is <2mA. FAULT can be reset by V_{CC} UVLO. EN shutdown (EN going low longer than 25ms) can also reset FAULT if two-step dimming is not selected.

At start-up, the FAULT pin is not activated, and remains inactive for at least 25ms. FAULT is active within 40ms. In PWM dimming mode, the FAULT counter works only when the dimming signal is high, which makes the inactive time 30ms/PWM dimming duty. This avoids any false functions from the system when multiple parts have connected FAULT pins and share the same EN signal. Individual parts are self-protected and latch off immediately if a fault condition is detected, regardless of whether FAULT asserts.

The FAULT pin can withstand a 30mA current and protects itself if the pin shorts to a high voltage (e.g. V_{BATT}). If FAULT is low (<1.6V), the FAULT sink current increases to enhance the pull-down capability. Figure 5 shows the detailed FAULT sink current when the FAULT pin is pulled low at different voltages.

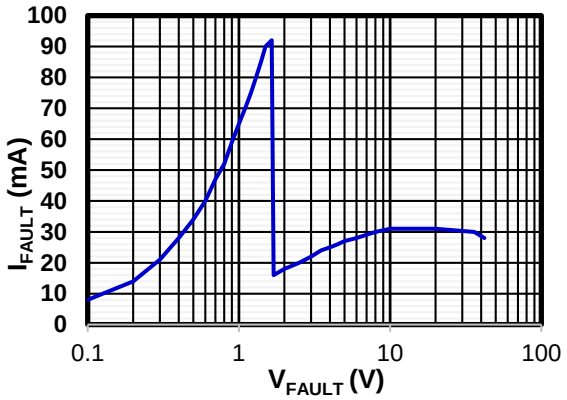

Figure 5: FAULT Sink Current vs. FAULT Voltage

In PWM dimming and two-step dimming, fault conditions may not be detected when the dimming on time is below 100µs. Ensure that the dimming on time exceeds 100µs for normal fault detection operation. Table 3 shows the fault detection options.

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Table 3: Fault Detection (9)

Fault Conditions	Detection	
	Buck Mode	Buck-Boost Mode
LED+ short to LED-	V_{OUT} UV (V_{OUT} < 1.1V)	INGND UV (V_{INGND} - V_{PGND} < 1.35V) (10)
LED+ short to PGND	V_{OUT} UV (V_{OUT} < 1.1V)	INGND UV (V_{INGND} - V_{PGND} < 1.35V)
LED+ short to INGND	V_{OUT} UV (V_{OUT} < 1.1V)	Normal condition
LED+ short to battery	Low LED current (I_{HS} < 60mA when $I_{LED_SETTING}$ < 600mA) (I_{HS} < 120mA when $I_{LED_SETTING}$ > 600mA)	Cannot assert FAULT due to V_{IN} - V_{INGND} UVLO
LED- short to INGND	Normal conditions	INGND UV (INGND - PGND < 1.35V)
LED- short to battery	Cannot assert FAULT due to V_{IN} - V_{INGND} UVLO	Cannot assert FAULT due to V_{IN} - V_{INGND} UVLO
LED open	Low LED current (I_{HS} < 60mA when $I_{LED_SETTING}$ < 600mA) (I_{HS} < 120mA when $I_{LED_SETTING}$ > 600mA)	INGND OV (V_{INGND} - V_{PGND} > 18V)
MODE detection wrong	V_{INGND} - V_{PGND} > 1.35V	INGND UV (V_{INGND} - V_{PGND} < 1.35V)
OTP	T_J > 170°C, or 0.18V< V_{NTC} < 0.38V for >256us	
ISET short (11)	(I_{ISET} > 120µA when $I_{LED_SETTING}$ < 600mA), or (I_{ISET} > 220µA when $I_{LED_SETTING}$ > 600mA)	I_{ISET} > 110µA
ISET open (11)	I_{ISET} < 1.4µA	
IREF short (11)	I_{IREF} > 90µA	I_{IREF} > 900µA
IREF open (11)	I_{IREF} < 3µA	I_{IREF} < 40µA
DUTY open (12)	V_{DUTY1} > 3.355V	
DUTY short (12)	V_{DUTY2} < 0.302V	
OCP	Current limit triggered three continuous times	

Notes:

9) If a fault mentioned in this table is detected, the part latches off and FAULT is asserted.
10) The FAULT pin may not work correctly if V_{INGND} - V_{PGND} is pulled below -0.3V, or if an LED+ short to LED- occurs with a long cable.
11) If the ISET or IREF pins experience a short or open fault before or after start-up, the part latches off and FAULT asserts.
12) If an IDUTY pin short or open fault occurs before start-up, the part latches off and FAULT asserts. After start-up, an IDUTY short or open fault cannot be detected.

Over-Current Protection (OCP)

The MP7200 has cycle-by-cycle peak current limit protection. I_L is monitored while the HS-FET is on. If I_L exceeds the current limit value (6.3A when I_{LED} is set above 600mA, or 3.15A when I_{LED} is set below 600mA), the HS-FET turns off immediately. Then the LS-FET turns on to discharge the energy, and I_L decreases. The HS-FET remains off until I_L drops to 0A, at which point another HS-FET on cycle starts. If the over-current (OC) condition still remains after three consecutive retries, the part latches off, reports a failure, and the FAULT pin is asserted.

Load Dump Protection

The MP7200's internal MOSFETs have a 50V absolute maximum rating and a maximum 42V operating voltage. In buck topologies, the maximum voltage can handle load dump conditions up to 42V. In buck-boost topologies, the voltage difference between VIN and PGND is the sum of the car battery's voltage plus the LED voltage. Under load dump conditions, the MP7200 can exceed its maximum value.

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To protect the part from load dump conditions in buck-boost mode, the MP7200 stops switching if V_{IN} - V_{PGND} exceeds 40V. A 100mA sink current at INGND is activated to discharge the output voltage, so the MOSFET only detects the VIN voltage stress. Once V_{IN} - V_{PGND} drops back to 39V, the part automatically restarts. Load dump protection does not always trigger a fault, and it is not active in buck mode. Load dump protection can reset the FAULT status caused by other fault conditions, but it cannot reset the MP7200 if the part is latched.

Power Derating

If V_{IN} falls below a specific voltage (typically 7V) in buck-boost mode, power derating starts. I_{LED} drops linearly with V_{IN} due to analog dimming. Derating continues until V_{IN} reaches the UVLO threshold, then I_{LED} drops by 29%. Power derating is enabled during start-up in buck-boost mode, but it is disabled during start-up in buck mode.

NTC Thermal Derating

Connect an NTC resistor network to the NTC pin to reduce the output current via analog dimming. This is especially useful when the sensed temperature exceeds the configured value. I_{LED} drops as the temperature rises. The activation of NTC and the dimming ratio are determined by the three-step NTC voltage (V_{NTC}) detection (see Figure 6).

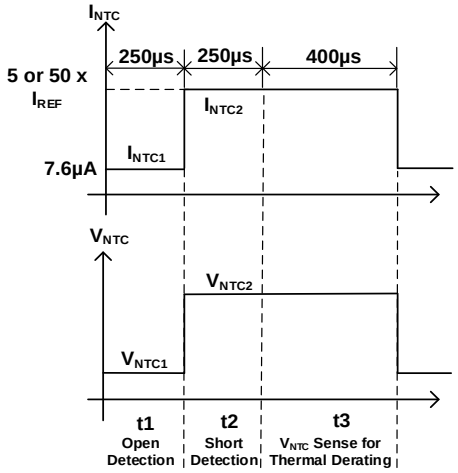

Figure 6: I_{NTC} Timing

At t1 and t2, the voltage on the NTC pin is detected to determine if the NTC is enabled. t1 and t2 both last for 250µs. At t3, V_{NTC} is sensed. The dimming ratio is generated at the end of t3. t3 lasts for 400µs.

During t1, the detection current (I_{NTC1}) is 7.6µA; during t2, it is 50 times I_{REF} (in buck mode) or 5 (in buck-boost mode) times I_{REF} (I_{NTC2}). To activate NTC thermal derating, V_{NTC} should be below 2V (with a <263kΩ resistor) during t1 (V_{NTC1}), and above 0.38V (with a resistor that is based on the values of V_{NTC2} and I_{NTC2}) during t2. If V_{NTC1} exceeds 2V during t1, an open pin fault is detected. If V_{NTC2} falls below 0.18V during t2, a short fault is detected. An open or short fault deactivates NTC thermal derating.

V_{NTC1} must be below 2V (even if the NTC value is large at low temperatures) to avoid triggering an open fault. V_{NTC2} must exceed 0.18V (even if the NTC resistor is small) at high temperatures to avoid triggering a short fault.

If NTC thermal derating is activated at the end of t2, V_{NTC2} is sensed during t3 to indicate the real temperature and determine the dimming ratio. The dimming ratio decreases as V_{NTC2} decreases, starting when V_{NTC2} drops below 1.25V. The dimming ratio decreases by a step of 2% if V_{NTC2} drops by 30mV. If V_{NTC2} falls to 0.5V, the dimming ratio decreases to 50%. This means the LED average current also falls to 50% of the set LED current.

If V_{NTC2} continues to drop to between 0.5V and 0.38V, the thermal derating remains at 50%. If V_{NTC2} is between 0.38V and 0.18V, the part latches off due to a thermal shutdown event and FAULT is asserted. The device can restart only after it is turned off then on again, or if EN is reset. If the voltage falls below 0.18V, the NTC pin is considered shorted to PGND, and the NTC circuitry is deactivated.

Thermal Shutdown (TSD)

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. If the die temperature exceeds 170°C, the entire chip shuts down and FAULT is asserted. The device restarts only after being turned off and on again, or after EN is reset.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. The bootstrap capacitor voltage is charged to about 5V from VCC through a pass transistor while the LS-FET is on.

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This floating driver has its own UVLO protection, with a rising threshold of 2.5V and hysteresis of 700mV. If the BST-to-SW voltage drops to 2.2V, the LS-FET turns on to refresh the BST voltage. It is recommended to use a 47nF to 220nF ceramic capacitor for the bootstrap capacitor. Consider the capacitor's DC voltage and temperature derating when selecting the capacitor to ensure that the real capacitance is between 47nF and 200nF. A maximum 22Ω resistor can be placed in series with the bootstrap capacitor to reduce SW voltage spikes.

The part integrates BST capacitor open-detection functionality. When VIN and VCC reach their UVLO rising thresholds, the BST capacitor is charged after the 1ms thermal derating finishes. If the voltage on the BST capacitor reaches the UVLO rising threshold within 45µs, the part detects a BST open fault and latches off. If VIN restarts frequently, the BST capacitor may not be able to discharge sufficiently, and an open fault may be mistriggered.

To avoid a mistrigger, place a small BST capacitor and a bleeding resistor in parallel with the BST capacitor. This ensures that the BST capacitor voltage is sufficiently low after a restart. It is recommended to use a 22nF capacitor and 15kΩ resistor.

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APPLICATION INFORMATION

Selecting Buck or Buck-Boost Mode

The device can be configured for buck or buck-boost mode by connecting a different resistor at the IREF pin (R_{IREF}). Select a 1.05kΩ ≤ R_{IREF} ≤ 9.09kΩ resistor for buck-boost mode, and a 14.7kΩ ≤ R_{IREF} ≤ 80.6kΩ resistor for buck mode.

Dimming Mode Selection

The dimming mode can be configured by connecting a different resistor at the IDUTY pin (R_{IDUTY}). Select a 4.87kΩ resistor to disable the internal PWM dimming function and enable external PWM dimming. Table 2 on page 44 lists resistors for two-step dimming, if that function is required.

Setting the LED Current

The external resistor connected to the ISET pin sets the LED current. The value of the external resistor can be calculated with Equation (2):

$$R_3 = \frac{16}{I_{LED}(A)}(k\Omega) \quad (2)$$

If I_{LED} is below 0.7A in buck-boost mode, certain LED setting resistors are recommended (see Table 4).

Table 4: Resistor Selection when I_{LED} ≤ 700mA in Buck-Boost Mode

I_{LED} (A)	R_{ISET} (kΩ)
0.7	22.6
0.65	24.2
0.6	26.1
0.55	23.2
0.5	30.9
0.45	34.0
0.4	37.4

Figure 7 shows the relationship between I_{LED} and R_{ISET} in buck-boost mode.

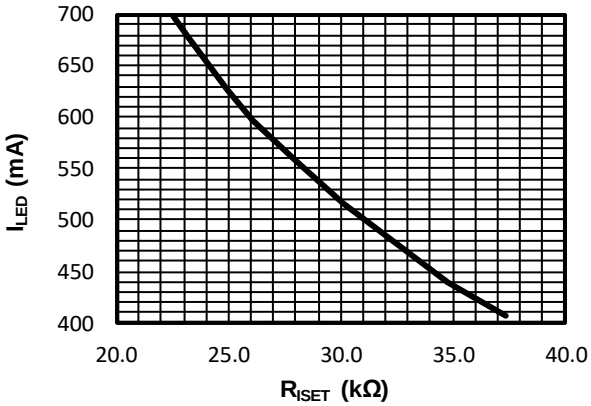

Figure 7: I_{LED} vs. R_{ISET} when I_{LED} ≤ 700mA in Buck-Boost Mode

Selecting the Inductor

For most applications, it is recommended to use an inductor between 2.2µH and 33µH with a DC current rating that exceeds the maximum inductor current. Include the inductor's DC resistance when estimating the output current and the inductor's power consumption.

For buck mode, the required inductance value can be estimated with Equation (3):

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}} \quad (3)$$

Choose an inductor ripple current that exceeds 20% of the LED current. The peak inductor current can be calculated with Equation (4):

$$I_{L_PEAK} = I_{L_AVG} + \frac{\Delta I_L}{2} \quad (4)$$

Where I_{L_AVG} is the average current through the inductor. In buck mode, I_{L_AVG} is equal to the output load current (LED current).

Under light-load conditions, use a larger-value inductor to improve efficiency and current precision. Table 5 lists the recommended inductor values for common LED currents in buck mode.

Table 5: Buck Mode Inductor Values for Common LED Currents

I_{LED} (A)	Recommend Inductor Value (µH)
[2A, 3A]	3.3
[0.8A, 2A)	4.7
[0.4A, 0.8A)	6.8
[0.3A,0.4A]	10

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For buck-boost applications, estimate the required inductance value with Equation (5):

$$L = \frac{V_{OUT} \times V_{IN}}{(V_{OUT} + V_{IN}) \times \Delta I_L \times f_{SW}} \quad (5)$$

Where ΔI_L is the inductor's peak-to-peak current ripple.

ΔI_L should exceed 25% of the inductor average current when I_{LED} > 0.7A. Select ΔI_L to exceed 20% of the inductor average current when I_{LED} < 0.7A. I_{L_AVG} can be calculated with Equation (6):

$$I_{L_AVG} = I_{LED} \times (1 + \frac{V_{OUT}}{V_{IN}}) \quad (6)$$

The peak inductor current can be calculated with Equation (7):

$$I_{L_PEAK} = I_{L_AVG} + \frac{\Delta I_L}{2} \quad (7)$$

Under light-load conditions, use a larger-value inductor to improve efficiency and current precision. Table 6 lists the recommended inductor values for common LED currents in buck-boost mode.

Table 6: Buck-Boost Mode Inductor Values for Common LED Currents

I_{LED} (A)	Recommend Inductor Value (μH)
(1A, 1.2A]	3.3
(0.8A, 1A]	4.7
(0.6A, 0.8A]	6.8
[0.4A,0.6A]	10

Selecting the Input Capacitor

The device has a discontinuous input current in both buck and buck-boost mode, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

For most applications, it is recommended to use a 4.7μF to 22μF capacitor. The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, it is strongly recommended to use an additional, lower-value capacitor (e.g. 0.1μF) with a small package size (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to VIN and GND (INGND = PGND in buck mode, for both INGND and PGND in buck-boost mode) as possible.

Since the input capacitor absorbs the input switching current in buck mode, the device requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (8):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (8)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (9):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (9)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current. The input voltage ripple caused by the capacitance can be estimated with Equation (10):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

If $I_{BANDVALLEY} \geq I_{LED}$ in buck-boost mode, the capacitance can be calculated with Equation (11):

$$\Delta V_{IN} = \frac{I_{LED} \times V_{OUT}}{(V_{IN} + V_{OUT}) \times f_{SW} \times C_{IN}} \quad (11)$$

In buck-boost mode, consider the capacitor between VIN and PGND for VCC regulator stability and improved EMC performance. If (V_{INGND} - V_{PGND}) > 5.1V, then the VCC regulator input switches to V_{INGND} to reduce power loss. Place a 0.44μF to 1.2μF ceramic capacitor between VIN and PGND to stabilize VCC when the VCC charging source changes from VIN to INGND. Two symmetric (0.1μF + 0.47μF) /50V X7R ceramic capacitors can be placed between VIN and PGND.

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Ceramic, tantalum, or low-ESR electrolytic capacitors are recommended. For the best results, use low-ESR capacitors to keep the output voltage ripple low.

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In buck mode, the output voltage ripple can be estimated with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (12)$$

Where L is the inductor value, and R_{ESR} is the output capacitor's equivalent series resistance (ESR) value.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (13):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (13)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (14):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (14)$$

If $I_{BANDVALLEY} \geq I_{LED}$ in buck-boost applications, the output capacitance can be calculated with Equation (15):

$$\Delta V_{OUT} = I_{LED} \times (R_{ESR} + \frac{V_{OUT}}{f_{sw} \times C_{OUT} \times (V_{IN} + V_{OUT})}) \quad (15)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (16):

$$\Delta V_{OUT} = I_{LED} \times R_{ESR} \quad (16)$$

A 10µF to 22µF ceramic capacitor is sufficient for most applications. Place a symmetric 4.7µF / 25V X7R ceramic capacitor between LED+ and LED-.

Selecting the Diode from PGND to INGND in Buck-Boost Mode

If the device is operating in buck-boost mode, place a Schottky diode between INGND and PGND to direct the charge current of the capacitor connected between VIN and PGND, especially when the VIN slew rate is high. When (V_{INGND} - V_{PGND}) < 5.1V, VCC is powered by VIN. The VCC charge current flows from the VCC capacitor to PGND, then back to INGND and the car battery. It is recommended to use a Schottky diode with a low forward voltage (V_F) of about 0.32V, with a 1A current rating and >20V VVRRM voltage. A PMEG2010EPAS Schottky diode is recommended.

Selecting the VCC Capacitor

A small VCC capacitor causes ringing on VCC, and makes the MOSFET unstable. It is recommended to place a ≥3µF decoupling ceramic capacitor at the VCC pin. When selecting a capacitor, consider the capacitance derating to ensure that the real capacitance is at least 3µF. A 10µF X7R with a ≥10V DC rated voltage capacitor is recommended. VCC is the reference to PGND/AGND.

BST Resistor and Capacitor

It is recommended to place a resistor in series with the BST capacitor to reduce the SW spike voltage. A higher resistance reduces SW spikes, but also reduces efficiency. It is recommended to use a 22nF to 220nF ceramic capacitor with a 10/16V DC derating.

Consider efficiency and EMI performance when choosing a resistor. Choose a maximum 22Ω resistor with a 0603/0402 package, as a large package is not required. During normal operation, the average current flowing through R_{BST} is about 20mA in buck mode and 10mA in buck-boost mode. If the capacitor is shorted, the current in the resistor is limited by the internal LDO. The device can quickly detect a failure if the LED current falls below its low limit. Then the part latches off and current is no longer sourced to the resistor. A 0402 package can handle power dissipation on R_{BST}.

The part integrates BST capacitor open-detection functionality. When VIN and VCC reach their UVLO rising thresholds, the BST capacitor is charged after the 1ms thermal derating finishes. If the voltage on the BST capacitor reaches the UVLO rising threshold within 45µs, the part detects a BST open fault and latches off. If VIN restarts frequently, the BST capacitor may not be able to discharge sufficiently, and an open fault may be mistriggered. To avoid a mistrigger, place a small BST capacitor and a bleeding resistor in parallel with the BST capacitor. This ensures that

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the BST capacitor voltage is sufficiently low after a restart. It is recommended to use a 22nF capacitor and a 15kΩ resistor (see Figure 8).

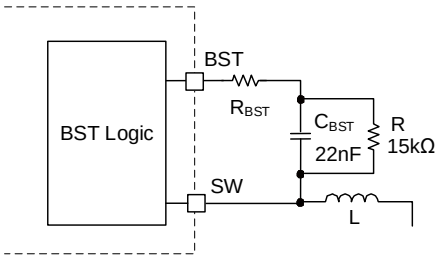

Figure 8: BST Recommend Circuitry in VIN Hot-Plug Application

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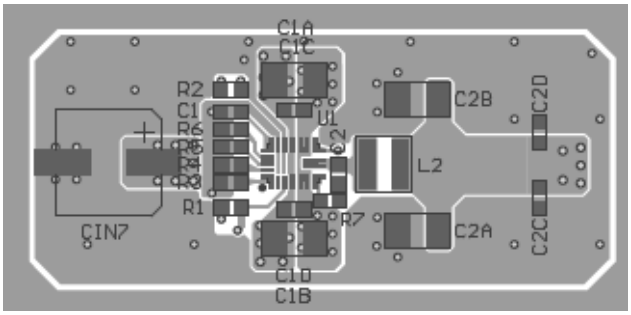
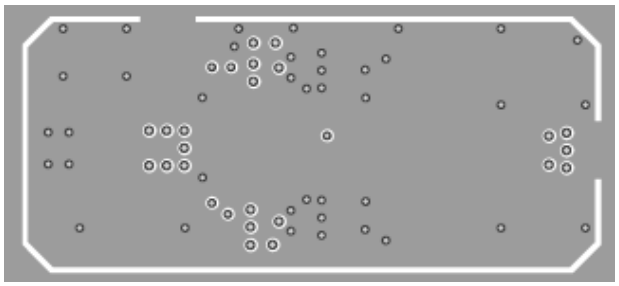
PCB Layout Guidelines (13) (14)

Efficient PCB layout, especially input capacitor placement, is critical for stable operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 9 and Figure 10, and follow the guidelines below:

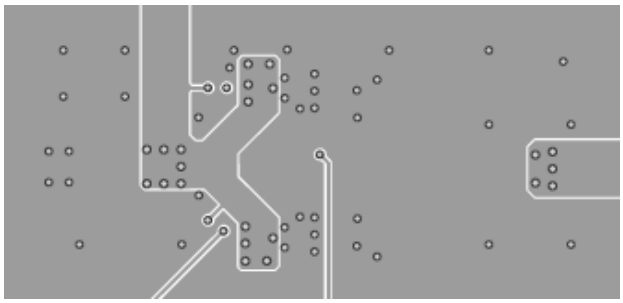
1. Place symmetric input capacitors as close to VIN and GND as possible. For buck-boost mode, connect the symmetric capacitors as close to VIN and PGND as possible.
2. connect the PGND pin directly to a large ground plane on the PCB.
3. If the bottom layer is a ground plane, add vias near PGND.
4. Ensure that the high-current paths at PGND and VIN have short, direct, and wide traces.
5. Place the ceramic input capacitor (especially the 0603small package size capacitor) as close to VIN and PGND as possible to minimize high-frequency noise.
6. Make the connection between the input capacitor and VIN as short and wide as possible.
7. Place the VCC capacitor as close to VCC and PGND as possible.
8. Route SW and BST away from sensitive analog areas.
9. Use multiple vias to connect the power planes to the internal layers.



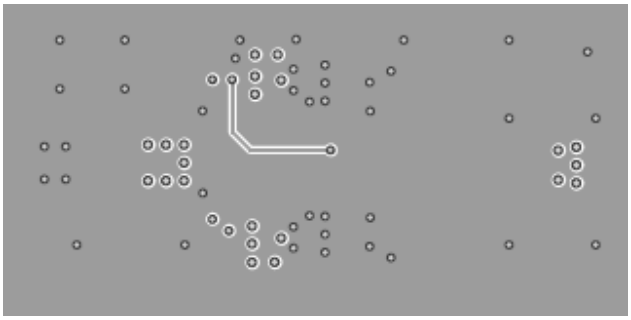
Top Layer



Inner Layer 1



Inner Layer 2



Bottom Layer

Figure 9: Recommended PCB Layout for Buck Mode (13)

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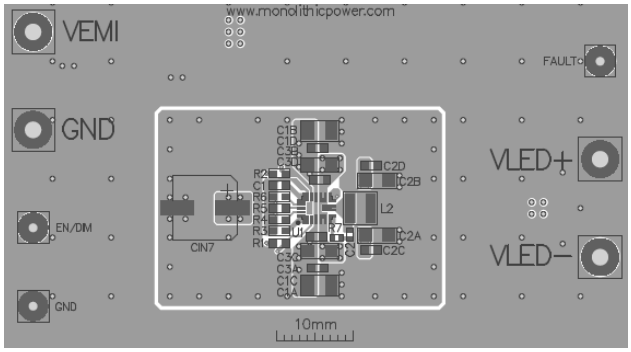
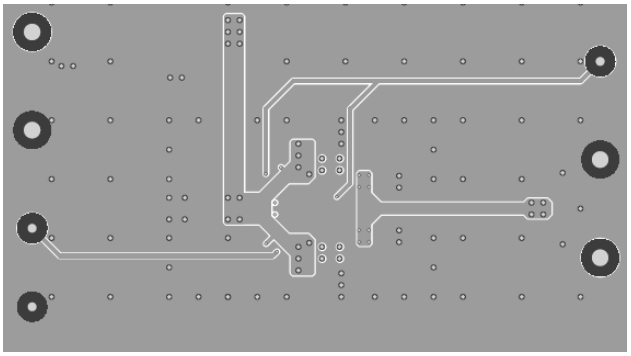
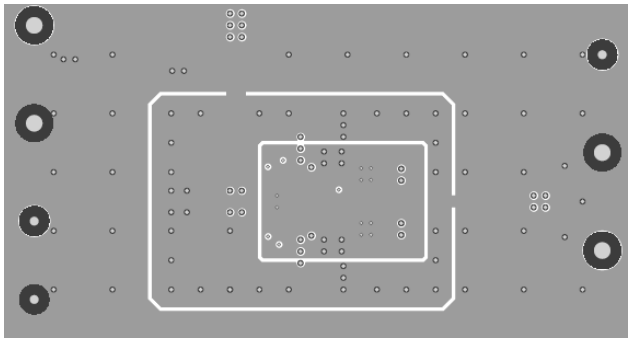


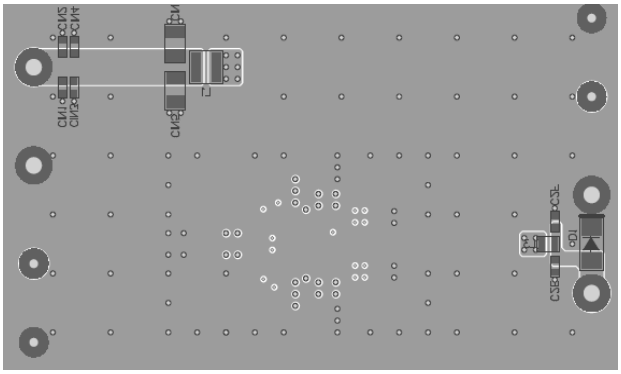
Top Layer



Inner Layer 2



Inner Layer 1



Bottom Layer

Figure 10: Recommended PCB Layout for Buck-Boost Mode (14)

Notes:

13) The recommended layout is based on Figure 11.
14) The recommended layout is based on Figure 12.

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TYPICAL APPLICATION CIRCUITS

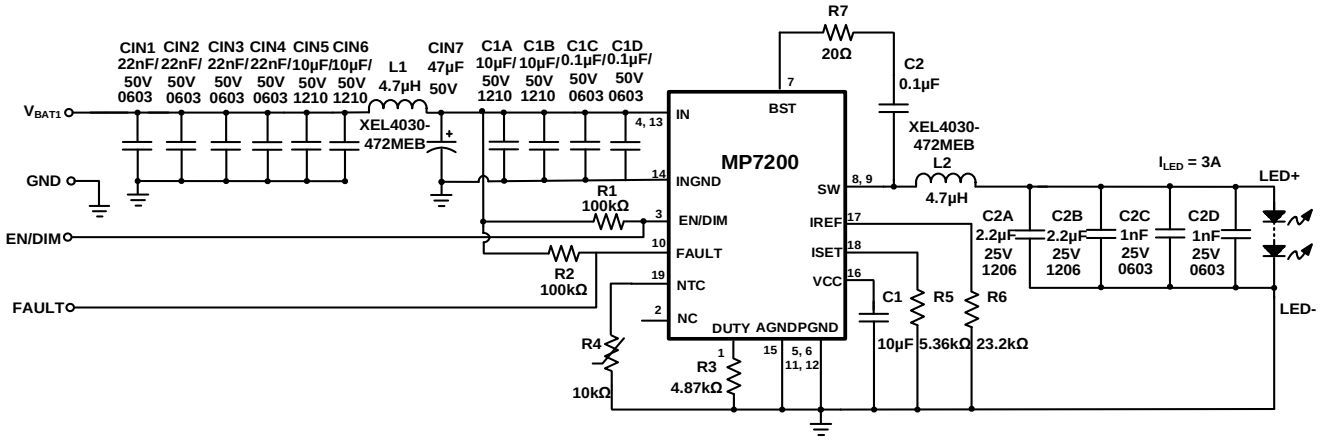

Figure 11: I_{LED} = 3A Buck Application Circuit with No Two-Step Dimming

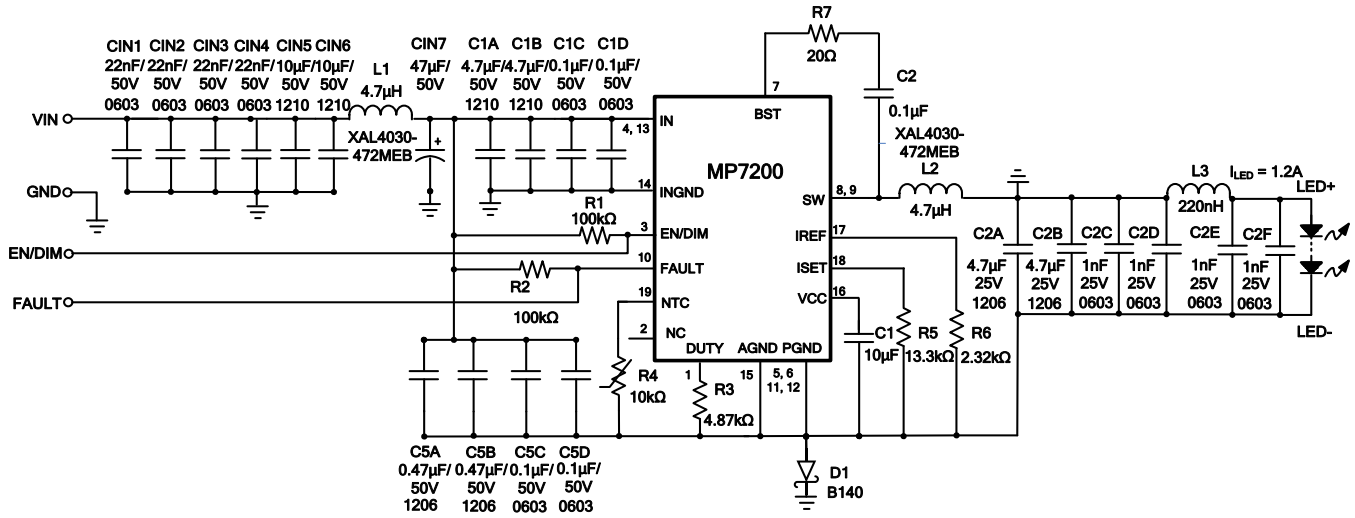

Figure 12: I_{LED} = 1.2A Buck-Boost Application Circuit with No Two-Step Dimming

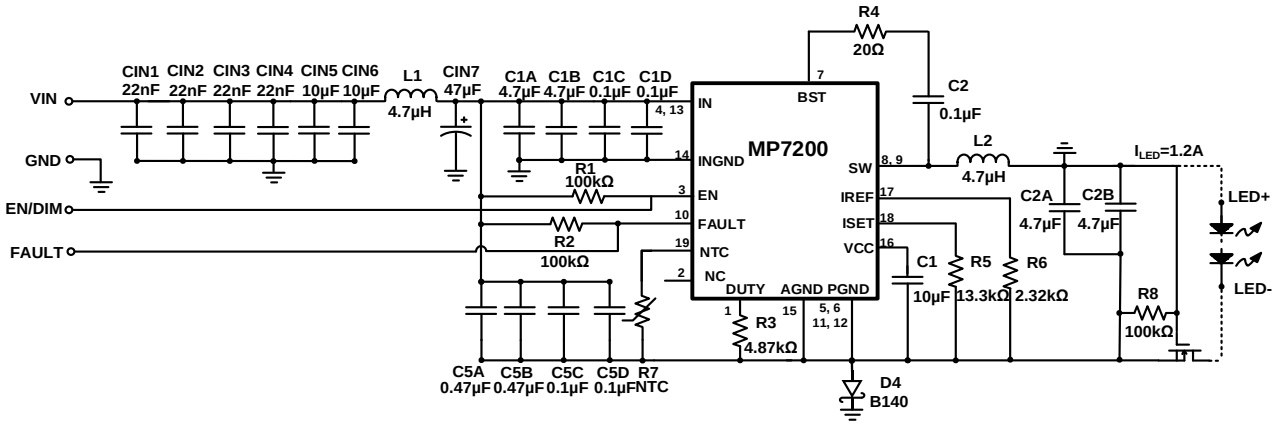

Figure 13: I_{LED} = 1.2A Buck-Boost Application Circuit with LED+ Short to Battery Protection

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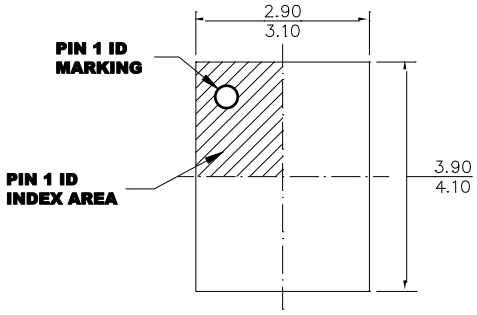
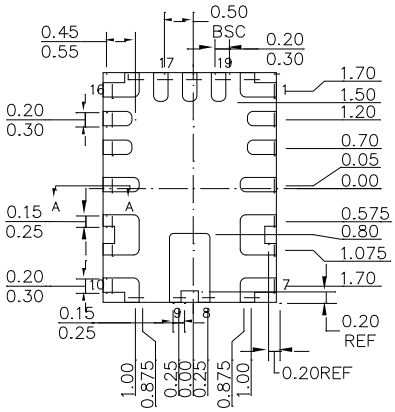
PACKAGE INFORMATION

QFN-19 (3mmx4mm)

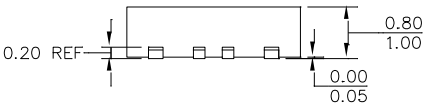
Wettable Flank



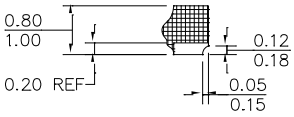
TOP VIEW



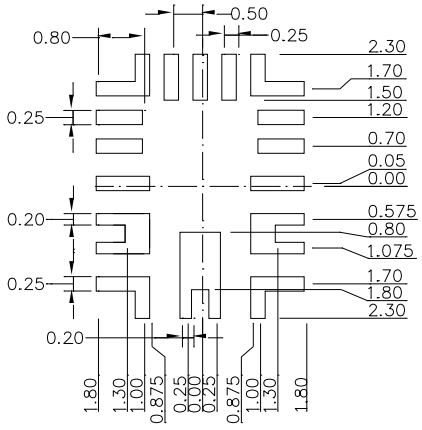
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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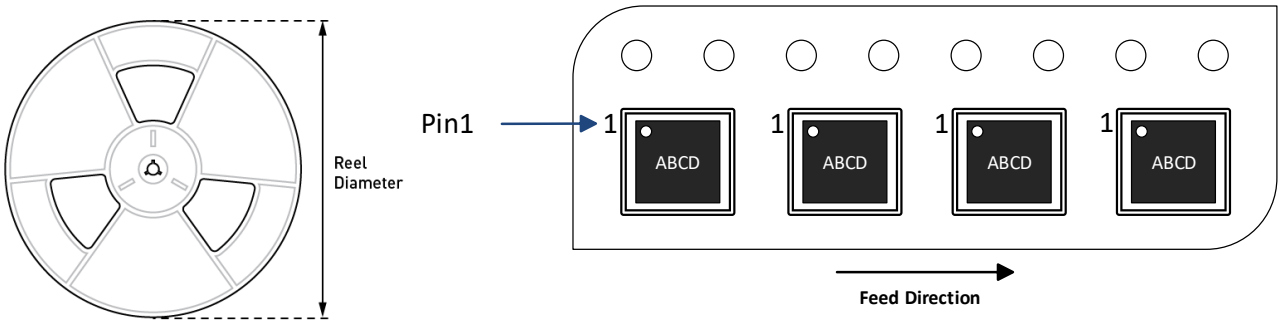
CARRIER INFORMATION



Part Number	Package Description	Quantity/Reel	Quantity /Tube	Quantiy /Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP7200GLE–Z	QFN-19 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	1/21/2021	Initial Release	-

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