MP6951

Fast Turn-Off Rectifier for Flyback Converter with Intelligent V_{DS} Ringing Detection

DESCRIPTION

The MP6951 is a secondary synchronous rectification driver using flip-chip assembly technology for high-frequency flyback converters. The device can support up to 1MHz flyback converters.

The forward drop of the external synchronous rectifier (SR) MOSFET is regulated to about 40mV. The MP6951 switches the SR MOSFET off as soon as the voltage becomes negative.

The MP6951 uses intelligent V_{DS} ringing detection technology. This helps prevent the MOSFETs' gate driver from being falsely triggered due to V_{DS} oscillations during discontinuous conduction mode (DCM) and quasi-resonant (QR) operation.

The MP6951 is available in a space-saving TSOT23-6 package.

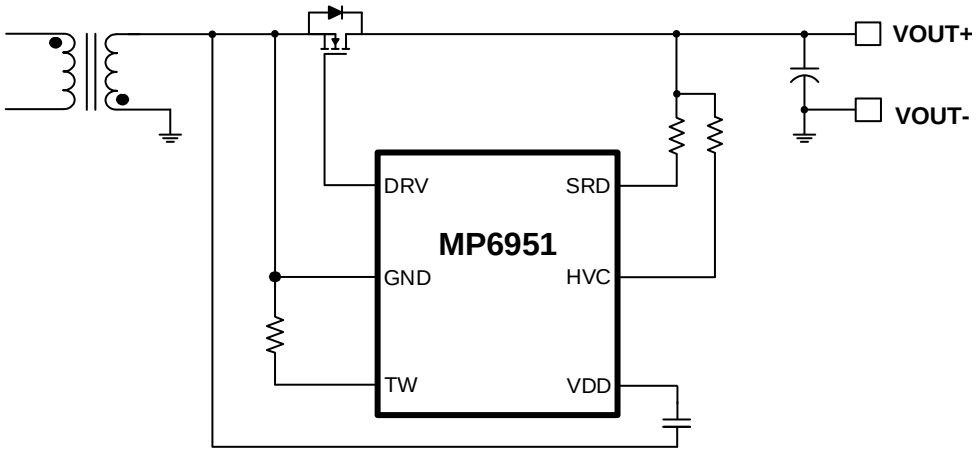
FEATURES

- Supports Discontinuous Conduction Mode (DCM), Continuous Conduction Mode (CCM), Quasi-Resonant (QR), Zero Voltage Switching (ZVS), Active Clamp Flyback and Hybrid Flyback (HFB)
- Supports Up to 1MHz Switching Frequency (f_{SW})
- Wide Output Voltage (V_{OUT}) Range Down to 0V
- No Need for Auxiliary Winding for High-Side or Low-Side Rectification
- V_{DS} Ringing Detection Prevents False Trigger during DCM, QR, and ZVS Operations
- Works with Logic Level MOSFET (GaN and SiC)
- Fast Turn-Off and Turn-On Delay
- <300μA Quiescent Current (I_Q)
- Supports High-Side and Low-Side Rectification
- Available in a TSOT23-6 Package

APPLICATIONS

- USB PD and Quick Chargers
- Adapters
- General Flyback Power Supplies

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP6951GJ	TSOT23-6	*See Below*

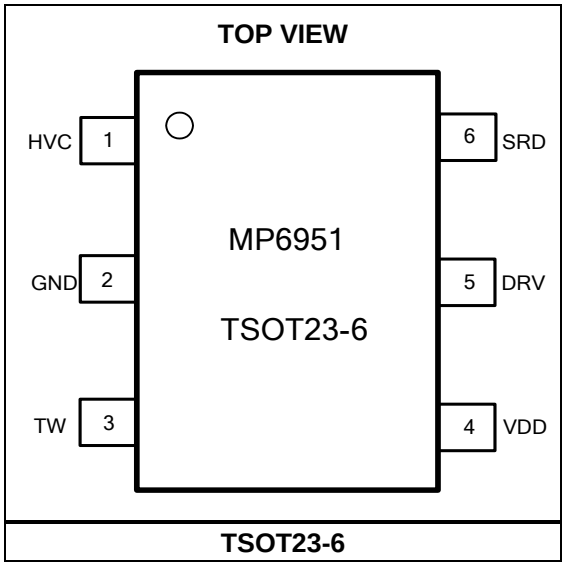
* For Tape & Reel, add suffix -Z (e.g. MP6951GJ-Z).

TOP MARKING

|BUJY

BUJ: Product code of MP6951GJ
Y: Year code

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	HVC	**HV linear regulator input.**
2	GND	**Ground.** The GND pin is the reference for MOSFET source sensing.
3	TW	**Configuration for the V_{DS} ringing detection time window.** Connect the TW pin to GND with an external resistor.
4	VDD	**Linear regulator output.** The VDD pin supplies power to the IC.
5	DRV	**MOSFET gate driver output.**
6	SRD	**MOSFET drain voltage sense.**

ABSOLUTE MAXIMUM RATINGS (1)

VDD, DRV to GND.....-0.3V to +14V
HVC, SRD to GND.....-1V to +180V
Other pins to GND .....-0.3V to+ 6.5V
Continuous power dissipation (T_A = 25°C) (2)
……..... 0.56W
Junction temperature ..... 150°C
Lead temperature (solder) .....260°C
Storage temperature ..... -55°C to +150°C

Recommended Operation Conditions (3)

VDD to GND .....4.5V to 13V
HVC, SRD to GND.....-1V to +150V
Maximum junction temp (T_J) .....125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TSOT23-6……...220.....110..°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{DD} = 6.7V, T_J = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
IC Supply Function						
VDD under-voltage lockout (UVLO) rising threshold	V_{UVLO}		4	4.2	4.4	V
VDD UVLO hysteresis	V_{UVLO_HYS}		0.1	0.2	0.3	V
VDD regulation voltage	V_{DD_HVC}	SRD = 12V, HVC = 12V	6.1	6.5	6.9	V
	V_{DD_SRD}	SRD = 12V, HVC = 3V	4.55	4.9	5.25	
VDD charge current	I_{VDD_SRD}	V_{DD} = 4V, SRD = 30V, C_{DD} = 1µF	23	43	63	mA
	I_{VDD_HVC}	V_{DD} = V_{DD_HVC} - 1V, HVC = 12V, C_{DD} = 1µF	20	50	80	
		V_{DD} = V_{DD_HVC}-1V, HVC = 30V, C_{DD} = 1µF	40	72	105	
Operating current	I_{CC}	V_{DD} = 6.7V, C_{LOAD} = 2.2nF, f_{SW} = 100kHz		2.3	3	mA
		V_{DD} = 5V, C_{LOAD}=2.2nF, f_{SW} = 100kHz		1.8	2.4	
Quiescent current	I_Q	V_{DD} = 5V			355	µA
Shutdown current	$I_{SD(VDD)}$	V_{DD} = V_{UVLO} - 0.1V			100	µA
High Voltage SRD Pin						
Input bias current on the SRD pin		V_{DD} = 100V			65	µA
		V_{DD} = 30V			28	
Regulation Control Section						
Forward regulation voltage (GND-SRD)	V_{FWD}			40		mV
Turn on threshold (SRD-GND)	V_{ON}		-110	-80	-50	mV
Turn off threshold (SRD-GND)	V_{OFF}		-14	-4	+5	mV
Turn-on delay	t_{DON_FAST}	C_{LOAD} = 2.2nF		30		ns
Turn-off delay	t_{DOFF}	C_{LOAD} = 2.2nF		20		ns
Turn-on delay during low gate charge mode	t_{DON_LGC}	C_{LOAD} = 2.2nF		300		ns
Turn-off propagation delay (5)				10		ns
Turn-on blanking time	t_{MOT}			0.62		us
Turn-off blanking threshold (SRD-GND)	V_{B-OFF}		1.3	1.8	2.1	V
Turn-off threshold during minimum on time (SRD-GND)	V_{B-ON}					
V_{DS} Ringing Detection						
Slew rate detection time window threshold	t_{W_SRD}	R_{TW} = 100kΩ	320	440	560	ns

ELECTRICAL CHARACTERISTICS *(continued)*

V_{DD} = 6.7V, T_J = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Gate Driver Section						
V_{DRV} (low)	V_{DRV-L}	I_{LOAD} = 10mA		5	15	mV
V_{DRV} (high)	V_{DRV-H}	I_{LOAD} = 0mA		V_{DD} - 0.1		V
Maximum source current at high gate charge mode (5)	I_{CH_HGC}			0.5		A
Maximum source current at low gate charge mode (5)	I_{CH_LGC}			100		mA
Maximum sink current (5)				3		A
Pull-down impedance		I_{LOAD} = 10mA		0.5	1	Ω

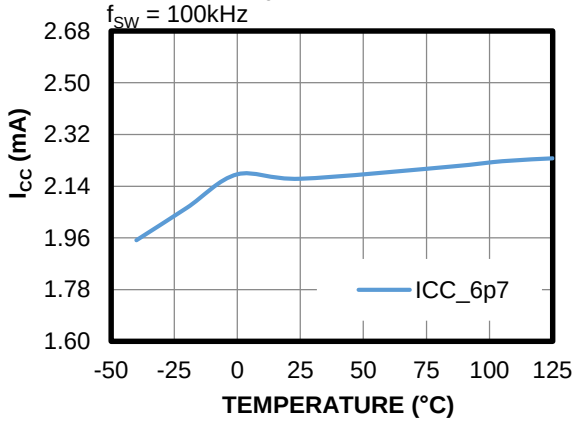
Note:

5) Guaranteed by characterization and design.

TYPICAL PERFORMANCE CHARACTERISTICS

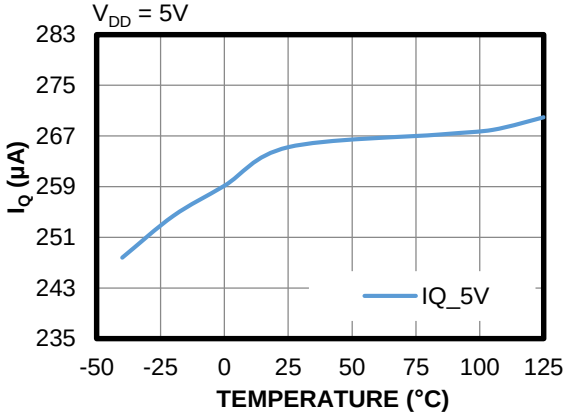
Operating Current vs. Temperature

V_{DD} = 6.7V, C_{LOAD} = 2.2nF, f_{SW} = 100kHz



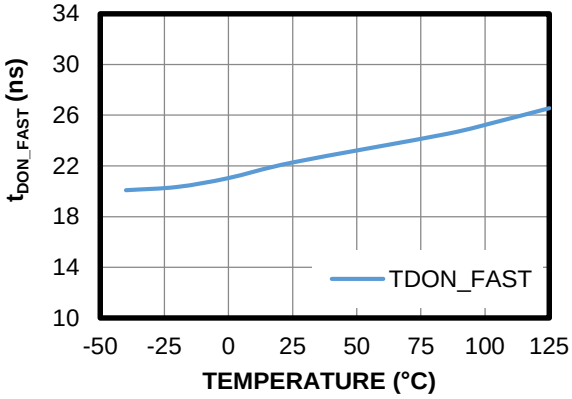
Quiescent Current vs. Temperature

V_{DD} = 5V



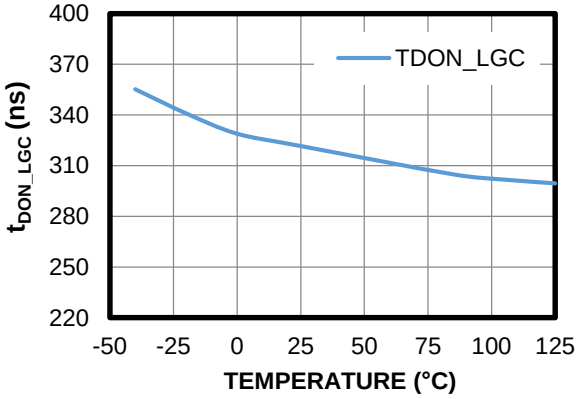
Turn-On Delay vs. Temperature

V_{DD} = 6.7V, C_{LOAD} = 2.2nF



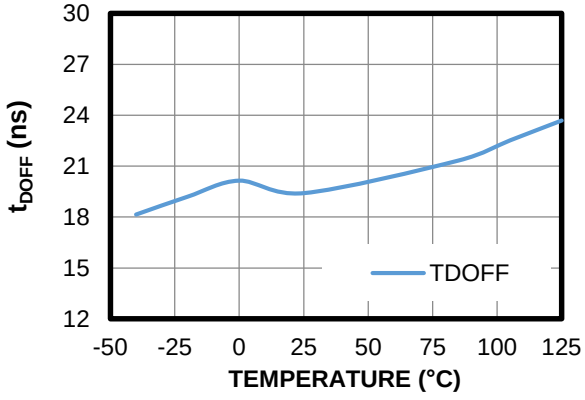
Turn-On Delay during LGC Mode

V_{DD} = 6.7V, C_{LOAD} = 2.2nF

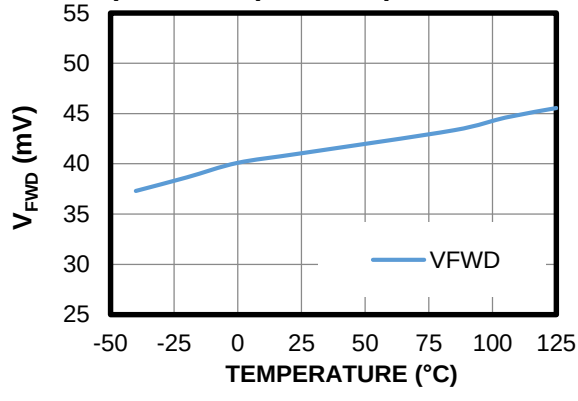


Turn-Off Delay vs. Temperature

V_{DD} = 6.7V, C_{LOAD} = 2.2nF



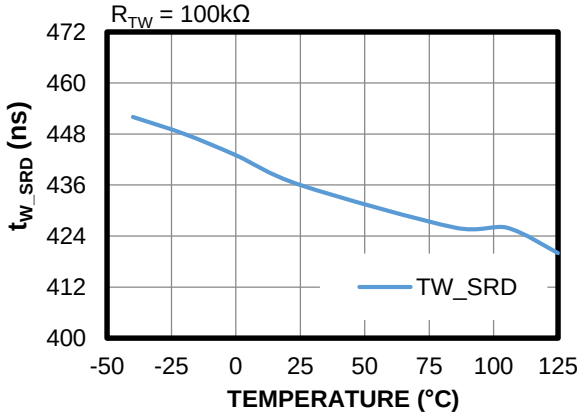
Forward Regulation Voltage (GND-SRD) vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

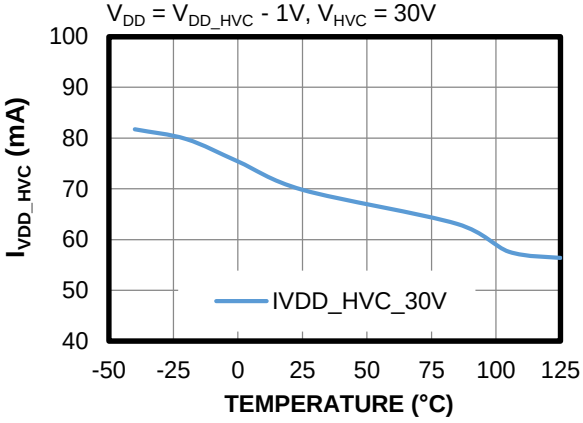
Slew Rate Detection Time Window Threshold vs. Temperature

R_{TW} = 100kΩ



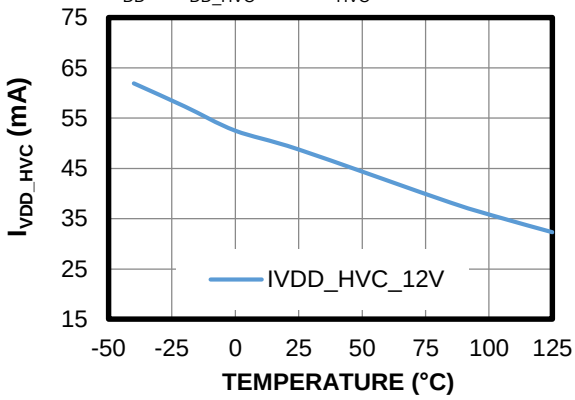
VDD Maximum Charging Current vs. Temperature

V_{DD} = V_{DD_HVC} - 1V, V_{HVC} = 30V



VDD Maximum Charging Current vs. Temperature

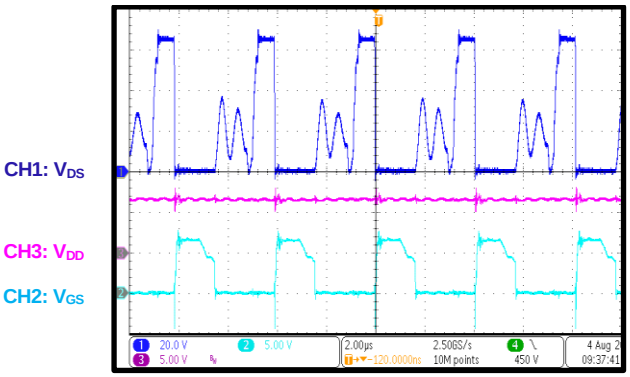
V_{DD} = V_{DD_HVC} - 1V, V_{HVC} = 12V



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

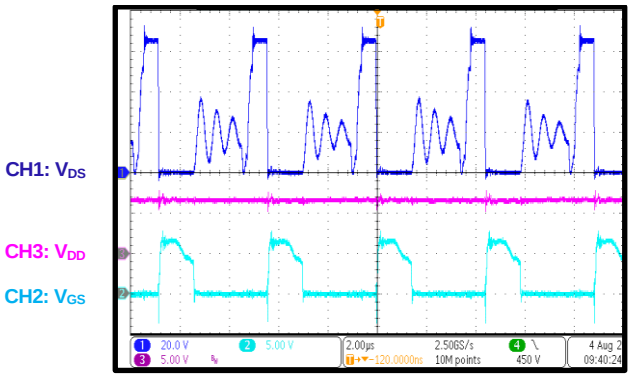
Operation in 65W ZVS Flyback Application

V_{IN} = 220V_{AC}, V_{OUT} = 20V, I_{OUT} = 3.25A,
HVC connected to MOSFET drain



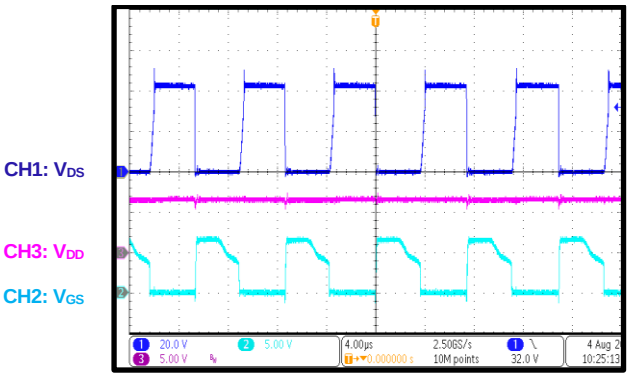
Operation in 45W ZVS Flyback Application

V_{IN} = 220V_{AC}, V_{OUT} = 20V, I_{OUT} = 2.25A,
HVC connected to MOSFET drain



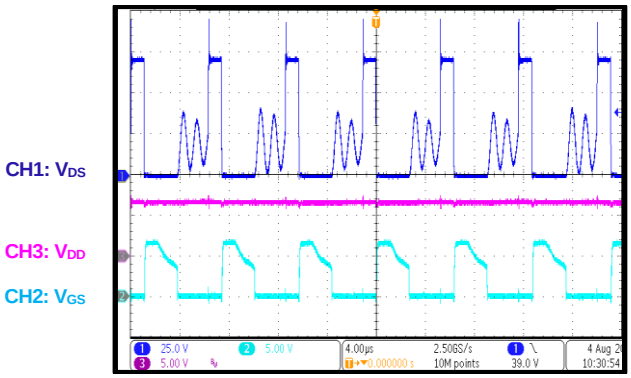
Operation in 65W QR Flyback Application

V_{IN} = 110V_{AC}, V_{OUT} = 20V, I_{OUT} = 3.25A,
HVC connected to MOSFET drain



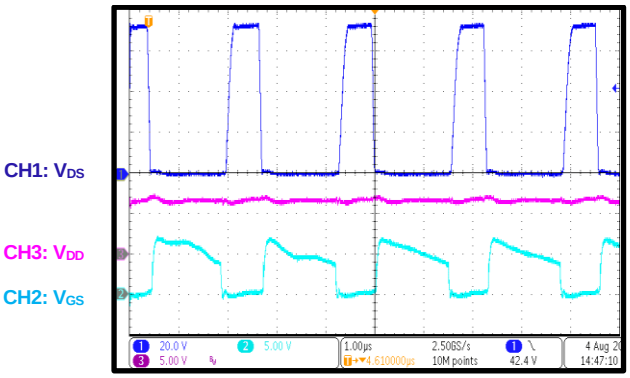
Operation in 65W QR Flyback Application

V_{IN} = 220V_{AC}, V_{OUT} = 20V, I_{OUT} = 3.25A,
HVC connected to MOSFET drain



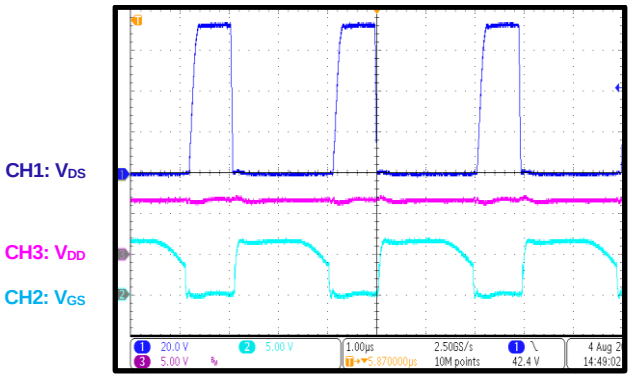
Operation in High Frequency (HF) Flyback Application

V_{IN} = 220V_{AC}, V_{OUT} = 20V, I_{OUT} = 1A,
HVC connected to MOSFET drain



Operation in HF Flyback Application

V_{IN} = 220V_{AC}, V_{OUT} = 20V, I_{OUT} = 3.25A,
HVC connected to MOSFET drain



FUNCTIONAL BLOCK DIAGRAM

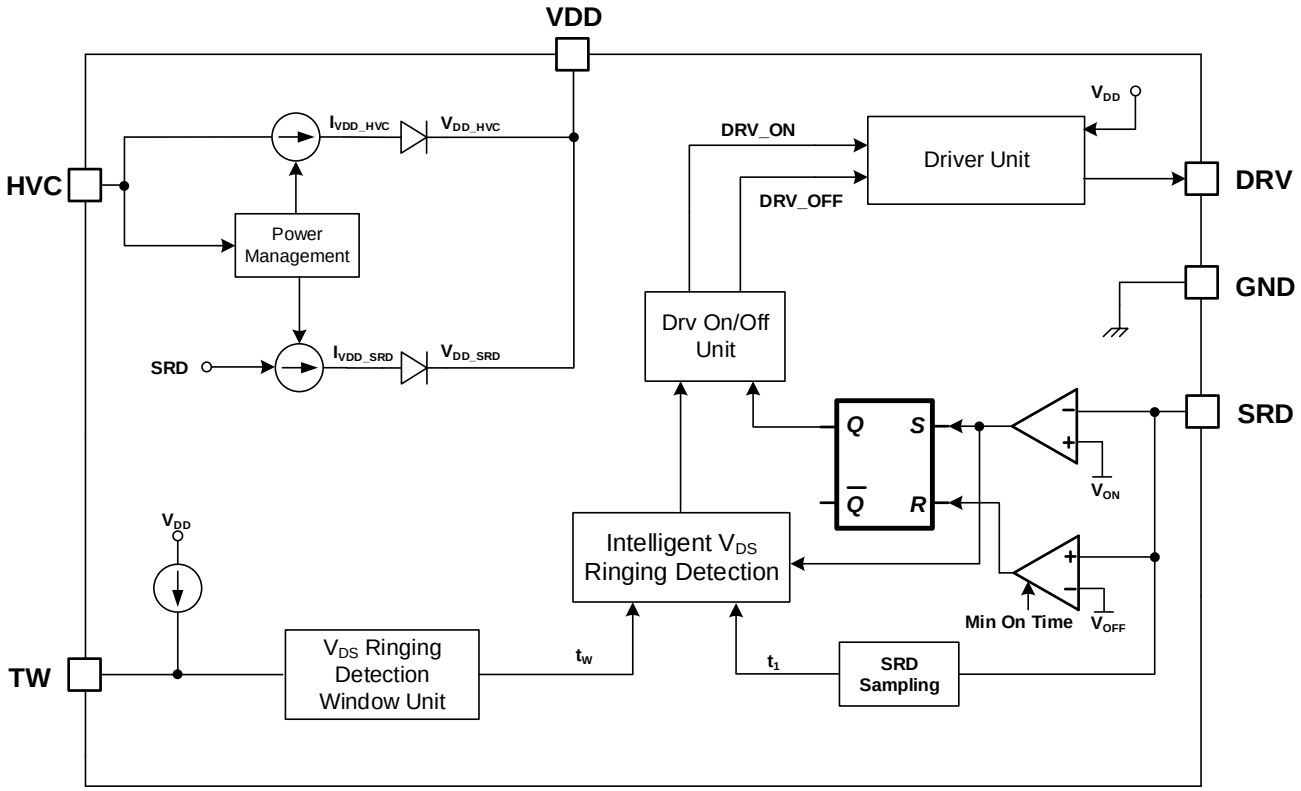


Figure 1: Functional Block Diagram

OPERATION

The MP6951 supports operation in discontinuous conduction mode, (DCM), continuous conduction mode (CCM), quasi-resonant (QR) mode, zero voltage switching (ZVS), and active clamp flyback. The control circuitry controls the gate in forward mode and turns the gate off when the synchronous rectifier (SR) MOSFET current drops to zero.

Self-Power Supply on VDD

The MP6951 is powered by the voltage on the VDD pin (V_{DD}), which can be charged by internal current sources through both HVC and SRD.

When V_{DD} < its under-voltage lockout threshold (V_{UVLO}), SRD charges the VDD capacitor via an internal current source (I_{VDD_SRD}).

When $V_{UVLO} \leq V_{DD} < V_{DD\_SRD}$, HVC can charge VDD via an internal current source (I_{VDD_HVC}), along with I_{VDD_SRD}.

When $V_{DD} \geq V_{DD\_SRD}$, SRD stops charging, and only HVC charges VDD via I_{VDD_HVC}. V_{DD} is clamped at V_{DD_HVC} for its maximum value.

Start-Up and Under-Voltage Lockout (UVLO)

When V_{DD} exceeds V_{UVLO}, the MP6951 exits the UVLO state and is operational. If V_{DD} drops below V_{UVLO} - V_{UVLO_HYS}, the MP6951 enters sleep mode and DRV stays low.

Turn-On Phase

If the VDS voltage (V_{SRD} - V_{GND}) falls below the turn-on threshold (V_{ON}) due to the conduction of the SR MOSFET's body diode, then the SR MOSFET turns on after a turn-on delay (see Figure 2).

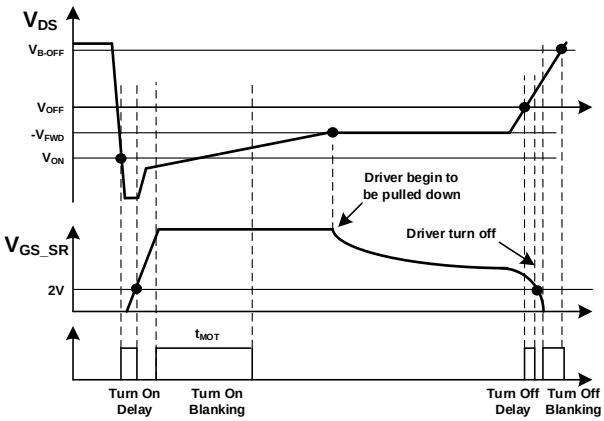


Figure 2: Turn-On/Off Timing Diagram

Intelligent V_{DS} Ringing Detection

The MP6951 employs a patented, intelligent method to detect the body diode conduction caused by V_{DS} ringing to avoid falsely triggering the SR gate (see Figure 3).

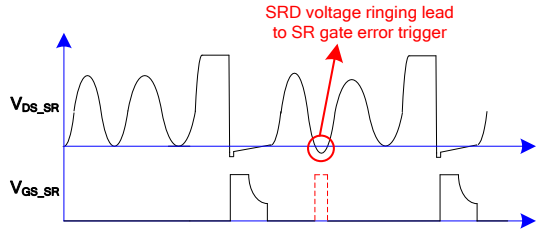


Figure 3: SR Gate Falsely Turns On due to SRD Voltage Ringing

The duration of the peak SRD voltage plateau (t_1) is sampled every cycle. If t_1 is longer than configurable detection time window (t_W), then the MP6951 enters high gate charge mode, and the internal SR_ACTIVE flag is pulled high. In high gate charge mode, once the VDS voltage falls below V_{ON}, the MP6951 turns on the SR MOSFET with maximum source current (I_{CH_HGC}) after a short turn-on delay (t_{DON_FAST}) (see Figure 4).

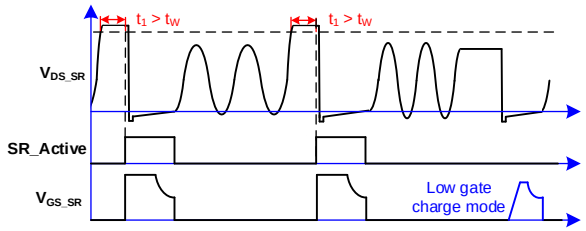


Figure 4: VDS Ring Detection of MP6951

If t_1 is detected to be shorter than t_W, then the MP6951 enters low gate charge mode. In this mode, the SR gate driver's max source current drops to I_{CH_LGC} with a large turn-on delay (t_{DON_LGC}) during the turn-on phase (see Figure 4). In low gate charge mode, the body diode conduction lead by V_{DS} ringing cannot trigger the SR MOSFET due to the SR driver's low source current and long turn-on delay.

At a high line input, the flyback primary's duty cycle drops low, and t_1 may always be shorter than t_W. The MP6951 can distinguish these conditions and keep the SR gate driver in high gate charge mode.

The V_{DS} ringing detection time window (t_W) can be configured via the TW pin. t_W can be calculated with Equation (1):

$$t_W = \frac{R_{TW}}{100k\Omega} t_{W\_SRD} \quad (1)$$

Turn-On Blanking

The control circuitry contains a blanking function. When the circuitry pulls the MOSFET on, it ensures that the on state lasts for the turn-on blanking time (t_{MOT}). t_{MOT} prevents the MOSFET from accidently turning off due to V_{DS} ringing, during which the turn-off threshold is blanked (see Figure 2 on page 11). However, if V_{DS} rises above V_{B-ON} during this turn-on blanking time, V_{GS_SR} pulls low to turn off the SR MOSFET immediately.

Conduction Phase

When V_{DS} rises above the forward regulation voltage ($-V_{FWD}$) according to how the switching current has decreased, the MP6951 pulls down the gate driver voltage level to raise the SR MOSFET's on resistance

With this control scheme, V_{DS} is adjusted to be about equal to $-V_{FWD}$, even when the current through the MOSFET is fairly low (see Figure 2 on page 11). This function pulls the driver voltage low when the SR MOSFET prepares to turn off, which boosts the turn-off speed.

Turn-Off Phase

When V_{DS} rises to trigger the turn-off threshold (V_{OFF}), the gate voltage is pulled to zero after a very short turn-off delay (t_{DOFF}) (see Figure 2 on page 12).

Turn-Off Blanking

After the gate driver's V_{GS_SR} is pulled to zero when V_{DS} reaches its turn-off threshold (V_{OFF}), a turn-off blanking time is applied. During this time, the gate driver signal latches off. Turn-off blanking is removed when V_{DS} rises to V_{B-OFF} (see Figure 2 on page 11).

APPLICATION INFORMATION

Intelligent V_{DS} Ringing Detection

During DCM, the demagnetizing ringing may bring V_{DS} down below 0V. If V_{DS} triggers the turn-on threshold during this ringing process, the SR controllers that cannot detect V_{DS} ringing may accidentally turn on their MOSFET. Figure.5 shows the waveform of this false turn-on scenario. Falsely turning on a MOSFET increases power loss and may also lead to shoot-through if the primary-side FET turns on within the minimum on time.

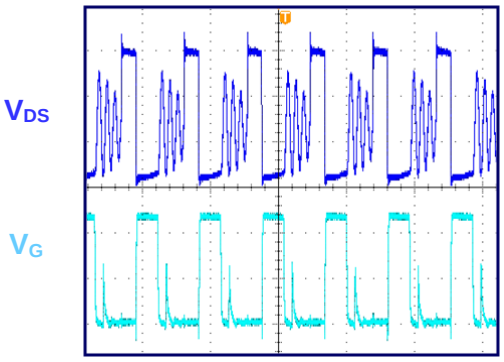


Figure 5: False Turn On without V_{DS} Ringing Detection

Since the ringing frequency is always much higher than primary MOSFET's switching frequency, the ringing time window length is shorter than the V_{DS} plateau's length. By setting a proper time length for t_W, the SR IC can distinguish V_{DS} ringing and the V_{DS} plateau due to the primary MOSFET turning on. This function helps to prevent a false turn on due to V_{DS} ringing (see Figure 6).

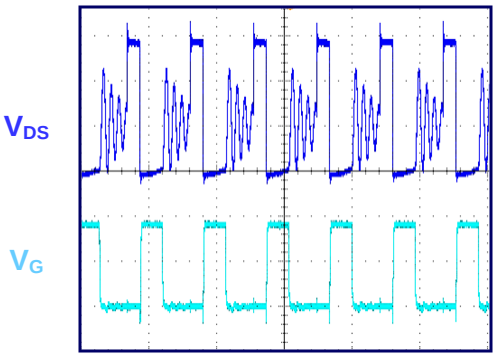


Figure 6: Preventing a False Turn On with V_{DS} Ringing Detection

Selecting the External Resistor on SRD and HVC

Over-voltage (OV) conditions can damage the device, so there must be appropriate design to guarantee the IC's safe operation, especially on the high-voltage pins (SRD and HVC).

When the body diode of the SR MOSFET is conducting, the forward voltage drop may exceed the negative rating on the SRD pin. In this case, it is recommended to place an external resistor between the SRD pin and the drain of the MOSFET. This resistance is recommended to be at least 300Ω.

Note that this resistor cannot be too large, because it compromises the VDD supply and affects V_{DS} ringing detection. In general, it is not recommended to use any resistance exceeding 1kΩ. For each practical case, choose the resistor based on the VDD supply and ringing detection.

In applications where HVC may also suffer from a negative voltage bias (e.g. in a high-side set-up without auxiliary winding), an external resistor of the same value must be placed on HVC. In addition, if a block diode is used, the reverse recovery time is recommended to be shorter than 250ns.

The HVC charging (V_{DD}) current may lead to a suboptimal voltage drop on the SRD resistor. In the scenario, connect a resistor to the SRD pin first; in addition, it may be beneficial to connect a resistor on the HVC pin.

Typical System Implementations

Figure 7 shows the MP6951 high-side rectification application when HVC is connected to the MOSFET drain.

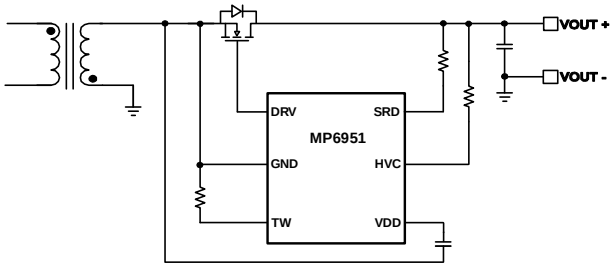


Figure 7: High-Side Rectification with HVC Connected to the MOSFET Drain

Figure 8 shows when HVC is connected to the secondary output ground through an external diode.

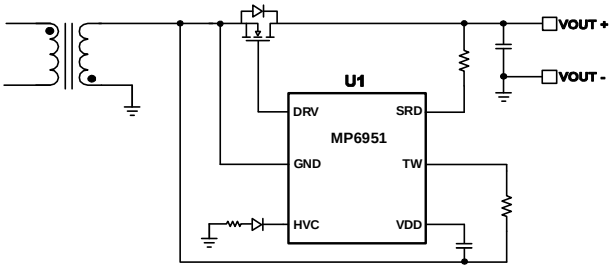


Figure 8: High-Side Rectification with HVC Connected to Output GND

The maximum voltage at HVC can be calculated with Equation (2):

$$V_{HVC(MAX)} = V_{IN} \times \frac{N_S}{N_P} \quad (2)$$

Figure 9 shows the low-side rectification application when HVC is connected to the output. For the MP6951, low-side rectification is only recommended for applications with an output voltage (V_{OUT}) that exceeds V_{DD_SRD}.

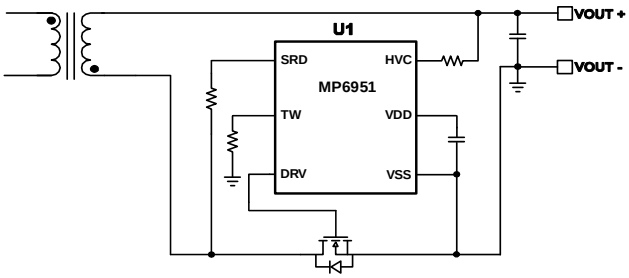


Figure 9: Low-Side Rectification with HVC Connected to the Output

Selecting the SR MOSFET

Power MOSFET selection is a tradeoff between the $R_{DS(ON)}$ and total gate charge (Q_G). To achieve higher efficiency, the MOSFET with the smaller $R_{DS(ON)}$ is preferred. Typically, Q_G is larger with a smaller $R_{DS(ON)}$, which lowers the turn-on/turn-off speed and increases power loss and driver loss.

Because V_{DS} is adjusted to be about equal to $-V_{FWD}$ during the driving period when the switching current is fairly small, a MOSFET with an $R_{DS(ON)}$ that is too low is not recommended. This is because the gate driver pulls low when $V_{DS} = -I_{SD} \times R_{DS(ON)}$ exceeds $-V_{FWD}$. The MOSFET's $R_{DS(ON)}$ does not contribute to conduction loss. The conduction loss can be calculated with Equation (3):

$$P_{CON} = -V_{DS} \times I_{SD} \approx I_{SD} \times V_{FWD} \quad (3)$$

To achieve a fairly high use of the MOSFET's $R_{DS(ON)}$, the MOSFET should be fully on for at least 50% of the SR conduction period. Estimate V_{DS} with Equation (4):

$$V_{DS} = -I_C \times R_{DS(ON)} = -I_{OUT} / D \times R_{DS(ON)} \leq -V_{FWD} \quad (4)$$

Where V_{DS} is the drain-source voltage of the MOSFET, D is the duty cycle of the secondary side, I_{OUT} is output current, and V_{FWD} is the forward voltage threshold.

Figure 10 shows the typical waveform of a flyback application. Assume it has a 50% duty cycle. The MOSFET's $R_{DS(ON)}$ is recommended to be at least 20 / I_{OUT} (in mΩ). For example, for a 5A application, the $R_{DS(ON)}$ should not be below 4mΩ.

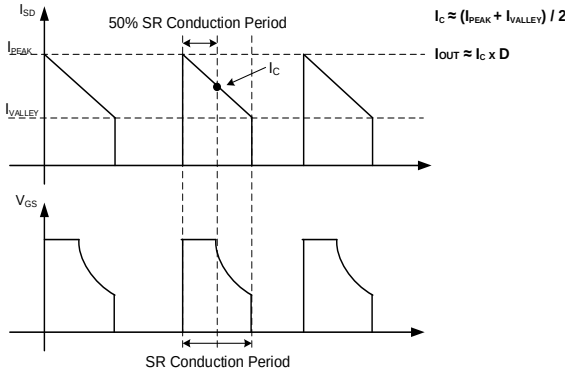


Figure 10: Typical Waveforms for Synchronous Rectification in a Flyback Application

PCB Layout Guidelines

PCB layout is critical for stable operation for the SR IC. For the best results, refer to Figure 11, Figure 12, and Figure 13, and follow the guidelines below.

Sensing for SRD/GND

1. Place the sensing connection (SRD/GND) as close as possible to the MOSFET (drain/source).
2. Make the sensing loop as small as possible.
3. Keep the IC out of the power loop to prevent the sensing loop and power loop from interrupting one other (see Figure 11).

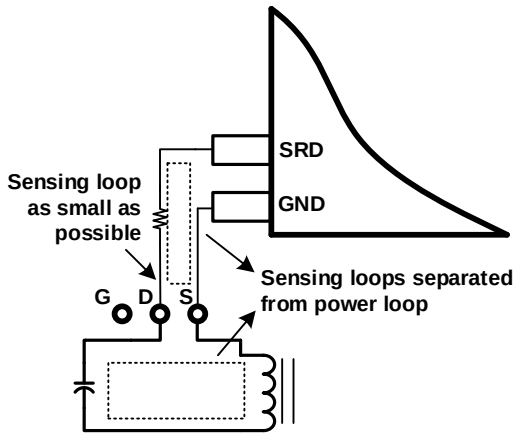


Figure 11: Voltage Sensing for SRD/GND

4. Place a decoupling ceramic capacitor from VDD to GND, and close to the IC for adequate filtering.

Gate Driver Loop

1. Make the gate driver loop as small as possible to minimize parasitic inductance.
2. Route the driver signal far away from the SRD sensing trace.

Layout Example

Figure 12 shows a layout example of a single layer with a through-hole transformer and a TO220 package SR MOSFET.

1. RSN and CSN comprise the RC snubber network for the SR MOSFET.
2. Minimize the sensing loop (SRD and GND to the SR MOSFET).
3. Separate the sensing loop from the power loop.
4. Place the VDD decoupling capacitor (C2) beside VDD.

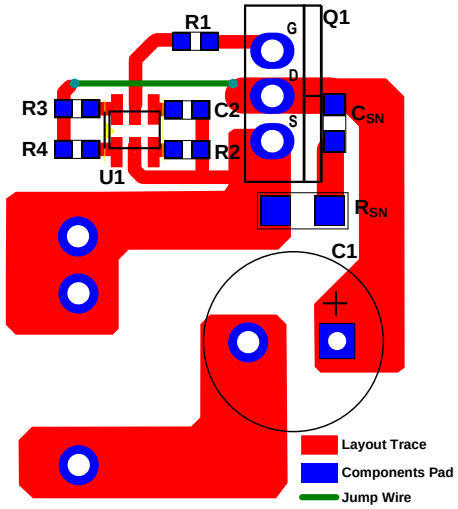


Figure 12: Recommended PCB Layout with TO220 Package SR MOSFET

Figure 13 shows another layout example of a single layer with a PowerPAK/SO8 package SR MOSFET.

1. Minimize the sensing loop and power loop to prevent the loops from interfering with one another.

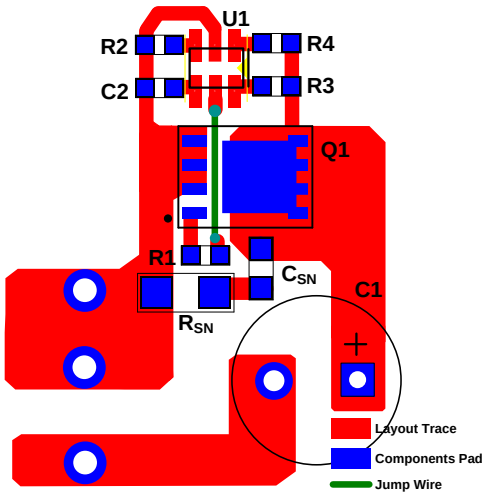


Figure 13: Recommended PCB Layout with PowerPAK/SO8 SR MOSFET

TYPICAL APPLICATION CIRCUIT

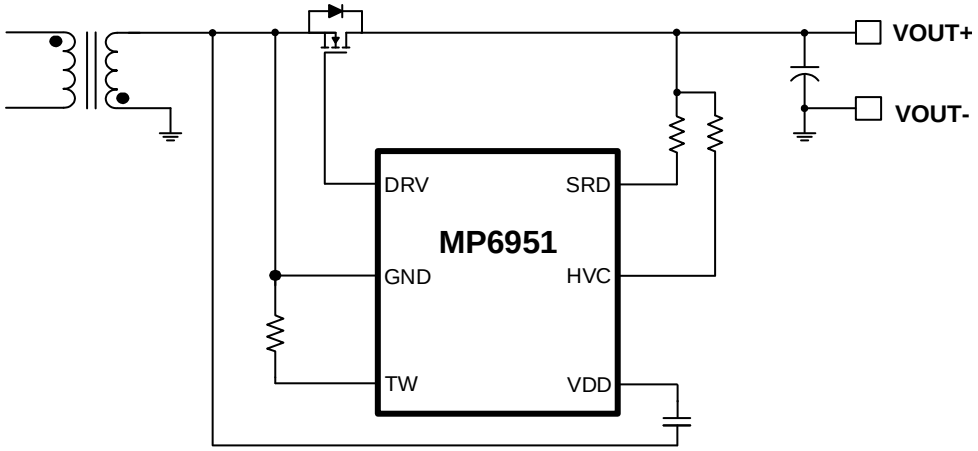
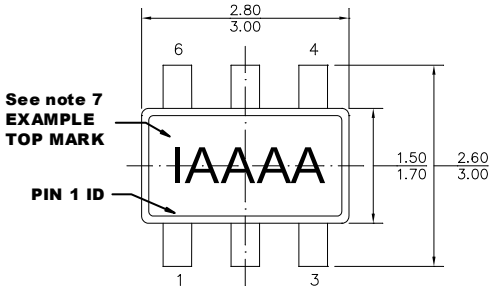


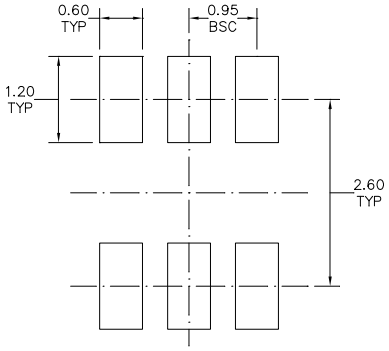
Figure 14: Typical Application Circuit

PACKAGE INFORMATION

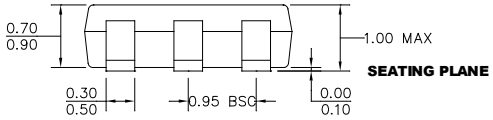
TSOT23-6



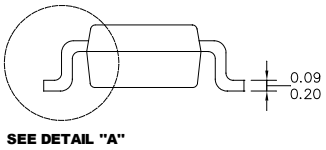
TOP VIEW



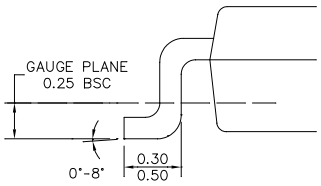
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

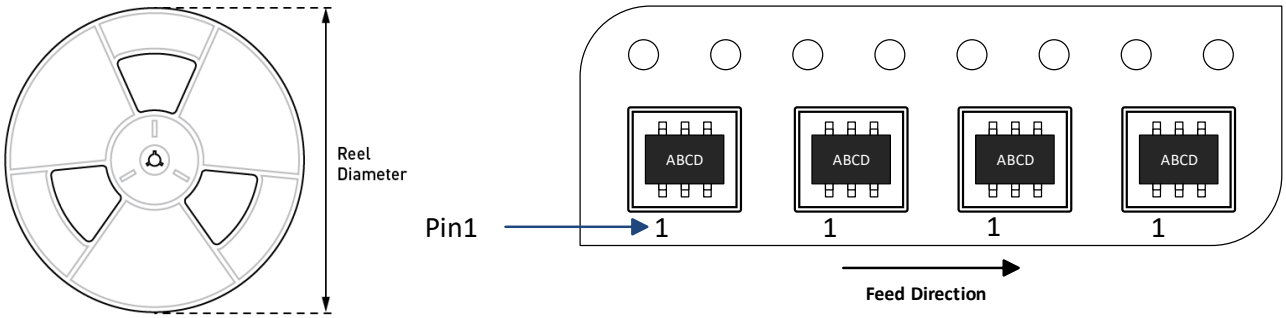


DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6951GJ-Z	TSOT23-6	3000	N/A	N/A	7in	8mm	4mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/28/2022	Initial Release	-