MP6910A

CCM/DCM Flyback Ideal Diode with Integrated 100V/15mΩ MOSFET

DESCRIPTION

The MP6910A is a fast turn-off intelligent rectifier for flyback converters that combines a 100V power switch that replaces diode rectifiers for high efficiency. The chip regulates the forward voltage drop of the internal power switch to about 65mV and turns off before the voltage goes negative.

FEATURES

- Integrated 15mΩ, 100V Power Switch
- Compatible with Energy Star
- VDD Range from 8.3V to 24V
- 65mV V_{DS} Regulation Function (1)
- Max 250kHz Switching Frequency
- Supports High-Side and Low-Side Rectification
- Available in SOIC-8 Package

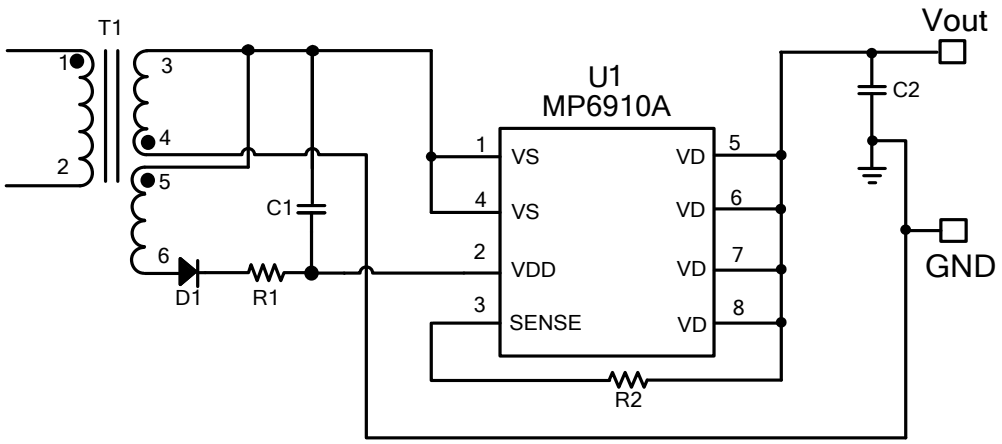
APPLICATIONS

- Laptop Adapters
- QC and USB Quick Charger
- High-Efficiency Flyback Converter

NOTE:

1) Related issued patent: US Patent US8, 067,973; US8,400,790. CN Patent ZL201010504140.4; ZL200910059751.X. Other patents pending.

TYPICAL APPLICATION

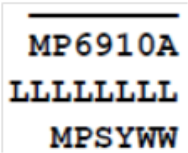


ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MP6910AGS*	SOIC-8	*See Below*	2

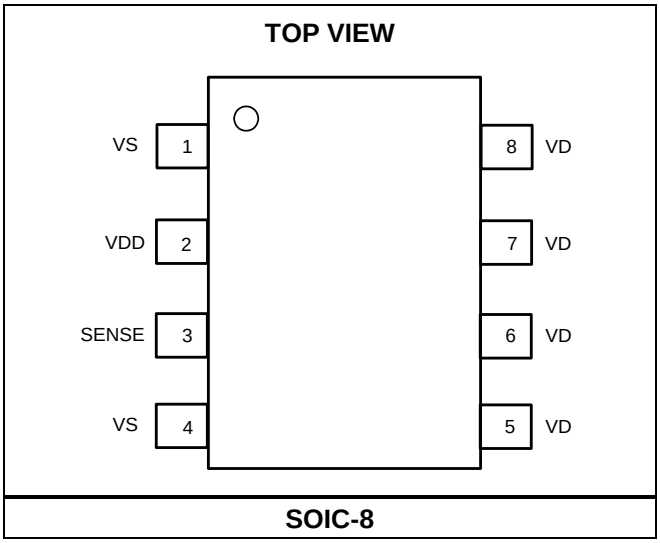
* For Tape & Reel, add suffix –Z (e.g. MP6910AGS–Z)

TOP MARKING



MP6910A: Part code of MP6910A
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1, 4	VS	**MOSFET source.** VS is also used as the reference for VDD.
2	VDD	**Supply voltage.**
3	SENSE	**MOSFET drain voltage sensing.**
5 - 8	VD	**MOSFET drain.**

ABSOLUTE MAXIMUM RATINGS (2)

VDD to VS ..... -0.3V to +25V
VD to VS..... -1.5V to +100V
SENSE to VS..... -1V to +180V
Maximum operating frequency.....250kHz
Continuous drain current (T_C = 25°C) 11.8A
Continuous drain current (T_C = 100°C) 7.5A
Pulsed drain current (3) 50A
Maximum power dissipation (4) 1.8W
Junction temperature.....150°C
Lead temperature (solder) .....260°C
Storage temperature .....-55°C to +150°C

ESD Rating

Human-body model (HBM)
Sense pin..... +1200V, -2000V
Other pins.....±2000V
Charged-device model (CDM).....±2000V

Recommended Operation Conditions (5)

VDD to VS ..... 8.3V to 24V
Operating junction temp. (T_J). .. -40°C to +125°C

Thermal Resistance (6)

	θ_{JA}	θ_{JC}	
SOIC-8	67	30	°C/W

NOTES:

2) Exceeding these ratings may damage the device.
3) Repetitive Rating: Pulse width=100µs, duty cycle limited by maximum junction temperature
4) T_A = +25°C. The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
5) The device is not guaranteed to function outside of its operating conditions.
6) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

VDD = 12V, T_J = -40 ~ 125°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VDD voltage range			8.3		24	
VDD UVLO rising			6.2	7.2	8.2	V
VDD UVLO hysteresis			0.8	1.1	1.4	V
Operating current	I_{CC}	f_{SW} = 100kHz		2.6	4	mA
Light-load mode current				255	350	µA
Control Circuitry Section						
VSS - VD forward voltage	V_{FWD}		45	65	85	mV
Turn-on delay (7)	t_{Don}			100		ns
Turn-off threshold (VSS - VD)			20	30	40	mV
Turn-off delay (8)	t_{Doff}			30		ns
Minimum on time	t_{MIN}		0.6	1	1.7	µs
Light-load enter delay	$t_{LL\text{-}Delay}$		70	120	170	µs
Light-load enter pulse width	t_{LL}		1.4	2.2	3.6	µs
Light-load enter pulse-width hysteresis(8)	$t_{LL\text{-}H}$			0.27		µs
Light-load mode exit pulse-width threshold (V_{DS})	$V_{LL\text{-}DS}$		-315	-190	-70	mV
Power Switch Section(9)						
Drain source breakdown voltage(7)	$V_{(BR)DSS}$		100			V
Single-pulse avalanche energy(7)	E_{AS}	V_{PS}=50V, V_{GS} = 10V, L = 1.0mH		100		mJ
Drain source on resistance	$R_{DS(ON)}$	VDD = 12V, I_D = 2A,		15	18.8	mΩ
Input capacitance(8)	C_{iss}	V_{DS} =40V, V_{GS} = 0V, f = 1MHz		1925		pF
Output capacitance(8)	C_{oss}			307		pF
Reverse transfer capacitance(8)	C_{rss}			20		pF
Source-Drain Diode Characteristics						
Source-drain diode forward voltage	V_{SD}	I_S = 20A, V_{GS} = 0V		0.8	1.2	V
Reverse recovery time(8)	t_{rr}	I_F = 10A, dI/dt = 100A/µs		79		ns
Diode reverse change(8)	Q_{rr}			106		nC

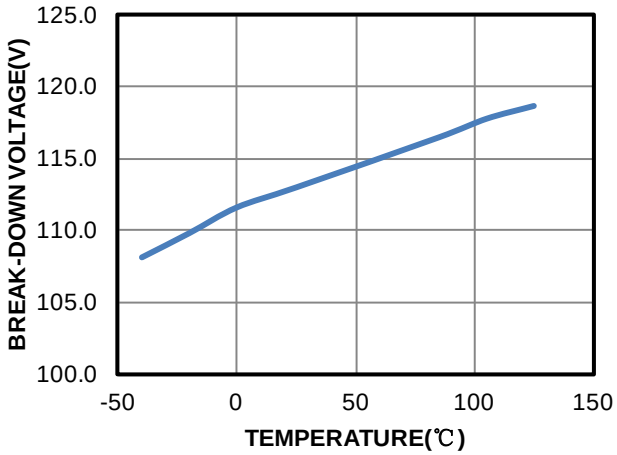
NOTES:

7) Guaranteed by characterization.
8) Guaranteed by design.
9) T_J=25°C.

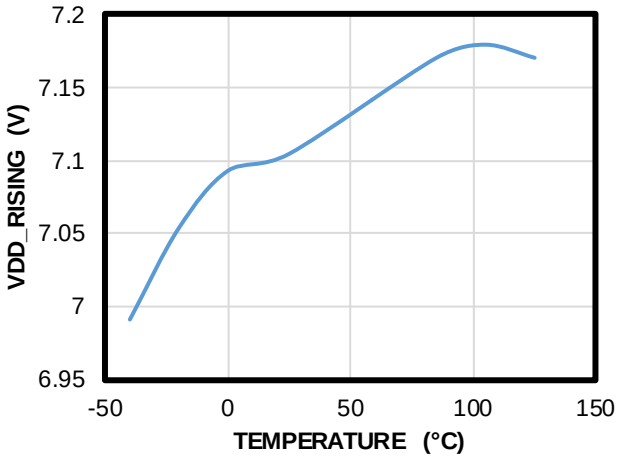
TYPICAL CHARACTERISTICS

VDD = 12V, unless otherwise noted.

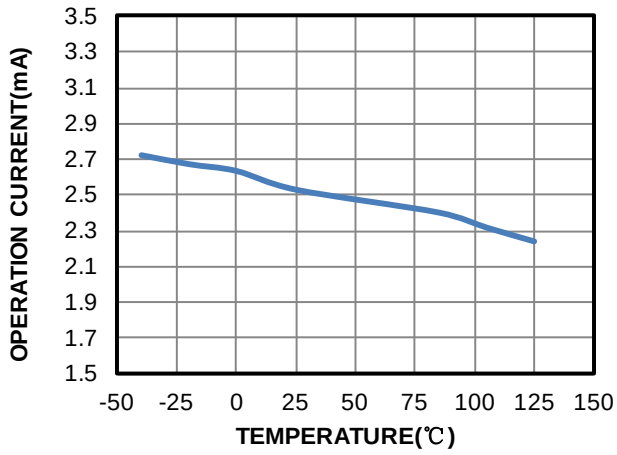
Breakdown Voltage vs. Temperature



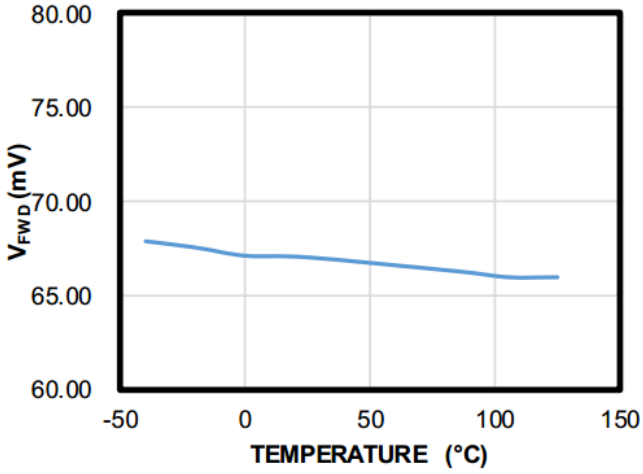
VDD Rising vs. Temperature



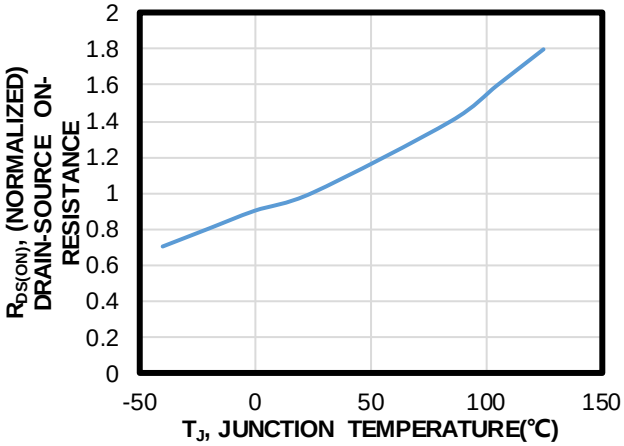
Operation Current vs. Temperature



V_{FWD} vs. Temperature



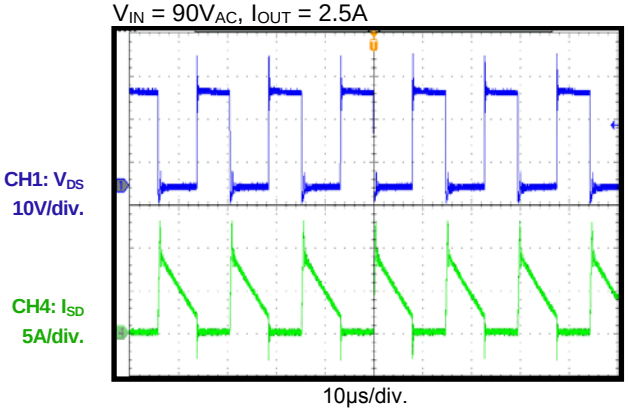
$R_{DS(ON)}$ vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS

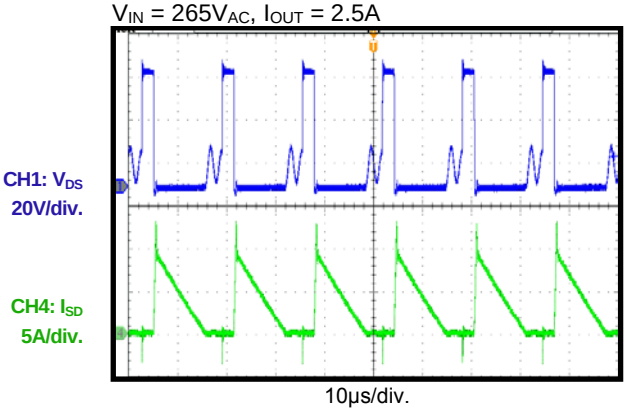
Operation in 30W Flyback Application

V_{IN} = 90V_{AC}, I_{OUT} = 2.5A



Operation in 30W Flyback Application

V_{IN} = 265V_{AC}, I_{OUT} = 2.5A



BLOCK DIAGRAM

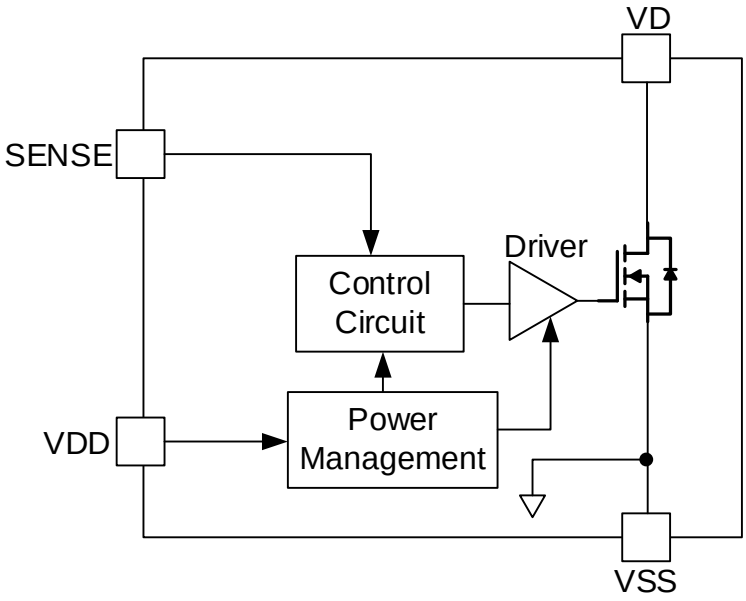


Figure 1: Functional Block Diagram

OPERATION

The MP6910A supports operation in flyback converters. The control circuitry controls the gate in forward mode and turns the gate off when the MOSFET current is fairly low.

Blanking

The control circuitry contains a blanking function. When the integrated MOSFET turns on, the circuitry ensures that the on state lasts for a specific amount of time. The turn-on blanking time is t_{MIN} (~1.0µs), which determines the minimum on time. During the turn-on blanking period, the turn-off threshold is not blanked completely, but changes the threshold voltage to about +50mV (instead of -30mV). This ensures that MP6910A can always be turned off, even during the turn-on blanking period (although it does so more slowly).

Under-Voltage Lockout (UVLO)

When the VDD is below the under-voltage lockout (UVLO) threshold, the MP6910A is in sleep mode, and the integrated MOSFET remains off.

Basic Operation

The basic operations of a flyback converter with the MP6910A are listed below.

1. Turn-on phase: The switch current first flows through the body diode of the integrate MOSFET, which generates a negative V_{DS} across it (less than -500mV). The voltage is much smaller than the turn-on threshold of the control circuitry (-65mV), which turns on the integrated MOSFET after a t_{Don} (100ns) turn-on delay (see Figure 2).

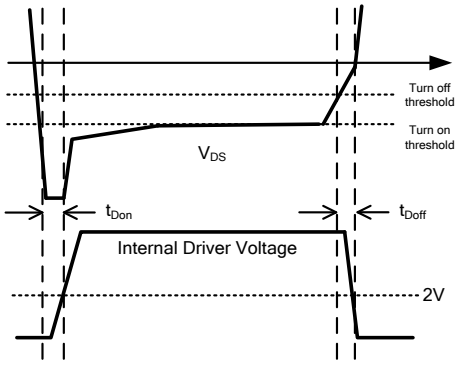


Figure 2: Turn-on and Turn-off Delay

2. Conducting phase: When the integrated MOSFET turns on, V_{DS} starts to rise according to its on resistance. Once V_{DS} rises above the turn-on threshold (-65mV), the control circuitry regulates the gate voltage of the integrated MOSFET to keep V_{DS} around $-V_{FWD}$ (-65mV), even when the current through the switch is fairly small. This function can make the internal driver voltage fairly low when the MOSFET is turned off to quicken the turn-off speed. This function is still active during the turn-on blanking period, which means that the integrated MOSFET can still be turned off even with a very small duty.

   Figure 3 shows the synchronous rectification operation at heavy-load condition. Due to the high current, the internal driver voltage is saturated first. After V_{DS} rises above $-V_{FWD}$, the driver voltage decreases to adjust the V_{DS} to a typical $-V_{FWD}$.

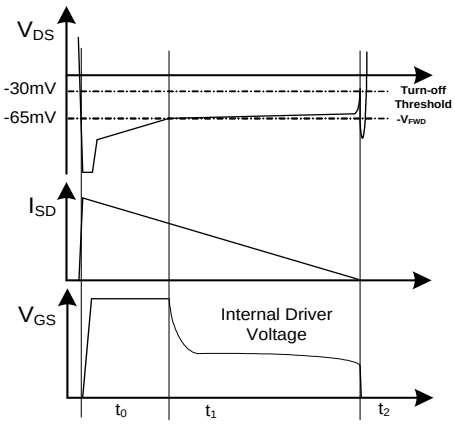


Figure 3: Synchronous Rectification Operation at Heavy Load

Figure 4 shows the synchronous rectification operation at light-load condition. Due to the low current, the driver voltage never saturates, but begins to decrease once the integrated MOSFET is turned on and adjusts V_{DS}.

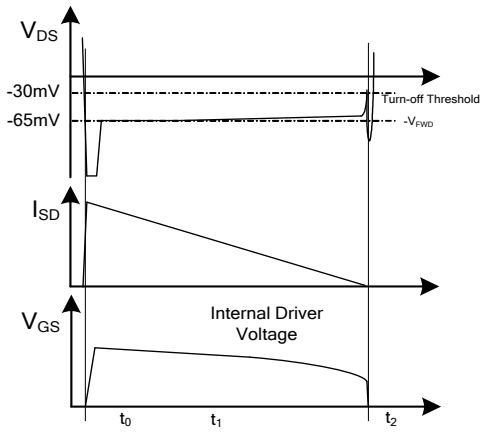


Figure 4: Synchronous Rectification Operation at Light Load

3. Turn-off phase: When V_{DS} rises to trigger the turn-off threshold (-30mV), the driver voltage of the switch is pulled low after t_{Doff} (30ns) of turn-off delay time by the control circuitry (see Figure 2). Similar with the turn-on phase, a 200ns blanking time is added after the switch turns off to avoid an erroneous trigger.

Light-Load Latch-Off Function

The gate driver of integrated MOSFET in the MP6910A is latched to save the driver loss at light-load condition to improve efficiency. The light-load enter pulse width (t_{LL}) is fixed internally (~2.2μs). When the synchronous power switch conducting period is lower than t_{LL} for longer than light-load enter delay ($t_{LL\ -Delay}$), MP6910A enters light-load mode and latches off the integrated MOSFET (see Figure 5).

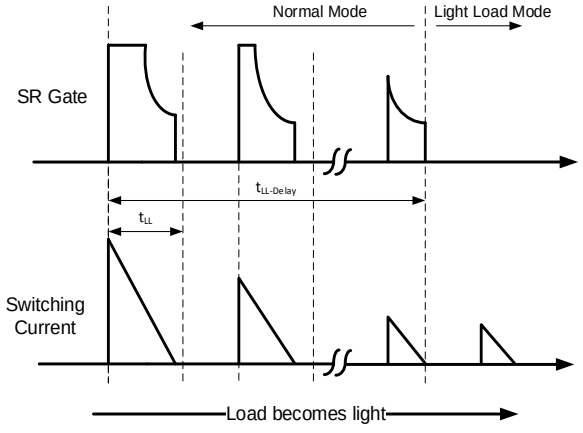


Figure 5: Entering Light-Load Mode

During light-load mode, MP6910A monitors the integrated MOSFET body diode conducting period by sensing V_{DS}. When V_{DS} exceeds the light-load mode exit pulse width threshold (V_{LL-DS}), MP6910A considers the integrated MOSFET body diode conducting time to be completed. If the MOSFET body diode conduction time is longer than t_{LL} + t_{LL-H} (t_{LL-H}, light-load enter pulse-width hysteresis), light-load mode finishes and the integrated MOSFET of MP6910A is unlatched to restart synchronous rectification (see Figure 6).

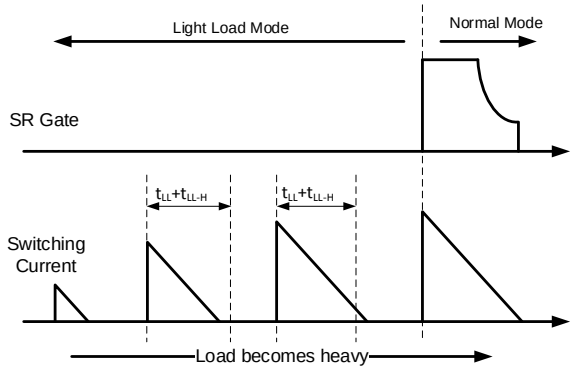


Figure 6: Exiting Light-Load Mode

External Resistor on SENSE

Over-voltage conditions may lead to damage to the device, so there must be appropriate application design to guarantee safe operation, especially on the high voltage pin.

One common over-voltage condition is when the body diode of the SR MOSFET is turned on, as the forward voltage drop may exceed the negative rating on the SENSE pin. In this case, it is recommended to place an external resistor about 300Ω to 1kΩ between SENSE and the MOSFET drain. But a resistor greater than 1kΩ is also not recommended for the sampling accuracy of VDS.

Typical System Implementations

Figure 7 shows the typical system implementation for the IC supply derived from output voltage, which is available in low-side rectification. The output voltage is recommended to be in the VDD range (from 8.3V to 24V).

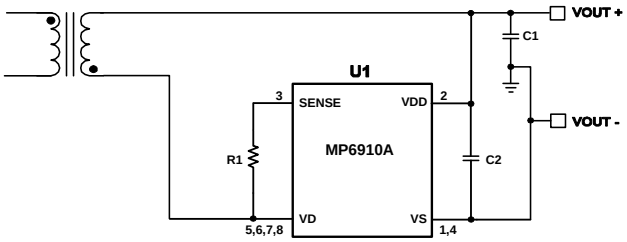


Figure 7: IC Supply Derived Directly from Output Voltage

If the output voltage is out of the VDD range or high-side rectification is used, it is recommended to use an auxiliary winding from the power transformer for the IC supply (see Figure 8 and Figure 9).

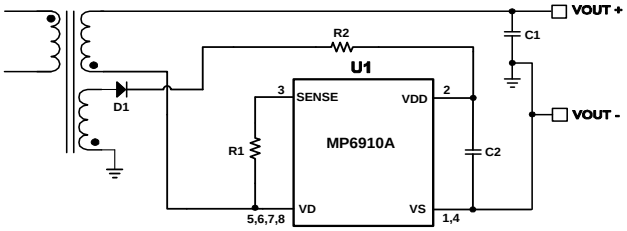


Figure 8: IC Supply Derived from Auxiliary Winding in Low-Side Rectification

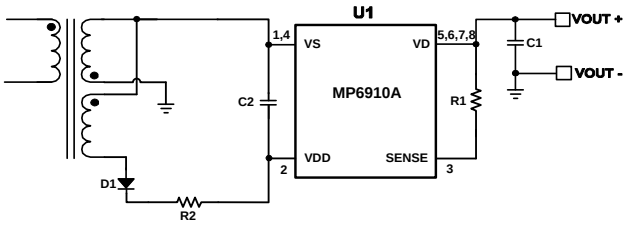


Figure 9: IC Supply Derived from Auxiliary Winding in High-Side Rectification

There is another non-auxiliary winding solution for the IC supply, which uses an external LDO circuit from the secondary transformer winding (see Figure 10 and Figure 11). Compared with an auxiliary winding for the IC supply, this solution has a slightly higher power loss, which is dissipated on the LDO circuit, especially when the secondary winding voltage is high.

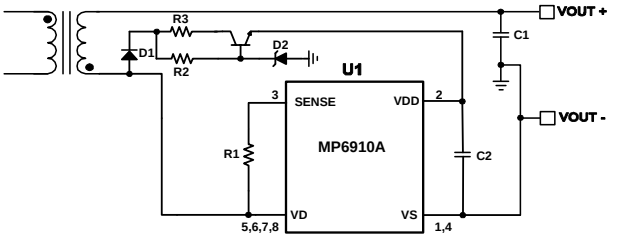


Figure 10: IC Supply Derived from Secondary Winding in Low-Side Rectification

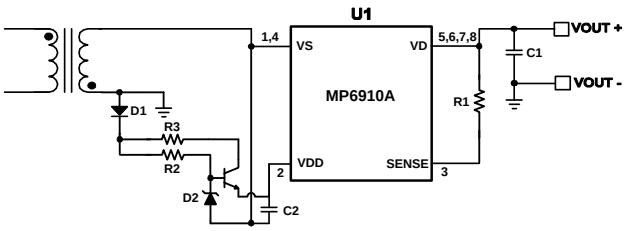


Figure 11: IC Supply Derived from Secondary Winding in High-Side Rectification

Maximum Output Current

The allowed temperature rise of the MP6910A limits the maximum output current that it can handle. The temperature rise is determined by its own power loss. Generally, for a universal input adapter, the recommended rated output current for MP6910A is 2.5A. For certain designs, the power loss of MP6910A can be calculated to determine the maximum output current.

The power loss of MP6910A can be separated into several parts: controller consumption, integrated MOSFET conduction loss, and so on. If MP6910A works in continuous conduction mode (CCM), reverse-recovery loss of the integrated MOSFET must also be considered. Each part of the loss can be calculated with Equation (1), Equation (2), and Equation (3), respectively:

$$P_{LOSS\_Controller} = V_{DD} \times I_{DD} \quad (1)$$

$$P_{LOSS\_SR\_Conduction} = f_{SW} \times \int_{0}^{t_{s\_on}} V_{SR\_SD}(t) \times I_{SR\_SD}(t)dt \quad (2)$$

$$P_{LOSS\_SR\_RR} = \frac{1}{2} \times V_{DS} \times I_{rr} \times t_{rr} \times f_{SW} \quad (3)$$

Where V_{DD} is the voltage and I_{DD} is the current of MP6910A. t_{s_on} is the SR on period, V_{SR_SD} is the voltage drop from the SR, and I_{SR_SD} is the current flowing through the SR. I_{rr} is the peak reverse current and t_{rr} is reverse recovery time.

The total loss of MP6910A (P_{LOSS}) is the sum of the above losses. If an RC snubber is adopted, the power loss caused by this snubber should also be taken into consideration.

The junction and case temperature rises can be calculated with the thermal resistance of the junction-to-ambient temperature (θ_{JA}) and junction-to-case temperature (θ_{JC}).

The junction temperature must be within ABS (typically 150°C). Calculate ΔT_{JA} and ΔT_{JC} with Equation (4) and Equation (5):

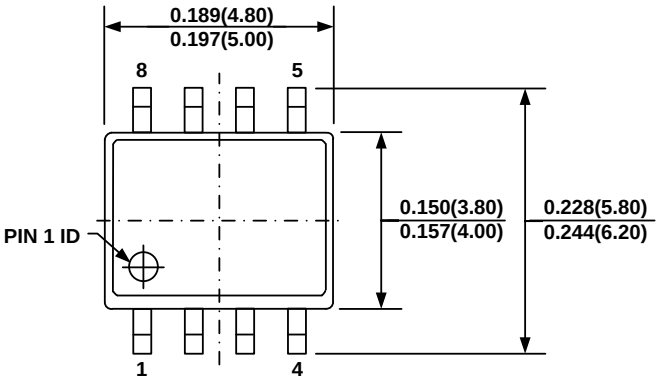
$$\Delta T_{JA} = P_{LOSS} \times \theta_{JA} \quad (4)$$

$$\Delta T_{JC} = P_{LOSS} \times \theta_{JC} \quad (5)$$

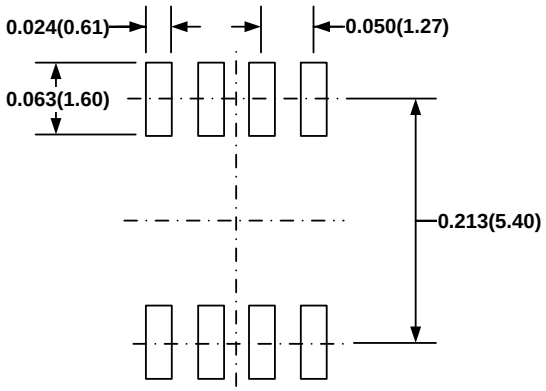
The thermal resistance can be reduced by laying thicker copper layer, placing more thermal dissipation vias and adopting heatsinks and so on. The real maximum output current can be set by considering the real tested data.

PACKAGE INFORMATION

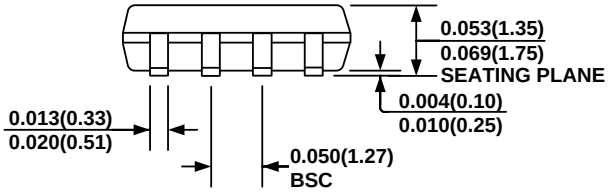
SOIC-8



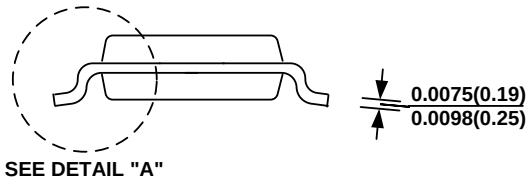
TOP VIEW



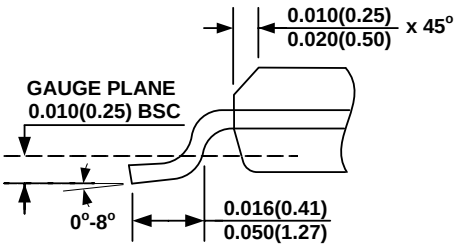
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

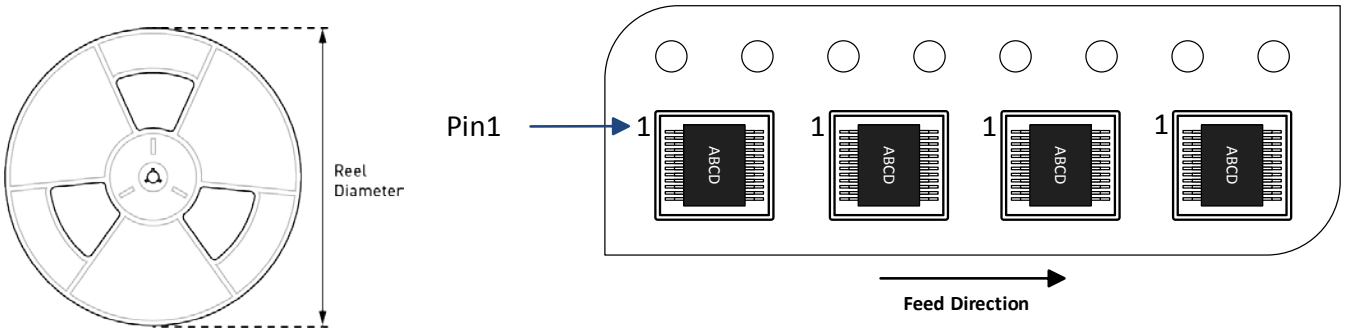


DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/Reel	Quantity/Tube	Quantity/Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6910AGS–Z	SOIC-8	2500	100	N/A	13 in.	12mm	8mm

Revision History

Revision #	Revision Date	Description	Pages Updated
1.2	05/25/2020	Some min/max specifications are added in the EC table.	Page 4