DESCRIPTION

The MP6902 is a Low-Drop Diode Emulator IC for Flyback converters which combined with an external switch replaces Schottky rectification diodes for high efficiency. The chip regulates the forward drop of an external switch to about 70mV and switches it off as soon as the voltage becomes negative. MP6902 has a light-load sleep mode that reduces the quiescent current to <300uA.

FEATURES

- Supports DCM and Quasi-Resonant Flyback Converters
- Works with 12V Standard and 5V Logic Level FETS
- Compatible with Energy Star, 1W Standby Requirements
- $V_{DD}$ Range From 8V to 24V
- 70mV $V_{DS}$ Regulation Function (1)
- Fast Turn-off Total Delay of 20ns
- Max 400kHz Switching Frequency
- Light Load Mode Function (1) with <300μA Quiescent Current
- Supports High-side and Low-side Rectification
- Power Savings of Up to 1.5W in a Typical Notebook Adapter

APPLICATIONS

- Industrial Power Systems
- Distributed Power Systems
- Battery Powered Systems
- Flyback Converters

Notes:

1) Related issued patent: US Patent US8,067,973; US8,400,790. CN Patent ZL201010504140.4; ZL200910059751.X. Other patents pending.

TYPICAL APPLICATION
**ORDERING INFORMATION**

<table>
<thead>
<tr>
<th>Part Number*</th>
<th>Package</th>
<th>Top Marking</th>
</tr>
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<tbody>
<tr>
<td>MP6902DS</td>
<td>SOIC8</td>
<td>MP6902DS</td>
</tr>
</tbody>
</table>

* For Tape & Reel, add suffix –Z (e.g. MP6902DS–Z); For RoHS Compliant Packaging, add suffix –LF; (e.g. MP6902DS–LF–Z)

**PACKAGE REFERENCE**

**TOP VIEW**

ABSOLUTE MAXIMUM RATINGS (2)

- $V_{DD}$ to $V_{SS}$: $-0.3V$ to $+27V$
- $PGND$ to $V_{SS}$: $-0.3V$ to $+0.3V$
- $V_G$ to $V_{SS}$: $-0.3V$ to $V_{CC}$
- $V_D$ to $V_{SS}$: $-0.7V$ to $+180V$
- $LL$, $EN$ to $V_{SS}$: $-0.3V$ to $+6.5V$
- Continuous Power Dissipation ($T_A=+25°C$) (3) 1.4W
- Junction Temperature: $150°C$
- Lead Temperature (Solder): $260°C$
- Storage Temperature: $-55°C$ to $+150°C$

**Recommended Operation Conditions** (4)

- $V_{DD}$ to $V_{SS}$: 8V to 24V
- Operating Junction Temp. ($T_J$): $-40°C$ to $+125°C$

**Thermal Resistance** (5) $\theta_{JA}$ $\theta_{JC}$

- SOIC8: $90 \ldots 45 °C/W$

**Notes:**

2) Exceeding these ratings may damage the device.

3) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J(MAX)$, the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX) = (T_J(MAX) - T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

4) The device is not guaranteed to function outside of its operating conditions.

5) Measured on JESD51-7, 4-layer PCB.
ELECTRICAL CHARACTERISTICS
V<sub>DD</sub> = 12V, T<sub>A</sub> = +25°C, unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
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<tbody>
<tr>
<td>V&lt;sub&gt;DD&lt;/sub&gt; Voltage Range</td>
<td></td>
<td></td>
<td>8</td>
<td>24</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;DD&lt;/sub&gt; UVLO Rising</td>
<td>C&lt;sub&gt;LOAD&lt;/sub&gt;=5nF, F&lt;sub&gt;SW&lt;/sub&gt;=100kHz</td>
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<td>5.0</td>
<td>6.0</td>
<td>7.0</td>
<td>V</td>
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<tr>
<td>V&lt;sub&gt;DD&lt;/sub&gt; UVLO Hysteresis</td>
<td>I&lt;sub&gt;CC&lt;/sub&gt;</td>
<td></td>
<td>0.8</td>
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<td>1.2</td>
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<td>Operating Current</td>
<td>I&lt;sub&gt;CC&lt;/sub&gt;</td>
<td>C&lt;sub&gt;LOAD&lt;/sub&gt;=5nF, F&lt;sub&gt;SW&lt;/sub&gt;=100kHz</td>
<td>8</td>
<td>10</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Quiescent Current</td>
<td>I&lt;sub&gt;q&lt;/sub&gt;</td>
<td>V&lt;sub&gt;SS&lt;/sub&gt;-V&lt;sub&gt;D&lt;/sub&gt;=0.5V</td>
<td>2</td>
<td>3</td>
<td></td>
<td>mA</td>
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<td>Shutdown Current</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt;=4V</td>
<td></td>
<td>210</td>
<td>255</td>
<td>375</td>
<td>µA</td>
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<tr>
<td>Light-load Mode Current</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt;=20V, EN=0V</td>
<td></td>
<td>290</td>
<td>380</td>
<td>440</td>
<td>µA</td>
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<tr>
<td>Thermal Shutdown</td>
<td></td>
<td></td>
<td>150</td>
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<td>°C</td>
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<tr>
<td>Thermal Shutdown Hysteresis</td>
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<td></td>
<td>30</td>
<td></td>
<td></td>
<td>°C</td>
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<tr>
<td>Enable UVLO Rising</td>
<td></td>
<td></td>
<td>1.1</td>
<td>1.5</td>
<td>1.9</td>
<td>V</td>
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<tr>
<td>Enable UVLO Hysteresis</td>
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<td></td>
<td>0.2</td>
<td>0.4</td>
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<td>V</td>
</tr>
<tr>
<td>Internal Pull-up Current On EN Pin</td>
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<td></td>
<td>10</td>
<td>15</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>V&lt;sub&gt;SS&lt;/sub&gt;–V&lt;sub&gt;D&lt;/sub&gt; Forward Voltage</td>
<td>V&lt;sub&gt;fwd&lt;/sub&gt;</td>
<td></td>
<td>55</td>
<td>70</td>
<td>85</td>
<td>mV</td>
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<tr>
<td>Turn-on Delay</td>
<td>T&lt;sub&gt;Don&lt;/sub&gt;</td>
<td>C&lt;sub&gt;LOAD&lt;/sub&gt;=5nF</td>
<td></td>
<td>150</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Input Bias Current On V&lt;sub&gt;D&lt;/sub&gt; Pin</td>
<td>T&lt;sub&gt;MIN&lt;/sub&gt;</td>
<td>V&lt;sub&gt;D&lt;/sub&gt;=180V</td>
<td></td>
<td>1</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>Light-load Mode Exit Pulse Width Threshold (V&lt;sub&gt;DS&lt;/sub&gt;)</td>
<td>V&lt;sub&gt;LL-DS&lt;/sub&gt;</td>
<td></td>
<td>-400</td>
<td>-250</td>
<td>-150</td>
<td>mV</td>
</tr>
<tr>
<td>Light-load Mode Enter Pulse Width Threshold (V&lt;sub&gt;GS&lt;/sub&gt;)</td>
<td>V&lt;sub&gt;LL-GS&lt;/sub&gt;</td>
<td></td>
<td>1.0</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>GATE DRIVER SECTION</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;G&lt;/sub&gt; (Low)</td>
<td>I&lt;sub&gt;LOAD&lt;/sub&gt;=1mA</td>
<td></td>
<td>0.05</td>
<td>0.1</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;G&lt;/sub&gt; (High)</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt;&gt;17V</td>
<td></td>
<td>13</td>
<td>14</td>
<td>15</td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;DD&lt;/sub&gt;&lt;17V</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt;&lt;17V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Turn-off Threshold (V&lt;sub&gt;SS&lt;/sub&gt;-V&lt;sub&gt;D&lt;/sub&gt;)</td>
<td>V&lt;sub&gt;D&lt;/sub&gt;=V&lt;sub&gt;SS&lt;/sub&gt;</td>
<td></td>
<td>30</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Turn-off Propagation Delay</td>
<td>V&lt;sub&gt;D&lt;/sub&gt;=V&lt;sub&gt;SS&lt;/sub&gt;, C&lt;sub&gt;LOAD&lt;/sub&gt;=5nF, R&lt;sub&gt;GATE&lt;/sub&gt;=0Ω</td>
<td></td>
<td>15</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Turn-off Total Delay</td>
<td>V&lt;sub&gt;D&lt;/sub&gt;=V&lt;sub&gt;SS&lt;/sub&gt;, C&lt;sub&gt;LOAD&lt;/sub&gt;=10nF, R&lt;sub&gt;GATE&lt;/sub&gt;=0Ω</td>
<td></td>
<td>T&lt;sub&gt;Doff&lt;/sub&gt;</td>
<td>35</td>
<td>45</td>
<td></td>
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<tr>
<td>Pull Down Impedance</td>
<td></td>
<td></td>
<td>1</td>
<td>2</td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>Pull Down Current (6)</td>
<td>3V &lt;V&lt;sub&gt;G&lt;/sub&gt;&lt;10V</td>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td>A</td>
</tr>
</tbody>
</table>

Notes:
6) Guaranteed by Design and Characterization.
## PIN FUNCTIONS

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PGND</td>
<td>Power Ground, return for driver switch</td>
</tr>
<tr>
<td>2</td>
<td>EN</td>
<td>Enable pin, active high</td>
</tr>
<tr>
<td>3</td>
<td>LL</td>
<td>Light load timing setting. Connect a resistor to set the light load timing.</td>
</tr>
<tr>
<td>4</td>
<td>VD</td>
<td>FET drain voltage sense</td>
</tr>
<tr>
<td>5</td>
<td>VSS</td>
<td>Ground, also used as reference for VD</td>
</tr>
<tr>
<td>6</td>
<td>VDD</td>
<td>Supply Voltage</td>
</tr>
<tr>
<td>7</td>
<td>NC</td>
<td>No connection</td>
</tr>
<tr>
<td>8</td>
<td>VG</td>
<td>Gate drive output</td>
</tr>
</tbody>
</table>
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{DD} = 12V$, unless otherwise noted.

**$V_{FWD}$ vs. Temperature**

**Turn off threshold vs. Temperature**

**Quiescent Current vs. Temperature**

**Shutdown Current vs. Temperature**

**$V_{DD}$ UVLO Rising vs. Temperature**

**Operation in 90W Flyback Application**

- $V_{IN}=250Vac, I_{OUT}=1A$

**Operation in 90W Flyback Application**

- $V_{IN}=250Vac, I_{OUT}=4.7A$

Notes:

7) See Figure 13 for the test circuit.
Figure 1—Function Block Diagram
OPERATION

The MP6902 supports operation in DCM and Quasi-Resonant Flyback converters. The control circuitry controls the gate in forward mode and will turn the gate off when the MOSFET current is fairly low.

Blanking

The control circuitry contains a blanking function. When it pulls the MOSFET on/off, it makes sure that the on/off state at least lasts for some time. The turn on blanking time is ~1.6us, which determines the minimum on-time. During the turn on blanking period, the turn off threshold is not totally blanked, but changes the threshold voltage to ~+50mV (instead of -30mV). This assures that the part can always be turned off even during the turn on blanking period. (Albeit slower)

VD Clamp

Because \( V_D \) can go as high as 180V, a High-Voltage JFET is used at the input. To avoid excessive currents when \( V_g \) goes below -0.7V, a small resistor is recommended between \( V_D \) and the drain of the external MOSFET.

Under-Voltage Lockout (UVLO)

When the VDD is below UVLO threshold, the part is in sleep mode and the \( V_g \) pin is pulled low by a 10k\( \Omega \) resistor.

Enable pin

If EN is pulled low, the part is in sleep mode.

Thermal shutdown

If the junction temperature of the chip exceeds 170\(^\circ\)C, the \( V_g \) will be pulled low and the part stops switching. The part will return to normal function after the junction temperature has dropped to 120\(^\circ\)C.

Thermal Design

If the dissipation of the chip is higher than 100mW due to switching frequencies above 100kHz.

Turn-on Phase

When the synchronous MOSFET is conducting, current will flow through its body diode which generates a negative \( V_d \) across it. Because this body diode voltage drop (<-500mV) is much smaller than the turn on threshold of the control circuitry (-70mV), which will then pull the gate driver voltage high to turn on the synchronous MOSFET after about 150ns turn on delay (Defined in Figure 2).

As soon as the turn on threshold (-70mV) is triggered, a blanking time (Minimum on-time: ~1.6us) will be added during which the turn off threshold will be changed from -30mV to +50mV. This blanking time can help to avoid error trigger on turn off threshold caused by the turn on ringing of the synchronous MOSFET.

![Figure 2—Turn on and Turn off delay](image-url)

Conducting Phase

When the synchronous MOSFET is turned on, \( V_d \) becomes to rise according to its on resistance, as soon as \( V_d \) rises above the turn on threshold (-70mV), the control circuitry stops pulling up the gate driver which leads the gate voltage is pulled down by the internal pull-down resistance (10k\( \Omega \)) to larger the on resistance of synchronous MOSFET to ease the rise of \( V_d \). By doing that, \( V_d \) is adjusted to be around -70mV even when the current through the MOS is fairly small, this function can make the driver voltage fairly low when the synchronous MOSFET is turned off to fast the turn off speed (this function is still active during turn on blanking time which means the gate driver could still be turned off even with very small duty of the synchronous MOSFET).
**Turn-off Phase**

When Vds rises to trigger the turn off threshold (-30mV), the gate voltage is pulled to low after about 20ns turn off delay (defined in Figure 2) by the control circuitry. Similar with turn-on phase, a 200ns blanking time is added after the synchronous MOSFET is turned off to avoid error trigger.

Figure 3 shows synchronous rectification operation at heavy load condition. Due to the high current, the gate driver will be saturated at first, during which the gate driver voltage is kept at ~2V lower than $V_{DD}$ (when $V_{DD}$>16V, gate driver will be internal clamped at 14V). After Vds goes to above -70mV, gate driver voltage decreases to adjust the Vds to typical -70mV.

Figure 4 shows synchronous rectification operation at light load condition. Due to the low current, the gate driver voltage never saturates but begins to decrease as soon as the synchronous MOSFET is turned on and adjust the Vds.

![Figure 3—Synchronous Rectification Operation at heavy load](image)

![Figure 4—Synchronous Rectification Operation at light load](image)

**Light-load Latch-off Function**

The gate driver of MP6902 is latched to save the driver loss at light-load condition to improve efficiency. When the synchronous MOSFET’s conducting period keeps lower than light load timing ($T_{LL}$) for longer than the light-load-enter delay ($T_{LL-Delay}$), MP6902 enters light-load mode and latches off the gate driver. Here the synchronous MOSFET’s conducting period is from turn on of the gate driver to the moment when $V_{GS}$ drops to below 1V ($V_{LL-GS}$). During light-load mode, MP6902 monitors the synchronous MOSFET’s body diode conducting period by sensing the time duration of the $V_{DS}$ below -250mV($V_{LL-DS}$). If it is longer than $T_{LL}+T_{LL-H}$ ($T_{LL-H}$, light-load-enter pulse width hysteresis), the light-load mode is finished and gate driver of MP6902 is unlatched to restart the synchronous rectification.

![Figure 5—Drain-Source and Gate Driver voltage on SR MOFET](image)
For MP6902, the light load enter timing (T_{LL}) is programmable by connecting a resistor (R_{LL}) on LL pin, by monitoring the LL pin current (the LL pin voltage keeps at ~2V internally), T_{LL} is set as following:

\[ T_{LL} \approx R_{LL} (k\Omega) \times \frac{2.2 \mu s}{100k\Omega} \]

**SR MOSFET Selection and Driver Ability**

The Power Mosfet selection proved to be a trade off between Ron and Qg. In order to achieve high efficiency, the Mosfet with smaller Ron is always preferred, while the Qg is usually larger with smaller Ron, which makes the turn-on/off speed lower and lead to larger power loss. For MP6902, because Vds is regulated at ~70mV during the driving period, the Mosfet with too small Ron is not recommend, because the gate driver may be pulled down to a fairly low level with too small Ron when the Mosfet current is still fairly high, which make the advantage of the low Ron inconspicuous.

Figure 6 shows the typical waveform of QR flyback. Assume 50% duty cycle and the output current is I_{OUT}.

To achieve fairly high usage of the Mosfet’s Ron, it is expected that the Mosfet be fully turned on at least 50% of the SR conduction period:

\[ V_{ds} = -Ic \times Ron = -2 \times I_{OUT} \times Ron \leq -V_{fwd} \]

Where V_{ds} is Drain-Source voltage of the Mosfet and V_{fwd} is the forward voltage threshold of MP6902, which is ~70mV.

So the Mosfet’s Ron is recommended to be no lower than ~35/I_{OUT} (m\Omega). (For example, for 5A application, the Ron of the Mosfet is recommended to be no lower than 7m\Omega)

Figure 7 shows the corresponding total delay during turn-on period (t_{Total}, see Figure 2) with driving different Qg Mosfet by MP6902. From Figure 7, with driving a 120nC Qg Mosfet, the driver ability of MP6902 is able to pull up the gate driver voltage of the Mosfet to ~5V in 300ns as soon as the body diode of the Mosfet is conducting, which greatly save the turn-on power loss in the Mosfet’s body diode.

Figure 8 shows the typical system implementation for the IC supply derived from output voltage, which is available in low-side rectification and the output voltage is recommended to be in the V_{DD} range of MP6902 (from 8V to 24V).

If output voltage is out of the V_{DD} range of MP6902 or high-side rectification is used, it is recommended to use an auxiliary winding from the power transformer for the IC supply, which is shown in Figure 9 and Figure.10.
There is another non-auxiliary winding solution for the IC supply, which uses an external LDO circuit from the secondary transformer winding. See Figure.11 and Figure.12, compared with using auxiliary winding for IC supply, this solution has a bit higher power loss which is dissipate on the LDO circuit especially when the secondary winding voltage is high.
Figure 13—MP6902 for Secondary Synchronous Controller in 90W Flyback Application
PACKAGE INFORMATION

SOIC8

TOP VIEW

RECOMMENDED LAND PATTERN

FRONT VIEW

SIDE VIEW

DETAIL "A"

NOTE:
1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

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