MP6655

18V, 2.5A, Single-Phase BLDC Fan Driver with Integrated MOSFETs and Hall Sensor

DESCRIPTION

The MP6655 is a single-phase brushless DC (BLDC) motor driver with integrated power MOSFETs and a Hall sensor. It drives single-phase BLDC motors with up to 2.5A of peak phase current. The input voltage (V_{IN}) ranges from 3.3V to 18V.

The MP6655 controls the motor speed through the pulse-width modulation (PWM) signal, with a PWM input frequency ranging from 60Hz to 100kHz.

The MP6655 has a rotational speed detector feature. The rotational speed detector (the FG/RD pin) is an open-drain output. It outputs a high or low voltage relative to the internal Hall comparator's output.

Rich protections include input over-voltage protection (OVP), under-voltage lockout (UVLO), locked-rotor protection, over-current protection (OCP), and thermal shutdown protection.

The MP6655 is available in TSOT23-6-SL and TSOT23-6-L packages.

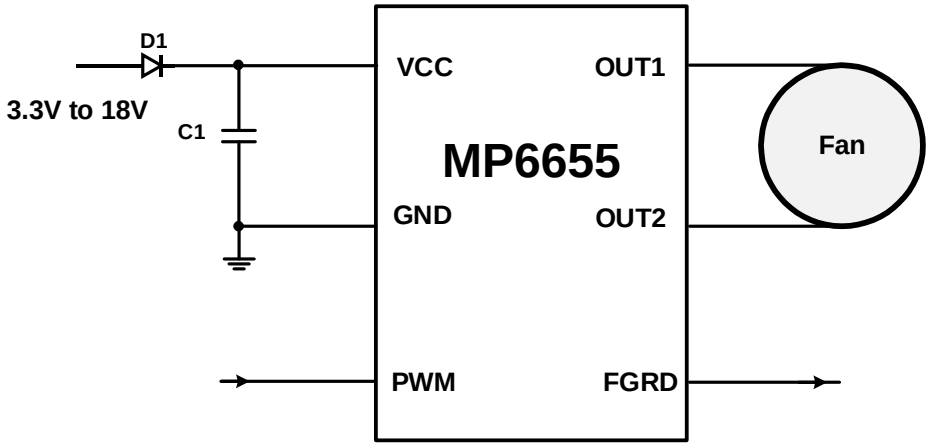
FEATURES

- 3.3V to 18V Operating Input Voltage (V_{IN}) Range
- 2.5A Peak Phase Current
- On-Chip Hall Sensor
- Integrated Power MOSFETs: Total 250mΩ High-Side MOSFETs (HS-FETs) and Low-Side MOSFETs (LS-FETs)
- 60Hz to 100kHz Pulse-Width Modulation (PWM) Input Range
- Curve Configurations
- Configurable Minimum Speed and Starting Duty Cycle
- Closed-Loop or Open-Loop Speed Control
- Configurable Soft-Start Time (t_{SS})
- Power-Save Mode
- 27kHz PWM Output Frequency
- Standby Mode
- Maximum Peak Current Protection
- Over-Voltage Protection (OVP)
- Locked-Rotor Protection
- Over-Current Protection (OCP)
- Thermal Shutdown with Auto-Recovery
- Selectable FG and RD Output
- Available in TSOT23-6-SL and TSOT23-6-L Packages

APPLICATIONS

- Server Fans
- Brushless DC (BLDC) Motors
- General 1-Phase Fans

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP6655GJS-xxxx**	TSOT23-6-SL	*See Below*	1
MP6655GJL-xxxx	TSOT23-6-L	*See Below*	1

* * For Tape & Reel, add suffix -Z (e.g. MP6655GJS-xxxx-Z).

** “xxxx” is the configuration code identifier. The first four digits of the suffix (xxxx) can be a hexadecimal value between 0 and F. The default code is “0000”. Work with an MPS FAE to create a unique number for non-default options.

TOP MARKING (MP6655GJS-xxxx)

CAGY
LLL

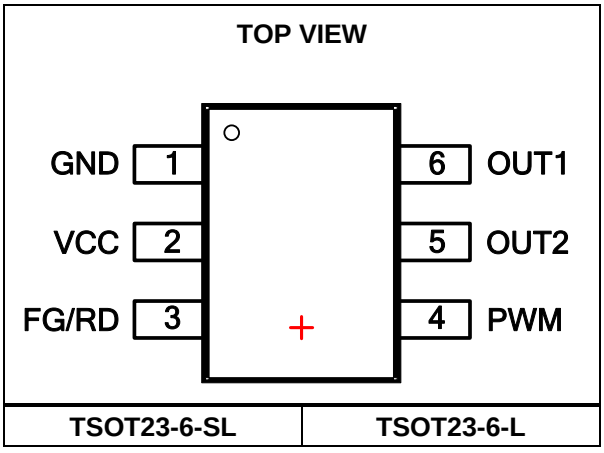
CAG: Product code
Y: Year code
LLLL: Lot number

TOP MARKING (MP6655GJL-xxxx)

| CAGY

CAG: Product code
Y: Year code

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	GND	**Ground.**
2	VCC	**Input voltage supply.** The VCC pin must be bypassed locally.
3	FG/RD	**Rotational speed detector (default) or locked-rotor indication (RD) signal.** The FG/RD pin is an open-drain output. FG/RD must be pulled up externally.
4	PWM	**Pulse-width modulation (PWM) input for rotational speed control.** The pulse-width modulation (PWM) frequency is from 60Hz to 100kHz.
5	OUT2	**Motor driver output 2.**
6	OUT1	**Motor driver output 1.**

ABSOLUTE MAXIMUM RATINGS (1)

V_{CC}, V_{PWM}, $V_{FG/RD}$ ..... -0.3V to +24V
$V_{OUT1/2}$ ..... -0.3V to V_{CC} + 0.3V
Junction temperature (T_J) ..... 150°C
Lead temperature ..... 260°C
Continuous power dissipation (T_A = 25°C) (2) 1.25W
Storage temperature ..... -60°C to +150°C
Operating temperature ..... -40°C to +125°C

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged-device model (CDM) ..... ±2kV

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 3.3V to 18V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TSOT23-6 ..... 100 ..... 55... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on a JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{CC} = 12V, T_J = -40°C to 125°C, unless otherwise noted.

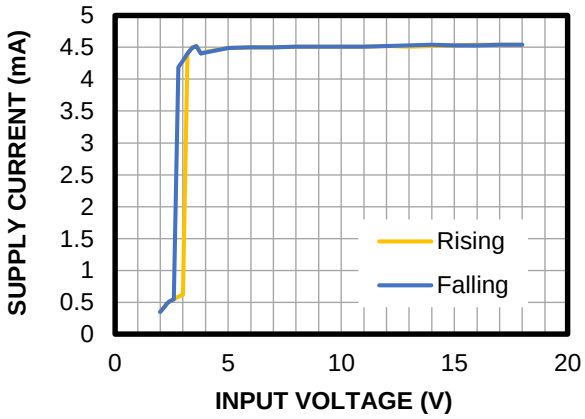
Parameters	Symbol	Condition	Min	Typ	Max	Units
Input under-voltage lockout (UVLO) rising threshold	V_{UVLO}			3	3.2	V
Input UVLO hysteresis				285		mV
Operating supply current	I_{CC}			4.5	6	mA
Standby current	I_{ST}	PWM stays low		35	50	μA
Pulse-width modulation (PWM) input high voltage	V_{PWMH}		2			V
PWM input low voltage	V_{PWML}				0.7	V
PWM input internal pull-up resistance				24		kΩ
Switching frequency	f_{SW}		25.92	27	28.08	kHz
High-side MOSFET (HS-FET) on resistance	R_{HS_ON}			220		mΩ
Low-side MOSFET (LS-FET) on resistance	R_{LS_ON}			130		mΩ
Over-current protection (OCP) threshold	I_{OCP}		2.2	2.5	2.8	A
Short-circuit protection (SCP) threshold	I_{SCP}			4		A
FG output low-level voltage	V_{FG_L}	$I_{FG/RD}$ = 3mA			0.35	V
Soft-on commutation angle	θ_{S_ON}	SON_ANG[4:0] = 0x10		45		deg
Soft-off commutation angle	θ_{S_OFF}	SOFF_ANG[4:0] = 0x10		45		deg
Locked-rotor detection time	t_{RD}			0.6		s
Locked-rotor retry time	t_{RE}	LOCK_SEL[1:0] = 10		3.6		s
Input over-voltage protection (OVP) threshold	V_{OVP}			19	20	V
OVP hysteresis	V_{OVP_HYS}			2		V
Thermal shutdown threshold	T_{TSD}			150		°C
Thermal shutdown hysteresis	T_{TSD_HYS}			25		°C
Minimum recommended magnetic field	B_{MIN}		-2		2	mT

TYPICAL CHARACTERISTICS

V_{CC} = 12V, T_J = -40°C to 125°C, unless otherwise noted.

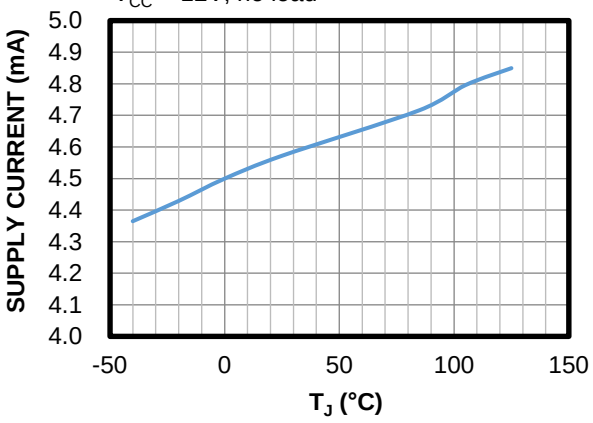
Supply Current vs. Input Voltage

V_{CC} = 2-18V, no load, T_J = 25°C

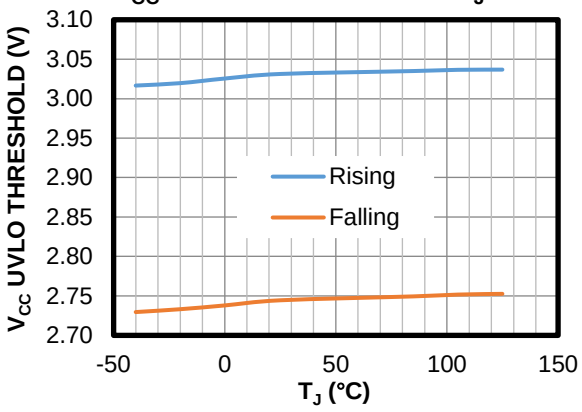


Supply Current vs. T_J

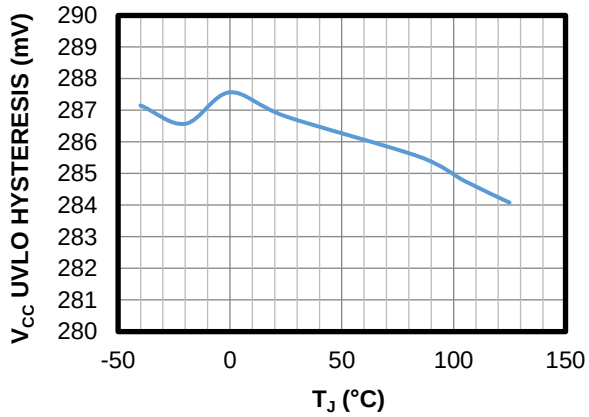
V_{CC} = 12V, no load



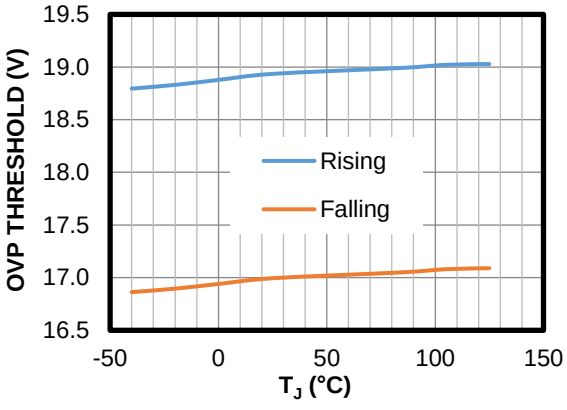
V_{CC} UVLO Threshold vs. T_J



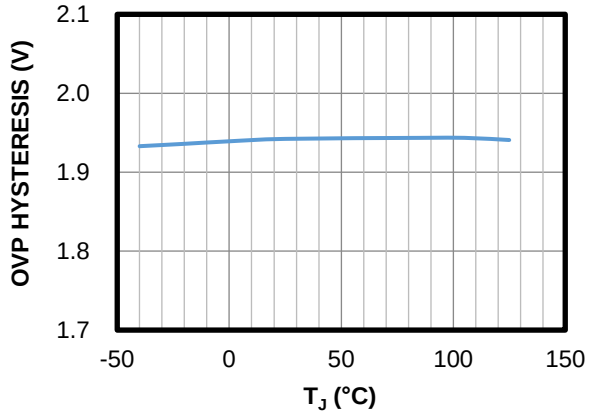
V_{CC} UVLO Hysteresis vs. T_J



OVP Threshold vs. T_J



OVP Hysteresis vs. T_J

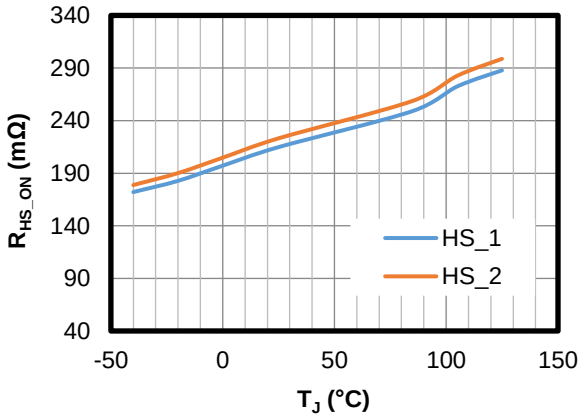


TYPICAL CHARACTERISTICS *(continued)*

V_{CC} = 12V, T_J = -40°C to 125°C, unless otherwise noted.

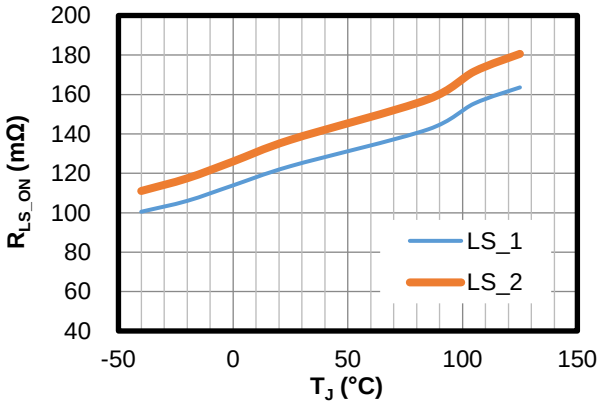
High-Side MOSFET On Resistance vs. T_J

V_{CC} = 12V



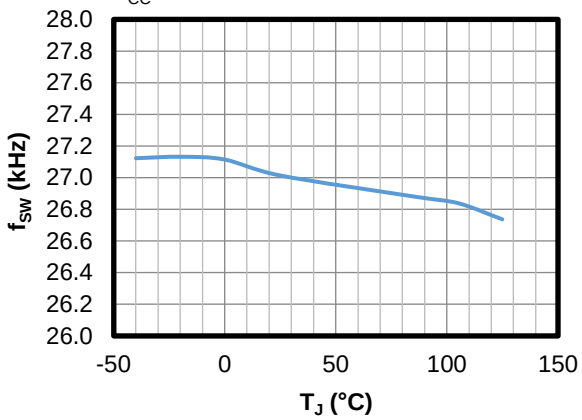
Low-Side MOSFET On Resistance vs. T_J

V_{CC} = 12V



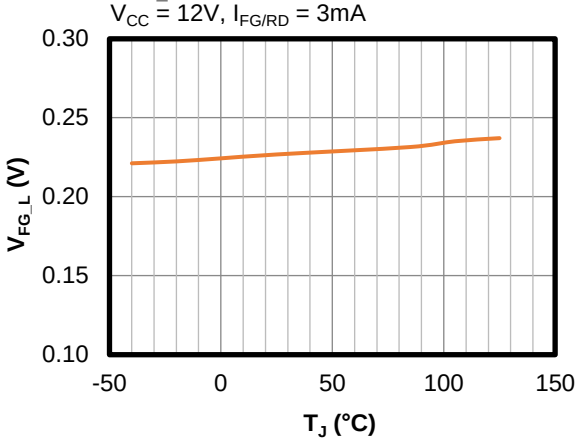
Switching Frequency vs. T_J

V_{CC} = 12V



V_{FG_L} vs. T_J

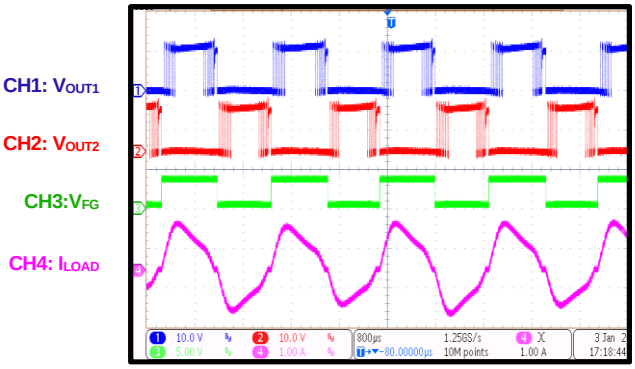
V_{CC} = 12V, $I_{FG/RD}$ = 3mA



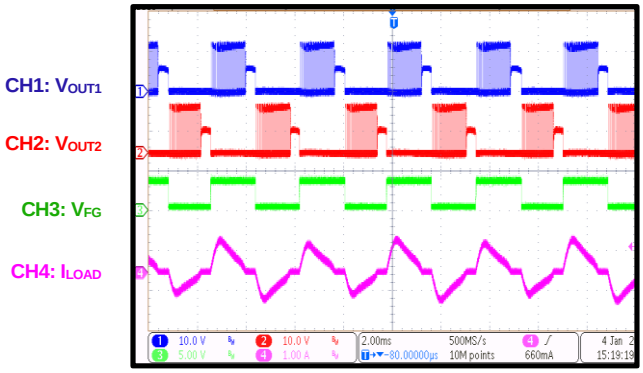
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 12V, PWM frequency is 20kHz, tested on a 4cm sever fan, max speed is 18000rpm, T_J = 25°C, unless otherwise noted.

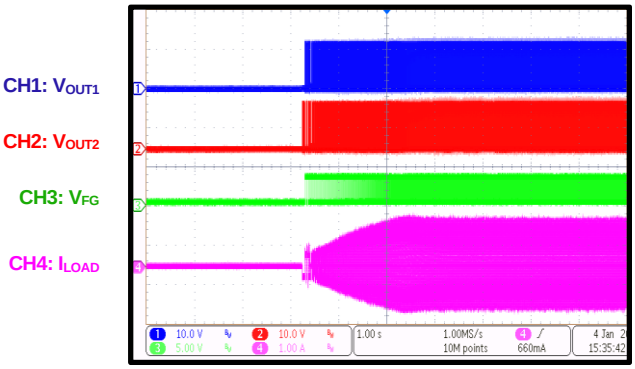
Steady State
PWM duty cycle = 100%



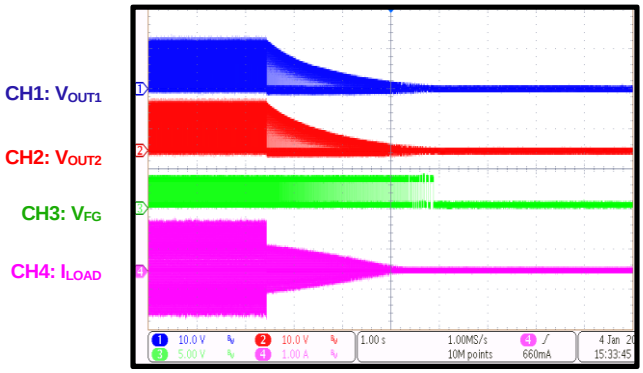
Steady State
PWM duty cycle = 50%



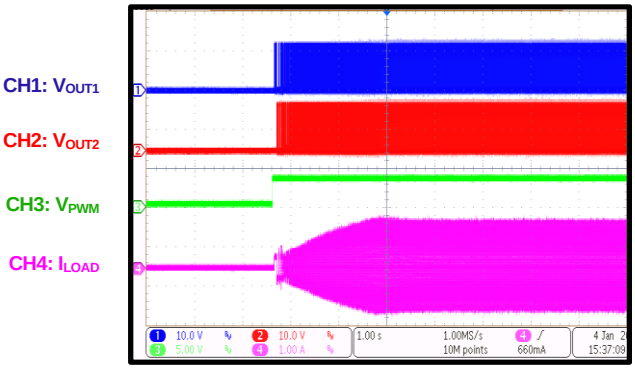
PWM On
PWM duty cycle = 0% to 100%



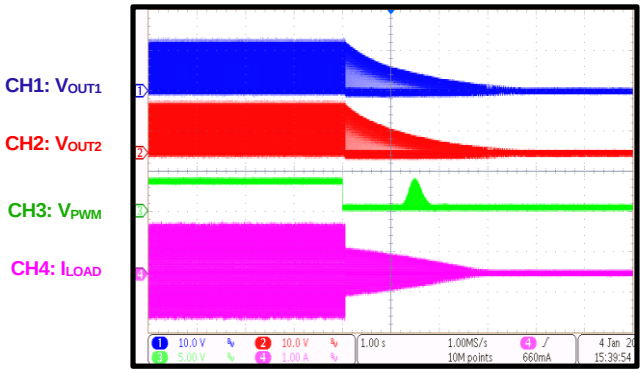
PWM Off
PWM duty cycle = 100% to 0%



PWM On
PWM duty cycle = 0% to 100%



PWM Off
PWM duty cycle = 100% to 0%

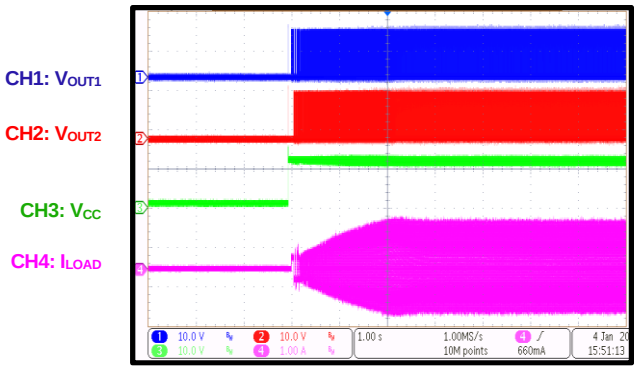


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{CC} = 12V, PWM frequency is 20kHz, tested on a 4cm sever fan, max speed is 18000rpm, T_J = 25°C, unless otherwise noted.

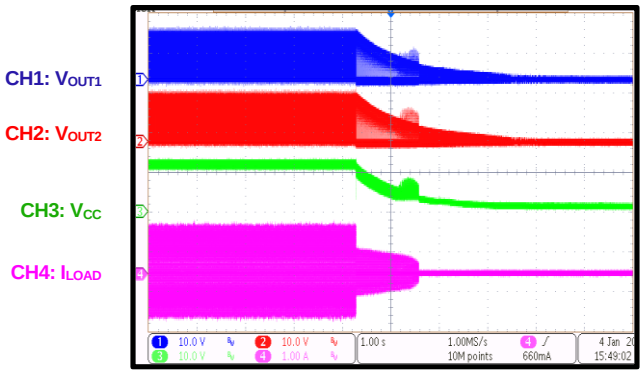
Start-Up through VCC

V_{CC} = 0V to 12V, PWM duty cycle = 100%



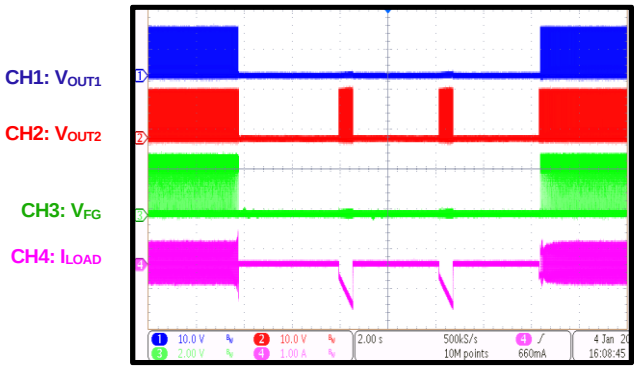
Shutdown through VCC

V_{CC} = 12V to 0V, PWM duty cycle = 100%



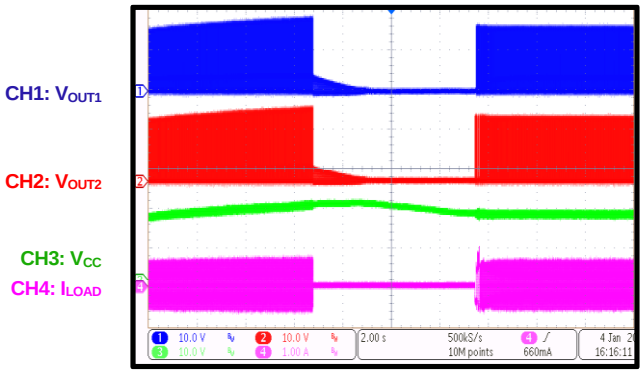
Locked Rotor and Retry

PWM duty cycle = 25%, locked rotor then release



Over-Voltage Protection

PWM duty cycle = 25%, V_{CC} ramps up, then ramps down



FUNCTIONAL BLOCK DIAGRAM

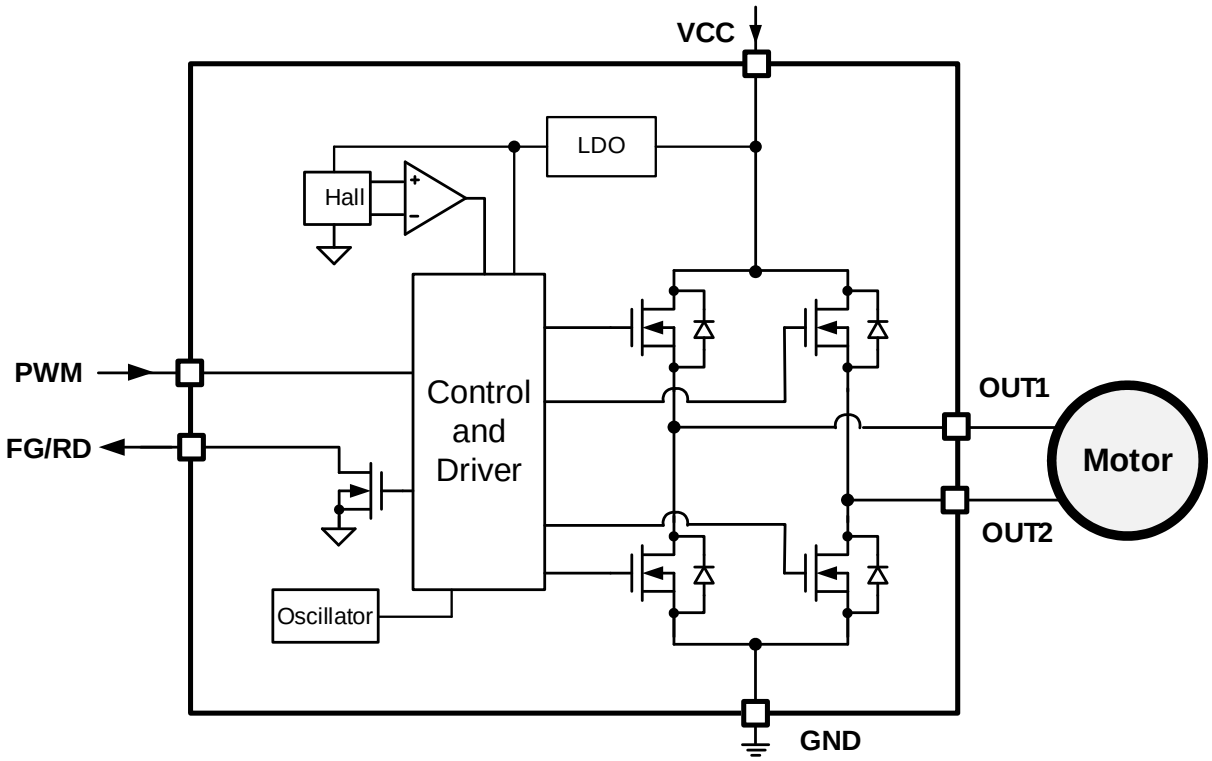


Figure 1: Functional Block Diagram

OPERATION

The MP6655 is a single-phase brushless DC (BLDC) motor driver with integrated power MOSFETs and a Hall sensor. It drives a single-phase BLDC motor with up to 2.5A of peak phase current. The input voltage (V_{IN}) ranges from 3.3V to 18V.

Speed Control

The MP6655 supports either open-loop (default) or closed-loop speed control. The duty cycle of the pulse-width-modulation (PWM) signal applied on the PWM pin controls the speed. The PWM signal frequency ranges from 60Hz to 100kHz.

In open-loop speed control, the OUT1 and OUT2 output duty cycles are controlled by the input PWM duty cycle with the speed curve configurations.

In closed-loop speed control, the motor's rotating speed is fed back to the control loop, and the output duty cycle is adjusted by the control loop, which controls the speed.

Starting Duty Cycle

When the input PWM duty cycle is below the starting duty cycle that is set via the D0[7:0] bits, the device takes one of two actions, depending on the SPD_ZERO bit (see Figure 2).

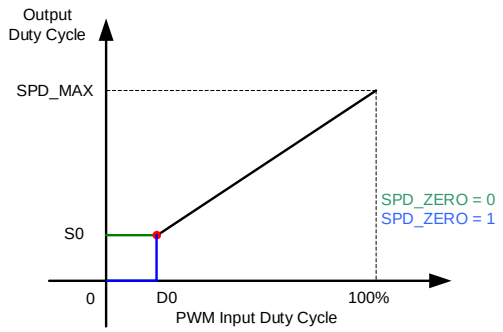


Figure 2: Starting Duty Cycle

- If SPD_ZERO = 0, OUT1 and OUT2 maintain the output duty cycle or speed set by S0[7:0].
- If SPD_ZERO = 1, the IC stop switching.

Operation Sequence

Figure 3 shows the operation sequence. All operations are based on the Hall signal coming from the embedded Hall sensor (HA_IN). HA_OUT is based on HA_IN with an offset angle (denoted as θ_E in Figure 3). The offset angle is set by the internal HAL_ANG[3:0] bits. The offset angle leading or lag is configured via the HAL_DIR bit.

If HA_OUT is low, then OUT1 keeps the low-side MOSFET (LS-FET) on, and OUT2 is the switching phase.

When HA_OUT is high, the OUT1 phase is the switching phase, and OUT2 keeps the LS-FET on.

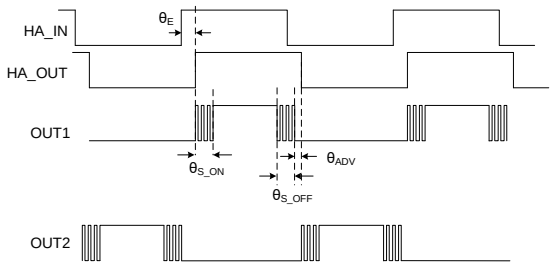


Figure 3: Operation Sequence

Soft-On Commutation

During soft-on commutation (denoted as θ_{S_ON} in Figure 3), the switching phase output duty cycle gradually increases from 0% to the steady duty cycle. The other phase keeps the LS-FET on. The soft-on commutation angle is configured via the internal SON_ANG[4:0] bits.

Soft-Off Commutation

During soft-off commutation (denoted as θ_{S_OFF} in Figure 3), the switching phase output duty cycle gradually drops from a steady duty cycle to 0%. The other phase keeps the LS-FET on. The soft-off commutation angle can be configured via the internal SOFF_ANG[4:0] bits.

Soft-On/Off Commutation Angle Linear Interpolation

The soft-on/off commutation angle can be set to change linearly when the output duty cycle varies. SON_ANG[4:0] and SOFF_ANG[4:0] set the soft-on and soft-off commutation angles when the steady output duty cycle is 100%, respectively. The commutation angle linearly increases to 90° when the steady output duty cycle drops to 0%.

Figure 4 shows the linear angle interpolation.

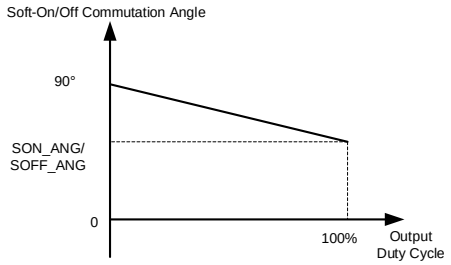


Figure 4: Soft-On/Off Commutation Angle Linear Interpolation

The soft-on/off commutating angle linear interpolation can be enabled or disabled via the register.

Advanced Soft-Off

The advanced soft-off angle (denoted as θ_{ADV} in Figure 5) provides a leading angle for soft-off commutation. The advanced soft-off angle can eliminate the reverse current (see Figure 5). This angle can be automatically adjusted or set to a fixed value.

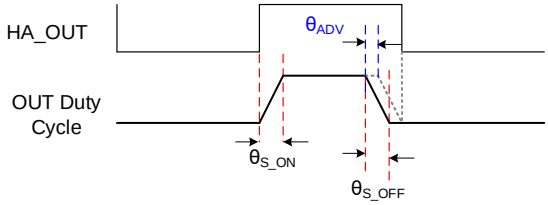


Figure 5: Advanced Soft-Off Angle

Curve Configurations

The device supports speed curve configurations. The input PWM duty cycle and the corresponding output duty cycle or speed can be configured via the register.

There are five configurable parameters, described in greater detail below (see Figure 6).

- D0[7:0] sets the starting duty cycle.
- S0[7:0] sets the corresponding output duty cycle or speed.
- D1[7:0], D2[7:0], and D3[7:0] set three different input duty cycles. The corresponding output duty cycle or speed is set via S1[7:0], S2[7:0], or S3[7:0], respectively.
- SPD_MAX[11:0] sets the output duty cycle or speed when the input duty cycle is 100%.

In open-loop speed control, the 8-bit LSB (SPD_MAX[7:0]) sets the output duty cycle when the input duty cycle is 100%.

In closed-loop speed control, a 12-bit register (SPD_MAX[11:0]) sets the speed when the input duty cycle is 100%. The electrical speed at 100% can be calculated with Equation (1):

$$\text{Speed (RPM)} = \text{SPD\_MAX[11:0]} \times 16 \quad (1)$$

Dx[7:0] sets the input duty cycle, which can be estimated with Equation (2):

$$\text{Input Duty Cycle} = \text{Dx[7:0]} / 256 \quad (2)$$

Where x = 0, 1, 2, or 3.

Sx[7:0] sets the output duty cycle in open-loop speed control, calculated with Equation (3):

$$\text{Output Duty Cycle} = \text{Sx[7:0]} / 256 \quad (3)$$

Where x = 0, 1, 2, or 3.

Sx[7:0] also sets the speed for closed-loop speed control. The electrical speed can be estimated with Equation (4)

$$\text{Speed (rpm)} = \text{Sx[7:0]} / 256 \times \text{SPD\_MAX[11:0]} \times 16 \quad (4)$$

Where x = 0, 1, 2, or 3.

Figure 6 shows the curve configurations.

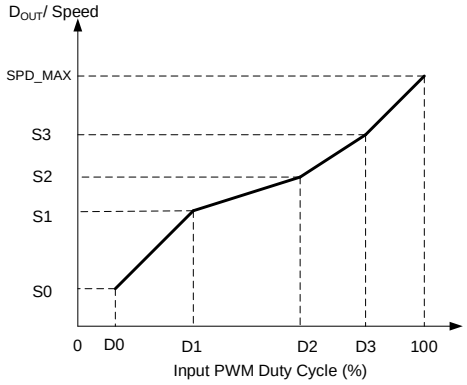


Figure 6: Curve Configurations

The MP6655 also supports the maximum speed when the input duty cycle is low.

If the MAX_EN bit = 1, the fan speed rises to its maximum when the input duty cycle is below 1.5%. The fan rotating speed is configured by curve configuration setting when the input PWM duty cycle exceeds 3.1% (see Figure 7 on page 13).

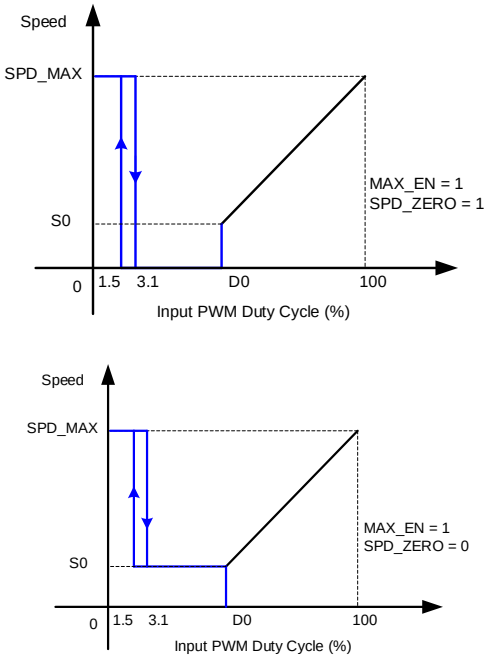


Figure 7: Maximum Speed at Low Duty Cycle

Standby Mode

When the VCC voltage (V_{CC}) exceeds its under-voltage lockout (UVLO) rising threshold and the PWM pin stays low, the MP6655 enters standby mode, and most internal circuits turn off. The MP6655 exits standby mode when the PWM input signal is detected, or when power on the device is cycled.

Pre Start-Up

When the input PWM duty cycle exceeds the starting duty cycle, the MP6655 enters the pre start-up stage. The output duty cycle increases with a slope that is set by the T_PRE[1:0] bits.

Soft Dynamic

To reduce the input inrush current during start-up, the MP6655 provides a configurable soft dynamic time via the register bits TIME_SS[1:0].

The soft shutdown time (output duty cycle or speed dropping) can be double its rising time, depending on the DN_SCALE bit.

Rotor Speed Indication (FG) or Locked-Rotor Indication (RD)

The FG/RD pin can be configured as a speed indicator (FG) or locked-rotor protection indicator (RD).

- If FGRD[2:0] = 000, then the FG/RD pin outputs 1 pulse every electrical cycle (1x).
- If FGRD[2:0] = 001, then the FG/RD pin outputs 1 pulse every 2 electrical cycles (1/2x).
- If FGRD[2:0] = 010, then the FG/RD pin outputs 2 pulses every electrical cycle (2x).
- If FGRD[2:0] = 011, then the FG/RD pin outputs 2 pulses every 3 electrical cycles (2/3x).
- If FGRD[2:0] = 100, the FG/RD pin is set for locked-rotor indication. The FG/RD pin outputs high for locked-rotor protection.
- If FGRD[2:0] = 101, the FG/RD pin is set for locked-rotor indication. The FG/RD pin outputs low for locked-rotor protection.
- If FGRD[2:0] = 110, the FG/RD pin is set as an external Hall signal input. The external input Hall signal is the control signal.

Protection Circuits

The MP6655 is fully protected against over-voltage (OV), under-voltage (UV), over-current (OC), and over-temperature (OT) events.

Over-Current Protection (OCP)

If the phase current exceeds the OCP threshold set by OCP_SEL[1:0] after a blanking time during normal operation, the high-side MOSFET (HS-FET) turns off. The MP6655 resumes switching in the next switching cycle. The OCP threshold is selected via OCP_SEL[1:0]. The following thresholds can be selected: 2.5A, 1.8A, 1.2A, or 0.6A.

Short-Circuit Protection (SCP)

If the current is not limited by OCP, the MP6655 has a maximum peak current limit. If the current flowing through any MOSFET exceeds the maximum peak current limit threshold (typically 4A) after a blanking time, all MOSFETs turn off immediately.

When SCP is triggered, the MP6655 tries to recover to normal operation after a locked retry time.

Thermal Shutdown (TSD)

The MP6655 features thermal monitoring. If the die temperature exceeds 160°C, the MOSFETs of the switching half-bridge turn off. Once the die temperature drops to a safe level, operation automatically resumes.

Under-Voltage Lockout (UVLO)

If V_{CC} ever falls below the under-voltage lockout (UVLO) threshold, all circuitry in the device is disabled, and the internal logic is reset. Operation resumes when V_{CC} exceeds the UVLO threshold.

Locked-Rotor Protection (RD)

If there is a locked-rotor condition and no Hall edge is detected during the 0.6s detection time, then locked-rotor protection is triggered. Both LS-FETs of the H-bridge turn on. After a lock retry time set by LOCK_SEL[1:0], the MP6655 automatically tries to start up again.

The lock retry time is configured via LOCK_SEL[1:0] with the following options: 1.8s, 3.6s, 5.4s, and 8.4s.

The FG/RD pin releases only after 3 Hall signal edges are detected, and after the locked-rotor condition is removed.

Over-Voltage Protection (OVP)

If V_{CC} exceeds the OV threshold (typically 19V), the drive is disabled. The MP6655 resumes normal operation when V_{CC} drops below the OVP threshold falling (typically 17V), and a Hall edge is detected during the OVP interval.

Test Mode and Factory Mode

To configure the internal register, the MP6655 has a test mode. In test mode, the internal register can be read/written. After the design is finalized, the register value can be configured to non-volatile memory (NVM).

REGISTER DESCRIPTION

Register Map

Add.	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
00h (OTP/REG)	D0[7:0]							
01h (OTP/REG)	D1[7:0]							
02h (OTP/REG)	D2[7:0]							
03h (OTP/REG)	D3[7:0]							
04h (OTP/REG)	S0[7:0]							
05h (OTP/REG)	S1[7:0]							
06h (OTP/REG)	S2[7:0]							
07h (OTP/REG)	S3[7:0]							
08h (OTP/REG)	SPD_MAX[7:0]							
09h (OTP/REG)	RESERVED	LOW_F	FAST_DN	PWM_INV	SPD_MAX[11:8]			
0Ah (OTP/REG)	CLOSE	KI[6:0]						
0Bh (OTP/REG)	SINE	SPD_SEL[1:0]		HAL_DIR	HAL_ANG[3:0]			
0Ch (OTP/REG)	LOCK_SEL[1:0]		SON_INT	SON_ANG[4:0]				
0Dh (OTP/REG)	DT	LCK_DIS	SOFF_INT	SOFF_ANG[4:0]				
0Eh (OTP/REG)	MAX_EN	SPD_ZERO	TADV[1:0]		FIX_ST[1:0]		T_PRE[1:0]	
0Fh (OTP/REG)	OVP_DIS	FGRD[2:0]			SOFF_MAX	DN_SCALE	TIME_SS[1:0]	
10h (OTP/REG)	OC_ST	OCP_RD	UD_SUP	PWM_WAIT	WAIT_DIS	WAIT_BH	WAIT_MD	WAIT_TH
11h (OTPREG)	OCP_SEL_HIG		OCP_SEL[1:0]		ASYNC_EN	RESERVED		

SPEED_CURVE_D0 (00h)

The SPEED_CURVE_D0 command sets the starting duty cycle.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	D0[7:0]	0x20	Sets the PWM input starting duty cycle, calculated with the following equation: Starting Duty Cycle = D0[7:0] / 256 The default is 12.5%.

SPEED_CURVE_D1 (01h)

The SPEED_CURVE_D1 command sets the input duty cycle for curve configurations.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	D1[7:0]	0x40	Sets the input duty cycle for curve configurations, calculated with the following equation: Input PWM Duty Cycle = D1[7:0] / 256

SPEED_CURVE_D2 (02h)

The SPEED_CURVE_D2 command sets the input duty cycle for curve configurations.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	D2[7:0]	0x80	Sets the input duty cycle for curve configurations, calculated with the following equation: Input PWM Duty Cycle = D2[7:0] / 256

SPEED_CURVE_D3 (03h)

The SPEED_CURVE_D3 command sets the input duty cycle for curve configurations.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	D3[7:0]	0xF0	Sets the input duty cycle for curve configurations, calculated with the following equation: Input PWM Duty Cycle = D3[7:0] / 256

SPEED_CURVE_S0 (04h)

The SPEED_CURVE_S0 command sets the output duty cycle or speed when the input PWM duty cycle is set by D0[7:0].

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	S0[7:0]	0x10	Sets the output duty cycle or speed when the input PWM duty cycle is set by D0[7:0]. In open-loop speed control, these bits set the output duty cycle when the input PWM duty cycle is set by D0[7:0], calculated with the following equation: Output Duty Cycle = S0[7:0] / 256 In closed-loop speed control, these bits set the speed reference when the input PWM duty cycle is set by D0[7:0]. The electrical speed can be calculated with the following equation: Speed (rpm) = S0[7:0] / 256 x SPD_MAX[11:0] x16

SPEED_CURVE_S1 (05h)

The SPEED_CURVE_S1 command sets the output duty cycle or speed when the input PWM duty cycle is set by D1[7:0].

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	S1[7:0]	0x40	Sets the output duty cycle or speed when the input PWM duty cycle is set by D1[7:0]. In open-loop speed control, these bits set the output duty cycle when the input PWM duty cycle is set by D1[7:0], calculated with the following equation: Output Duty Cycle = S1[7:0] / 256 In closed-loop speed control, these bits set the speed reference when the input PWM duty cycle is set by D1[7:0]. The electrical speed can be calculated with the following equation: Speed (rpm) = S1[7:0] / 256 x SPD_MAX[11:0] x16

SPEED_CURVE_S2 (06h)

The SPEED_CURVE_S2 command sets the output duty cycle or speed when the input PWM duty cycle is set by D2[7:0].

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	S2[7:0]	0x80	Sets the output duty cycle or speed when the input PWM duty cycle is set by D2[7:0]. In open-loop speed control, these bits set the output duty cycle when the input PWM duty cycle is set by D2[7:0], calculated with the following equation: Output Duty Cycle = S2[7:0] / 256 In closed-loop speed control, these bits set the speed reference when the input PWM duty cycle is set by D2[7:0]. The electrical speed can be calculated with the following equation: Speed (rpm) = S2[7:0] / 256 x SPD_MAX[11:0] x16

SPEED_CURVE_S3 (07h)

The SPEED_CURVE_S3 command sets the output duty cycle or speed when the input PWM duty cycle is set by D3[7:0].

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	S3[7:0]	0xF0	Sets the output duty cycle or speed when the input PWM duty cycle is set by D3[7:0]. In open-loop speed control, these bits set the output duty cycle when the input PWM duty cycle is set by D3[7:0], calculated with the following equation: Output Duty Cycle = S3[7:0] / 256 In closed-loop speed control, these bits set the speed reference when the input PWM duty cycle is set by D3[7:0]. The electrical speed can be calculated with the following equation: Speed (rpm) = S3[7:0] / 256 x SPD_MAX[11:0] x16

SPEED_CURVE_SPDMAX (08h)

The SPEED_CURVE_SPD_MAX command sets the output duty cycle or speed when the input PWM duty cycle = 100%.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	SPD_MAX[7:0]	0xFF	Sets the output duty cycle or speed when the input PWM duty cycle = 100%. In open-loop speed control, these bits set the output duty cycle when the input PWM duty cycle = 100%. It can be calculated with the following equation: Output Duty Cycle = SPD_MAX[7:0] / 256 In closed-loop speed control, these bits set the speed reference when the input PWM duty cycle= 100%. These bits work with SPD_MAX[11:8] to set the maximum speed (electrical speed). The electrical speed can be calculated with the following equation: Max Speed (rpm) = SPD_MAX[11:0] x16

PWM_SPDMAX (09h)

The PWM_SPDMAX command sets the PWM input frequency range, PWM input signal polarity, PWM fast-off, and maximum speed reference.

Bits	Access	Bit Name	Default	Description
7	N/A	RESERVED	0	Reserved.
6	OTP/REG	LOW_F	0	Sets the input PWM frequency. 0: High frequency is selected. 2kHz to 100kHz (default) 1: Low frequency is selected. 60Hz to 2kHz
5	OTP/REG	FAST_DN	1	Enables PWM fast-off. 0: Disable fast-off 1: Enable fast-off when the PWM is off. The MP6655 stops switching when the input duty cycle falls below the starting duty cycle (default)
4	OTP/REG	PWM_INV	0	Selects the input PWM polarity. 0: Positive duty cycle (default) 1: Negative duty cycle
3:0	OTP/REG	SPD_MAX[11:8]	0011	In closed-loop speed control, these bits set the speed reference when the input PWM duty cycle = 100%. These bits work with SPD_MAX[7:0] to set the maximum speed (electrical speed). The speed can be calculated with the following equation: Max Speed = 16rpm / LSB

CLOSE_KI (0Ah)

The CLOSE_KI command sets the speed control mode and integral parameter for closed-loop speed control.

Bits	Access	Bit Name	Default	Description
7	OTP/REG	CLOSE	0	Selects the speed control loop. 0: Open-loop speed control (default) 1: Closed-loop speed control
6:0	OTP/REG	KI[6:0]	0x08	Sets the integral parameter for closed-loop speed control.

SINE_CLOCK_HALL (0Bh)

The SINE_CLOCK_HALL command sets the soft-on/off mode, digital clock, and Hall offset angle.

Bits	Access	Bit Name	Default	Description
7	OTP/REG	SINE	0	Selects the soft-on/off mode. 0: Linear (default) 1: Sine
6:5	OTP/REG	SPD_SEL[1:0]	01	Selects the digital clock. A higher frequency leads to a higher calculation resolution; however, it also leads to a higher minimum speed. These bits indicate the supported minimum speed (electrical speed). 00: 200rpm 01: 800rpm (default) 10: 1600rpm 11: 3200rpm
4	OTP/REG	HAL_DIR	0	Selects the Hall offset angle lag/lead. 0: Lag (default) 1: Lead
3:0	OTP/REG	HAL_ANG[3:0]	0000	Sets the Hall offset angle. 1.4° per step. 0000: 0° (default) 0001: 1.4° … 1111: 21° Hall Offset Angle = HAL_ANG[3:0] x 1.4°

TLOCK_SON (0Ch)

The TLOCK_SON command sets the lock protection retry time and soft-on commutation angle.

Bits	Access	Bit Name	Default	Description
7:6	OTP/REG	LOCK_SEL[1:0]	10	Selects the lock retry time. 00: 8.4s 01: 5.4s 10: 3.6s (default) 11: 1.8s
5	OTP/REG	SON_INT	1	Enables the soft-on angle linear interpolation. 0: Disabled 1: Enabled. The soft-on angle linearly increases to 90° when the duty cycle drops (default)
4:0	OTP/REG	SON_ANG[4:0]	0x10	Sets the soft-on commutation angle. 2.8° per step. 00000: 0° 00001: 2.8° … 10000: 45° (default) … 11111: 87.2° Soft-On Angle = (SON_ANG[4:0]) x 2.8°

TD_LOCK_SOFF (0Dh)

The TD_LOCK_SOFF command sets the lock protection disabling and soft-off commutation angle.

Bits	Access	Bit Name	Default	Description
7	OTP/REG	TD	0	Select delay time of commutation. 0: 1.2ms (default) 1: 2.4ms
6	OTP/REG	LOCK_DIS	0	Enables locked-rotor protection. 0: Enabled (default) 1: Disabled
5	OTP/REG	SOFF_INT	1	Enables the soft-on angle linear interpolation enable bit. 0: Disabled 1: Enabled. The soft-off angle linearly increases to 90° when the duty cycle drops (default)
4:0	OTP/REG	SOFF_ANG[4:0]	0x10	Sets the soft-off commutation angle. 2.8° per step. 00000: 0° 00001: 2.8° … 10000: 45° (default) … 11111: 87.2° Soft-Off Angle = (SOFF_ANG[4:0]) x 2.8°

CFR_1 (0Eh)

The CFR_1 command sets the speed at low duty cycles, advanced soft-off angle, and pre start-up time.

Bits	Access	Bit Name	Default	Description
7	OTP/REG	MAX_EN	0	Enables setting the maximum speed at low duty cycles. 0: The speed is the same as the SPD_ZERO setting 1: Maintain the maximum speed when the PWM input duty cycle < 1.5%. The speed is determined by the SPD_ZERO setting when 3.1% < the PWM input duty cycle < D0[7:0]
6	OTP/REG	SPD_ZERO	1	Indicates the speed when the PWM input duty cycle < D0[7:0]. 0: Maintain the minimum speed when the PWM input duty cycle < D0[7:0] 1: Stop when the PWM input duty cycle < D0[7:0] (default)
5:4	OTP/REG	TADV [1:0]	00	Sets the advanced soft-off angle. 00: Auto (default) 01: 5.6° 10: 11.2° 11: 22.5°
3:2	OTP/REG	FIX_ST [1:0]	01	Selects the initial output duty cycle at start-up. 00: 3.125% 01: 9.375% (default) 10: 15.625% 11: 21.875%
1:0	OTP/REG	T_PRE [1:0]	01	Sets the pre start-up time. 00: 18.96ms 01: 9.481ms 10: 4.74ms 11: 2.37ms

CFR_2 (0Fh)

The CFR_2 command sets the functions for over-voltage protection (OVP), FG/RD pin output, output duty cycle ramp-down scale, and soft-start time.

Bits	Access	Bit Name	Default	Description
7	OTP/REG	OVP_DIS	0	Enables OVP. 0: Enabled (default) 1: Disabled
6:4	OTP/REG	FGRD[2:0]	000	Sets the output of the FG/RD pin. 000: FG (default) 001: 1/2 x FG 010: 2 x FG 011: 2/3 x FG 100: The FG/PD pin is set to RD. It outputs high during locked-rotor protection 101: The FG/PD pin is set to RD. It outputs low during locked-rotor protection 110: FGRD_HALL_IN. The FG/RD pin is set as an external Hall input pin.
3	OTP/REG	SOFF_MAX	0	Sets the maximum soft-off angle during start-up. 0: Enabled (default) 1: Disabled
2	OTP/REG	DN_SCALE	1	Selects the PWM output duty ramp-down scale as the output duty cycle drops from 100% to 0%. 0: 1 x soft-start time 1: 2 x soft-start time (default)
1:0	OTP/REG	TIME_SS [1:0]	01	Sets the soft-start time. 00: 1.21s 01: 2.43s 10: 4.85s 11: 9.71s

CFR_3 (10h)

The CFR_3 command sets the over-current protection (OCP) function at start-up and RD, waiting mode, and wait threshold.

Bits	Access	Bit Name	Default	Description
7	OTP/REG	OCP_ST	0	Sets the current limit at start-up. 0: Normal (default) 1: Minimum OC at start-up
6	OTP/REG	OCP_RD	1	Sets the current limit at locked-rotor protection. 0: Normal 1: Minimum OC at lock (default)
5	OTP/REG	UN_SUP	0	Enables speed undershoot suppression during closed-loop speed control. 0: Disabled (default) 1: Enabled
4	OTP/REG	PWM_WAIT	1	Enables the waiting function at the PWM during start-up. 0: Disabled 1: Enabled (default)

3	OTP/REG	WAIT_DIS	0	Disables the waiting function at start-up. 0: Wait until the speed drops to a set threshold or wait for a fixed time during start-up 1: Directly start up without waiting
2	OTP/REG	WAIT_BH	0	Selects whether to coast or brake while waiting for the fan's speed to drop. 0: Coast during wait 1: Coast then brake during wait
1	OTP/REG	WAIT_MD	0	Selects the waiting mode at start-up. 0: Speed mode. The IC does not drive until the speed drops below the threshold speed during start-up (default) 1: Time mode. The IC does not drive for a fixed time during start-up
0	OTP/REG	WAIT_TH	1	Selects the waiting time or speed threshold at start-up. When combined with WAIT_SEL, these bits can select the fixed time that the IC waits before output switching, or the motor speed threshold at which the IC starts driving the motor. The waiting time or speed threshold can be selected as follows: If WAIT_MD = 0, then the device waits for the motor speed to drop to a certain speed. 0: 1000rpm (electrical speed) 1: 500rpm If WAIT_MD = 1, this bit sets the wait time. 0: 4.8s 1: 2.4s

OCP (11h)

The OCP command sets the current limit.

Bits	Access	Bit Name	Default	Description
7:6	OTP/REG	OCP_SEL_HIG [1:0]	10	Selects the current-limit threshold at high-speed start-up. 00: 0.3A 01: 0.6A 10: 1.2A 11: 2.0A
5:4	OTP/REG	OCP_SEL[1:0]	11	Selects the current-limit threshold. 00: 0.6A 01: 1.2A 10: 1.8A 11: 2.5A
3	OTP/REG	ASYNC_EN	1	Enables the asynchronous function. 0: Disable 1: Enable (default)
2:0	N/A	RESERVED	000	Reserved.

APPLICATION INFORMATION

Selecting the Input Capacitor

Place an input capacitor (C_{IN}) as close to the VCC and GND pins as possible to maintain a stable input voltage (V_{CC}) and reduce noise at the input. C_{IN} must have a low impedance at the switching frequency.

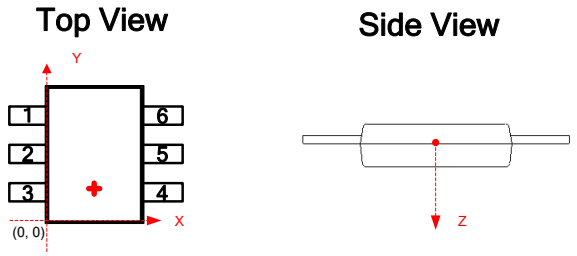
Ceramic capacitors with X7R dielectrics are recommended for their low-ESR characteristics. The ceramic capacitance is dependent on the DC voltage rating. If the ceramic capacitor is biased to its DC voltage rating, then its capacitance drops below 50%.

Ensure that the capacitor has a large enough voltage rating margin. The input capacitance must exceed 10μF.

In some applications, an additional larger-value, electrolytic capacitor may be required to absorb the motor's energy.

Embedded Hall-Effect Sensor

Figure 8 shows the Hall sensor's position of the package.



(X, Y, Z) = (800μm, 783μm, 80μm)

Figure 8: Hall Sensor Position

Selecting a Reverse-Blocking Diode

A reverse-blocking diode can prevent the IC from damage when the input voltage is connected reversely. The reverse-blocking diode also prevents the bus voltage from charging up via the fan's reverse current.

The blocking diode's reverse voltage rating must exceed 30V, and the forward current rating of the blocking diode should exceed the input current (I_{IN}).

Input Clamping Circuit

To avoid high voltage spikes caused by the energy stored in the motor, a voltage-clamping circuit may be required (especially for high-current and large fan inertial applications). A 15V, SOD-123 package TVS diode or Zener diode is sufficient for most 12V applications.

Input Snubber

Due to the input capacitor energy charge/discharge during phase commutation, I_{IN} has switching cycle ringing. If necessary, add a 2Ω resistor in series with a ceramic capacitor as an RC snubber. This snubber should be placed in parallel with C_{IN}. This prevents switching cycle ringing.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 8 and follow the guidelines below:

1. Place the input capacitor as close to the VCC and GND pins as possible.

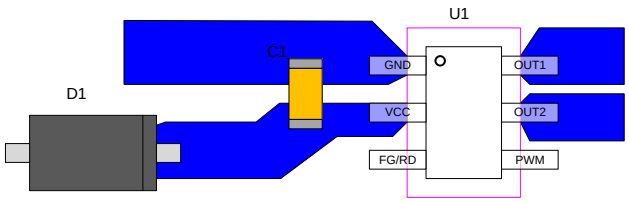


Figure 9: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

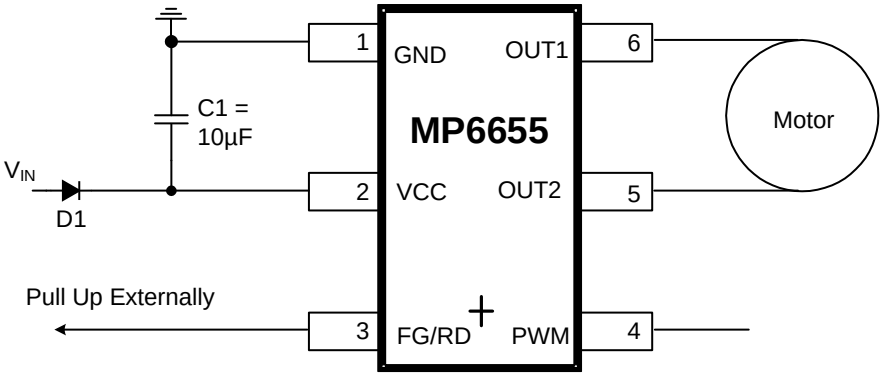


Figure 10: Typical Application Circuit

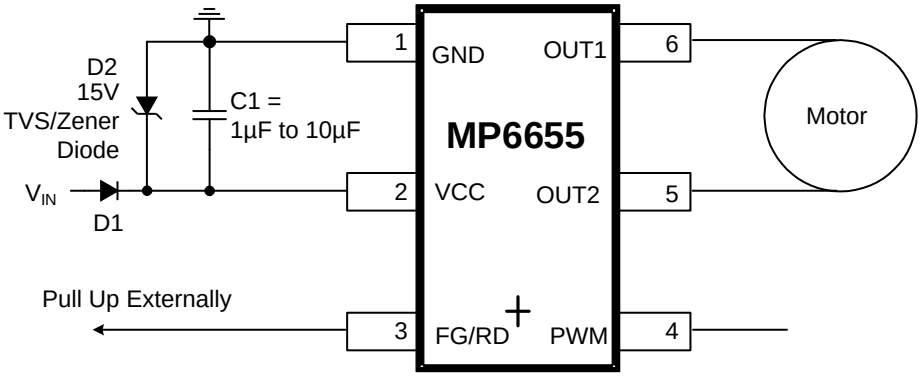
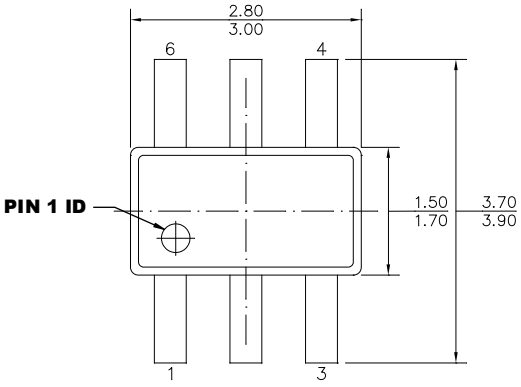


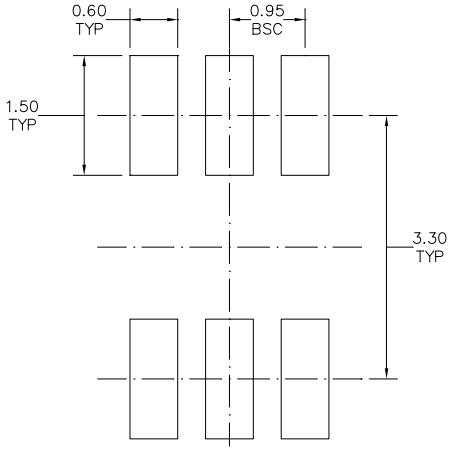
Figure 11: Typical Application Circuit with Clamping Circuit

PACKAGE INFORMATION

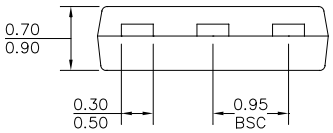
TSOT23-6-SL



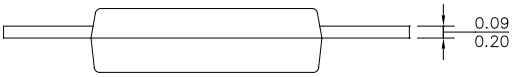
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



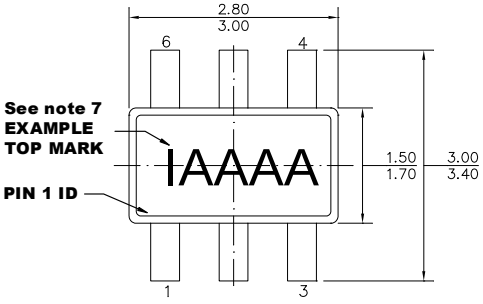
SIDE VIEW

NOTE:

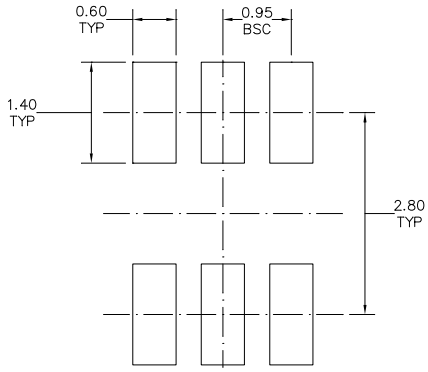
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING REFERENCE IS JEDEC MO-193,
6) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(continued)*

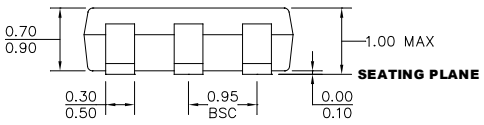
TSOT23-6-L



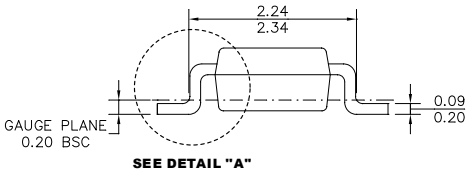
TOP VIEW



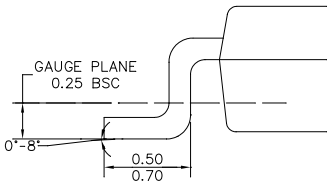
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

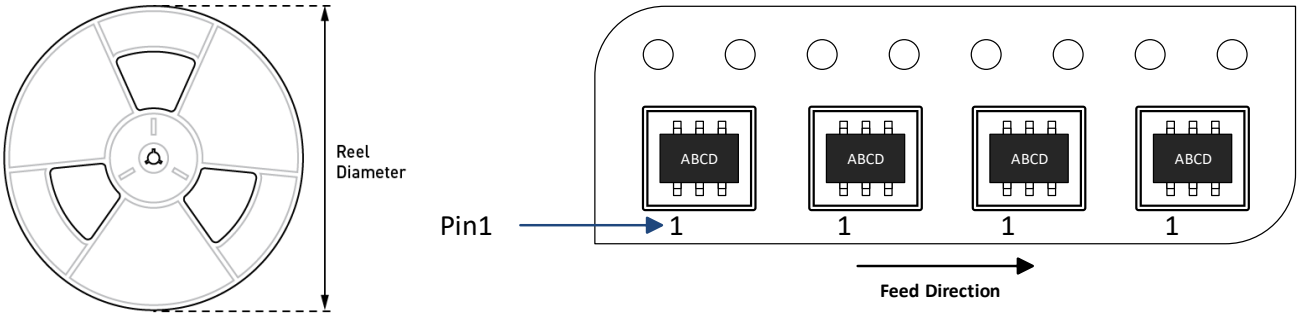


DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING REFERENCE TO JEDEC MO-193, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT (SEE EXAMPLE TOP MARK).

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6655GJS-xxxx-Z	TSOT23-6-SL	5000	N/A	N/A	13in	12mm	8mm
MP6655GJL-xxxx-Z	TSOT23-6-L	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/12/2024	Initial Release	-