MP6616B

18V, 2A, Single-Phase BLDC Motor Driver with Closed/Open-Loop Speed Control and Enhanced ESD Capability

DESCRIPTION

The MP6616B is a single-phase, brushless DC (BLDC) motor driver with integrated MOSFETs and an embedded Hall-effect sensor. It can drive up to 2A of continuous output current across a 3.3V to 18V input supply voltage (V_{CC}) range.

The MP6616B supports both speed open-loop and closed-loop control. The speed is controlled via the pulse-width modulation (PWM) signal on the PWM pin. The device features a configurable soft commutation angle and Hall offset angle. The Hall offset angle can be flexibly optimized for low-speed and high-speed performance across the full speed range.

The FG/RD pin can function as a rotational speed detector or rotor deadlock indicator. This pin is an open-drain output that must be pulled up externally.

Rich protection features include input over-voltage protection (OVP), under-voltage lockout (UVLO) protection, locked-rotor protection, over-current protection (OCP), and thermal shutdown.

The MP6616B is available in a QFN-10 (2mmx3mm) package.

FEATURES

- High-Sensitivity, Embedded Hall-Effect Sensor
- 3.3V to 18V Operating Input Supply Voltage (V_{CC}) Range
- 2A Continuous Output Current
- 100mΩ Integrated Power MOSFETs
- Configurable Speed (40000rpm Max)
- Configurable Minimum Speed and Starting Duty Cycle
- Selectable Closed-Loop or Open-Loop Speed Control
- High-Speed Accuracy in Closed-Loop Mode
- Configurable Soft Commutation Angle (45° Max)
- Configurable Hall Offset Angle (±45° Max)
- 4-Step Configurable Current Limit (4A Max)
- 1kHz to 100kHz Pulse-Width Modulation (PWM) Input Range
- Configurable Soft-Start Time (t_{SS})
- 27kHz Fixed Switching Frequency (f_{SW})
- Standby Mode
- Locked-Rotor Protection with Auto-Recovery
- Thermal Shutdown with Auto-Recovery
- Enhanced Electrostatic Discharge (ESD) Capability
- Built-In Input Over-Voltage Protection (OVP), Under-Voltage Lockout (UVLO) Protection, and Auto-Recovery
- Available in a QFN-10 (2mmx3mm) Package

APPLICATIONS

- 1U and 2U Server Fans
- High-Current Cooling Fans
- Central Processing Unit (CPU) and Personal Computer (PC) Fans

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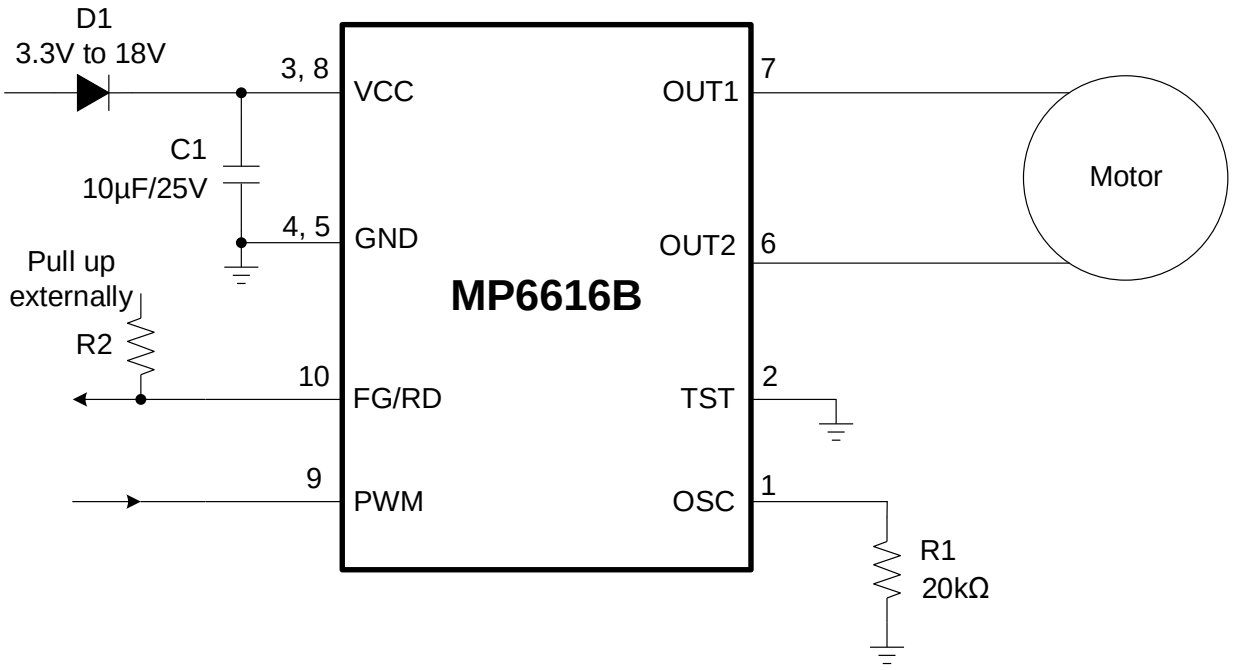
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP6616BGD-xxxx**	QFN-10 (2mmx3mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP6616BGD-xxxx-Z).

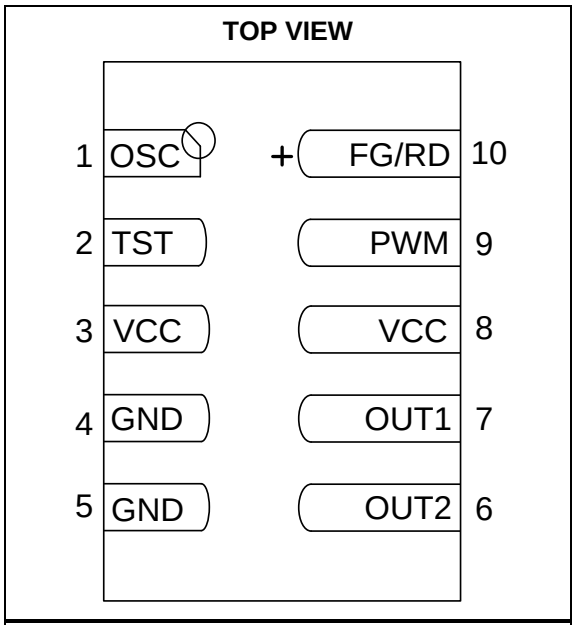
** “xxxx” is the configuration code identifier. The first four digits of the suffix (xxxx) can be a hexadecimal value between 0 and F. The default code is “0000”. Contact an MPS FAE to create this unique number, even if ordering the “0000” code.

TOP MARKING

CAC
YWW
LLLL

CAC: Product code of MP6616BGD
Y: Year code
WW: Week code
LLLL: Lot number

PACKAGE REFERENCE



QFN-10 (2mmx3mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	OSC	**Internal oscillator setting.** Connect a 20kΩ, high-accuracy resistor (with 1% or greater accuracy) between the OSC and GND pins.
2	TST	**Test pin.** Connect the TST pin to GND.
3, 8	VCC	**Input power.** The VCC pin must be bypassed locally. Place a bypass capacitor as close to the IC as possible.
4, 5	GND	**Ground.**
6	OUT2	**Motor driver output 2.** If the Hall-effect sensor outputs high, then the OUT2 pin is in a low state.
7	OUT1	**Motor driver output 1.** If the Hall-effect sensor outputs low, then the OUT1 pin is in a low state.
9	PWM	**Pulse-width modulation (PWM) input for speed control.** A 1kHz to 100kHz PWM signal is recommended for normal operation.
10	FG/RD	**Selectable rotational speed or rotor lock indication.** The FG/RD pin is an open-drain output. FG/RD must be pulled up externally.

ABSOLUTE MAXIMUM RATINGS (1)

V_{CC}, $V_{FG/RD}$, V_{PWM}.....-0.3V to +25V
V_{OUT1}, V_{OUT2}.....-0.3V to V_{CC} + 0.3V
All other pins.....-0.3V to +5V
Continuous power dissipation (T_A = 25°C) (2)
QFN-10 (2mmx3mm)..... 1.9W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -60°C to +150°C

ESD Ratings

Human body model (HBM)
VCC, PWM, FG/RD…… ..... ±8kV
Other pins…… ..... ±4kV
Charged-device model (CDM) ..... ±2kV

Recommended Operating Conditions (3)

Supply voltage (V_{CC}) .....3.3V to 18V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-10 (2mmx3mm) …….....65…....12...°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on a JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{CC} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Test Condition	Min	Typ	Max	Units
Input supply under-voltage lockout (UVLO) rising threshold	$V_{CC_UVLO_RISING}$		2.7	3	3.3	V
Input supply UVLO hysteresis	$V_{CC_UVLO_HYS}$			0.16		V
Operating supply current	I_{CC}	No load		5		mA
Standby current	I_{STB}	PWM is low, STB = 1, T_J = 25°C		430	500	µA
Pulse-width modulation (PWM) input high voltage	V_{PWM_HIGH}		2			V
PWM input low voltage	V_{PWM_LOW}				0.8	V
PWM input internal pull-up resistance				190		kΩ
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)_HS}$	I_{OUT} = 100mA		48		mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)_LS}$	I_{OUT} = 100mA		44		mΩ
Cycle-by-cycle over-current protection (OCP) current limit	I_{OCP}	OCP_SEL = 11		4.3		A
Over-voltage protection (OVP) rising threshold	V_{OVP_RISING}		18	19	20	V
OVP hysteresis	V_{OVP_HYS}			1		V
PWM output frequency	f_{PWM}	R_{OSC} = 20kΩ, T_J = 25°C	26.73	27	27.27	kHz
FG/RD pin output low-level voltage	V_{FG/RD_LOW}	$I_{FG/RD}$ = 3mA, V_{PULL} = 5V, T_J = 25°C		0.19		V
Soft-on angle at 100% PWM output duty cycle	θ_{S_ON}	SON = 11111		43		deg
Soft-off angle at 100% PWM output duty cycle	θ_{S_OFF}	SOFF = 11111		43		deg
Locked-rotor detection time	t_{RD}			0.6		sec
Minimum recommended magnetic field					±2	mT
Thermal shutdown (5)	T_{SD}		150	160	180	°C
Thermal shutdown hysteresis (5)	T_{SD_HYS}			40		°C

Note:

5) Guaranteed by design.

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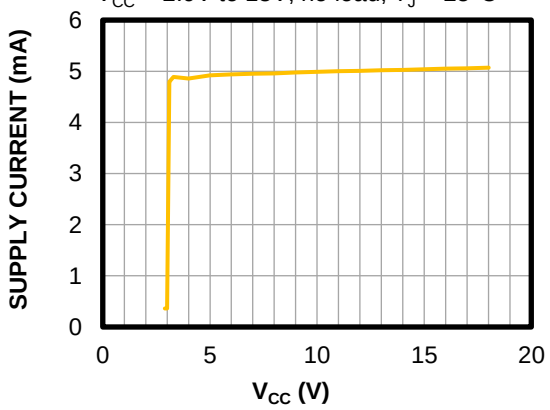
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 12V, T_J = -40 to +125°C, unless otherwise noted.

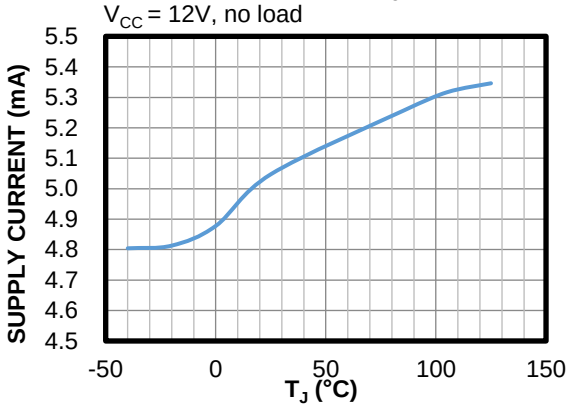
Supply Current vs. Input Supply Voltage

V_{CC} = 2.9V to 18V, no load, T_J = 25°C

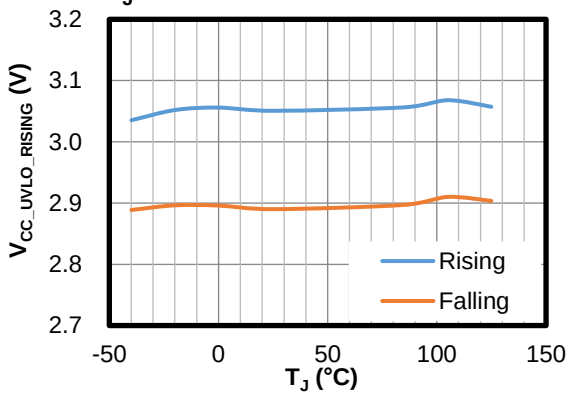


Supply Current vs. T_J

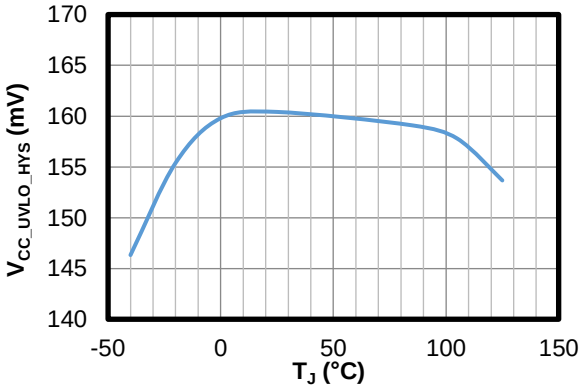
V_{CC} = 12V, no load



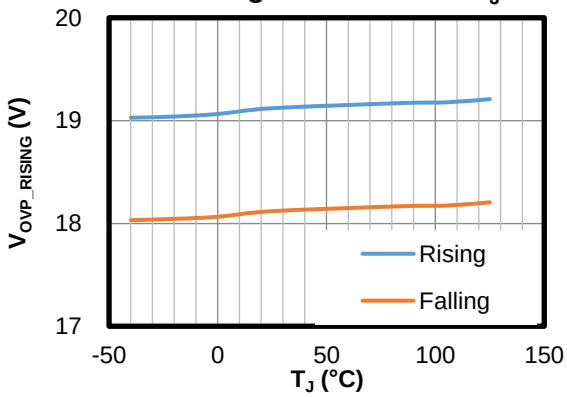
VCC UVLO Rising Threshold vs. T_J



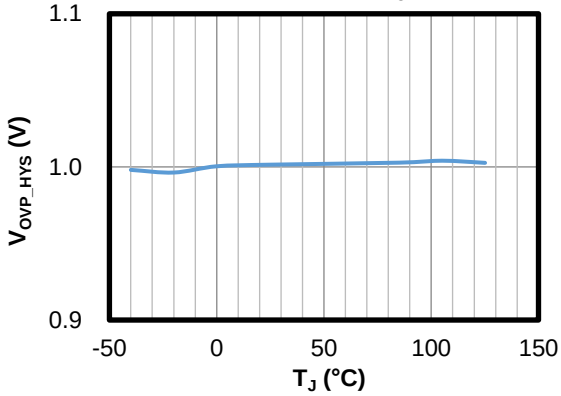
VCC UVLO Hysteresis vs. T_J



OVP Rising Threshold vs. T_J



OVP Hysteresis vs. T_J



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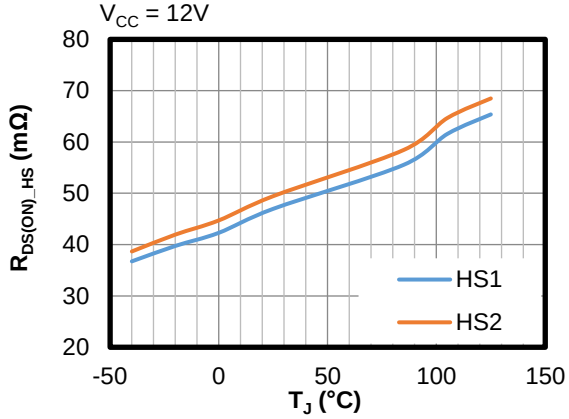
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{CC} = 12V, T_J = -40 to +125°C, unless otherwise noted.

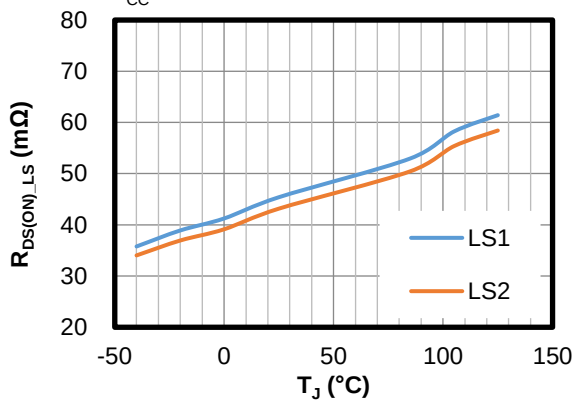
High-Side MOSFET On Resistance vs. T_J

V_{CC} = 12V



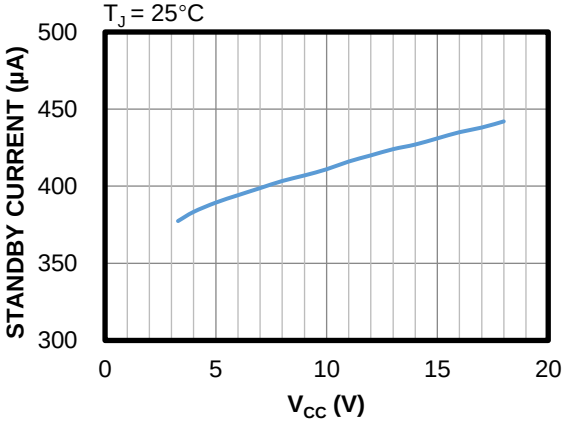
Low-Side MOSFET On Resistance vs. T_J

V_{CC} = 12V



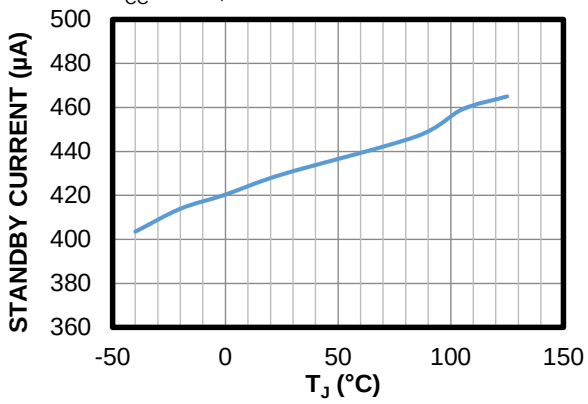
Standby Current vs. Input Supply Voltage

V_{CC} = 3.3V to 18V, PWM = low, T_J = 25°C



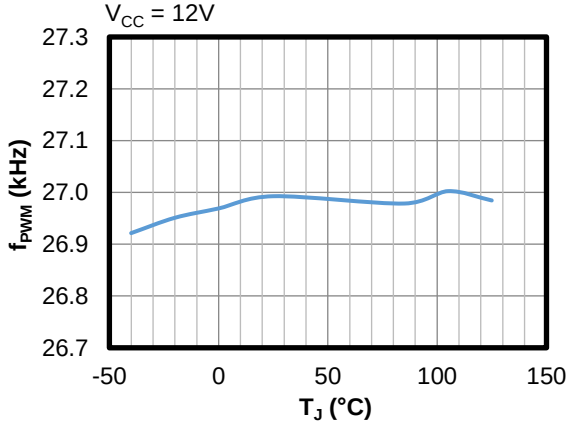
Standby Current vs. T_J

V_{CC} = 12V, PWM = low



PWM Output Frequency vs. T_J

V_{CC} = 12V



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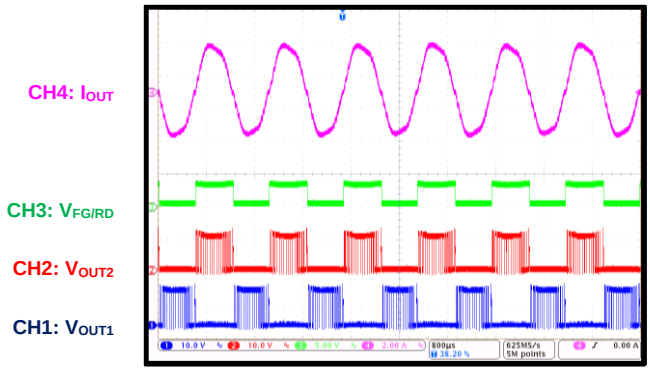
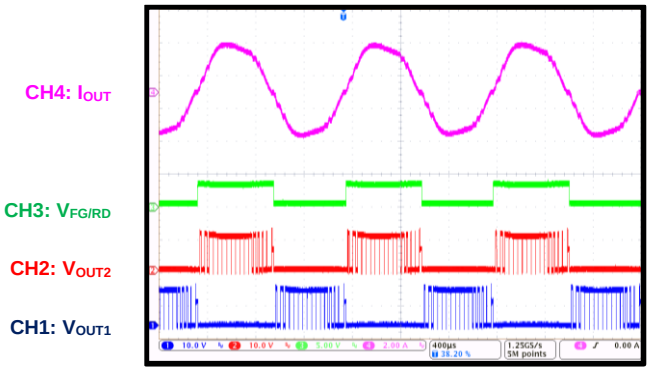
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 12V, f_{PWM} = 20kHz, tested on a 4cm server fan, max speed is 24000rpm unless otherwise noted.

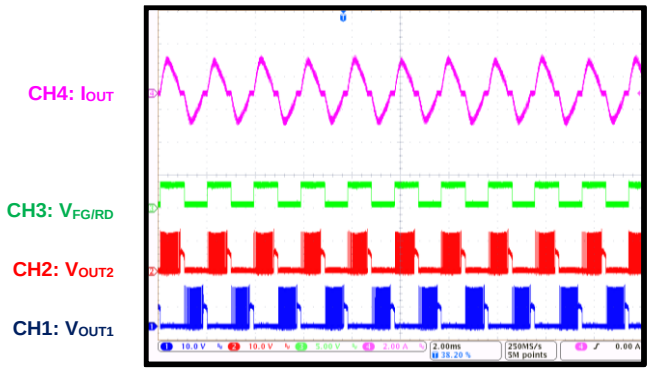
Steady State
PWM duty cycle at 100%



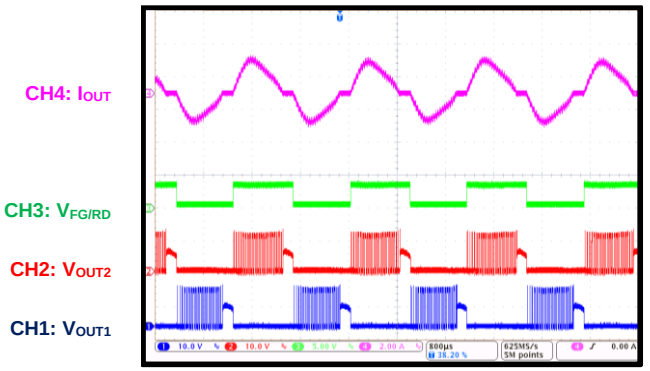
Steady State
PWM duty cycle at 100%



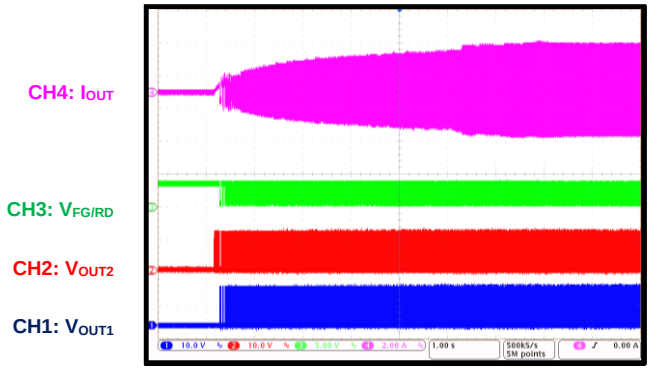
Steady State
PWM duty cycle at 50%



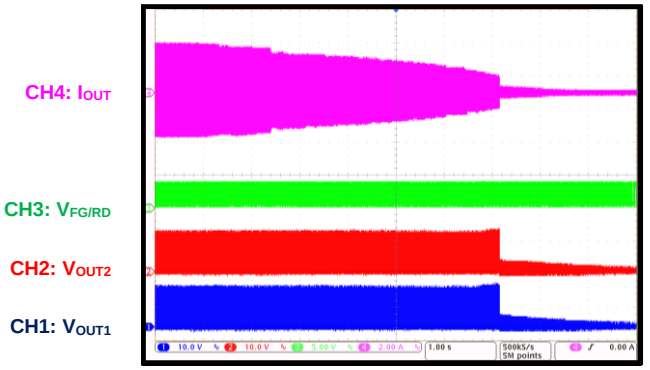
Steady State
PWM duty cycle at 50%



PWM Signal On
PWM duty cycle from 0% to 100%



PWM Signal Off
PWM duty cycle from 100% to 0%



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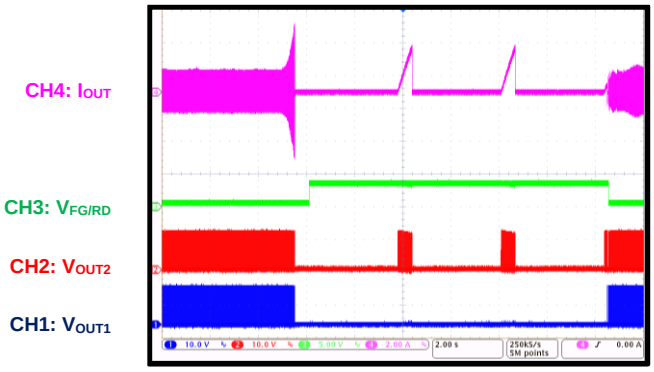
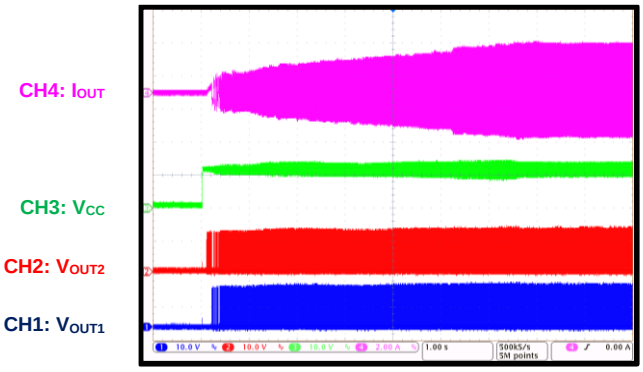
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{CC} = 12V, f_{PWM} = 20kHz, tested on a 4cm server fan, max speed is 24000rpm unless otherwise noted.

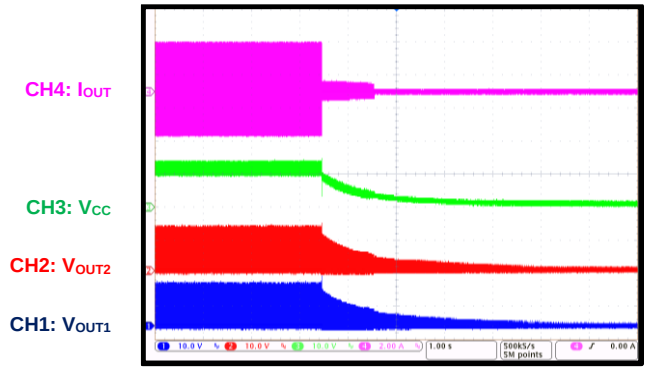
Rotor Lock
PWM duty cycle at 25%



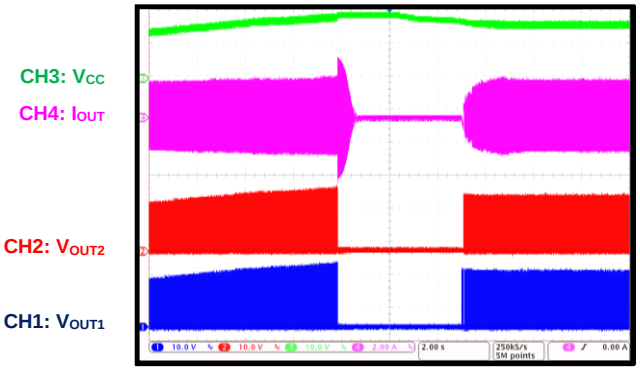
Start-Up through VIN
PWM duty cycle at 100%



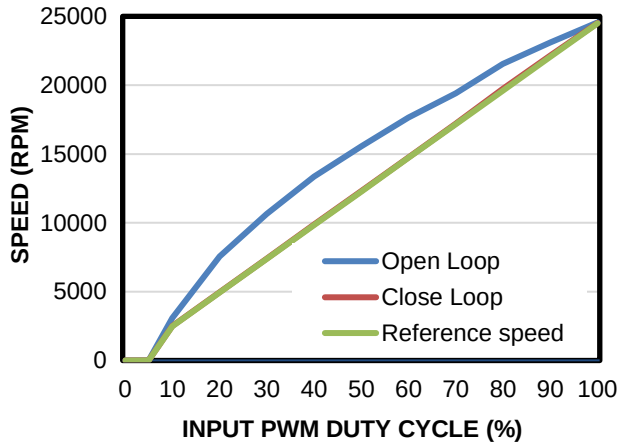
Shutdown through VCC
PWM duty cycle at 100%



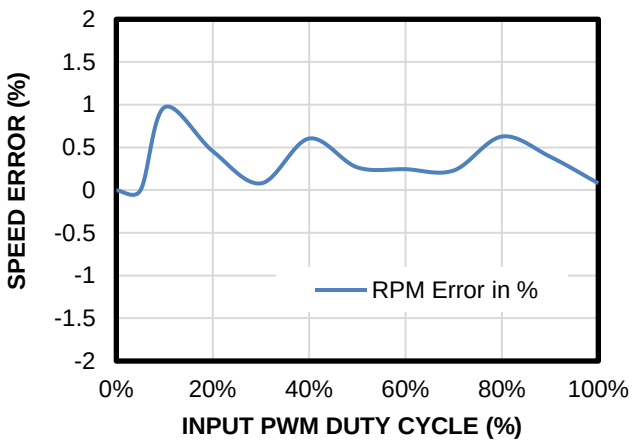
Over-Voltage Protection (OVP)
PWM duty cycle at 25%



Speed vs. PWM Input Duty Cycle



Speed Error vs. PWM Input Duty Cycle



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FUNCTIONAL BLOCK DIAGRAM

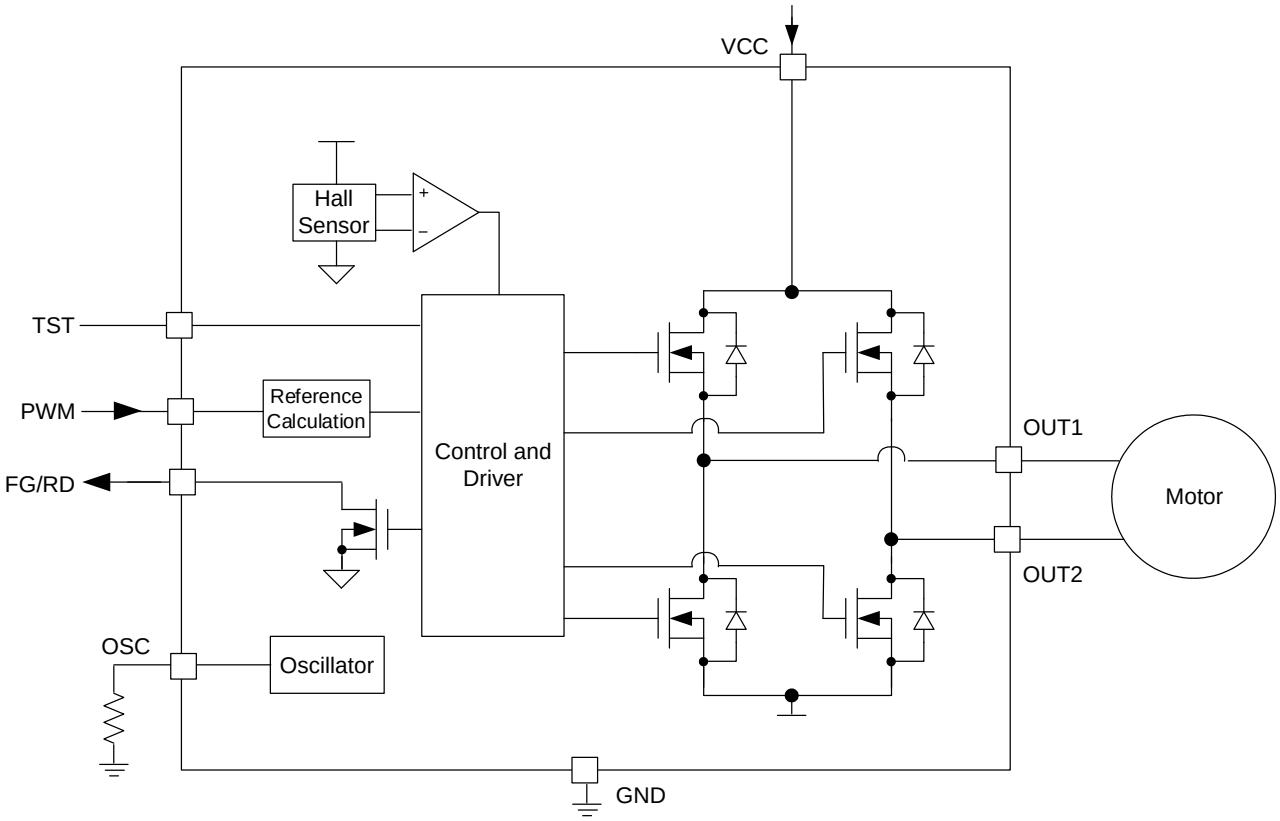

Figure 1: Functional Block Diagram

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OPERATION

The MP6616B is a single-phase, brushless DC (BLDC) motor driver with an embedded Hall-effect sensor and integrated power MOSFETs. The device controls the motor speed with closed-loop or open-loop control via the pulse-width modulation (PWM) signal on the PWM pin. The MP6616B features a configurable soft commutation angle and Hall offset angle. The Hall offset angle can be flexibly optimized for low-speed and high-speed performance across the full speed range.

The MP6616B also features a rotational speed detector (the FG/RD pin). FG/RD is an open drain that outputs a high or low voltage relative to the internal Hall comparator's output.

Protection features include input over-voltage protection (OVP), under-voltage lockout (UVLO) protection, locked rotor protection, over-current protection (OCP), and thermal shutdown.

Speed Control

The PWM signal accepts a wide range of input frequencies (1kHz to 100kHz). There are two speed control modes: closed-loop mode and mixed (closed-loop and open-loop) mode.

Closed-Loop Mode

Closed-loop mode (DIN_OPEN = 0xFF) controls the motor speed by detecting the PWM signal duty cycle. In closed-loop mode, the Hall sensor's signal speed is detected internally and fed back to the control loop, which adjusts the PWM output duty. This makes the motor speed follow the reference.

The SPD_MAX register sets the maximum speed when the input PWM duty cycle is 100%. The SPD_MIN register sets the minimum speed once the input duty starts corner duty, which is set by the DIN_MIN register.

If the PWM input duty cycle is below the duty cycle set by DIN_MIN, then the fan speed can support three modes, depending on the register settings:

1. If SPD_ZERO = 0 and MAX_EN = 0, then SPD_MIN determines the speed (see Figure 2).

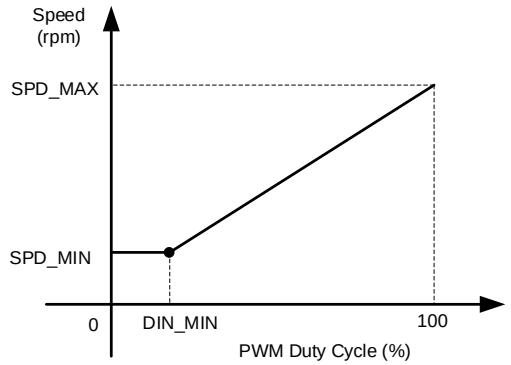

Figure 2: Speed Curve if SPD_ZERO = 0 and MAX_EN = 0

2. If SPD_ZERO = 0 and MAX_EN = 1, then SPD_MAX determines the speed (see Figure 3).

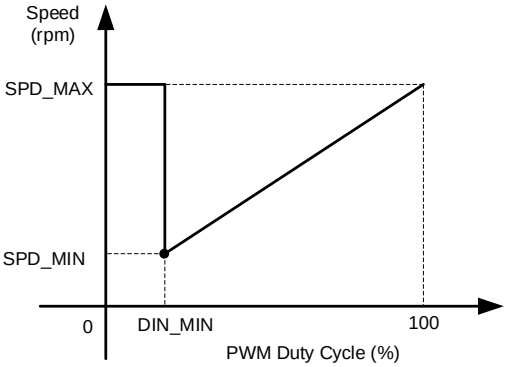

Figure 3: Speed Curve if SPD_ZERO = 0 and MAX_EN = 1

3. If SPD_ZERO = 1 and MAX_EN = x, then the speed is 0rpm (see Figure 4).

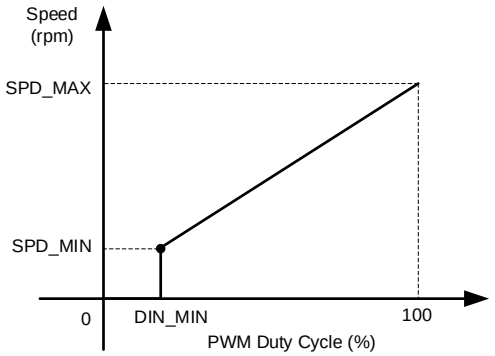

Figure 4: Speed Curve if SPD_ZERO = 1 and MAX_EN = x

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Mixed Mode

Mixed mode employs closed-loop and open-loop operation. The DIN_OPEN register sets the closed-loop and open-loop control boundaries. If the PWM input duty cycle is below DIN_OPEN, then the IC operates with a closed loop. If the PWM input duty cycle is above DIN_OPEN, then the IC operates with an open loop. Figure 5 shows mixed mode.

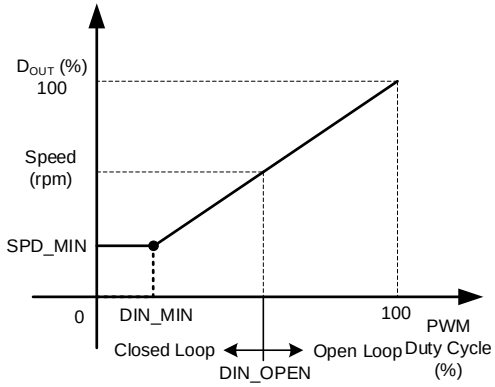

Figure 5: Mixed Mode

OUT1 and OUT2 Operation

To reduce speed variation and increase system efficiency during normal operation, the MP6616B controls the H-bridge MOSFET switching according to the timing sequence. The operation sequence is based on the embedded Hall-effect sensor signal:

- The HALL_TRIM signal has a Hall offset angle with a maximum 45° phase shift (lead or lag).
- If the HALL_TRIM signal is high, then OUT2 is low while OUT1 is the switching phase.
- If the HALL_TRIM signal is low, then OUT1 is low while OUT2 is the switching phase.

The Hall offset angle is set by the corresponding registers with the PWM input duty cycle:

- If the input duty cycle is below the DIN_HAL_L value (DIN_HAL_L/64), then the Hall offset angle is determined by HAL_ANG1.
- If the input duty cycle is between DIN_HAL_L/64 and the DIN_HAL_H value (DIN_HAL_H/64), then the Hall offset angle is determined by HAL_ANG2.
- If the input duty cycle is above DIN_HAL_H/64, then the Hall offset angle is determined by HAL_ANG3.

The Hall offset angle lead and lag directions are set by HAL_FLAG.

Soft-On Commutation

During soft-on commutation, the switching phase output duty cycle gradually increases from 0% to steady duty cycle (see θ_{S_ON} in Figure 6). The maximum transition phase angle set by SON_ANG is 45°. The resolution is 1.4°.

Soft-Off Commutation

During soft-off commutation, the switching phase output duty cycle gradually decreases from steady duty cycle to 0% (see θ_{S_OFF} in Figure 6). The maximum transition phase angle set by SOFF_ANG is 45°. The resolution is 1.4°.

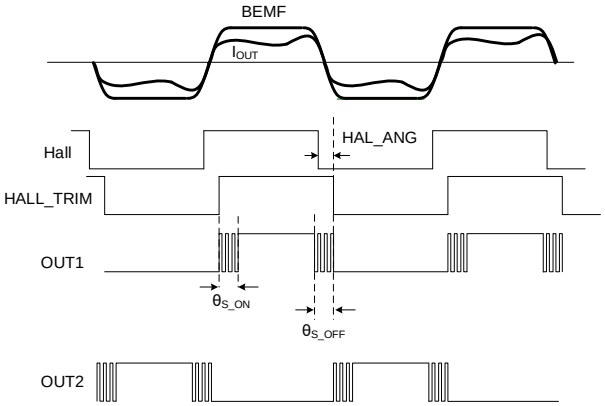

Figure 6: Soft Commutation and Hall Offset Angle

Advanced Soft-Off Angle

The advanced soft-off angle provides a leading non-zero angle to begin soft-off commutation. Figure 7 shows the advanced soft-off angle (θ_{ADV}), which takes an advanced angle once soft-off commutation begins. SOFFADV sets θ_{ADV}, which has a maximum angle of 45°.

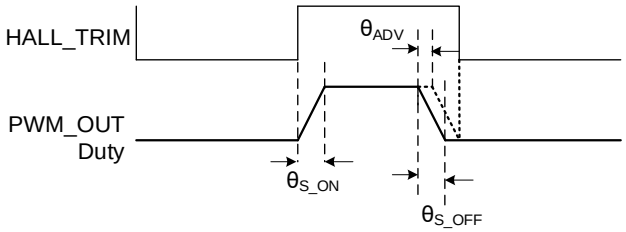

Figure 7: Advanced Soft-Off Angle

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Pre-Start Timer

Once V_{CC} is powered, the switching phase output duty cycle increases gradually. DUTY_SLOPE [1:0] can configure the output duty cycle's incremental slope.

Configured via DUTY_SLOPE:

- 00: 9.3ms timer
- 01: 4.6ms timer
- 10: 2.3ms timer
- 11: 1.2ms timer

During the pre-startup stage, the fan can robustly spin up and the fan current increases smoothly.

A longer timer leads to a lower pre-startup current and longer pre-startup time.

Soft Start (SS)

After the pre-startup stage, the MP6616B initiates a soft start (SS). TIME_SS sets the soft-start time (t_{SS}). In closed-loop control, TIME_SS sets the internal speed reference's increasing or decreasing slope. In open-loop control, TIME_SS sets the PWM output duty cycle's ramping up and down time. The configurable t_{SS} reduces the input inrush current during start-up.

Closed-Loop Integrator Gain

In closed-loop mode, KI_TIMER, bits[1:0] and ERR_GAIN, bits[1:0] configure the closed-loop integrator gain.

Configured via KI_TIMER:

- 00: 9.3ms integrator refresh timer
- 01: 1.2ms integrator refresh timer
- 10: 145µs integrator refresh timer
- 11: 18µs integrator refresh timer

Configured via ERR_GAIN:

- 00: Integrator gain coefficient of 1/8
- 01: Integrator gain coefficient of 1/4
- 10: Integrator gain coefficient of 1/2
- 11: Integrator gain coefficient of 1

A smaller KI_TIMER time or larger ERR_GAIN coefficient leads to a quicker loop response once the loop is steady.

Setting the Switching Frequency (f_{SW})

To provide an accurate clock for speed control, connect a 20kΩ, high-accuracy resistor between the OSC and GND pins. It is recommended to use a resistor with 1% or greater accuracy. The switching frequency (f_{SW}) is about 27kHz.

Digital Oscillator Clock

The digital clock is used for all Hall angle calculations and closed-loop calculations. The digital clock is selected via the SPD_SEL bits. A higher frequency leads to a higher calculation resolution; however, it also leads to a higher minimum speed.

Standby Mode

The STB register bit turns standby mode on and off. Standby mode is off by default.

If standby mode is enabled while the PWM input remains low and there is no Hall signal edge for 600ms, then the MP6616B enters standby mode. In standby mode, most of the internal circuitries are turned off to conserve power. The standby current (I_{STB}) is about 430µA.

Once the PWM pulse is detected on the PWM pin, the MP6616B exits standby mode.

Cycle-by-Cycle Over-Current Protection (OCP)

If the current flowing through the H-bridge HS-FET exceeds the threshold set by OCP_SEL after a blanking time (about 1µs), then the HS-FET turns off and the LS-FET turns on. At the next switching cycle, the HS-FET turns on again and resumes normal operation. The over-current (OC) limit threshold has four configurable values.

Speed Detection

The FG signal on the FG/RD pin outputs an internal Hall-change signal for speed indication. The FG frequency can be 1x, 1/2x, 2/3x, or 2x the Hall frequency, set via the corresponding register bits.

FG/RD is an open-drain output that must be pulled up externally.

Locked-Rotor Protection

If the Hall signal polarity does not change

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during the 0.6s detection time in a rotor-lock fault, then the MP6616B turns both LS-FETs on and auto-restarts after a recovery time (set by LOCK_SEL).

If FGRD_SEL is set to 11, then the FG/RD pin is the rotor lock indicator (RD). Set RD_H_L to 1 to keep the FG/RD signal high during a rotor-lock fault. Set RD_H_L to 0 to keep the FG/RD signal low during a rotor-lock fault.

Over-Voltage Protection (OVP)

If the VCC pin voltage (V_{CC}) exceeds the over-voltage (OV) threshold (19V), then the HS-FETs turn off and the LS-FETs turn on. Once V_{CC} drops below 18V, the MP6616B resumes normal operation.

Thermal Shutdown

Thermal shutdown prevents the device from operating at exceedingly high temperatures. If the IC's junction temperature (T_J) exceeds the thermal shutdown threshold (typically 160°C), then one phase's LS-FET remains on and the other phase's LS-FET goes into a tri-state. Once T_J drops below 120°C, the MP6616B starts up and resumes normal operation.

Under-Voltage Lockout (UVLO) Protection

If V_{CC} drops below the UVLO threshold, then the device shuts down and the internal logic is reset. Once V_{CC} exceeds the UVLO threshold, the MP6616B starts up and resumes normal operation.

Test Mode

The MP6616B includes a test mode to configure the internal register. In test mode, all of the internal registers can be read and written. After designs are finalized, the register values can be configured to the two-time programmable non-volatile memory (NVM). Refer to the MPS Fan Driver GUI software for more information.(6)

Note:

6) Contact an MPS FAE to request the MPS Fan Driver GUI software.

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REGISTER DESCRIPTION

Register Map

Address	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
00h (OTP/REG)	RESERVED	SPD_SEL[1:0]		SOFFADV[4:0]				
01h (OTP/REG)	SPD_MAX[7:0]							
02h (OTP/REG)	SPD_MAX[15:8]							
03h (OTP/REG)	SPD_MIN[7:0]							
04h (OTP/REG)	DIN_MIN[7:0]							
05h (OTP/REG)	DIN_OPEN[7:0]							
06h (OTP/REG)	TIME_SS[2:0]			RVSI_EN	KI_TIMER[1:0]		ERR_GAIN[1:0]	
07h (OTP/REG)	SPD_ZERO	OCP_SEL[1:0]		SON_ANG[4:0]				
08h (OTP/REG)	RD_H_L	LOCK_SEL[1:0]		SOFF_ANG[4:0]				
09h (OTP/REG)	RESERVED		HAL_FLAG	HAL_ANG1[4:0]				
0Ah (OTP/REG)	RESERVED			HAL_ANG2[4:0]				
0Bh (OTP/REG)	DUTY_SLOPE[1:0]		RESERVED	HAL_ANG3[4:0]				
0Ch (OTP/REG)	FGRD_SEL[1:0]		DIN_HAL_L[5:0]					
0Dh (OTP/REG)	RESERVED		DIN_HAL_H[5:0]					
0Eh (OTP/REG)	RESERVED			STB	2FG	MAX_EN	RESERVED	
0Fh (REG)	OTP_PAGE[1:0]		RESERVED					

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DIGITAL_FREQ_SOFT_OFF_ADV (00h)

The DIGITAL_FREQ_SOFT_OFF_ADV command sets the digital clock and advanced soft-off angle.

Bits	Access	Bit Name	Default	Description
7	R	NA	0	Reserved
6:5	R/W	SPD_SEL[1:0]	00	Sets the digital clock. A higher frequency leads to a higher calculation resolution; however, it also leads to a higher minimum speed. These bits indicate the supported minimum speeds (2-pair-pole motor). 00: 100r/min (default) 01: 400r/min 10: 800r/min 11: 1600r/min
4:0	R/W	SOFFADV[4:0]	00000	Sets the advanced soft-off angle after soft-off commutation starts. 00: 1.4° (default) 01: 2.8° …1F: 45° 1.4° per step, θ_{ADV} = 1.4° x (SOFFADV + 1)

SPD_MAX1 (01h)

The SPD_MAX1 command sets the maximum speed in closed-loop control.

Bits	Access	Bit Name	Default	Description
7:0	R/W	SPD_MAX[7:0]	0x20	Sets the maximum speed. LSB of the maximum speed. This register works together with SPD_MAX[15:8] to set the speed when the PWM input duty cycle is 100%. 1 LSB = 1rpm. The default is 20000rpm (2-pair-pole motor).

SPD_MAX2 (02h)

The SPD_MAX2 command sets the maximum speed in closed-loop control.

Bits	Access	Bit Name	Default	Description
7:0	R/W	SPD_MAX[15:8]	0x4E	Sets the maximum speed. MSB of the maximum speed. This register works together with SPD_MAX[7:0] to set the speed when the PWM input duty is 100%. The default is 20000rpm (2-pair-pole motor).

SPD_MIN (03h)

The SPD_MIN command sets the minimum speed in closed-loop control or the output duty cycle at the starting duty cycle.

Bits	Access	Bit Name	Default	Description
7:0	R/W	SPD_MIN[7:0]	0x33	These bits have three functions: 1. Set the minimum speed. 2. Set the speed once the PWM input duty cycle = DIN_MIN in closed-loop control. The minimum speed = SPD_MIN x 32 (default 1632rpm). 3. Set the output duty cycle once the PWM input duty cycle = DIN_MIN in open-loop control. The output duty cycle = SPD_MIN / 255 (default 20%).

DIN_MIN (04h)

The DIN_MIN command sets the PWM input starting corner duty cycle.

Bits	Access	Bit Name	Default	Description
7:0	R/W	DIN_MIN[7:0]	0x33	PWM input starting corner duty. The starting corner duty is DIN_MIN / 255. The default duty is 20%.

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DIN_OPEN (05h)

The DIN_OPEN command sets the PWM input corner duty cycle for closed-loop and open-loop control.

Bits	Access	Bit Name	Default	Description
7:0	R/W	DIN_OPEN[7:0]	0x00	Sets the PWM input corner duty for closed-loop and open-loop control. If the input duty cycle exceeds DIN_OPEN / 255, the IC operates in open-loop mode. If the input duty cycle drops below DIN_OPEN / 255, the IC operates in closed-loop mode.

SS_RVS_KI_GAIN (06h)

The SS_RVS_KI_GAIN command sets the soft-start time (t_{SS}), enables reverse current detection, and controls the integral timer and gain in closed-loop mode.

Bits	Access	Bit Name	Default	Description
7:5	R/W	TIME_SS[2:0]	010	Sets the soft-start time. 000: 2.4s 001: 4.8s 010: 7.2s (default) 011: 9.6s 100: 12s 101: 14.4s 110: 16.8s 111: 19.2s
4	R/W	RVSI_EN	1	Enables reverse current detection. 0: Disabled 1: Enabled (default)
3:2	R/W	KI_TIMER[1:0]	10	Controls the integral timer in closed-loop mode. 00: 9.3ms 01: 1.2ms 10: 145µs (default) 11: 18µs
1:0	R/W	ERR_GAIN[1:0]	11	Controls the integral gain in closed-loop mode. 00: 1/8 01: 1/4 10: 1/2 11: 1 (default)

SPD0_OCP_SON (07h)

The SPD0_OCP_SON command enables the zero speed function, and sets the current limit threshold and soft-on commutation angle.

Bits	Access	Bit Name	Default	Description
7	R/W	SPD_ZERO	1	Indicates the speed when the PWM input duty cycle < DIN_MIN. 0: Maintains the minimum or maximum speed 1: Stop (default)
6:5	R/W	OCP_SEL[1:0]	11	Sets the current limit. 00: 1A 01: 2A 10: 3A 11: 4.3A (default)

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4:0	R/W	SON_ANG[4:0]	0x1F	Sets the soft-on phase transition angle. 00: 1.4° 01: 2.8° … 1F: 45° (default) 1.4° per step, θ_{S_ON} = 1.4° x (SON_ANG + 1)

RD_SOFF (08h)

The RD_SOFF command sets the FG/RD output high/low selection, the lock retry time for rotor-lock protection, and the soft-off commutation angle.

Bits	Access	Bit Name	Default	Description
7	R/W	RD_H_L	1	Sets the FG/RD high/low output. 0: FG/RD outputs low during locked-rotor protection 1: FG/RD outputs high during locked-rotor protection (default)
6:5	R/W	LOCK_SEL[1:0]	00	Sets the rotor-lock retry time. 00: 3.6s (default) 01: 4.8s 10: 6s 11: 8.4s
4:0	R/W	SOFF_ANG[4:0]	0x1F	Sets the soft-off phase transition angle. 00: 1.4° 01: 2.8° … 1F: 45°(default) 1.4° per step, θ_{S_OFF} = 1.4° x (SOFF_ANG + 1)

HAL_ANG1 (09h)

The HAL_ANG1 command sets the Hall offset angle lead or lag, and the Hall offset angle at low duty cycles.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	00	Reserved.
5	R/W	HAL_FLAG	0	Sets the Hall offset angle for lead or lag. 0: Lag 1: Lead
4:0	R/W	HAL_ANG1[4:0]	00000	Sets the Hall offset angle when the PWM duty cycle < DIN_HAL_L. 00: 1.4° (default) 01: 2.8° … 1F: 45° 1.4° per step, Hall offset angle = 1.4° x (HAL_ANG1 + 1)

HAL_ANG2 (0Ah)

The HAL_ANG2 command sets the Hall offset angle at middle duty cycles.

Bits	Access	Bit Name	Default	Description
7:5	R	RESERVED	000	Reserved.

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4:0	R/W	HAL_ANG2[4:0]	00000	Sets the Hall offset angle when DIN_HAL_L < PWM duty < DIN_HAL_H. 00: 1.4° (default) 01: 2.8° … 1F: 45° 1.4° per step, Hall offset angle = 1.4° x (HAL_ANG2 + 1)

SLOPE_HAL_ANG3 (0Bh)

The SLOPE_HAL_ANG3 command sets the pre-startup timer and Hall offset angle at high duty cycles.

Bits	Access	Bit Name	Default	Description
7:6	R/W	DUTY_SLOPE [1:0]	00	Sets the pre-startup timer. 00: 9.3ms (default) 01: 4.6ms 10: 2.3ms 11: 1.2ms
5	R	RESERVED	1	Reserved.
4:0	R/W	HAL_ANG3[4:0]	00000	Sets the Hall offset angle when the PWM duty cycle > DIN_HAL_H. 00: 1.4° (default) 01: 2.8° … 0x1F: 45° 1.4° per step, Hall offset angle = 1.4° x (HAL_ANG3 + 1)

FGRD_DIN_HAL_L (0Ch)

The FGRD_DIN_HAL_L command sets the FG/RD pin output and PWM input duty cycle low threshold for the Hall offset angle.

Bits	Access	Bit Name	Default	Description
7:6	R/W	FGRD_SEL[1:0]	00	Selects the FG/RD pin output. 00: 1x (default) 01: 1/2x 11: RD If FGRD_SEL = 10, then the 2FG bit selects the FG/RD pin output (2/3x or 2x). See register 0Eh on page 22 for more details.
5:0	R/W	DIN_HAL_L[5:0]	0x10	Sets the PWM input duty cycle for the Hall offset angle's low threshold: Duty Cycle = DIN_HAL_L / 64 The default duty cycle is 25%.

DIN_HAL_H (0Dh)

The DIN_HAL_H command sets the PWM input duty cycle high threshold for the Hall offset angle.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	00	Reserved.
5:0	R/W	DIN_HAL_H[5:0]	0x30	Sets the PWM input duty cycle for the Hall offset angle's high threshold. Duty Cycle = DIN_HAL_H / 64 The default duty cycle is 75%.

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CFR (0Eh)

The CFR command enables standby mode, and sets the FG/RD pin output and maximum speed below the starting duty cycle.

Bits	Access	Bit Name	Default	Description
7:5	R	RESERVED	000	Reserved.
4	R/W	STB	0	Enables standby mode. 0: Disabled (default) 1: Enabled
3	R/W	2FG	0	Selects the FG/RD pin output (2/3x or 2x) when FGRD_SEL = 10. FGRD_SEL = 10, 2FG = 0: 2/3x (default) FGRD_SEL = 10, 2FG = 1: 2x
2	R/W	MAX_EN	0	Enables the maximum speed when the PWM input duty cycle < DIN_MIN. This bit is only active when SPD_ZERO = 0. 0: Disabled (default) 1: Enabled
1:0	R	RESERVED	00	Reserved.

OTP_PAGE(0Fh)

The OTP_PAGE command indicates which one-time programmable (OTP) memory page is programmed.

Bits	Access	Bit Name	Default	Description
7:6	R	OTP_PAGE[1:0]	00	OTP page program indicator, read-only. 00: No OTP pages are programmed (default) 01: 1st page of OTP is programmed 10: 2nd page of OTP is programmed.
5:0	R	RESERVED	N/A	Reserved.

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APPLICATION INFORMATION

Selecting the Input Capacitor

Place an input capacitor (C_{IN}) as close to the VCC and GND pins as possible to maintain a stable input supply voltage (V_{CC}) and reduce noise at the input. C_{IN} must have a low impedance at f_{SW}.

Ceramic capacitors with X7R dielectrics are recommended for their low ESR characteristics. The ceramic capacitance is dependent on the DC voltage rating. If the ceramic capacitor is biased to its DC voltage rating, then its capacitance drops below 50%.

Ensure that C_{IN} has a large enough voltage rating margin. C_{IN} must be greater than 10µF.

In some applications, an additional large, electrolytic capacitor may be required to absorb the motor's energy.

Embedded Hall-Effect Sensor

Figure 8 shows the position of the MP6616B's embedded Hall-effect sensor.

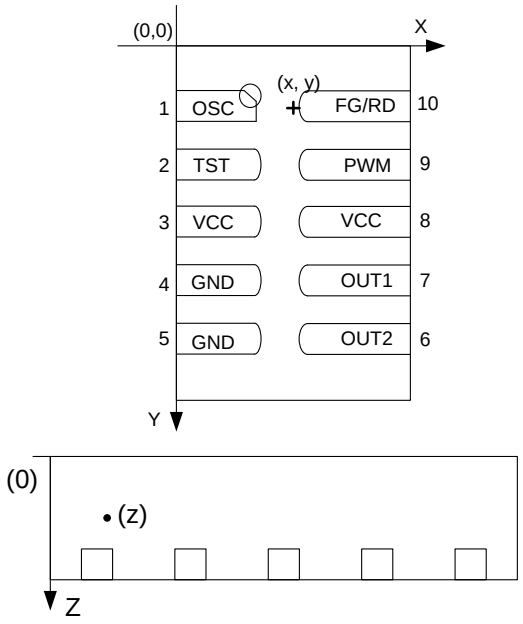

Figure 8: Embedded Hall Sensor (7)

Note:

7) Where x = 1003 ± 40µm, y = 620 ± 40µm, and z = 370 ± 40µm.

Selecting the Reverse-Blocking Diode

A reverse-blocking diode is required while the fan is plugged in reversely to avoid damage. The reverse-blocking diode prevents the bus voltage (V_{BUS}) from charging up via the fan's reverse current.

The blocking diode's maximum reverse voltage should exceed 30V, and the forward current rating of the blocking diode should exceed the input current (I_{IN}).

Selecting the OSC Resistor

A 20kΩ OSC resistor is required to set up the internal clock. A high-accuracy resistor is recommended. For most applications, a resistor with 1% or greater accuracy is sufficient.

Place the OSC resistor close to the IC. The OSC's resistor must be routed away from the power path to avoid changing the internal clock's frequency under different load currents.

Selecting the Input Clamping Circuit

A voltage-clamping circuit is required, particularly in large current applications and inertial fan applications, to avoid high-voltage spikes caused by the energy stored in the motor inductor (see Figure 13 on page 17). For most 12V input applications, a 15V TVS diode or Zener diode in a SOD-123 package is sufficient. The clamping voltage should be below the OVP threshold. Typically, if the maximum operating ambient temperature rises, then ZD1's clamping voltage threshold rises.

System-Level Electrostatic Discharge (ESD)

Some fan products may be required to pass a system-level electrostatic discharge (ESD) test. Different from chip-level ESD (HBM), the system-level ESD surge energy is much higher.

Figure 9 shows a typical chip-level ESD human body model (HBM) ESD circuit.

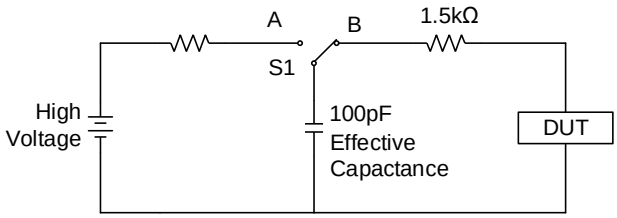

Figure 9: Typical HBM ESD Test Circuit

Figure 10 shows a system-level ESD circuit that follows the IEC61000-4-2 standard.

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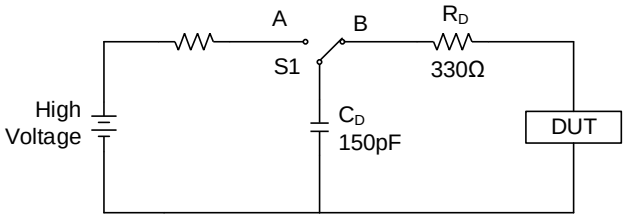

Figure 10: IEC ESD Test Circuit

The system-level (IEC61000-4-2) ESD test circuit's discharge capacitance is greater than that of the HBM ESD test circuit. The IEC ESD test circuit's discharge resistor is also smaller than that of the HBM ESD test circuit. The IEC ESD test has greater energy and surge current than the HBM ESD test.

The MP6616B can directly pass IEC ESD contact 8kV ESD discharge testing without any additional circuitry.

Placing a series resistor on the FG/RD pin and a resistor on the PWM pin can sufficiently enhance ESD capability (see Figure 11).

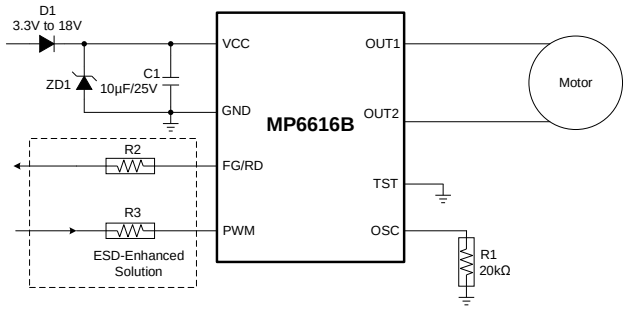

Figure 11: ESD Enhancement via Resistors

If a higher ESD level is required, an external clamping circuit may be needed. Figure 12 shows as an example to pass >12kV IEC ESD testing with an external ESD-enhanced circuit. The external resistors (R2 and R3) and external clamping diodes (ZD2 and ZD3) enhance ESD capability. For most applications, R2 and R3 should be between 30Ω and 100Ω. ZD2 and ZD3 should be Zener diodes, ESD diodes, or TVS diodes in SOD-323 or SOD-523 packages.

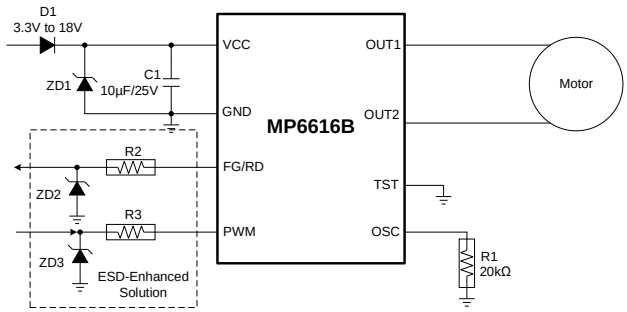

Figure 12: External ESD-Enhanced Circuit

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PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 13 and follow the guidelines below:

1. To reduce noise at the input, place a 10µF or greater input capacitor as close to the IC as possible (see C2 and C3 in Figure 13).
2. To reduce high-frequency noise, place a 10nF to 100nF input capacitor in a small, 0402 package as close to the VCC and GND pins as possible (see C1 in Figure 13).
3. Place the OSC resistor as close to the IC as possible. Route the OSC resistor away from any power paths (see R1 in Figure 13).

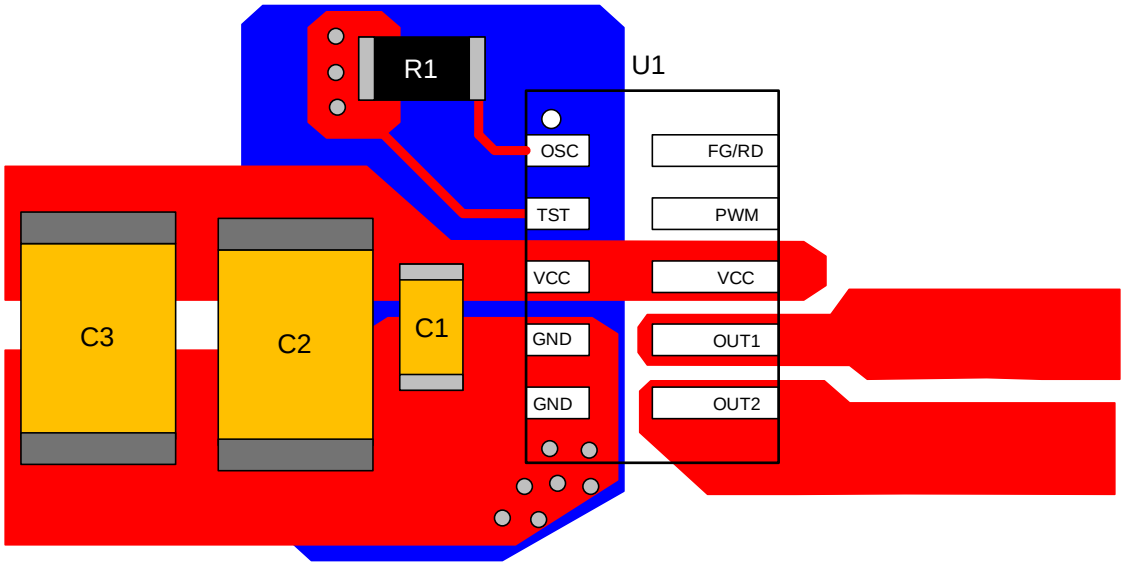

Figure 13: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUIT

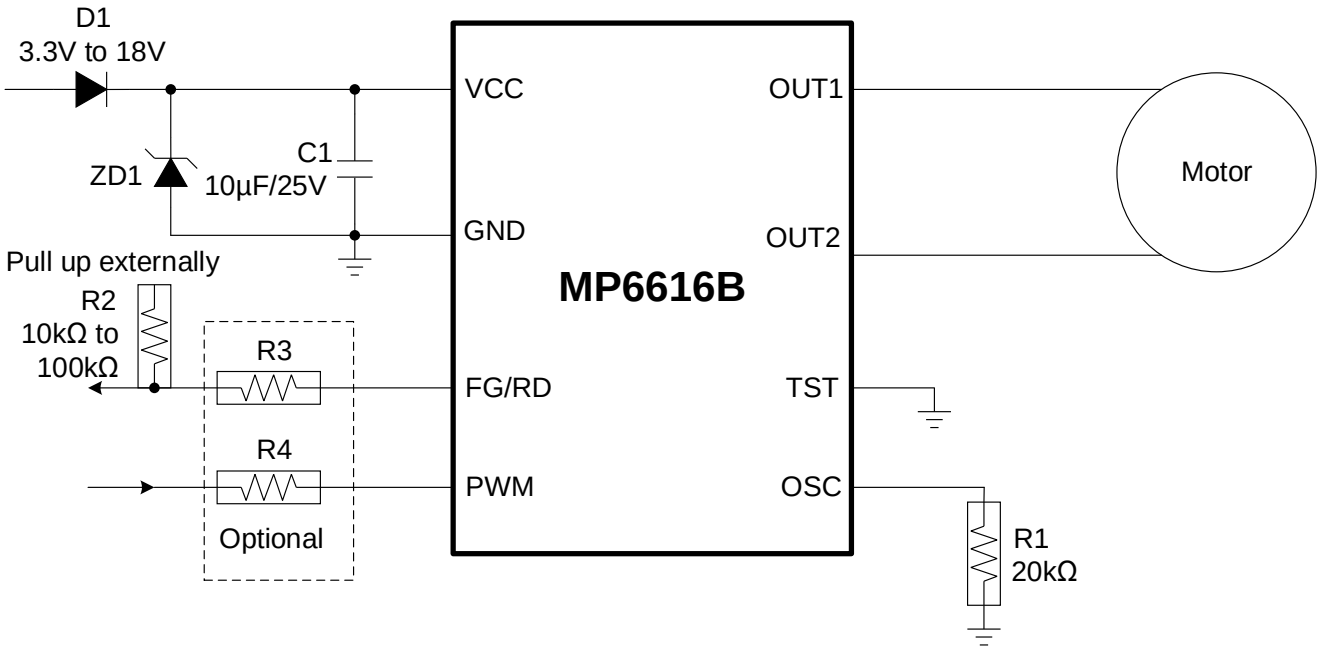

Figure 14: Typical Application Circuit

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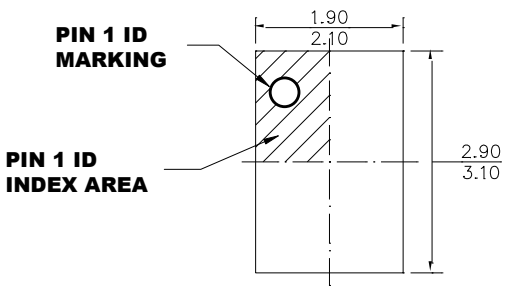
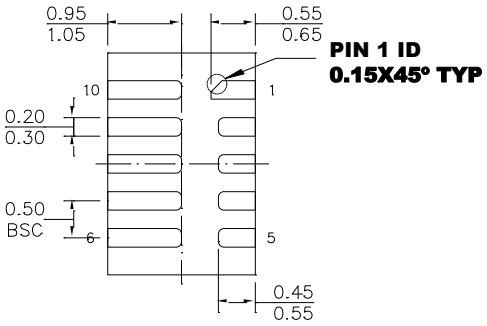
PACKAGE INFORMATION

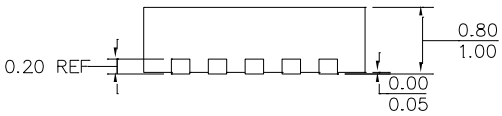
QFN-10 (2mmx3mm)



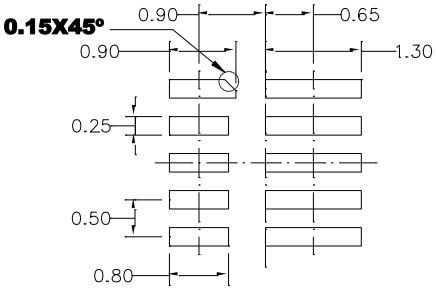
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

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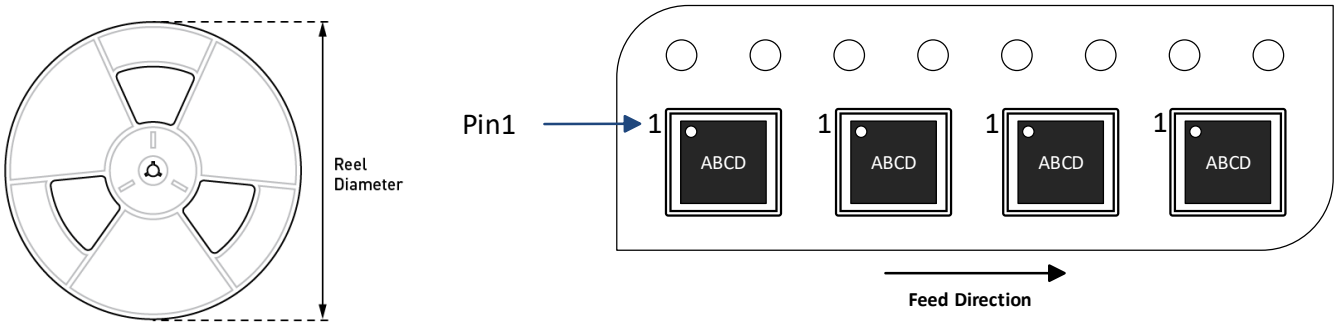
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6616BGD-Z	QFN-10 (2mmx3mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/12/2025	Initial Release	-

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