MP6540H, MP6540HA

50V, 5A, Three-Phase Power Stage

DESCRIPTION

The MP6540H and MP6540HA are three-phase brushless DC motor drivers. These devices integrate three half-bridges consisting of six N-channel power MOSFETs, pre-drivers, gate drive power supplies, and current-sense amplifiers.

The MP6540H has enable (EN) and PWM inputs for each half-bridge, while the MP6540HA has separate high-side and low-side inputs. Otherwise, both parts are identical. References to the MP6540H in this document also apply to the MP6540HA, unless otherwise noted.

The MP6540H can deliver up to 6A of peak current and 5A of continuous output current, based on thermal and PCB conditions. The MP6540H uses an internal charge pump to generate the gate drive supply voltage for the high-side MOSFETs, and a trickle charge circuit that maintains sufficient gate drive voltage to operate at 100% duty cycle.

Internal safety features include thermal shutdown, under-voltage lockout (UVLO), and over-current protection (OCP).

The MP6540H is available in a QFN-26 (5mmx5mm) package.

FEATURES

- 5.5V to 50V Operating Supply Voltage
- Three Integrated Half-Bridge Drivers
- Maximum 5A Output Current, 6A Peak Current
- MOSFET On Resistance: HS + LS 45mΩ
- MP6540H: PWM and Enable Inputs
  MP6540HA: HS and LS Inputs
- Internal Charge Pump Supports 100% Duty Cycle Operation
- Automatic Synchronous Rectification
- UVLO and Thermal Shutdown Protection
- Over-Current Protection (OCP)
- Integrated Bidirectional Current-Sense Amplifiers
- Available in a QFN-26 (5mmx5mm) Package

APPLICATIONS

- Brushless DC Motors
- Permanent Synchronous Magnet Motors

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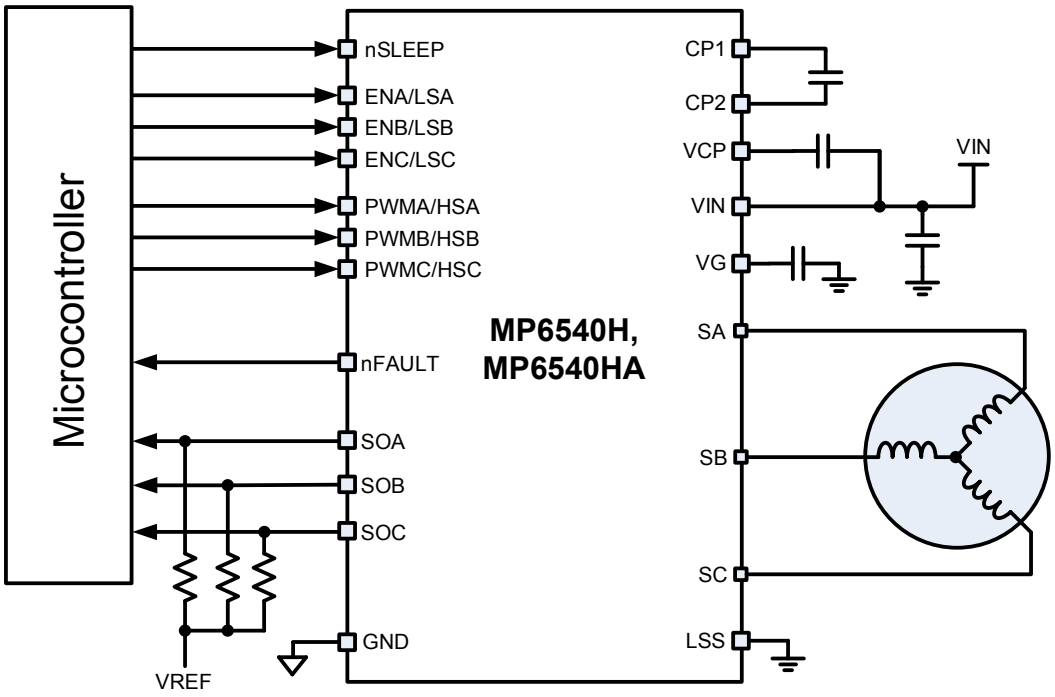
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MP6540HGU*	QFN-26 (5mmx5mm)	*See Below*	1
MP6540HGU-A**	QFN-26 (5mmx5mm)	*See Below*	

* For Tape & Reel, add suffix –Z (e.g. MP6540HGU–Z).
** For Tape & Reel, add suffix –Z (e.g. MP6540HGU-A–Z).

TOP MARKING (MP6540HGU)

MPSYYWW
MP6540H
LLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP6540H: Part number
LLLLLLL: Lot number

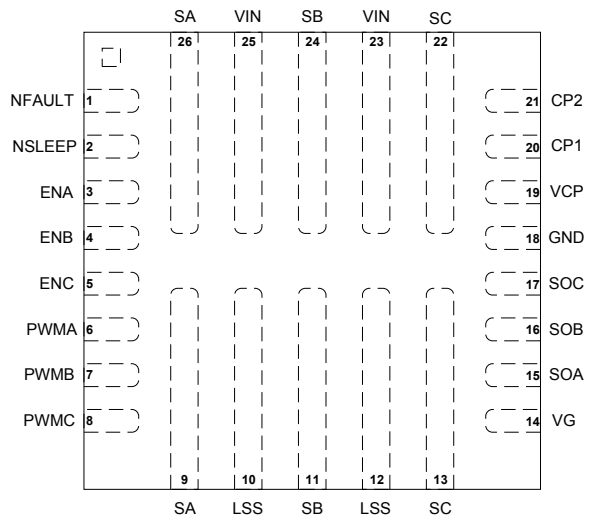
TOP MARKING (MP6540HGU-A)

MPSYYWW
MP6540H
LLLLLLL
A

MPS: MPS prefix
YY: Year code
WW: Week code
MP6540H: Part number
LLLLLLL: Lot number
A: Part number suffix

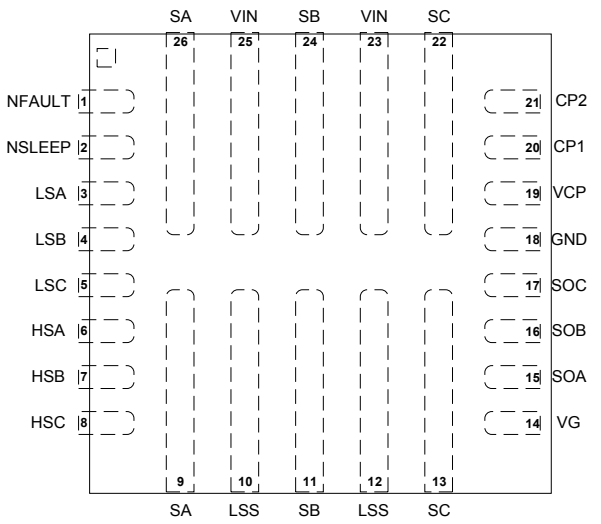
PACKAGE REFERENCE

TOP VIEW



MP6540H
QFN-26 (5mmx5mm)

TOP VIEW



MP6540HA
QFN-26 (5mmx5mm)

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PIN FUNCTIONS

Pin #	MP6540H	MP6540HA	Description
1	nFAULT		**Fault indication.** nFAULT is an open-drain output. nFAULT is in logic low under fault conditions.
2	nSLEEP		**Sleep mode input.** Drive nSLEEP to logic low to enter low-power sleep mode. Drive nSLEEP to logic high for normal operation. nSLEEP is pulled down internally.
3	ENA	N/A	**Enable pin for phase A.**
	N/A	LSA	**Enable low-side MOSFET for phase A.**
4	ENB	N/A	**Enable pin for phase B.**
	N/A	LSB	**Enable low-side MOSFET for phase B.**
5	ENC	N/A	**Enable pin for phase C.**
	N/A	LSC	**Enable low-side MOSFET for phase C.**
6	PWMA	N/A	**PWM input pin for phase A.**
	N/A	HSA	**Enable high-side MOSFET for phase A.**
7	PWMB	N/A	**PWM input pin for phase B.**
	N/A	HSB	**Enable high-side MOSFET for phase B.**
8	PWMC	N/A	**PWM input pin for phase C.**
	N/A	HSC	**Enable high-side MOSFET for phase C.**
9, 26	SA		**Phase A output.**
10, 12	LSS		**Low-side MOSFET source connection for Phases A, B, and C.** LSS must be connected directly to ground.
11, 24	SB		**Phase B output.**
13, 22	SC		**Phase C output.**
14	VG		**Low-side gate drive voltage bypass.** Connect a 4.7μF, 10V, X7R ceramic capacitor from VG to ground.
15	SOA		**Current-sense output for phase A.**
16	SOB		**Current-sense output for phase B.**
17	SOC		**Current-sense output for phase C.**
18	GND		**Ground.**
19	VCP		**Charge pump output.** Connect a 1μF, 16V, X7R ceramic capacitor from VCP to VIN.
20	CP1		**Charge pump capacitor pins.** Connect a 100nF, X7R ceramic capacitor (with a voltage rating that at minimum meets the VIN voltage) between these terminals.
21	CP2		
23, 25	VIN		**Input supply voltage.**

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ABSOLUTE MAXIMUM RATINGS (1)

Input supply voltage (V_{IN})..... -0.3V to +60V
VCP, CP2.....V_{IN} to V_{IN} + 6.5V
SA/B/C, CP1 ..... -0.3V to +60V
All other pins to GND ..... -0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
..... 5.58W
Storage temperature .....-55°C to +150°C
Junction temperature ..... 150°C
Lead temperature (solder) ..... 260°C

ESD Rating

Human body model (HBM) ..... ±2kV
Charged device model (CDM) ..... ±2kV

Recommended Operating Conditions (3)

Input supply voltage (V_{IN})..... 5.5V to 50V
Operating junction temp (T_J).....-40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-26 (5mmx5mm)…….…22.4….18.4…°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the device will go into thermal shutdown.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, T_A = 25°C, LSS = GND = 0V, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input supply voltage	V_{IN}		5.5		50	V
Quiescent current	I_Q	nSLEEP = 1, ENx = 0		0.8	1.3	mA
	I_{SLEEP}	nSLEEP = 0		0.75	3.5	µA
Operation current		nSLEEP = 1, ENx = 1, PWMx = 20kHz		4	5.5	mA
		nSLEEP = 1, ENx = 1, PWMx = 50kHz		8	9.5	mA
		nSLEEP = 1, ENx = 1, PWMx = 100kHz		14	16.5	mA
		nSLEEP = 1, ENx = 1, PWMx = 200kHz		25	29.5	mA
Control Logic						
Input logic low threshold	V_{IL}		0.8		1.45	V
Input logic high threshold	V_{IH}		1.1		2	V
Logic input current	$I_{IN(H)}$	V = 5V		4.7	6	µA
	$I_{IN(L)}$	V = 0V	-1		+1	µA
Start-up delay	t_{PUD}	At V_{IN} rising or nSLEEP rising	3		10	ms
Internal pull-down resistance	R_{PD}	All logic inputs		1		MΩ
nFAULT pull-down R_{ON} (5)	$R_{ON(NFAULT)}$			27		Ω
Protection Circuits						
UVLO threshold	V_{UVLO}	V_{IN} rising	4		5.5	V
UVLO hysteresis	ΔV_{UVLO}			250		mV
HS OCP threshold (5)	$I_{OCP(HS)}$		10	13	17	A
LS OCP threshold (5)	$I_{OCP(LS)}$		10	13	17	A
OCP deglitch time (5)	t_{OCD}			0.4		µs
OCP retry time (5)	t_{OCR}			10		ms
Thermal shutdown (5)	T_{TSD}			150		°C
Thermal shutdown hysteresis (5)	ΔT_{TSD}			25		°C
Current Sense						
Current-sense ratio		LS-FET current = ±3A	1/10500	1/9200	1/7800	A/A
Current-sense output current		LS-FET current = 1A	103	114	125	µA
		LS-FET current = -1A	103	114	125	µA
Current-sense output voltage swing		Sink or source 0.25A into Sx pin	0		5.5	V
Output						
HS-FET on resistance	$R_{ON(HS)}$	I_{OUT} = 1A, T_J = 25°C		25	29	mΩ
		I_{OUT} = 1A, T_J = 125°C		32		
LS-FET on resistance	$R_{ON(LS)}$	I_{OUT} = 1A, T_J = 25°C		20	23.5	
		I_{OUT} = 1A, T_J = 125°C		26		
Output rise time		I_{OUT} = 1A		0.33		V/ns
Output fall time		I_{OUT} = 1A		0.32		V/ns

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, T_A = 25°C, LSS = GND = 0V, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Charge Pump						
Charge pump output voltage	V_{CP}			V_{IN} + 5.5		V
V_{CP} switching frequency	f_{CP}			196		kHz

Note:

5) Guaranteed by design.

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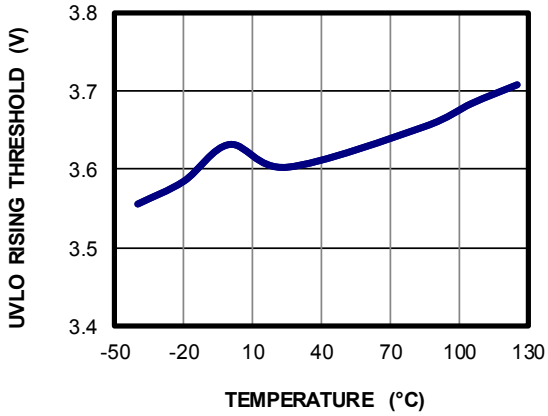
TYPICAL CHARACTERISTICS

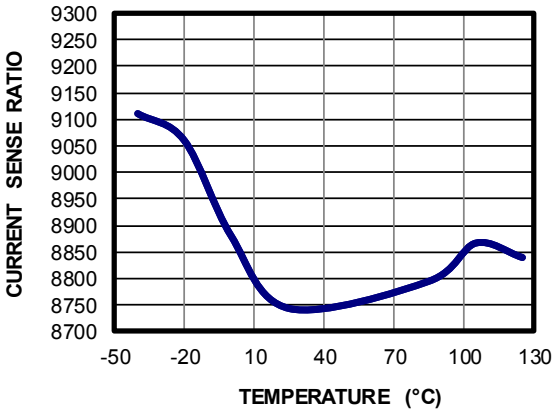
V_{IN} = 24V, T_A = 25°C, LSS = GND = 0V, unless otherwise noted

UVLO Rising Threshold vs. Temperature



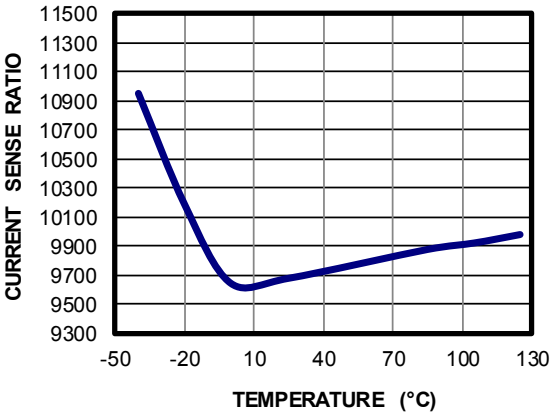
Phase A Current-Sense Ratio vs. Temperature

V_{IN} = 24V, I_{OUT} = 1A



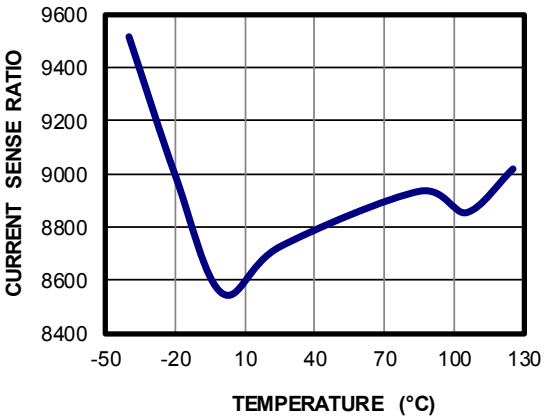
Phase B Current-Sense Ratio vs. Temperature

V_{IN} = 24V, I_{OUT} = 1A



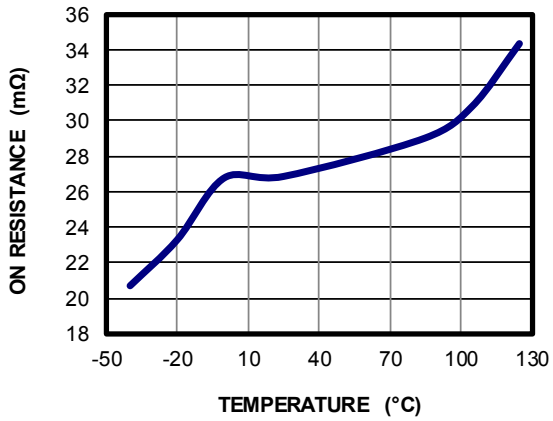
Phase C Current-Sense Ratio vs. Temperature

V_{IN} = 24V, I_{OUT} = 1A



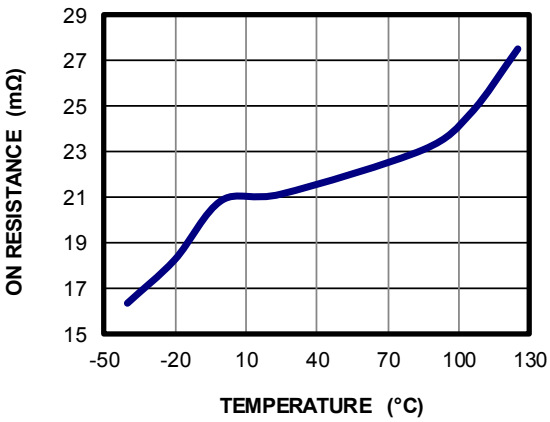
HS On Resistance vs. Temperature

V_{IN} = 24V, I_{OUT} = 1A



LS On Resistance vs. Temperature

V_{IN} = 24V, I_{OUT} = 1A



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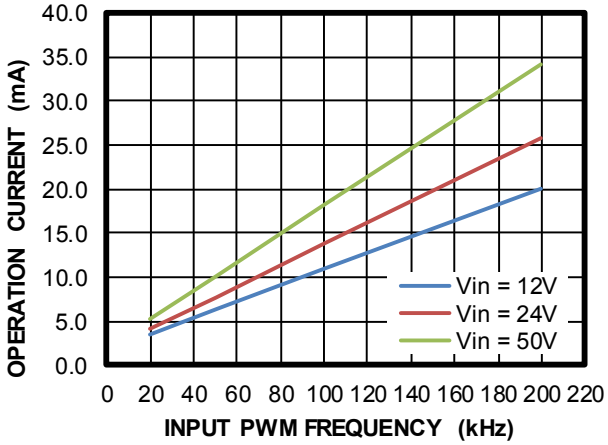
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, T_A = 25°C, LSS = GND = 0V, unless otherwise noted

Operation Current vs. PWM Frequency

Three half-bridges use one 50% duty input PWM signal, no load



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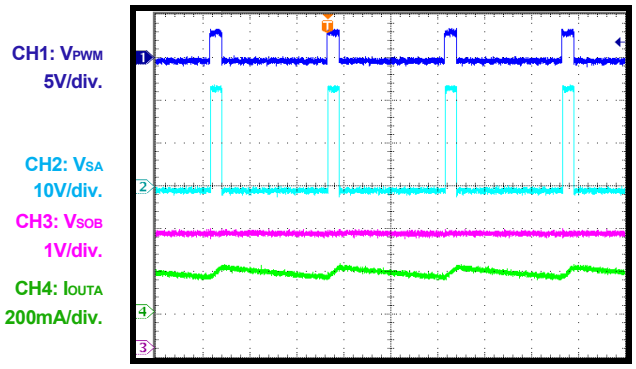
TYPICAL PERFORMANCE CHARACTERISTICS

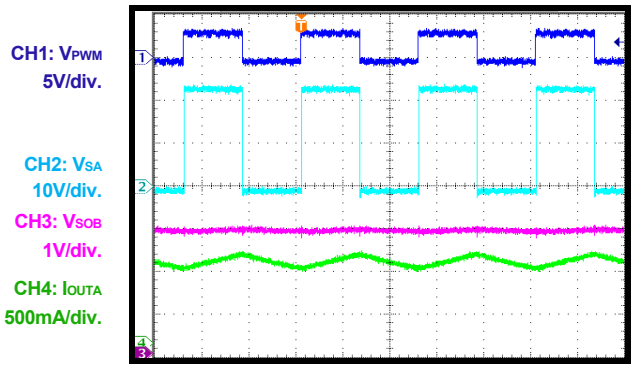
V_{IN} = 24V, V_{REF} = 5V, phase A switching with 20kHz frequency, phase B LS on, phase C disabled, current-sense resistor divider = 5kΩ, resistor and inductor load: R = 5Ω, L = 1mH/phase with star connection, T_A = 25°C, unless otherwise noted.

Steady State
Duty cycle = 10%



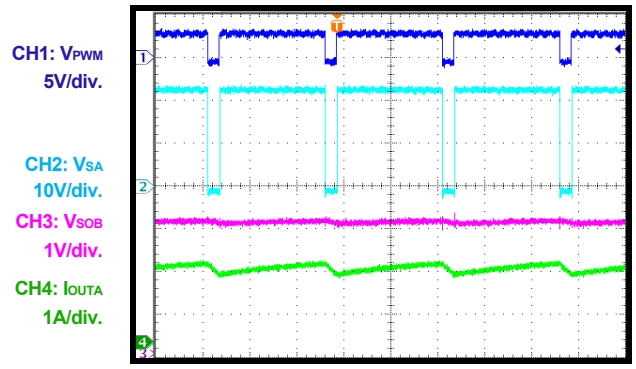
20µs/div.

Steady State
Duty cycle = 50%



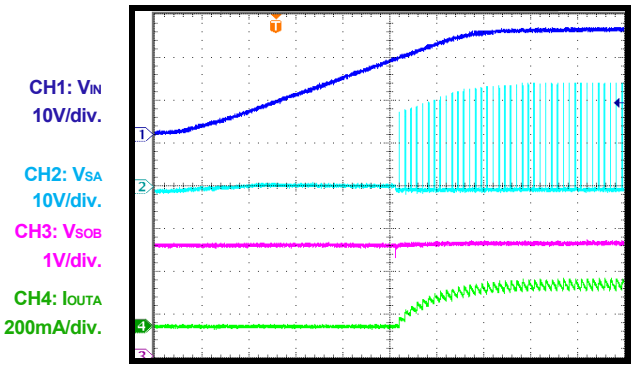
20µs/div.

Steady State
Duty cycle = 90%



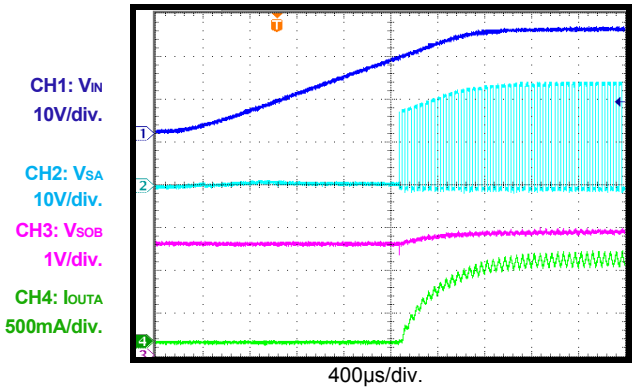
20µs/div.

Power Ramp-Up
Duty cycle = 10%



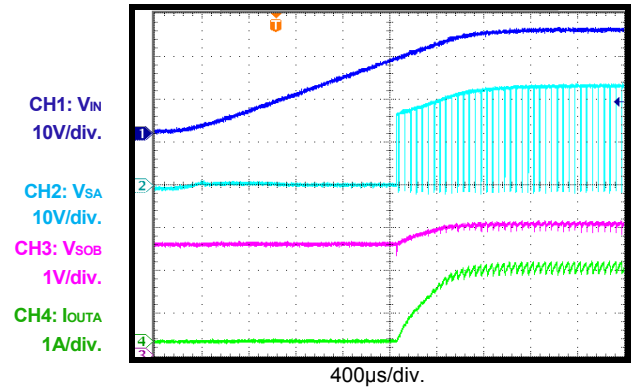
400µs/div.

Power Ramp-Up
Duty cycle = 50%



400µs/div.

Power Ramp-Up
Duty cycle = 90%



400µs/div.

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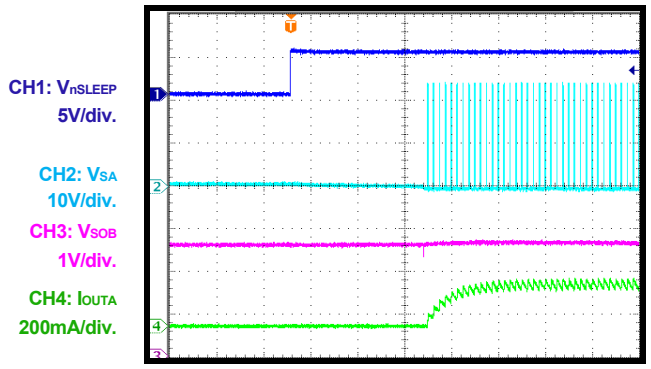
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

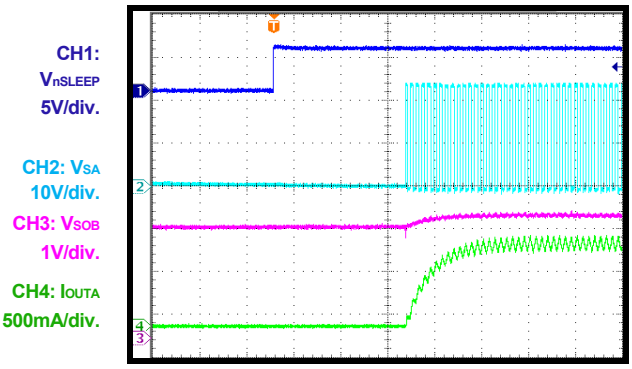
V_{IN} = 24V, V_{REF} = 5V, phase A switching with 20kHz frequency, phase BLS on, phase C disabled, current-sense resistor divider = 5kΩ, resistor and inductor load: R = 5Ω, L = 1mH/phase with star connection, T_A = 25°C, unless otherwise noted.

Sleep Recovery
Duty cycle = 10%



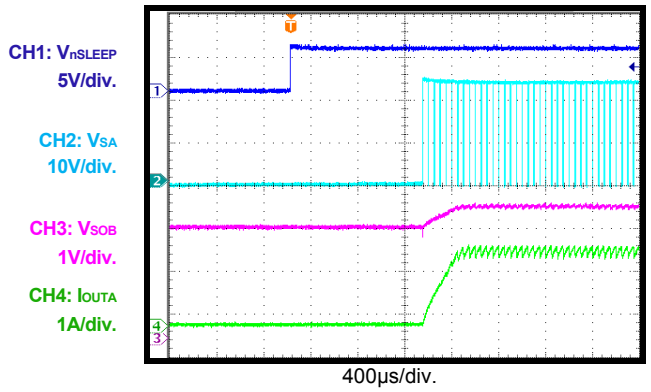
400µs/div.

Sleep Recovery
Duty cycle = 50%



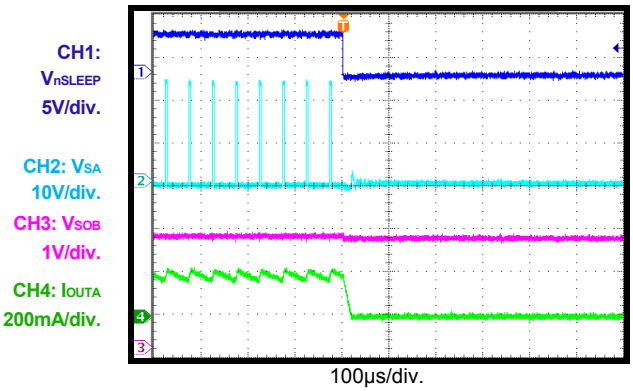
400µs/div.

Sleep Recovery
Duty cycle = 90%



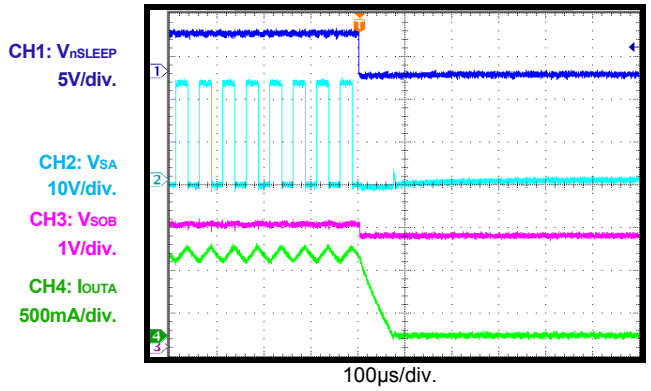
400µs/div.

Sleep Entry
Duty cycle = 10%



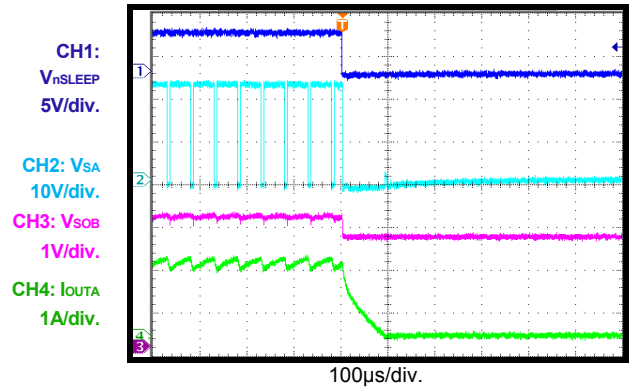
100µs/div.

Sleep Entry
Duty cycle = 50%



100µs/div.

Sleep Entry
Duty cycle = 90%



100µs/div.

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FUNCTIONAL BLOCK DIAGRAM

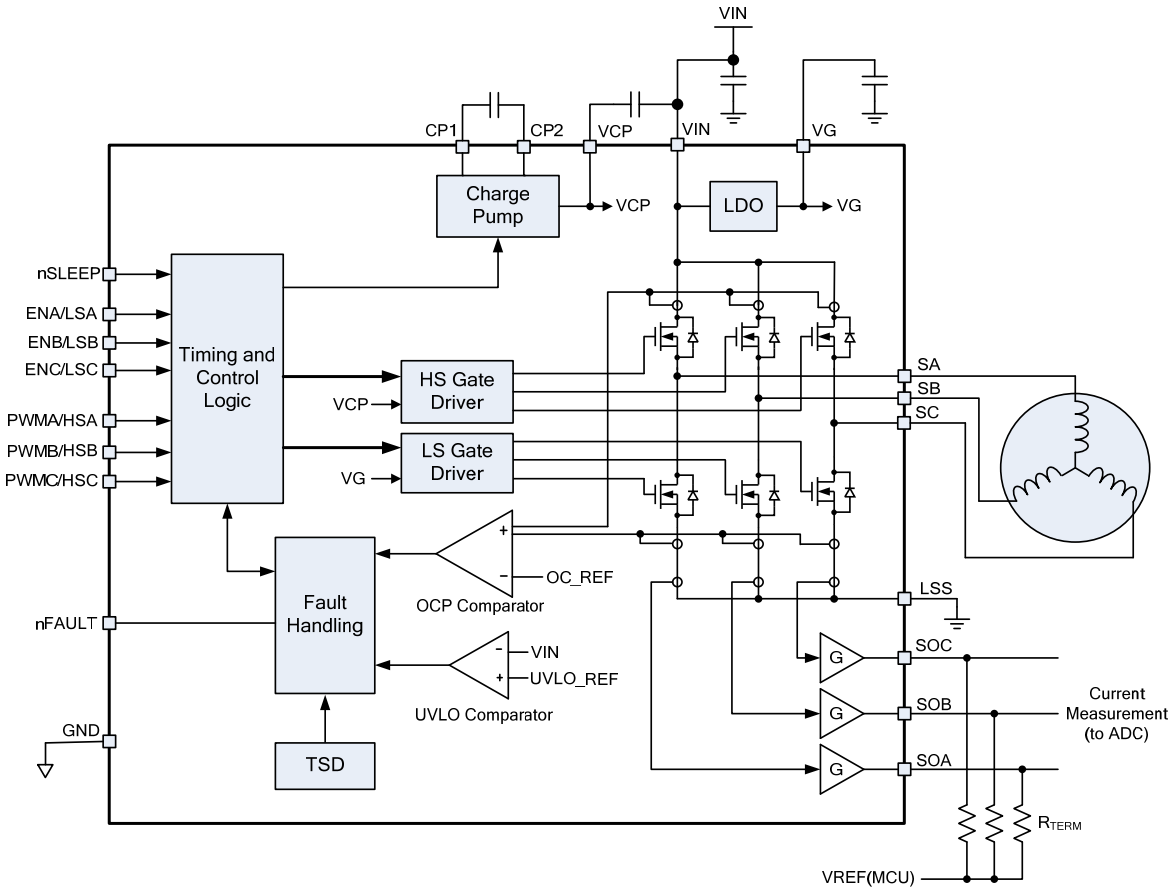

Figure 1: Functional Block Diagram

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OPERATION

Input Logic

The MP6540H has three logic input pins (ENA, ENB, and ENC) that enable corresponding outputs (SA, SB, and SC). When ENx is low, the corresponding output is disabled (output is at high impedance), and the PWM input on that phase is ignored. When ENx is high, the output is enabled, and the PWM input controls the state of the output (see Table 1).

Table 1: PWM Input Logic Truth Table

ENx	PWMx	Sx
H	H	VIN
H	L	GND
L	X	High impedance

The MP6540HA has separate inputs that enable the high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET) of each phase independently (see Table 2).

Table 2: HS-FET and LS-FET Input Logic Truth Table

HSx	LSx	Sx
L	L	High impedance
L	H	GND
H	L	VIN
H	H	High impedance

Note that the logic inputs have weak internal pull-down resistors.

nSLEEP Operation

Driving nSLEEP low puts the device in a low-power sleep state. In this state, all internal circuits are disabled. All inputs are ignored when nSLEEP is active low. When the device wakes up from sleep mode, there is a delay (about 1ms) before the device responds to the inputs. The nSLEEP input has a weak pull-down resistor.

Current-Sense Amplifiers

The current flowing in each of the three outputs is sensed by the internal current-sensing circuits. An output pin for each phase sources or sinks a current proportional to the current flowing in each phase. Only the current flowing in the LS-FET is sensed, and this current is sensed in both forward and reverse directions.

To convert this current into a voltage (to input to an A/D converter), a termination resistor (R_{TERM}) is pulled up to the reference voltage. When there is no current flowing, the resulting output is equal to the reference voltage. When current is flowing, the voltage can be calculated with Equation (1):

$$V_{SOUT} = V_{REF} + (R_{TERM} \times I_{LOAD}) / 9200 \quad (1)$$

To terminate the outputs when using an A/D converter with inputs that are ratiometric to its supply voltage, connect two equal-value resistors to the ADC supply and ground. The resulting ADC code is half-scale at zero current.

Figure 2 shows a simplified drawing of the current measurement circuit.

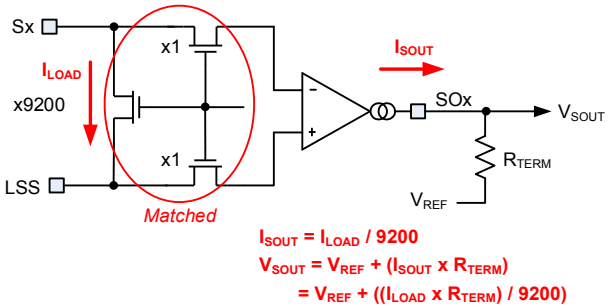

Figure 2: Current Measurement Circuit

Automatic Synchronous Rectification

If the output MOSFETs are both turned off when a current is driven through an inductive load, the recirculation current must continue flowing. This current is typically passed through the MOSFET body diodes. To prevent excess power dissipation in the body diodes, the MP6540H implements an automatic synchronous rectification feature.

When both the HS-FET and LS-FET are turned off and the voltage on an Sx output pin is driven below ground, the LS-FET turns on until the current flowing through it reaches near zero, or the HS-FET is commanded to turn on. If Sx rises above V_{IN}, the HS-FET turns on until the current reaches near zero, or the LS-FET turns on.

nFAULT Output

The MP6540H provides an nFAULT output pin, which is driven to active low during fault conditions, such as over-current protection (OCP) or over-temperature protection (OTP). nFAULT is an open-drain output and must be pulled up by an external pull-up resistor.

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Input Under-Voltage Lockout (UVLO) Protection

If the input voltage (V_{IN}) falls below the under-voltage lockout (UVLO) threshold, all circuitry in the device is disabled, and the internal logic is reset. Operation resumes when V_{IN} rises above the UVLO threshold.

Thermal Shutdown

If the die temperature exceeds the thermal shutdown threshold of 150°C (T_{TSD}), all output MOSFETs are disabled and the nFAULT pin is driven low. Once the die temperature falls to a safe level (about 25°C), operation resumes automatically.

Over-Current Protection (OCP)

The over-current protection (OCP) circuit limits the current through each MOSFET by disabling its gate driver. If the over-current limit threshold is reached and lasts for longer than the over-current deglitch time, all six output MOSFETs are disabled (outputs have high impedance), and nFAULT is driven low. During this time, synchronous rectification decays the current. The outputs are disabled for about 10ms, and are re-enabled automatically.

Over-current conditions on both high- and low-side devices (e.g. a short to ground, supply, or across the motor winding) result in an over-current shutdown.

For special applications, pull nSLEEP up to VIN with a 50kΩ to 100kΩ resistor to disable over-current protection.

Figure 3 shows a simplified diagram of the OCP circuit for an output.

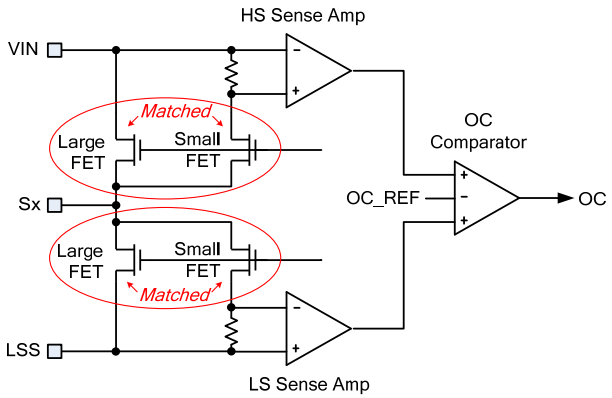

Figure 3: OCP Measurement Circuit

Charge Pump and VG Regulator

An internal LDO regulator generates a low-side gate drive voltage of about 5.5V. A bypass capacitor between 4.7µF and 10µF is required from VG to ground.

A charge pump generates the gate drive for the HS-FETs. The charge pump requires two external capacitors: a 0.1µF ceramic capacitor with a minimum voltage rating that meets the VIN voltage between CP1 and CP2, and a 1µF ceramic capacitor with a minimum 10V voltage rating between VCP and VIN.

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APPLICATIONS INFORMATION

Charge Pump External Capacitors

Table 3 shows how to select appropriate external charge pump capacitors.

Table 3: External Charge Pump Capacitor Selector

Capacitor Parameters	Min	Nom	Max	Unit
CP1 - CP2 capacitance		0.1		µF
CP1 - CP2 capacitor voltage	V_{IN}			V
V_{CP} - V_{IN} capacitance		1		µF
V_{CP} - V_{IN} capacitor voltage	10			V
V_G capacitance	4.7		10	µF
V_G capacitor voltage	10			V

PCB Layout Guidelines

PCB layout is critical for stable operation. For the best results, follow Figure 4, Figure 5, and the guidelines below:

1. Place supply bypass and charge pump capacitors as close as possible to the IC (ideally, place them adjacent to the IC pins on the same PCB layer).
2. Supply bypass and charge pump capacitors can also be placed on the opposite side of the PCB directly under the IC, using vias to make connections.
3. Place as much copper as possible on the long pads.
4. Place large copper areas on the pads and on the same outer copper layer as the device.
5. Thermal vias can be placed inside the pad area to move heat to the copper layers.
6. Place vias just outside the pad area if via-in-pad construction is not allowed.

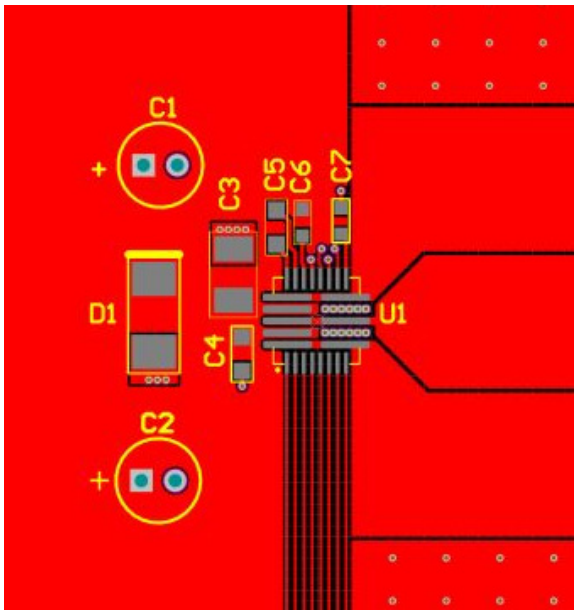

Figure 4: Recommended PCB Layout

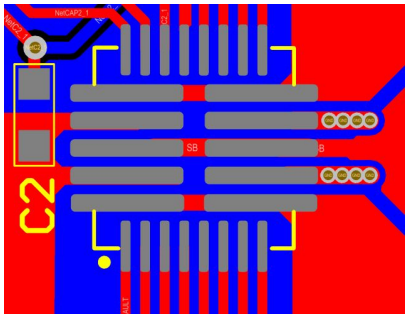

Figure 5: Thermal Vias Outside Pads

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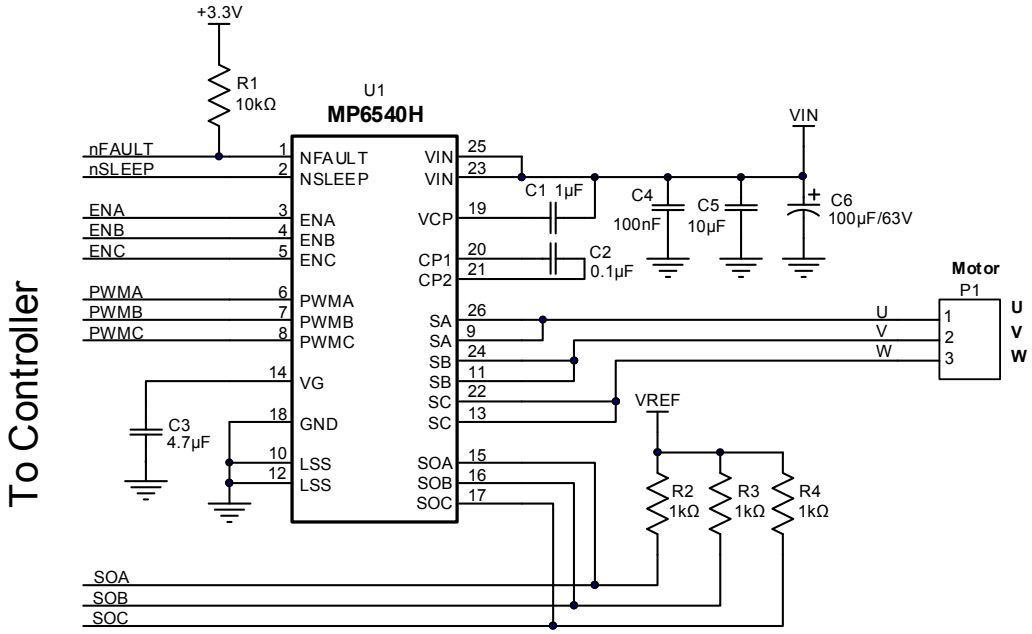
TYPICAL APPLICATION CIRCUIT



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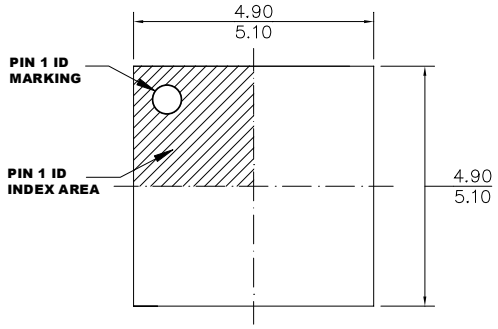
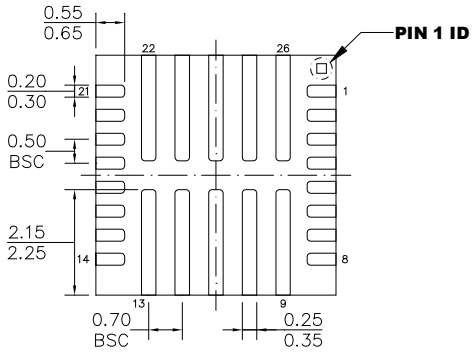
PACKAGE INFORMATION

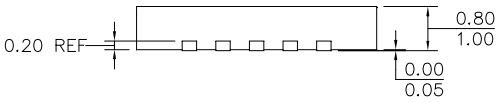
QFN-26 (5mmx5mm)



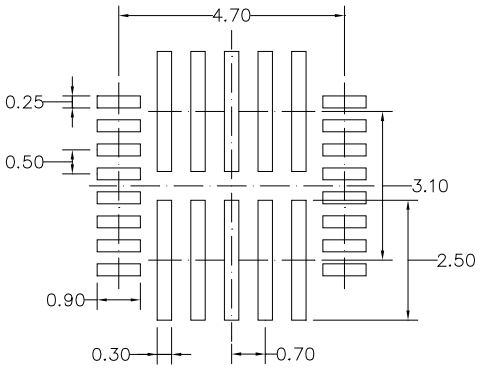
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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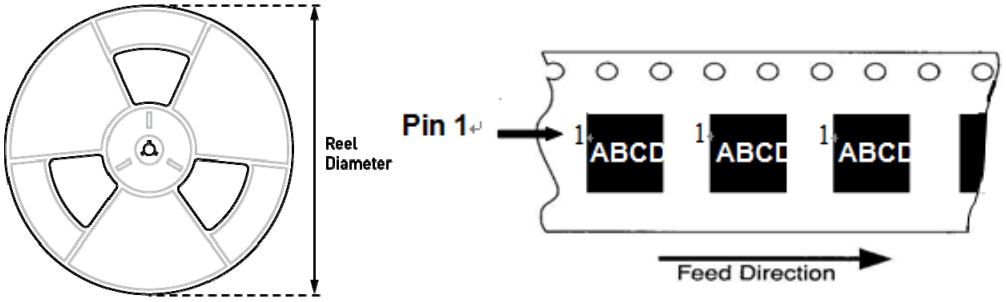
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6540HGU-Z MP6540HGU-A-Z	QFN (5mmx5mm)	5000	N/A	13in	12mm	8mm

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