MP6529

5V to 35V, Three-Phase, Brushless DC Motor Pre-Driver

The Future of Analog IC Technology®

DESCRIPTION

The MP6529 is a gate driver IC designed for three-phase, brushless DC motor driver applications; it is capable of driving three half-bridges consisting of six N-channel power MOSFETs up to 35V.

The MP6529 uses a bootstrap capacitor to generate a supply voltage for the high-side MOSFET driver. An internal trickle-charge circuit maintains a sufficient gate driver voltage at 100% duty cycle.

Full protection features include programmable over-current protection (OCP), adjustable dead-time control, under-voltage lockout (UVLO), and thermal shutdown.

The MP6529 is available in a 28-pin TSSOP (9.7mmx6.4mm) package with an exposed thermal pad and a 28-contact QFN (4mmx4mm) package with an exposed thermal pad.

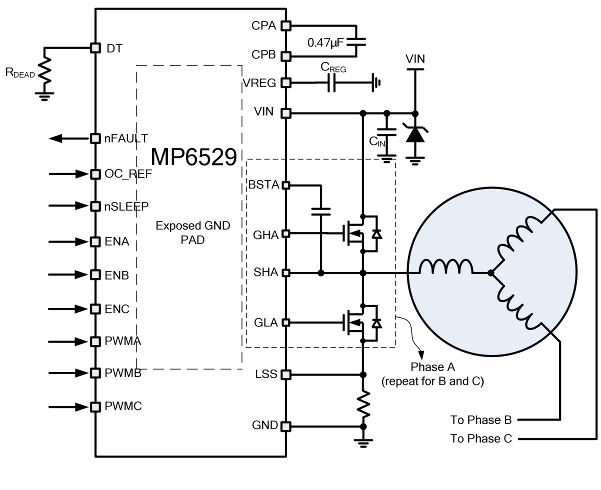
FEATURES

- Wide 5V to 35V Input Voltage Range
- Bootstrap Gate Driver with Trickle-Charge Circuit Supports 100% Duty Cycle Operation
- Low-Power Sleep Mode for Battery-Powered Applications
- Programmable Over-Current Protection of External MOSFETs
- Adjustable Dead-Time Control to Prevent Shoot-Through
- Thermal Shutdown and UVLO Protection
- Fault Indication Output
- Thermally Enhanced Surface-Mount Package

APPLICATIONS

- Three-Phase, Brushless DC Motors and Permanent Magnet Synchronous Motors
- Power Drills
- Impact Drivers
- E-Cigar
- E-Bike

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number	Package	Top Marking
MP6529GR*	QFN-28 (4mmx4mm)	*See Below*
MP6529GF**	TSSOP-28 EP (9.7mmx6.4mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP6529GR–Z)
** For Tape & Reel, add suffix –Z (e.g. MP6529GF–Z)

TOP MARKING (MP6529GR)

MPSYWW
MP6529
LLLLLL

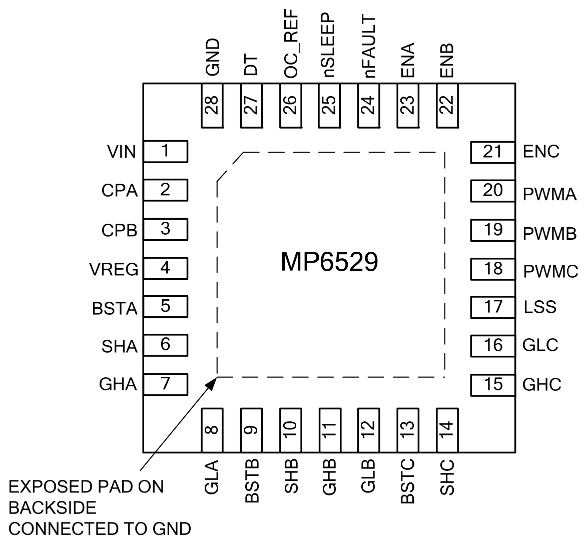
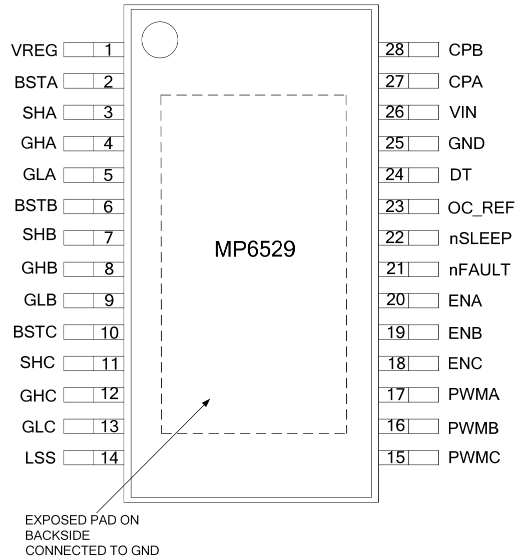
MPS: MPS prefix
Y: Year code
WW: Week code
MP6529: Part number
LLLLLL: Lot number

TOP MARKING (MP6529GF)

MPSYYWW
MP6529
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP6529: Part number
LLLLLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW	TOP VIEW
	
QFN-28 (4mmx4mm)	TSSOP-28 EP (9.7mmx6.4mm)

ABSOLUTE MAXIMUM RATINGS (1)

Input voltage (V_{IN}) .... -0.3V to 40V
CPA .... -0.3V to 40V
CPB .... -0.3V to 12.5V
VREG .... -0.3V to 13V
BSTA/B/C .... -0.3V to 55V
GHA/B/C .... -0.3V to 55V
SHA/B/C .... -0.3V to 40V
GLA/B/C .... -0.3V to 13V
All other pins to AGND .... -0.3V to 6.5V
Continuous power dissipation (T_A = +25°C) (2)
QFN-28 (4mmx4mm)……………………...2.9W
TSSOP-28 EP (9.7mmx6.4mm)………....3.9W
Storage temperature ....-55°C to +150°C
Junction temperature .... +150°C
Lead temperature (solder) .... +260°C

Recommended Operating Conditions (3)

Input voltage (V_{IN}) .... 5V to 35V
OC_REF voltage (V_{OC}) .... 0.125V to 2.4V
Operating junct. temp (T_J).........-40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
QFN-28 (4mmx4mm)	42	9	°C/W
TSSOP-28 EP (9.7mmx6.4mm)	32	6	°C/W

NOTES:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input supply voltage	V_{IN}		5		35	V
Quiescent current	I_Q	nSLEEP = 1, gate not switching		0.95	2	mA
	I_{SLEEP}	nSLEEP = 0			1	μA
Control Logic						
Input logic low threshold	V_{IL}				0.8	V
Input logic high threshold	V_{IH}		2			V
Logic input current	$I_{IN(H)}$	V_{IH} = 5V	-20		20	μA
	$I_{IN(L)}$	V_{IL} = 0.8V	-20		20	μA
nSLEEP pull-down current	$I_{SLEEP-PD}$			1		μA
Internal pull-down resistance	R_{PD}			880		kΩ
Fault Outputs (Open-Drain Outputs)						
Output low voltage	V_{OL}	I_O = 5mA			0.5	V
Output high leakage current	I_{OH}	V_O = 3.3V			1	μA
Protection Circuit						
UVLO rising threshold	V_{IN_RISE}		3.3	3.9	4.5	V
UVLO hysteresis	V_{IN_HYS}			200		mV
VREG rising threshold	V_{REG_RISE}		6.8	7.6	8.4	V
VREG hysteresis	V_{REG_HYS}			0.54	1	V
VREG start-up delay	t_{REG}			700		μs
OC_REF threshold	V_{OC}	V_{OC} = 1V	0.8	1	1.2	V
		V_{OC} = 2.4V	2.18	2.4	2.62	V
OCP deglitch time	t_{OC}			3		μs
SLEEP wake-up time	t_{SLEEP}			1		ms
LSS OCP threshold	$V_{LSS-OCP}$		0.4	0.5	0.6	V
Thermal shutdown	T_{TSD}			150		°C

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Gate Drive						
Bootstrap diode forward voltage	V_{FBOOT}	I_D = 10mA			0.9	V
		I_D = 100mA			1.3	V
VREG output voltage	V_{REG}	V_{IN} = 5.5V-35V	10	11.5	12.8	
		V_{IN} = 5V	$2xV_{IN}-1$			V
Maximum source current	I_{OSO}(5)			0.8		A
Maximum sink current	I_{OSI}(5)			1		A
Gate drive pull-up resistance	R_{UP}	V_{DS} = 1V		8		Ω
HS gate drive pull-down resistance	R_{HS-DN}	V_{DS} = 1V	1.2		4.7	Ω
LS gate drive pull-down resistance	R_{LS-DN}	V_{DS} = 1V	1		5.5	Ω
LS passive pull-down resistance	R_{LS-PDN}			590		kΩ
LS automatic turn-on time	t_{LS}			1.8		μs
Charge pump frequency	f_{CP}			110		kHz
Dead time	t_{DEAD}	Leave DT open		6		μs
		R_{DT} = 200kΩ		0.74		μs
		DT tied to GND		30		ns

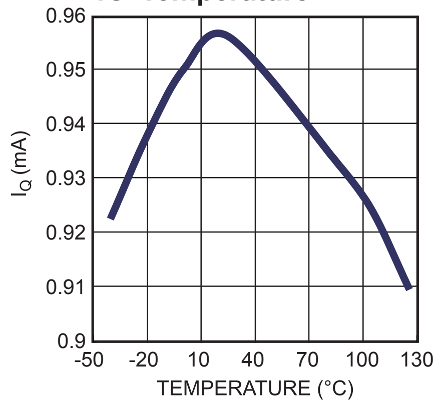
NOTE:

5) Guaranteed by design.

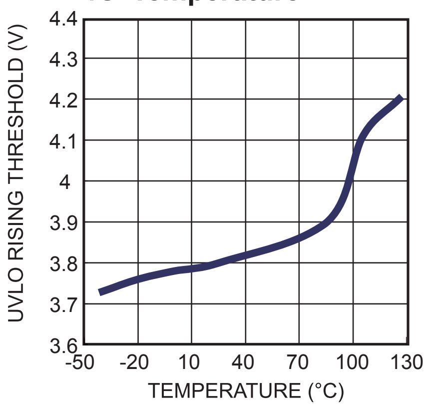
TYPICAL CHARACTERISTICS

V_{IN} = 24V, OC_REF = 0.5V, R_{DT} = 200k, ENA = ENC = H, F_{PWMA} = 20kHz, T_A = 25°C, resistor + inductor load: 5Ω + 1mH/phase with star connection, unless otherwise noted.

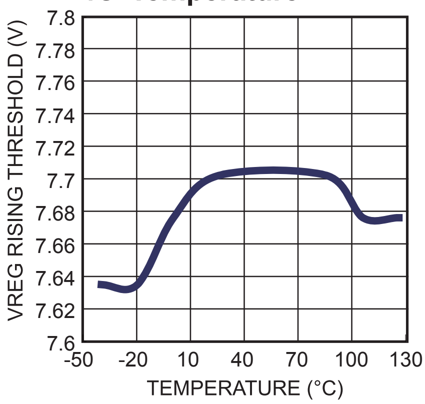
Quiescent Current vs. Temperature



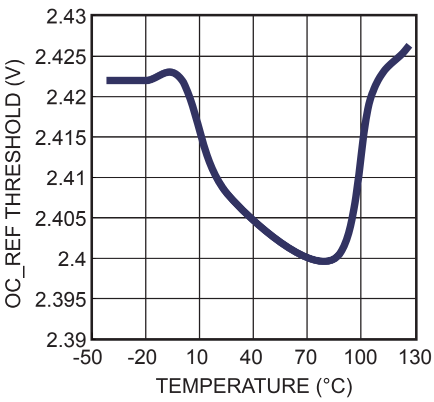
UVLO Rising Threshold vs. Temperature



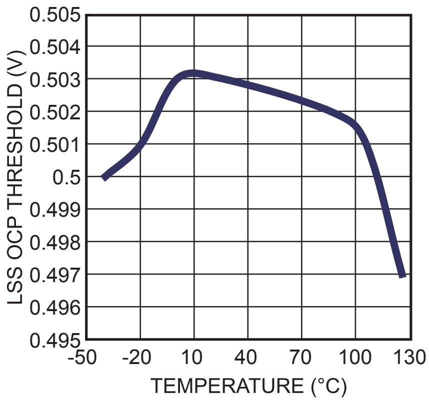
VREG Rising Threshold vs. Temperature



OC_REF Threshold vs. Temperature



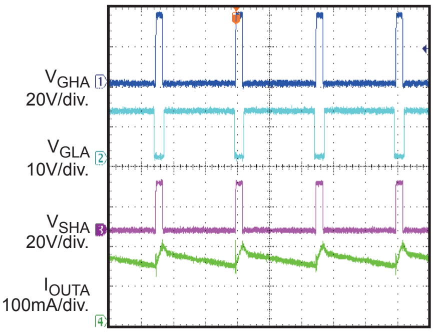
LSS OCP Threshold vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

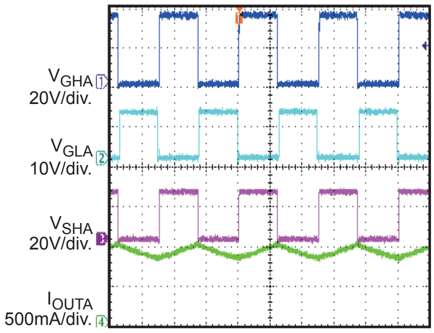
V_{IN} = 24V, OC_REF = 0.5V, R_{DT} = 200k, ENA = ENC = H, F_{PWMA} = 20kHz, T_A = 25°C, resistor + inductor load: 5Ω + 1mH/phase with star connection, unless otherwise noted.

Steady State
Duty=10%



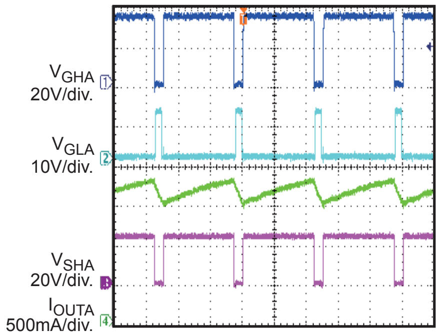
20µs/div.

Steady State
Duty=50%



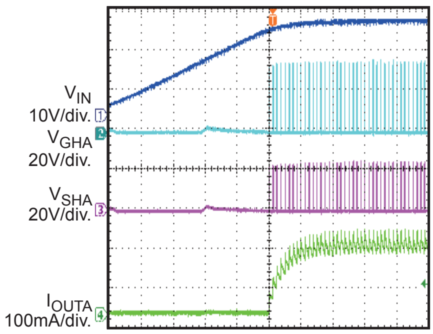
20µs/div.

Steady State
Duty=90%



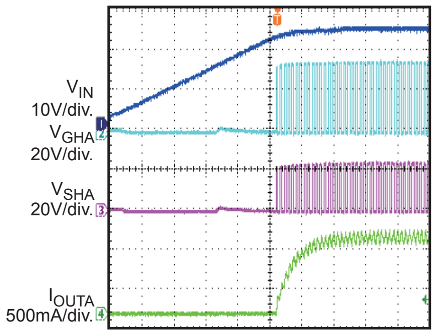
20µs/div.

Power Ramp Up
Duty=10%



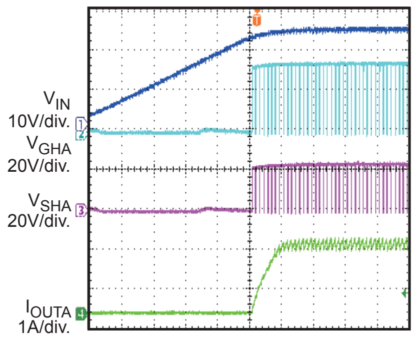
400µs/div

Power Ramp Up
Duty=50%



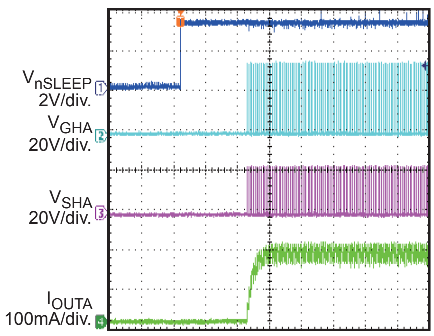
400µs/div

Power Ramp Up
Duty=90%



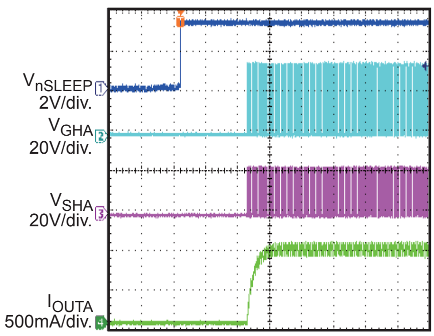
400µs/div

Sleep Recovery
Duty=10%



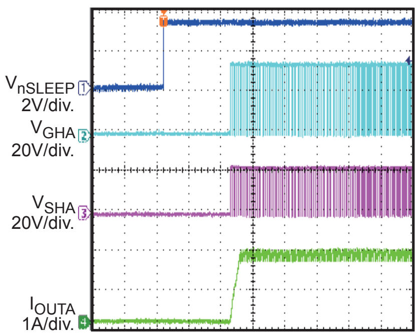
1ms/div

Sleep Recovery
Duty=50%



1ms/div

Sleep Recovery
Duty=90%

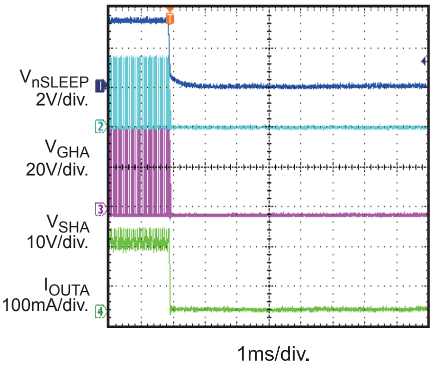


1ms/div

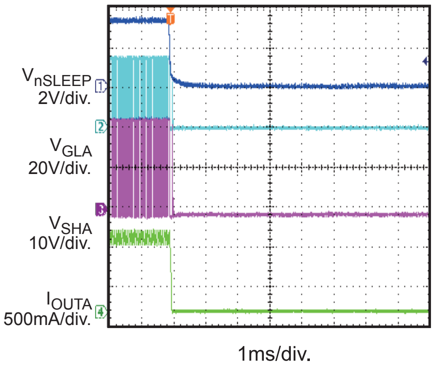
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, OC_REF = 0.5V, R_{DT} = 200k, ENA = ENC = H, F_{PWMA} = 20kHz, T_A = 25°C, resistor + inductor load: 5Ω + 1mH/phase with star connection, unless otherwise noted.

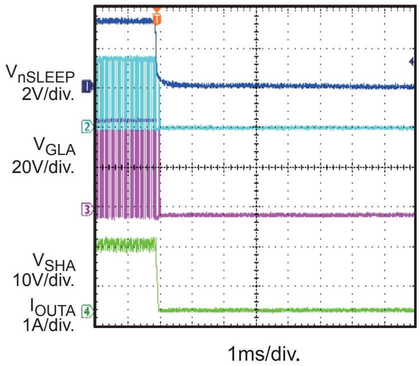
Sleep Entry
Duty=10%



Sleep Entry
Duty=50%



Sleep Entry
Duty=90%



PIN FUNCTIONS

QFN-28 Pin #	TSSOP-28 Pin #	Name	Description
1	26	VIN	**Input supply voltage.**
2	27	CPA	**Charge pump capacitor connect terminal.**
3	28	CPB	**Charge pump capacitor connect terminal.**
4	1	VREG	**Gate driver supply output.**
5	2	BSTA	**Bootstrap output phase A.**
6	3	SHA	**High-side source connection phase A.**
7	4	GHA	**High-side gate drive phase A.**
8	5	GLA	**Low-side gate drive phase A.**
9	6	BSTB	**Bootstrap output phase B.**
10	7	SHB	**High-side source connection phase B.**
11	8	GHB	**High-side gate drive phase B.**
12	9	GLB	**Low-side gate drive phase B.**
13	10	BSTC	**Bootstrap output phase C.**
14	11	SHC	**High-side source connection phase C.**
15	12	GHC	**High-side gate drive phase C.**
16	13	GLC	**Low-side gate drive phase C.**
17	14	LSS	**Low-side source connection.**
18	15	PWMC	**PWM input for phase C.**
19	16	PWMB	**PWM input for phase B.**
20	17	PWMA	**PWM input for phase A.**
21	18	ENC	**Enable for phase C.** Pull ENC below the specified threshold to disable the gate driver output for phase C.
22	19	ENB	**Enable for phase B.** Pull ENB below the specified threshold to disable the gate driver output for phase B.
23	20	ENA	**Enable for phase A.** Pull ENA below the specified threshold to disable the gate driver output for phase A.
24	21	nFAULT	**Fault indication.** Open-drain output. nFAULT is in a fault condition at logic low.
25	22	nSLEEP	**Sleep mode input.** Logic low to enter low-power sleep mode; high to enable. Internal pulldown.
26	23	OC_REF	**Over-current protection reference input.**
27	24	DT	**Dead time setting.**
28	25	GND	**Ground.**

BLOCK DIAGRAM

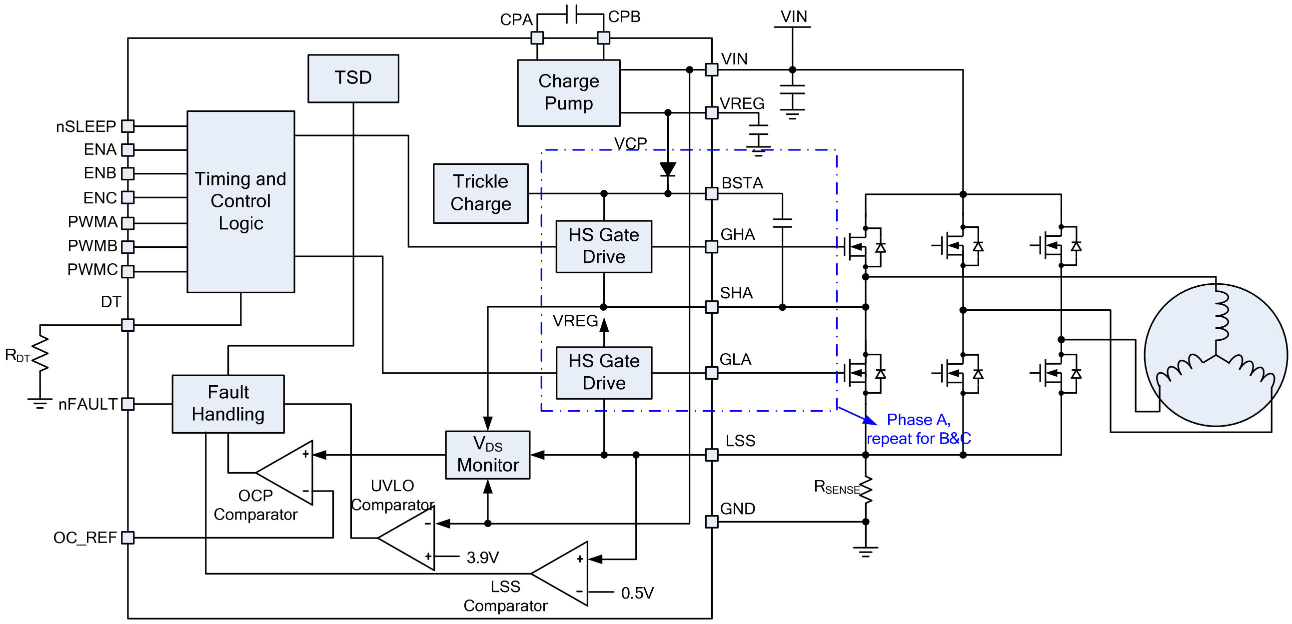


Figure 1: Functional Block Diagram

OPERATION

The MP6529 is a three-phase, BLDC motor pre-driver that can drive three half-bridges with a 0.8A source and a 1A sink current capability over a wide input voltage range of 5V to 35V. It is designed for use in battery-powered equipment. The MP6529 features a low-power sleep mode, which disables the device and draws a very low supply current.

The MP6529 provides several flexible functions, such as adjustable dead-time control and over-current protection (OCP), which allow the device to cover a wide range of application fields.

Input Logic

Driving nSLEEP low will put the device into a low-power sleep state. In this state, all the internal circuits are disabled, and all inputs are ignored. nSLEEP has an interval pulldown, so it must be driven high for the device to operate. When exiting sleep mode, a brief time period of approximately 1ms must pass before issuing a PWM command. This time period allows the internal circuitry to stabilize.

ENx controls the gate driver outputs of this phase. When ENx is low, the gate driver outputs are disabled, and the PWM inputs are ignored. When ENx is high, the gate driver outputs are enabled, and the PWM inputs are recognized. Refer to Table 1 below for the logic truth table.

Table 1: Input Logic Truth Table

ENx	PWMx	SHx
H	H	VIN
H	L	GND
L	x	High impendence

nFAULT

nFAULT reports to the system when a fault condition is detected, such as OCP and OTP. nFAULT can be an open-drain output, and is driven low once a fault condition occurs. If the fault condition is released, nFAULT is pulled high by an external pull-up resistor.

Over-Current Protection (OCP)

The MP6529 implements VDS sensing circuitry to protect the power stage from damage caused by high currents. Based on the R_{DS-ON} of the power MOSFETs and the maximum allowed I_{DS}, a voltage threshold can be calculated, which triggers the over-current protection (OCP) feature when exceeded.

This voltage threshold level is programmable through the OC_REF terminal by applying an external reference voltage with a DAC. Also, OCP occurs if the LSS voltage exceeds 0.5V. Once an OCP event is detected, the MP6529 will enter a latched fault state and disable all functions. The MP6529 will stay latched off until it is reset by nSLEEP or UVLO.

OCP Deglitch Time

Usually, a current spike occurs during the switching transition due to either the body diode's reverse-recovery current or the distributed inductance or capacitance. This current spike requires filtering to prevent it from erroneously triggering OCP and shutting down the external MOSFET. An internal fixed deglitch time (t_{OC}) (which is also the minimum on time for the MOSFET) blanks the output of the VDS monitor when the outputs are switched.

Dead-Time Adjustment

To prevent a shoot-through at any phase of the bridge, it is necessary to have a dead time (t_{DEAD}) between a high- or low-side turn-off and the next complementary turn-on event. The dead time for all three phases is set by a single dead-time resistor (R_{DT}) between DT and ground and is calculated with Equation (1):

$$t_{DEAD}(nS) = 3.7 * R(k\Omega) \quad (1)$$

If DT is tied to GND directly, an internal minimum dead time of 30ns is applied. Leaving DT open generates a 6μs dead time.

Input UVLO Protection

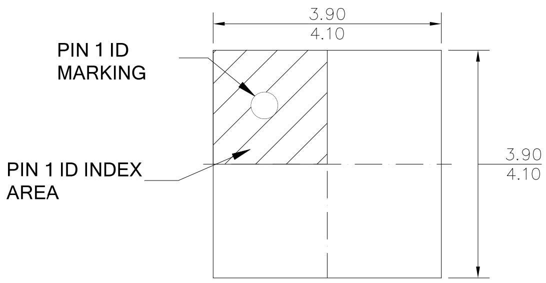
If at any time the voltage on VIN falls below the under-voltage lockout threshold voltage, all circuitry in the device is disabled, and the internal logic resets. Operation resumes when VIN rises above the UVLO threshold.

Thermal Shutdown

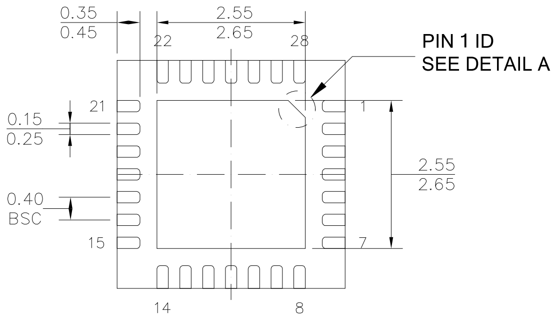
If the die temperature exceeds its safe limits, the MP6529 enters a latched fault-state similar to an OCP event, and nFAULT is driven low. Only a reset by nSLEEP or UVLO unlatches the device from an OTP fault lockout.

PACKAGE INFORMATION

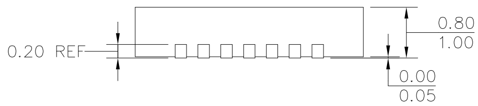
QFN-28 (4mmx4mm)



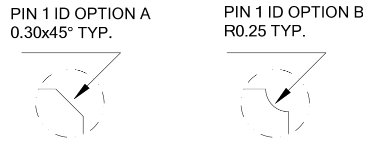
TOP VIEW



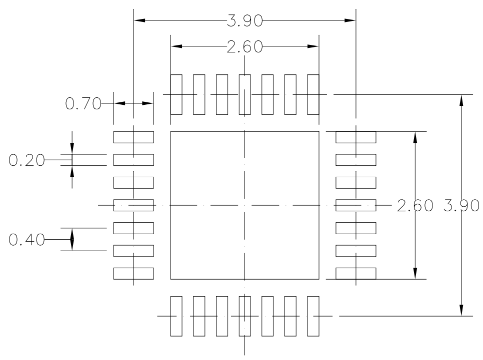
BOTTOM VIEW



SIDE VIEW



DETAIL A



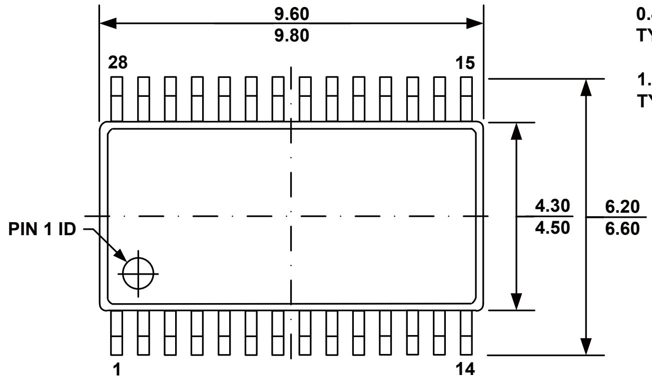
RECOMMENDED LAND PATTERN

NOTE:

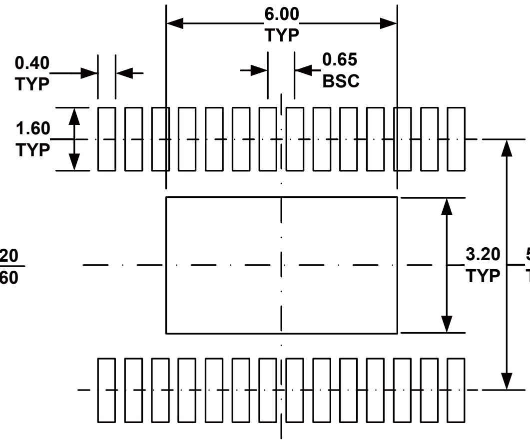
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) DRAWING CONFORMS TO JEDEC MO-220.
5) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION

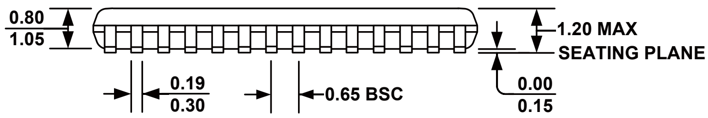
TSSOP-28 EP (9.7mmx6.4mm)



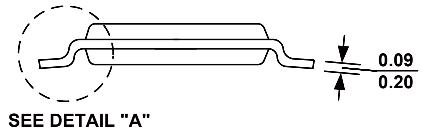
TOP VIEW



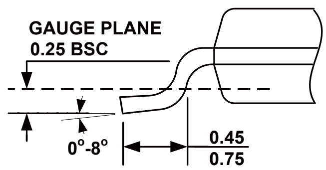
RECOMMENDED LAND PATTERN



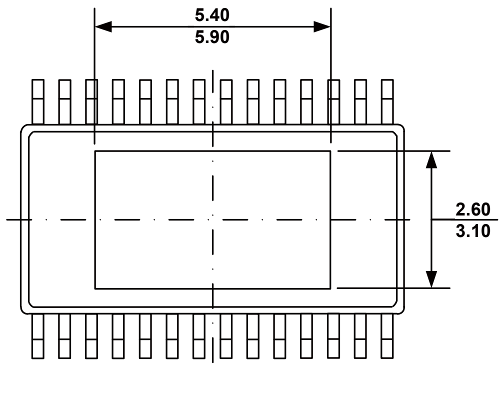
FRONT VIEW



SIDE VIEW



DETAIL "A"



BOTTOM VIEW

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION AET.
6) DRAWING IS NOT TO SCALE.