MP6519A

2.5V to 28V, 5A, Full H-Bridge Current Regulator

DESCRIPTION

The MP6519A is a monolithic, step-down, current-source driver for applications that require accurate and fast current response control. The MP6519A achieves up to 5A of output current (I_{OUT}), with excellent load and line regulation across a wide input voltage (V_{IN}) supply range.

The MP6519A provides H-bridge control with four integrated MOSFETs to achieve fast dynamic load response and an ultra-high efficiency solution. For ease of use, the output polarity can be controlled by pulling the MODE pin high or low.

By setting the full-scale I_{OUT} through an external resistor, I_{OUT} can be dimmed by the pulse-width modulation (PWM) input signal from 0% to 100% of the full-scale current range.

Full protection features include open-load protection, load-short protection, over-current protection (OCP), over-temperature protection (OTP), and input over-voltage protection (OVP).

The MP6519A is available in a QFN-19 (3mmx3mm) package.

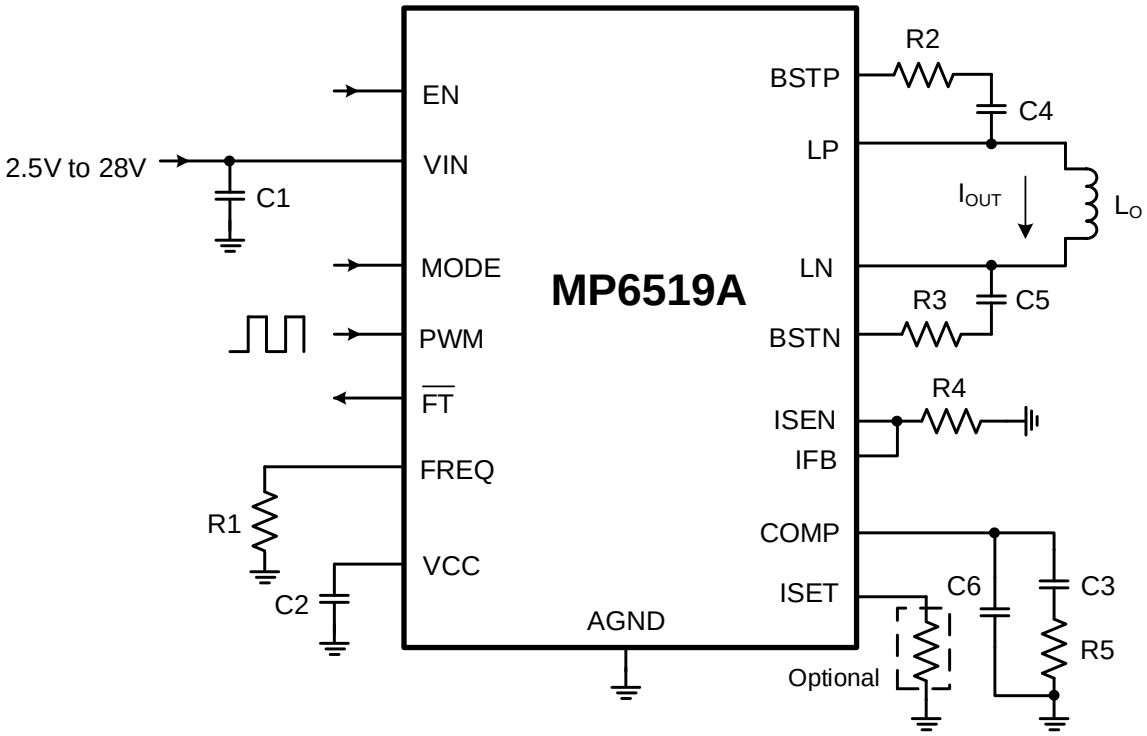
FEATURES

- Wide 2.5V to 28V Operating Input Voltage (V_{IN}) Range
- Up to 5A of Output Current (I_{OUT})
- ± 2% Accuracy at Full-Scale Output Current (I_{OUT_FULL}) Reference
- 65mΩ On Resistance ($R_{DS(ON)}$) for Each MOSFET of the H-Bridge
- 100% Duty Cycle Operation of the H-Bridge
- 30kHz to 300kHz Configurable Switching Frequency (f_{SW})
- 20kHz to 100kHz Pulse-Width Modulation (PWM) Input for Current Regulation
- Configurable I_{OUT_FULL}
- Up to 94% Efficiency
- Selectable Current Polarity Mode
- Switching Automatically Disabled by PWM Input Detection
- 1μA Shutdown Mode
- Inherent Open-Load Protection
- Cycle-by-Cycle Over-Current Protection (OCP)
- Output Short-Circuit Protection (SCP)
- Input Over-Voltage Protection (OVP)
- Over-Temperature (OT) Shutdown
- Available in a QFN-19 (3mmx3mm) Package

APPLICATIONS

- Current Regulators
- DC Motors
- Solenoids and Actuators

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP6519AGQ	QFN-19 (3mmx3mm)	*See Below*	1

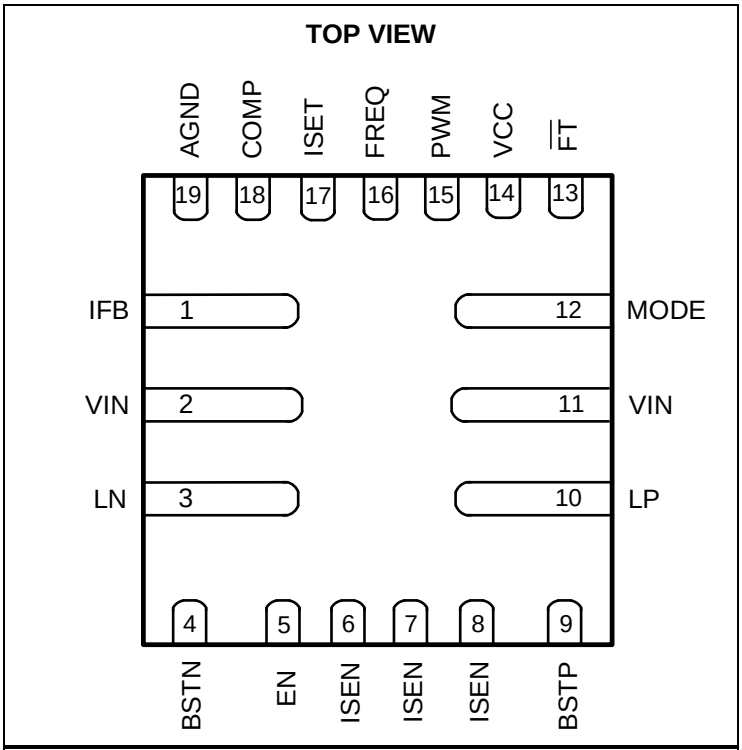
* For Tape & Reel, add suffix -Z (e.g. MP6519AGQ-Z).

TOP MARKING

$\overline{\text{CCQY}}$
LLLL

CCQ: Product code
Y: Year code
LLLL: Lot number

PACKAGE REFERENCE



QFN-19 (3mmx3mm)

PIN FUNCTIONS

Pin #	Name	Description
1	IFB	**Current-sense signal feedback.** Connect the IFB and ISEN pins together.
2, 11	VIN	**Input supply.**
3	LN	**Negative switching node of the H-bridge.**
4	BSTN	**Bootstrap for the LN high-side MOSFET (HS-FET) gate driver.** Connect a capacitor between the BSTN and LN pins.
5	EN	**IC enable.**
6, 7, 8	ISEN	**Current sense.** Connect a current-sense resistor between the ISEN pin and power ground.
9	BSTP	**Bootstrap for the LP HS-FET gate driver.** Connect a capacitor between the BSTP and LP pins.
10	LP	**Positive switching node of the H-bridge.**
12	MODE	**Current polarity setting.** If the current direction flowing from LP to LN is positive, pull the MODE pin high to run the current from LP to LN; pull MODE low to run the current from LN to LP.
13	$\overline{FT}$	**Fault indication output.** The $\overline{FT}$ pin is active low for fault conditions.
14	VCC	**5V low-dropout (LDO) output for internal driver and logic.**
15	PWM	**Pulse-width modulation (PWM) signal input for current dimming.** Apply a >20kHz PWM signal to the PWM pin.
16	FREQ	**Switching frequency setting.** Connect a resistor between the FREQ pin and AGND.
17	ISET	**Full-scale current reference setting.** Connect a resistor between AGND and the ISET pin.
18	COMP	**Loop compensation setting.**
19	AGND	**Ground for internal logic.**

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 35V
V_{LP}, V_{LN} ..... -0.3V to V_{IN} + 0.3V
V_{BSTP} ..... V_{LP} + 6V
V_{BSTN} ..... V_{LN} + 6V
All other pins ..... -0.3V to +6V
Continuous power dissipation (T_A = 25°C) (2)
QFN-19 (3mmx3mm) 2.5W
Junction temperature (T_J) ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged-device model (CDM) ..... ±750V

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 2.5V to 28V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}
QFN-19 (3mmx3mm)	50	8	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operation conditions.
4) Measured on a JESD51-7, 4-layer board.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage						
VIN operating range	V_{IN}		2.5		28	V
Turn-on threshold	V_{IN_ON}	VIN rising edge		2.3	2.45	V
Turn-on hysteretic voltage	V_{IN_HY}			0.15		V
IC Supply						
Shutdown current	I_{IN_SD}	EN = low			1	µA
Quiescent current	I_{IN_SBY}	Standby mode		370	450	µA
VCC regulator voltage	V_{CC}	V_{IN} > 5.2V	4.5	5	5.5	V
VCC regulator dropout voltage		V_{IN} < 5V, 20mA load		100		mV
Logic						
Enable (EN) high threshold	V_{EN_HIGH}				1.5	V
EN low threshold	V_{EN_LOW}		0.4			V
MODE input high threshold	V_{EN_HIGH}				1.5	V
MODE input low threshold	V_{EN_LOW}		0.4			V
Pulse-width modulation (PWM) high threshold	V_{PWM_HIGH}				1.5	V
PWM low threshold	V_{PWM_LOW}		0.4			V
IC start-up delay	t_{DELAY}	EN active to switching		230	350	µs
Switching Frequency						
Switching frequency	f_{SW}	R_{FREQ} = 75kΩ	255	300	345	kHz
		R_{FREQ} = 750kΩ	22	30	38	kHz
Current Reference						
Current reference accuracy	V_{REF_FB}	V_{REF_FB} = 200mV	196	200	204	mV
		V_{REF_FB} = 100mV	97	99	101	mV
Loop Compensation						
Transconductance	G_{EA}			270		µA/V
Maximum source current				50		µA
Maximum sink current				50		µA
Power MOSFET						
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$		42	65	93	mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$		42	65	93	mΩ
Minimum on time				200		ns
Bootstrap for High-Side (HS) Driver						
Forward voltage for bootstrap charge				0.5		V
Bootstrap under-voltage lockout (UVLO) threshold		Rising edge		2		V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

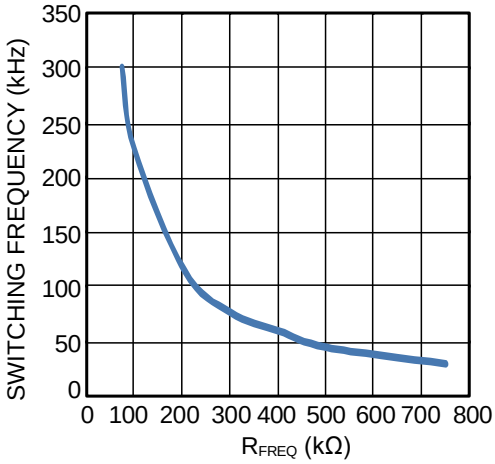
Parameters	Symbol	Condition	Min	Typ	Max	Units
Protection						
Hiccup over-current (OC) threshold		Float R_{ISET}	255	300	345	mV
Load short hiccup recovery time				1		ms
Latch-off OC threshold		Float R_{ISET}, R_{SEN} = 40mΩ		13		A
Input over-voltage protection (OVP) threshold	V_{IN_OVP}		28.2	30	31	V
Thermal shutdown (5)				150		°C
Thermal shutdown hysteresis				20		°C

Note:

5) Guaranteed by design.

TYPICAL CHARACTERISTICS

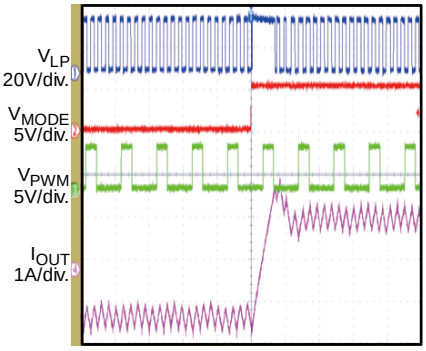
Switching Frequency vs. R_{FREQ}



TYPICAL PERFORMANCE CHARACTERISTICS

Mode Transfer

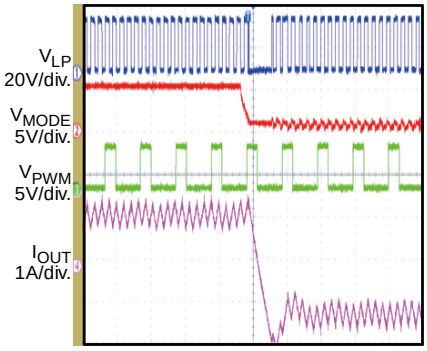
V_{IN} = 24V, V_{EN} = 5V, duty = 50%,
MODE low to high, 1Ω + 100μH load



20μs/div.

Mode Transfer

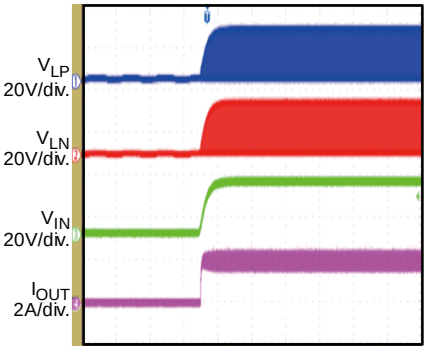
V_{IN} = 24V, V_{EN} = 5V, duty = 50%,
MODE high to low, 1Ω + 100μH load



20μs/div.

Start-Up through VIN

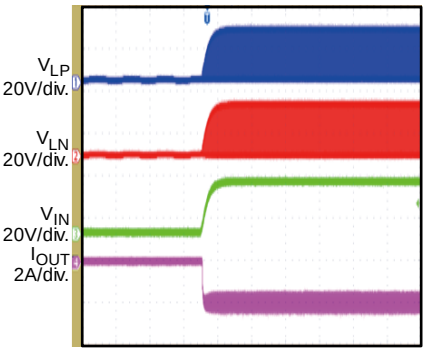
V_{IN} = 24V, V_{EN} = 5V, duty = 50%,
MODE = high 1Ω + 100μH load



20ms/div.

Start-Up through VIN

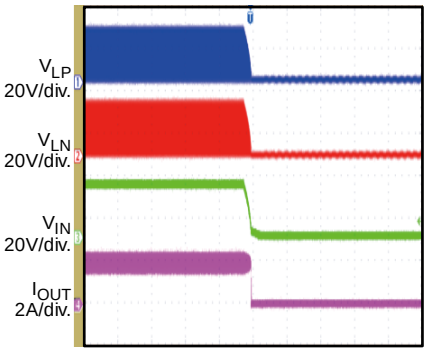
V_{IN} = 24V, V_{EN} = 5V, duty = 50%,
MODE = low, 1Ω + 100μH load



20ms/div.

Shutdown through VIN

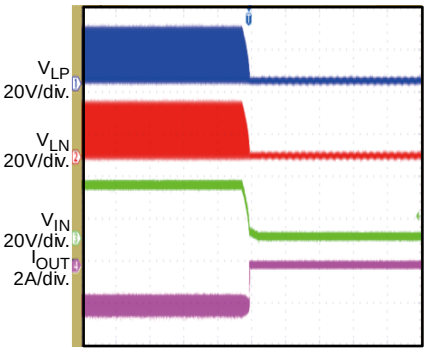
V_{IN} = 24V, V_{EN} = 5V, duty = 50%,
MODE = high, 1Ω + 100μH load



100ms/div.

Shutdown through VIN

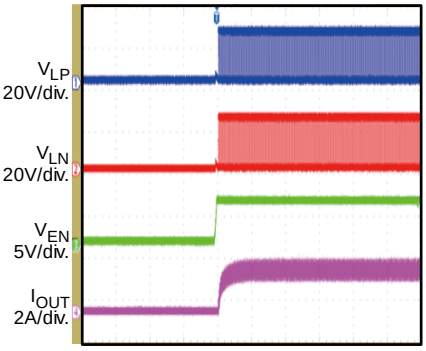
V_{IN} = 24V, V_{EN} = 5V, duty = 50%,
MODE = low, 1Ω + 100μH load



100ms/div.

Start-Up through EN

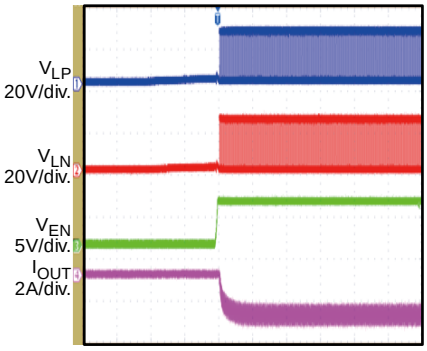
V_{IN} = 24V, V_{EN} = 5V, duty = 50%,
MODE = high, 1Ω + 100μH load



2ms/div.

Start-Up through EN

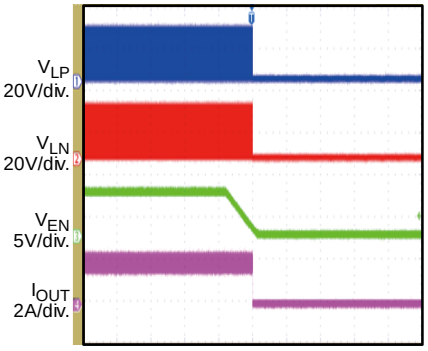
V_{IN} = 24V, V_{EN} = 5V, duty = 50%,
MODE = low, 1Ω + 100μH load



2ms/div.

Shutdown through EN

V_{IN} = 24V, V_{EN} = 5V, duty = 50%,
MODE = high, 1Ω + 100μH load

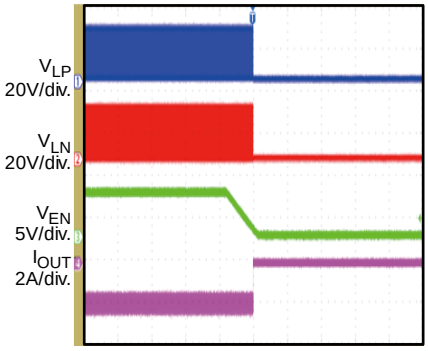


40ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

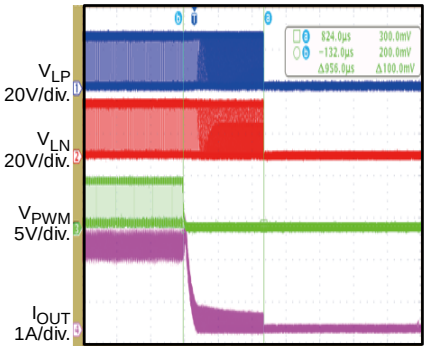
Shutdown through EN

V_{IN} = 24V, V_{EN} = 5V, duty = 50%, MODE = low, 1Ω + 100μH load



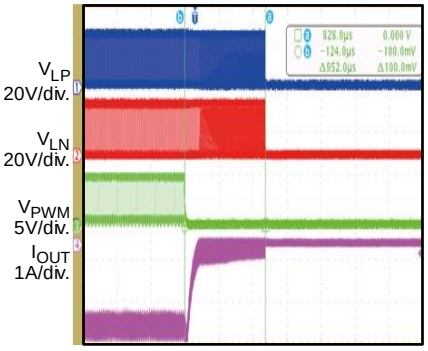
Sleep Entry

V_{IN} = 24V, V_{EN} = 5V, duty = 50%, MODE = high, 1Ω + 100μH load



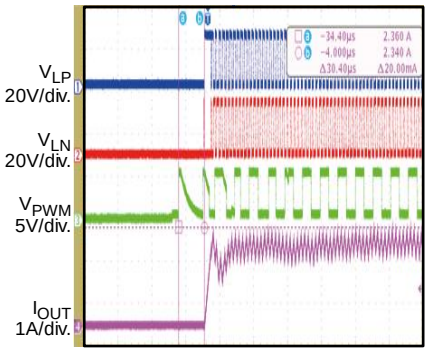
Sleep Entry

V_{IN} = 24V, V_{EN} = 5V, duty = 50%, MODE = low, 1Ω + 100μH load



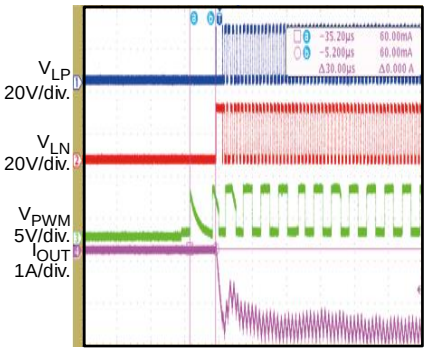
Sleep Recovery

V_{IN} = 24V, V_{EN} = 5V, duty = 50%, MODE = high, 1Ω + 100μH load



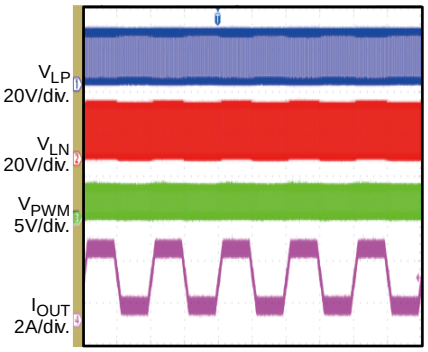
Sleep Recovery

V_{IN} = 24V, V_{EN} = 5V, duty = 50%, MODE = low, 1Ω + 100μH load



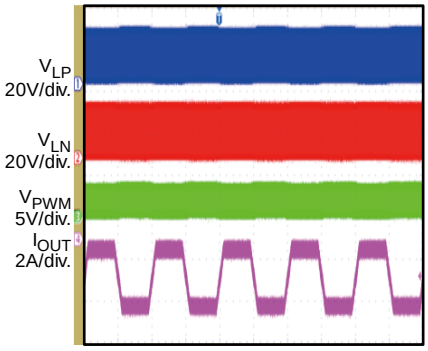
Trapezoidal Wave

V_{IN} = 24V, V_{EN} = 5V, duty = 50%, MODE = high, 1Ω + 100μH load



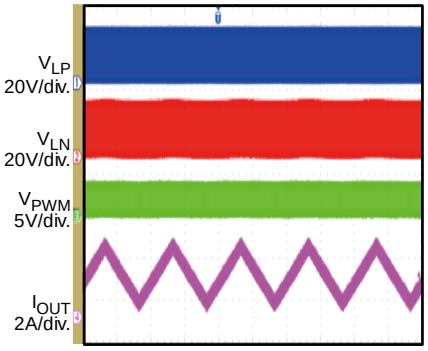
Trapezoidal Wave

V_{IN} = 24V, V_{EN} = 5V, duty = 50%, MODE = low, 1Ω + 100μH load



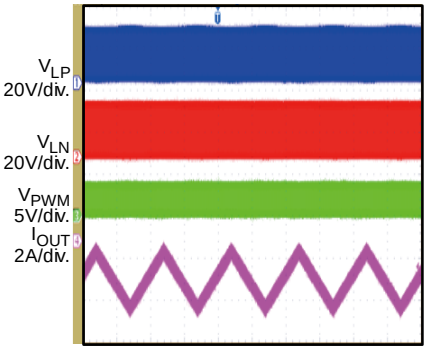
Triangle Wave

V_{IN} = 24V, V_{EN} = 5V, duty = 50%, MODE = high, 1Ω + 100μH load



Triangle Wave

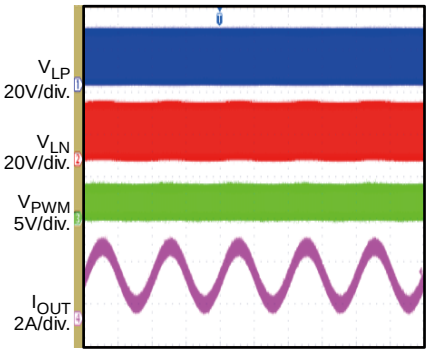
V_{IN} = 24V, V_{EN} = 5V, duty = 50%, MODE = low, 1Ω + 100μH load



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Sine Wave

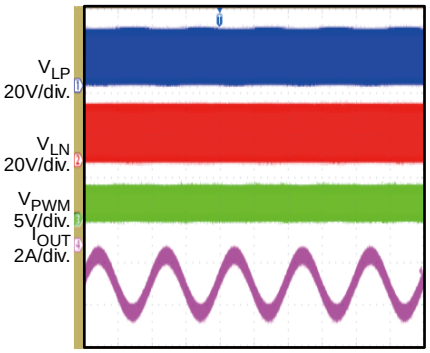
V_{IN} = 24V, V_{EN} = 5V, duty = 50%,
MODE = high, 1Ω + 100μH load



10ms/div.

Sine Wave

V_{IN} = 24V, V_{EN} = 5V, duty = 50%,
MODE = low, 1Ω + 100μH load



10ms/div.

FUNCTIONAL BLOCK DIAGRAM

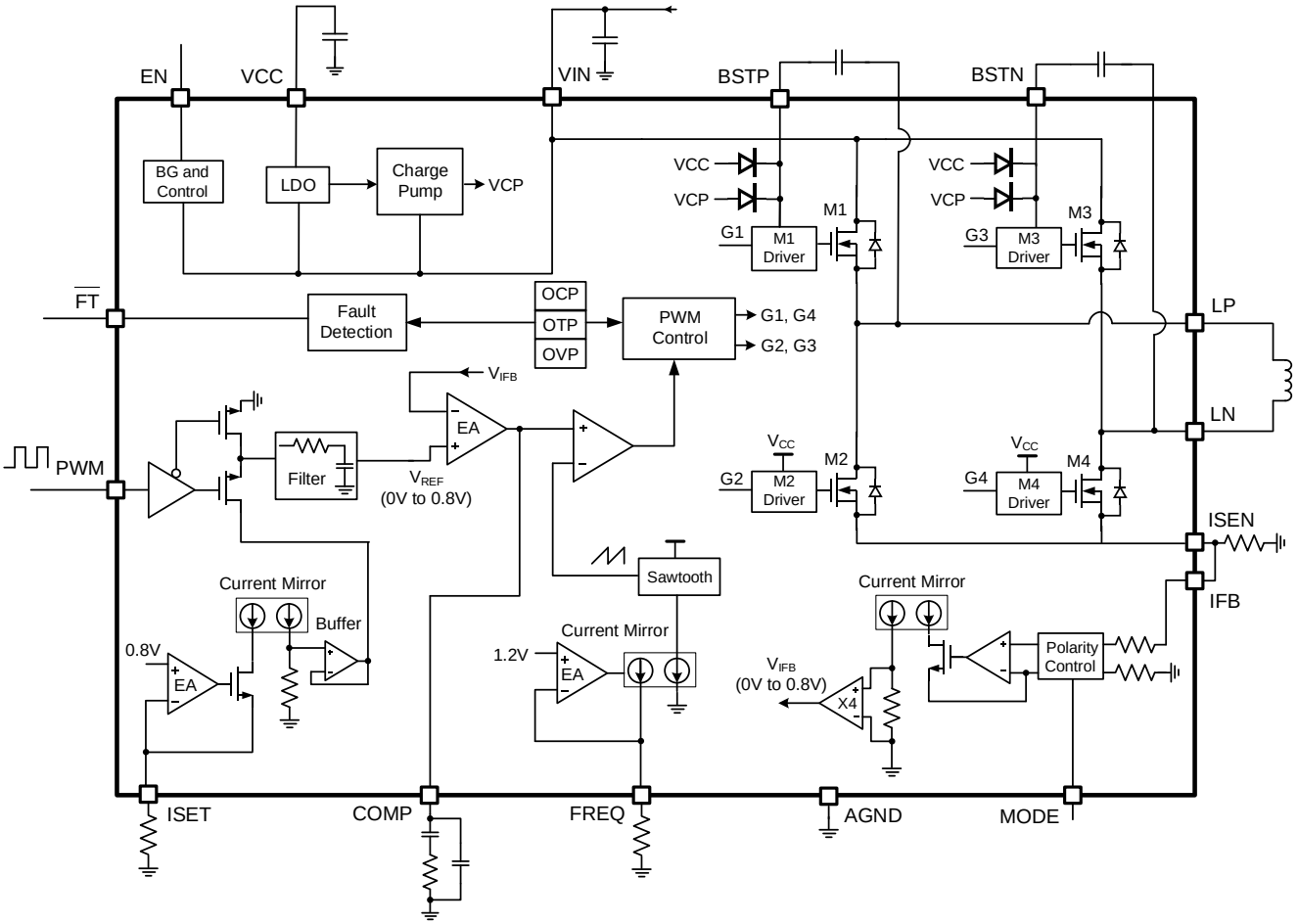


Figure 1: Functional Block Diagram

OPERATION

The MP6519A is a current driver for applications that require accurate load current (I_{LOAD}) control and fast dynamic current response. The MP6519A works in step-down mode with four fully integrated MOSFET H-bridges (M1, M2, M3, and M4) to provide small size and high efficiency. The full-scale output current (I_{OUT_FULL}) can be set by the external resistor, and the current polarity can be controlled by the MODE pin to set the bidirectional current.

H-Bridge General Operation

The MP6519A works in a quad-MOSFET H-bridge topology and uses pulse-width-modulation (PWM) with average current control to achieve a bidirectional current output and fast dynamic current response. The switching frequency (f_{SW}) is configurable between 30kHz and 300kHz.

When enabled in normal operation, M1 and M4, turn on and off in the same sequence, and M2 and M3 turn on and off in the same sequence. M1/M4 and M2/M3 turn on and off in complementary operation with a dead time (DT) of about 25ns to avoid damage to the device due to shoot-through. All the MOSFET switches have a minimum on time of about 200ns. If the I_{OUT} direction is set to positive by pulling the MODE pin high, then I_{OUT} sensed by M2 and M4 is sent to the negative input of the error amplifier (EA). By comparing the I_{OUT} feedback signal with the current reference signal at the EA's positive node, the EA outputs an appropriate voltage that is compared with a sawtooth signal to provide a driver signal for M1/M4 and M2/M3. The device can enter four different modes to control the working sequence: shutdown mode, standby mode, normal switching mode, and current polarity mode.

Shutdown Mode

When the enable (EN) signal is pulled low, the MP6519A enters shutdown mode. In this mode, all circuits and blocks are disabled, and the MP6519A consumes below 1μA of shutdown current (I_{IN_SD}). There is a deglitch time of about 150ns to avoid mistriggering EN shutdown.

Standby Mode

The MP6519A enters standby mode if either of the following conditions is met:

- During start-up, the PWM signal on the PWM pin is low while EN is high.
- After start-up in normal switching operation, the PWM signal remains low for longer than 1ms if EN is high.

In this mode, the bandgap block and other control blocks begin working, except for the gate drive block of the internal switching MOSFETs. The device stops switching to reduce the quiescent current (I_{IIN_SBY}) at no load. Standby mode can also minimize the time during which I_{OUT} tracks the reference signal of the PWM input, which occurs after the EN signal. Since the MP6519A requires some time to establish the bandgap signal and other required control blocks, it is recommended to apply the PWM signal after a minimum of 300μs passes from the EN signal switching high.

Normal Switching Mode

If both the PWM and EN signals remain high, then the MP6519A enters normal switching mode immediately. In this mode, the feedback I_{OUT} closely follows the reference signal, which is received from the PWM input signal through an RC filter (for more details, see the Current Feedback section on page 14 and the Pulse-Width Modulation (PWM) Input Current Dimming section on page 13).

The H-bridge MOSFETs work with a fixed f_{SW} (see the Setting the Switching Frequency section on page 13). The I_{OUT} polarity can be changed easily by pulling MODE high or low (see the Current Polarity Mode section below).

Current Polarity Mode

The current polarity is set by MODE. If MODE is pulled high, the current is positive, and the current direction goes from LP to LN. By pulling MODE low, the current is negative, and the current direction goes from LN to LP. There is a deglitch time of about 150ns to avoid mistriggering changes in current polarity mode.

Setting the Full-Scale Output Current

The full-scale I_{OUT} reference voltage (V_{REF_FULL}) is set by connecting a resistor between the ISET pin and AGND. When I_{SET} is floated, V_{REF_FULL} is set to 200mV by default. If a resistor is connected between I_{SET} and AGND, then V_{REF_FULL} can be reduced below 200mV to reduce power loss on the feedback resistor. The MP6519A requires about 0.3ms to detect whether a resistor is available on ISET when the IC starts up for the first time. During this time, the MP6519A is not switching. V_{REF_FULL} can be calculated with Equation (1):

$$V_{REF\_FULL} = 0.2 \times \frac{40}{R_{ISET}(k\Omega)} \quad (1)$$

For example, if the ISET resistance (R_{ISET}) is 80kΩ, then the reference voltage is 100mV. For improved accuracy, a 40kΩ to 80kΩ R_{ISET} is recommended to achieve a 200mV to 100mV current reference voltage.

Start-Up Sequence

The MP6519A requires about 0.3ms to detect whether a resistor is available on ISET when the IC starts up for the first time. During this time, the MP6519A is not switching. It is recommended to apply a PWM signal after a minimum of 0.3ms passes from the EN signal (see Figure 2 and Figure 3).

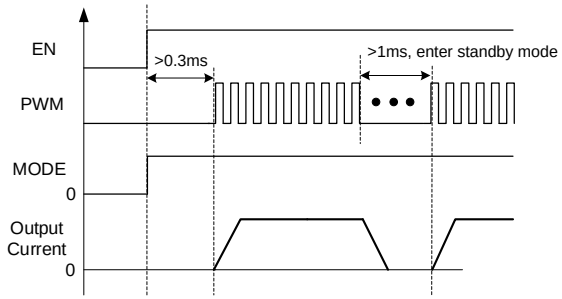


Figure 2: Positive Output Current Mode

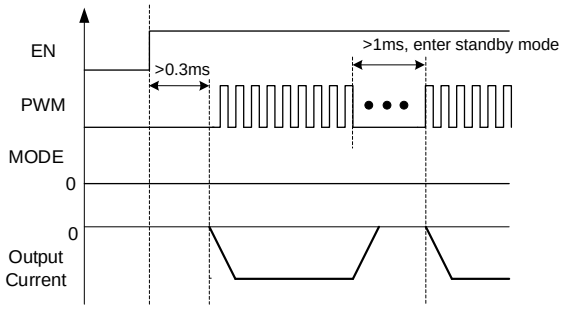


Figure 3: Negative Output Current Mode

Setting the Switching Frequency

The H-bridge MOSFET's f_{SW} is set by connecting a resistor between the FREQ pin and AGND. With a proper resistance, f_{SW} can be set between 30kHz and 300kHz. A higher f_{SW} results in smaller current ripple; however, the MOSFETs' switching loss is also larger. Therefore, a tradeoff is required for the design. The FREQ frequency (f_{FREQ}) can be calculated with Equation (2):

$$f_{FREQ} = \frac{22500}{R_{FREQ}(k\Omega)} \quad (2)$$

Pulse-Width Modulation (PWM) Input Current Dimming

If V_{REF_FULL} is set, then the actual I_{OUT} reference voltage (V_{REF_FB}) sent to the EA can be further controlled by applying a PWM input signal to the PWM pin. As a result, V_{REF_FULL} is chopped by the PWM input signal, and the current reference voltage is received from this chopped PWM voltage through the internal low-pass filter. For a smaller I_{OUT} reference ripple, the PWM input frequency is recommended to be between 20kHz and 100kHz. Considering the full-scale reference, V_{REF_FB} can be calculated with Equation (3):

$$V_{REF\_FB} = 0.2 \times \frac{40}{R_{ISET}(k\Omega)} \times D_{PWM} \quad (3)$$

Where D_{PWM} is the duty cycle of the PWM input.

Current Feedback

The current flowing through the load is sensed via a resistor connected between the IFB pin and AGND. This sensing voltage on IFB is sent to the feedback block circuit and used to generate the average feedback voltage (V_{IFB}),

which is equal to the average I_{OUT} multiplied by the sensing resistance (R_{IFB}). V_{IFB} is sent to the EA's negative node and compared with the I_{OUT} reference voltage on the EA's positive node. The EA output is COMP, and the COMP voltage (V_{COMP}) generates the internal MOSFET switch's on and off times. Figure 4 shows the current feedback loop.

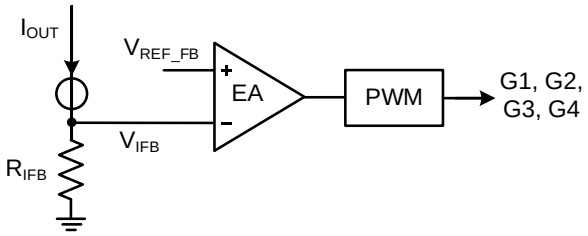


Figure 4: Current Feedback Loop

VCC Low-Dropout (LDO) Regulator

The MP6519A employs a low-dropout (LDO) regulator to provide a constant voltage (5V) at VCC. The VCC voltage (V_{CC}) is used for the internal power supply of the logic circuit and driver circuit. When the input voltage (V_{IN}) is sufficiently high (exceeds 5.2V), the VCC output is 5V. When V_{IN} drops below 5V, V_{CC} drops with V_{IN}. The dropout voltage is about 100mV. If V_{CC} drops below 2.15V, then the IC triggers a power reset sequence and shuts down. The IC resumes normal operation when V_{CC} exceeds 2.3V.

High-Side MOSFET (HS-FET) Driver

M1 and M3's high-side MOSFETs (HS-FETs) are N-channel MOSFETs. When M1 and M3 turn on, a bootstrap supply voltage across the BSTP and BSTN pins is required. The bootstrap voltage (V_{BST}) is generated by a combination of the internal charge pump and a 5V VCC. This allows the IC to work at 100% duty cycle to provide sufficient driver voltage for M1 and M3's HS-FETs.

Over-Current Protection (OCP)

To provide robust protection during an over-current (OC) event, the IC uses a two-level protection mode.

If the current flowing through the MOSFETs exceeds 150% of the full-scale setting value during two consecutive switching cycles, then the IC stops switching and triggers a power reset sequence to restart after 1ms.

If the current flowing through the MOSFETs exceeds 200% of the full-scale setting value, then the IC latches off. If the HS-FET triggers an OC fault, the HS-FET turns off immediately and the $\overline{FT}$ pin is pulled low. At the same time, the two low-side MOSFETs (LS-FETs) turn on for several ms before turning off, and the IC latches off. If the LS-FET triggers an OC fault, the LS-FET turns off immediately and the $\overline{FT}$ pin is pulled low. At the same time, the HS-FETs turn on for several ms before turning off, and the IC latches off.

Input Over-Voltage Protection (OVP)

During operation, the energy stored in I_{LOAD} is delivered to the input side during the free-wheeling time. If V_{IN} and I_{OUT} are sufficiently high, the energy sent back to the input side causes V_{IN} to rise. The MP6519A employs V_{IN} protection to avoid damage to the IC due to a high voltage spike. If V_{IN} exceeds the input over-voltage (OV) threshold for four consecutive switching cycles, then the IC stops switching and latches off immediately.

Junction Over-Temperature Protection (OTP)

If the IC's junction temperature (T_J) exceeds 150°C, then the IC stops switching. Once T_J drops below 130°C, the IC resumes normal operation.

Fault Indication Output ($\overline{FT}$)

During normal operation, $\overline{FT}$ is a high-impedance open-drain pin. If any fault occurs during operation, $\overline{FT}$ pulls low to indicate the fault condition for the external system. Recycle the input power or toggle the EN signal to remove the fault latch condition.

Enable (EN)

To enable the IC, a logic-high signal must be applied to EN, and the high-level signal time must be longer than 10µs. To shut down the IC, pull EN to logic low, and the low-level signal must be longer than 100ns.

APPLICATION INFORMATION

Selecting the Input Capacitor

The input capacitor (C_{IN}) reduces the surge current drawn from the input supply as well as the device's switching noise. The impedance of C_{IN} at f_{SW} must be below the input source impedance to prevent the high-frequency switching current from passing through to the input. Ceramic capacitors with X5R or X7R dielectrics are recommended for their low-ESR and small temperature coefficients. A larger-value capacitor is helpful for reducing V_{IN} ripple and noise. For most applications, two 22µF ceramic capacitors in parallel are sufficient. It is recommended to connect a capacitor on each VIN pin.

Setting the Full-Scale Output Current

If a resistor is connected between ISET and AGND, I_{OUT} can be calculated with Equation (4):

$$I_{OUT} = 0.2 \times \frac{40}{R_{ISET}(k\Omega)} \times \frac{1}{R_{IFB}(\Omega)} \quad (4)$$

If ISET is floated, I_{OUT} can be calculated with Equation (5):

$$I_{OUT} = \frac{0.2}{R_{IFB}(\Omega)} \quad (5)$$

For example, if R_{ISET} is 80kΩ, then the V_{REF_FULL} is 100mV. For improved accuracy, a 40kΩ to 80kΩ R_{ISET} is recommended to achieve a 200mV to 100mV V_{REF_FULL}.

Setting the Feedback Resistor

The power loss of the sensing resistor (P_{LOSS_RIFB}) can be calculated with Equation (6):

$$P_{LOSS\_RIFB} = \frac{V_{REF\_FULL}^{2}}{R_{IFB}(\Omega)} \quad (6)$$

To guarantee a current reference, the nominated power rating of P_{LOSS_RIFB} is recommended to be twice the calculated power loss with a minimum 1% accuracy resistor.

Setting the Switching Frequency

A higher f_{SW} results in smaller current ripple; however, the MOSFETs' switching loss is also higher. Therefore, a tradeoff is required for the design. f_{FREQ} can be calculated with Equation (7):

$$f_{FREQ} = \frac{22500}{R_{FREQ}(k\Omega)} \quad (7)$$

Since the power loss of this resistor is small, a 0603 or 0402 resistor size is sufficient.

Selecting the Compensation Loop

The loop compensation components stabilize the closed loop and achieve improved transient response (see Figure 5).

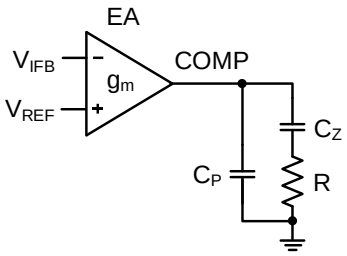


Figure 5: Compensation Loop

The transfer function of loop compensation from the EA input to the EA output (G_C) can be calculated with Equation (8):

$$G_C(s) = \frac{g_m}{(C_Z + C_P)s} \frac{(1 + sRC_Z)}{(1 + sR\frac{C_Z C_P}{C_Z + C_P})} \quad (8)$$

Where g_m is the EA's transconductance.

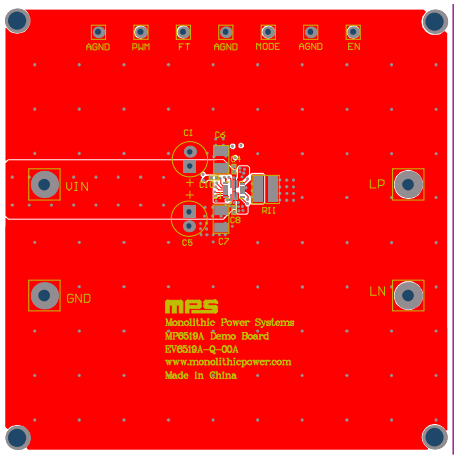
The transfer function's zero point is comprised of R and the zero point (C_z). The pole point is comprised of R and C_Z in parallel with the polar point (C_P).

Typically, for an inductive load with resistance, the compensation zero can be set as the load pole, which is comprised of the load inductance (L) and its resistance. The compensation pole point is typically set to about f_{SW} to eliminate high-frequency noise. After the zero and pole point of the compensation is fixed, R can be used to increase the loop bandwidth. 1/10 to 1/5 of f_{SW} can be set as the closed-loop bandwidth to achieve optimal system response.

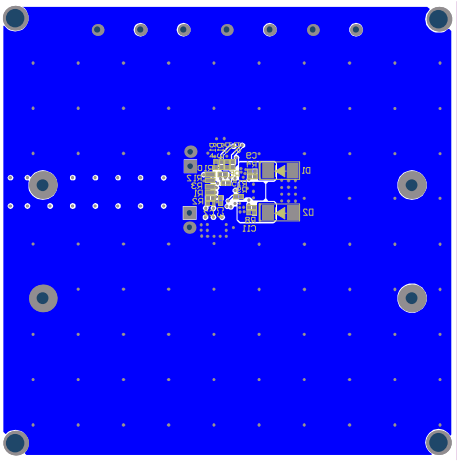
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 6 and follow the guidelines below:

1. Place C_{IN} close to the VIN pin.
2. Use wider copper for the input, output, and ground-connecting wire to improve thermal performance.
3. Place as many ground vias near the output capacitor (C_{OUT}) and C_{IN} as possible to improve thermal performance.
4. Keep the IFB feedback signal far away from noise sources.



Top Layer



Bottom Layer

Figure 6: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

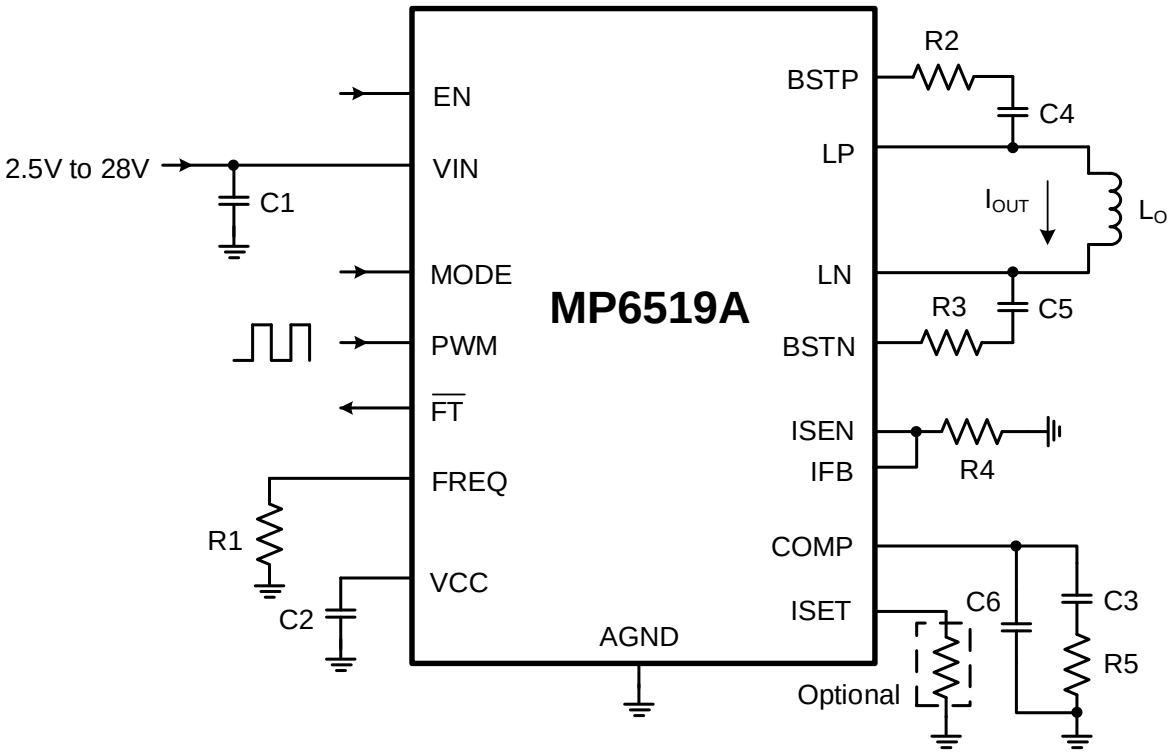
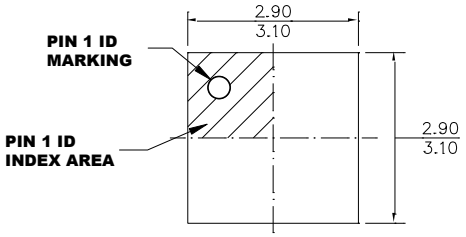


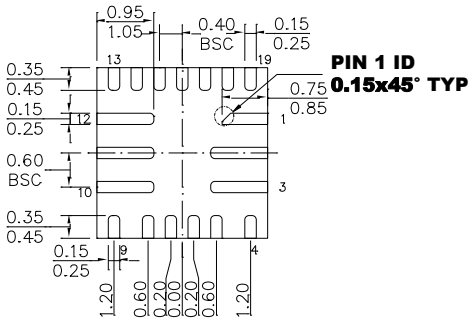
Figure 7: Typical Application Circuit

PACKAGE INFORMATION

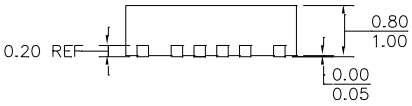
QFN-19 (3mmx3mm)



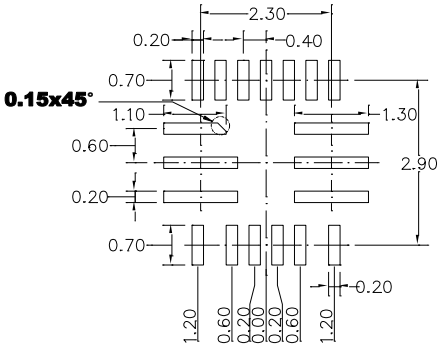
TOP VIEW



BOTTOM VIEW



SIDE VIEW

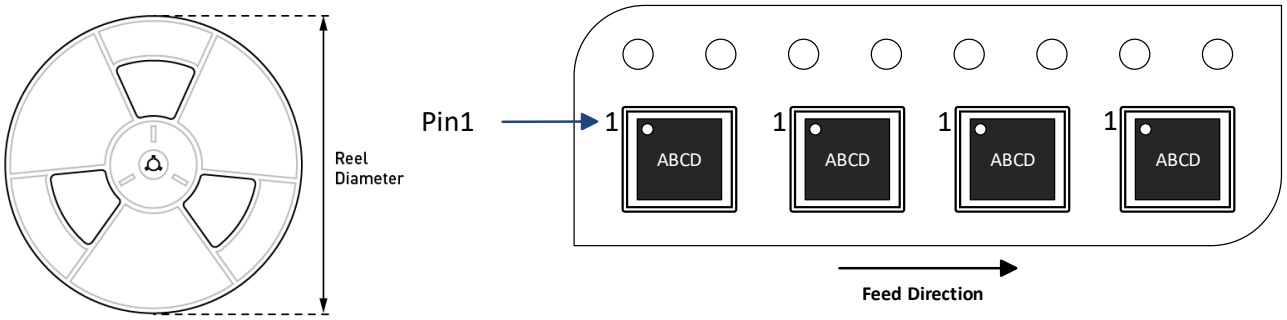


RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERNS OF PIN2,3,10,11 AND 12 HAVE THE SAME SHAPE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6519AGQ	QFN-19 (3mmx3mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	7/15/2024	Initial Release	-