MP6509

2.7V-to-18V, 1.2A, Bipolar Stepper Motor Driver with Integrated MOSFETs

The Future of Analog IC Technology

DESCRIPTION

The MP6509 is a bipolar stepper-motor driver with dual, built-in full-bridges consisting of N-channel power MOSFETs.

It operates from a supply voltage ranging from 2.7V to 18V and can deliver motor current up to 1.2A per channel. The Internal safety features include over-current protection(OCP), under-voltage lockout protection(UVLO) and thermal shutdown. A fault output flag is available to indicate OCP and thermal shutdown.

The MP6509 comes in 20-pin, 6.5mmx6.4mm TSSOP-EP package with an exposed thermal pad on the backside.

FEATURES

- Wide 2.7V to 18V Input Voltage Range
- Two Internal Full Bridge Drivers
- Low On Resistance(HS:250mΩ; LS:250mΩ)
- Four Selectable Current Attenuation Modes
- Internal Charger Pump for the High-Side Driver
- Low Quiescent Current:1.6mA
- Low Sleep Current: 1uA
- Over-Current Protection
- Thermal Shutdown and UVLO Protection
- Fault Indication Output
- Thermally-Enhanced Surface-Mount Package

APPLICATIONS

- POS Printers
- Video Security Camera
- Digital Still Cameras
- Battery Powered Toys

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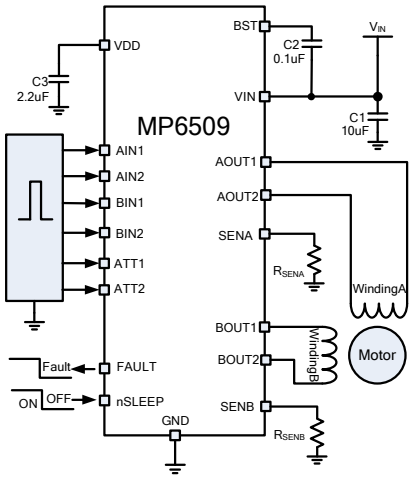
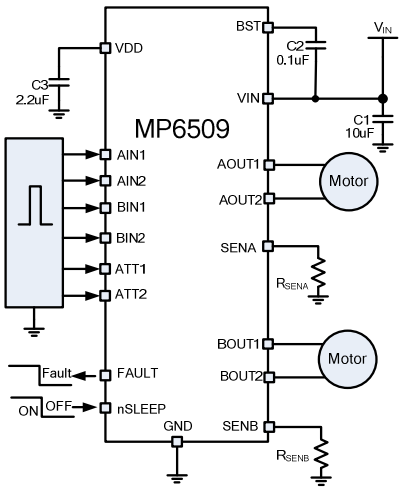
TYPICAL APPLICATION



Stepper Motor Application



Dual DC Motor Application

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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP6509GF*	TSSOP-20 EP	*See Below*

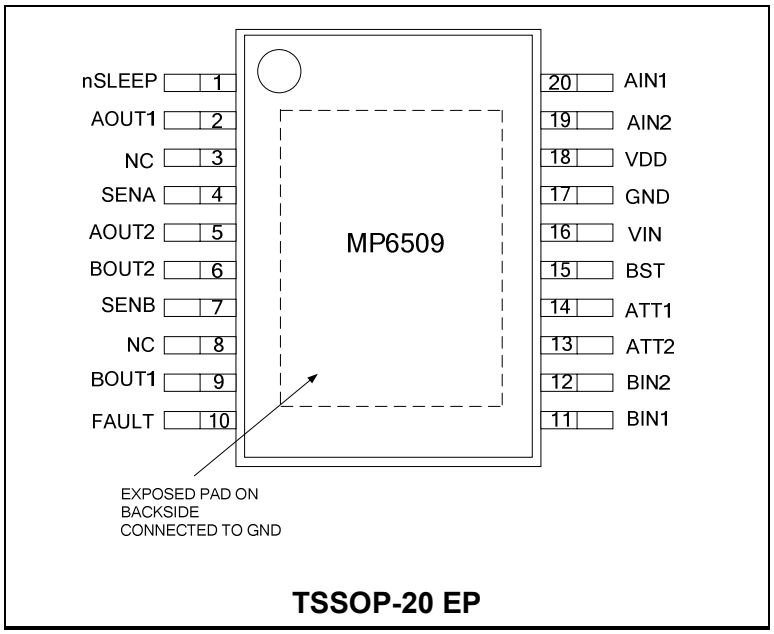
* For Tape & Reel, add suffix –Z (e.g. MP6509GF–Z);

TOP MARKING

MPSYYWW
MP6509
LLLLLLLLL

MPS: MPS prefix:
YY: year code;
WW: week code:
MP6509: part number;
LLLLLLLLL: lot number;

PACKAGE REFERENCE



TSSOP-20 EP

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ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} ..... -0.3V to 20V
AOUTx Voltage V_{AOUTx} .....-0.3V to V_{IN}+1V
BOUTx Voltage V_{BOUTx} .....-0.3V to V_{IN}+1V
BST Voltage V_{BST}.....-0.3V to V_{IN}+6.5V
Sense Voltage V_{SENx} ..... -0.3V to 0.5V
All Other Pins..... -0.3V to 6.5V
Junction Temperature.....150°C
Lead Temperature .....260°C
Continuous Power Dissipation (T_A = +25°C) (2)
TSSOP-20 EP 3.1W
Operating Temperature.....-40°C to +85°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 2.7V to 18V
Output Current $I_{A/BOUT}$.....1.2A
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TSSOP-20 EP	40	8	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN}=9V, T_A =25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input Supply Voltage	V_{IN}		2.7		18	V
V_{DD} Voltage	V_{DD}			4.85		V
Quiescent Current	I_{IN}	nSLEEP=1, I_{OUT}=0, Output disable		1.6	1.8	mA
	I_{IN_SLEEP}	nSLEEP=0, V_{IN}=9V			1	μA
Integrated MOSFETs						
Output On Resistance	R_{HS}	I_{OUT}=500mA, V_{IN}=9V T_J=25°C		250	350	mΩ
		I_{OUT}=500mA, V_{IN}=2.7V T_J=25°C		310	400	mΩ
		I_{OUT}=500mA, V_{IN}=9V T_J=85°C		350		mΩ
		I_{OUT}=500mA, V_{IN}=2.7V T_J=85°C		400		mΩ
	R_{LS}	I_{OUT}=500mA, V_{IN}=9V T_J=25°C		235	350	mΩ
		I_{OUT}=500mA, V_{IN}=2.7V T_J=25°C		310	400	mΩ
		I_{OUT}=500mA, V_{IN}=9V T_J=85°C		310		mΩ
		I_{OUT}=500mA, V_{IN}=2.7V T_J=85°C		400		mΩ
Body-Diode Forward Voltage	V_F	I_{OUT}=500mA			1	V
Control Logic						
UVLO Threshold (Rising)	V_{IN_RISE}				2.5	V
UVLO Hysteresis	V_{HYS}		30	75	120	mV
Input Logic 'Low' Threshold	V_{IL}				0.6	V
Input Logic 'High' Threshold	V_{IH}		2			V
nSLEEP Logic, Low	V_{SLEEP_L}				0.4	V
nSLEEP Logic, High	V_{SLEEP_H}		2			V
Fault Output Logic, Low	V_{FAULT_L}	Flag triggered by OTP 1mA Current.			200	mV
Fault Output Leakage Current	I_{LEAK_FAULT}	V_{FAULT}=5V			1	μA
Constant Off Time	T_{OFF}		21	26	31	μs
Propagation Delay Time (On)	T_{ON_DELAY}(HS)	10mA Source Current	100	200	300	ns
	T_{ON_DELAY}(LS)		20	55	90	ns
Propagation Delay Time (Off)	T_{OFF_DELAY}(HS)		135	180	225	ns
	T_{OFF_DELAY}(LS)		80	130	180	ns

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN}=9V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Cross Over Delay	T_{CROSS}	LS off to HS on for one bridge arm	350	450	550	ns
		HS off to LS on for one bridge arm	275	355	435	ns
Sleep Mode Wakeup Time	T_{WAKE}	Sleep active high to full bridge turn on (V_{BST}=100nF)	0.65	0.75	0.9	ms
Protection Circuitry						
Current Limit Sense Trip Voltage	V_{REF}	ATT1=L, ATT2=L	175	204	233	mV
	V_{TRIP}	ATT1=H, ATT2=L	135	163	191	mV
		ATT1=L, ATT2=H	76	103	130	mV
		ATT1=H, ATT2=H	15	44	73	mV
Blanking Time	T_{BLANK}		2	2.5	3	µs
Over-Current Trip Level	I_{OCP1}	High Side	2.2	3.4	4.6	A
	I_{OCP2}	Low Side	1.8	2.4	3	A
Over-Current Deglitch Time	T_{DEG}		0.75	1.1	1.45	µs
Over-Current Protection Period	T_{OCP}		1.3	1.8	2.3	ms
Thermal Shutdown				165		°C
Thermal Shutdown Hysteresis				15		°C

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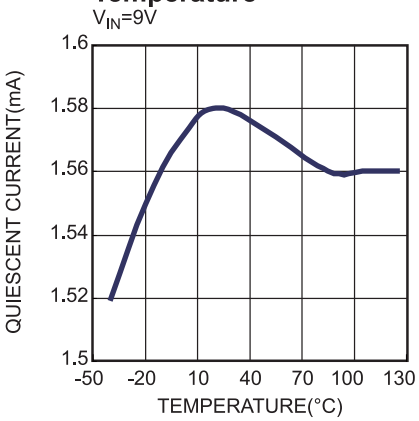
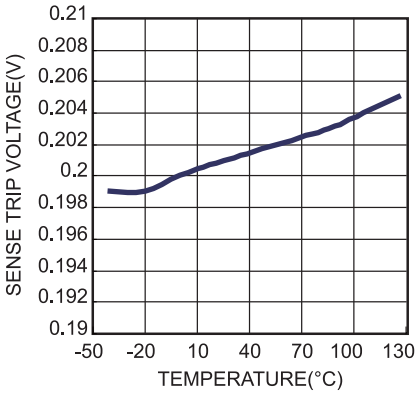
TYPICAL CHARACTERISTICS

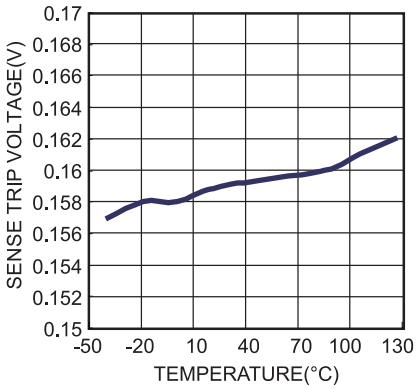
Quiescent Current vs. Temperature



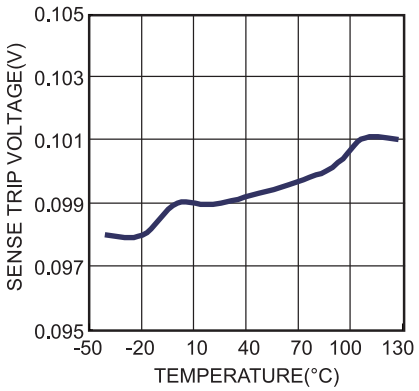
Sense Trip Voltage vs. Temperature



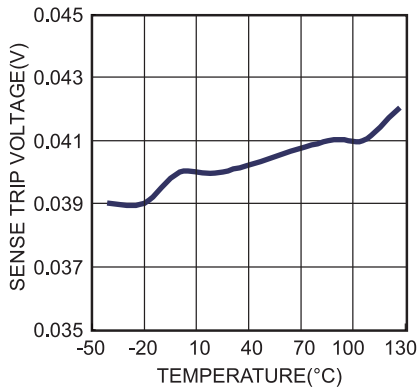
80% Sense Trip Voltage vs. Temperature



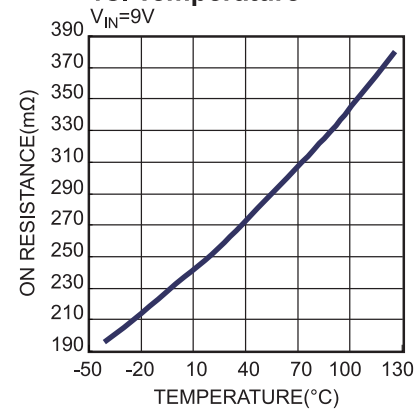
50% Sense Trip Voltage vs. Temperature



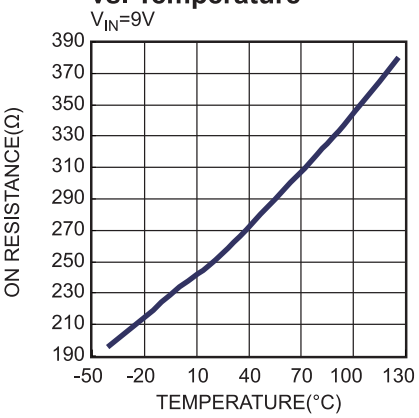
20% Sense Trip Voltage vs. Temperature



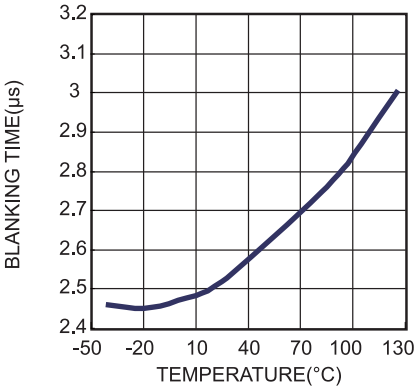
Bridge A HS On Resistance vs. Temperature



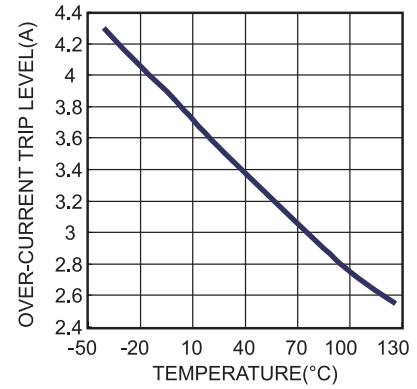
Bridge B HS On Resistance vs. Temperature



Blanking Time vs. Temperature



Bridge A HS Over-Current Trip Level vs. Temperature



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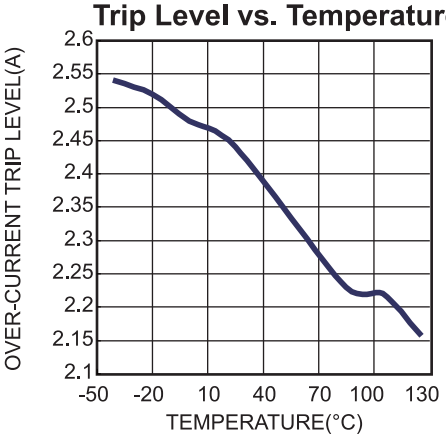
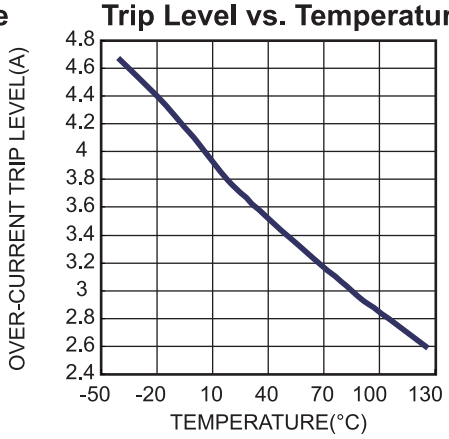
TYPICAL CHARACTERISTICS

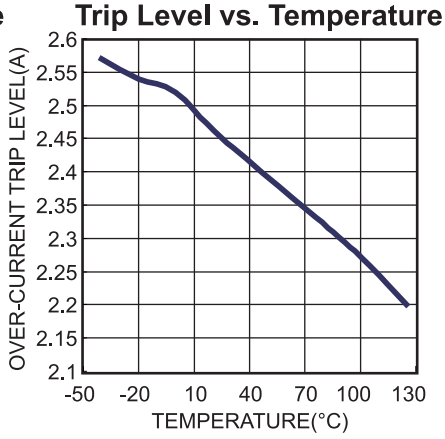
Bridge A LS Over-Current Trip Level vs. Temperature



Bridge B HS Over-Current Trip Level vs. Temperature



Bridge B LS Over-Current Trip Level vs. Temperature



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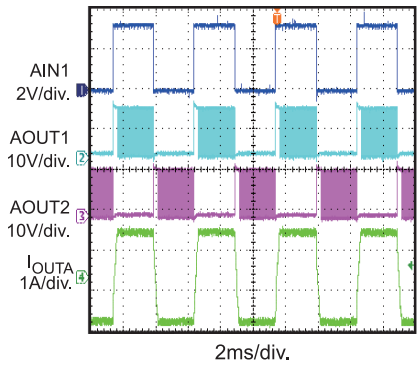
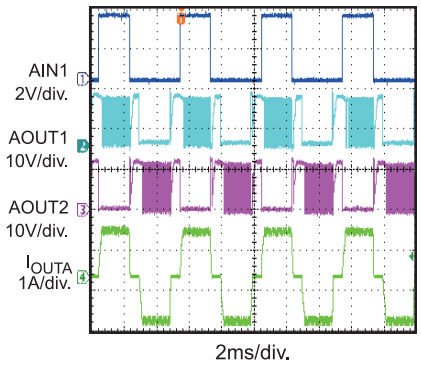
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section. V_{IN}=12V, I_{OUT}=1.2A, F_{STEP}=200Hz, R+L Load: L=2mH, R=3.3Ω, T_A=25°C, unless otherwise noted.

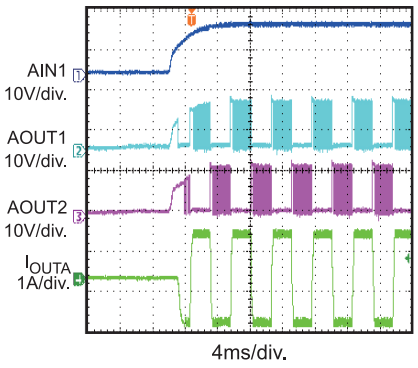
Steady State-Full Step



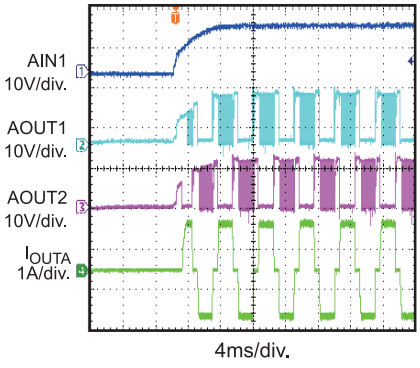
Steady State-Half Step



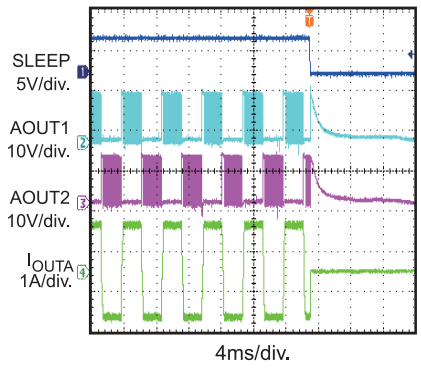
Power Ramp Up-Full Step



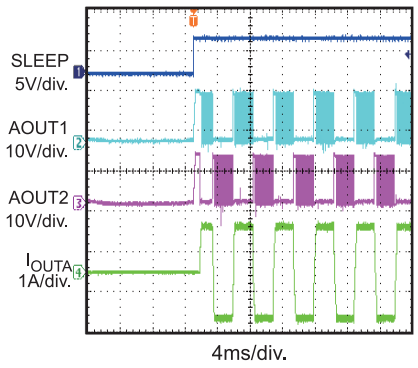
Power Ramp Up-Half Step



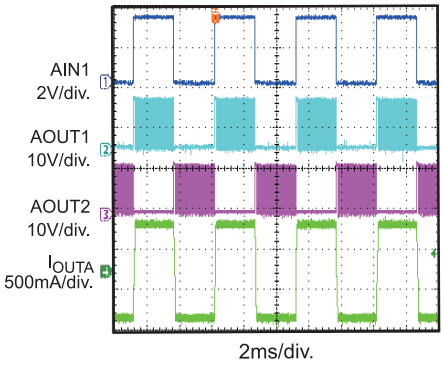
Sleep Entry-Full Step



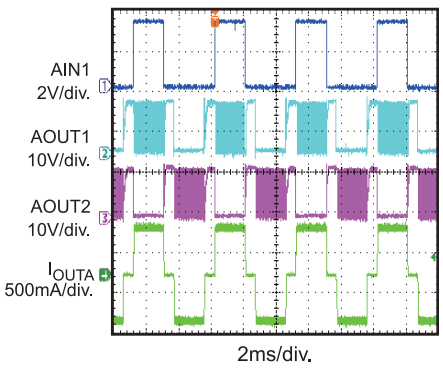
Sleep Recovery-Full Step



50% Current Attenuation-Full Step



50% Current Attenuation-Half Step



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PIN FUNCTIONS

Pin #	Name	Description
1	nSLEEP	Sleep Mode Input. Logic low to enter low-power sleep mode. Internal pull down.
2	AOUT1	Bridge A Output Terminal 1.
3,8	NC	Not Connected.
4	SENA	Bridge A Sense Resistor Connector. Connect to current sensor resistor for bridge A
5	AOUT2	Bridge A Output Terminal 2.
6	BOUT2	Bridge B Output Terminal 2.
7	SENB	Bridge B Sense Resistor Connector. Connect to current sensor resistor for bridge B.
9	BOUT1	Bridge B Output Terminal 1.
10	FAULT	Fault Indication. Open-drain output type, logic low when in fault condition (OCP, OTP).
11	BIN1	Gate signal input to control BOUT1.
12	BIN2	Gate signal input to control BOUT2.
13	ATT2	Current Attenuation Mode Select. See applications notes for details. ATT1, ATT2 set the current setting reference voltage attenuation ratio –100%, 80%, 50%, 20%. Internal pull down.
14	ATT1	
15	BST	Charge Pump Output. Connect a 10nF-to-100nF ceramic capacitor to VIN.
16	VIN	Power Supply Input. Ranges from 2.7V to 18V.
17	GND	Ground.
18	VDD	Internal control and logic supply voltage.
19	AIN2	Gate signal input to control AOUT2.
20	AIN1	Gate signal input to control AOUT1.

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BLOCK DIAGRAM

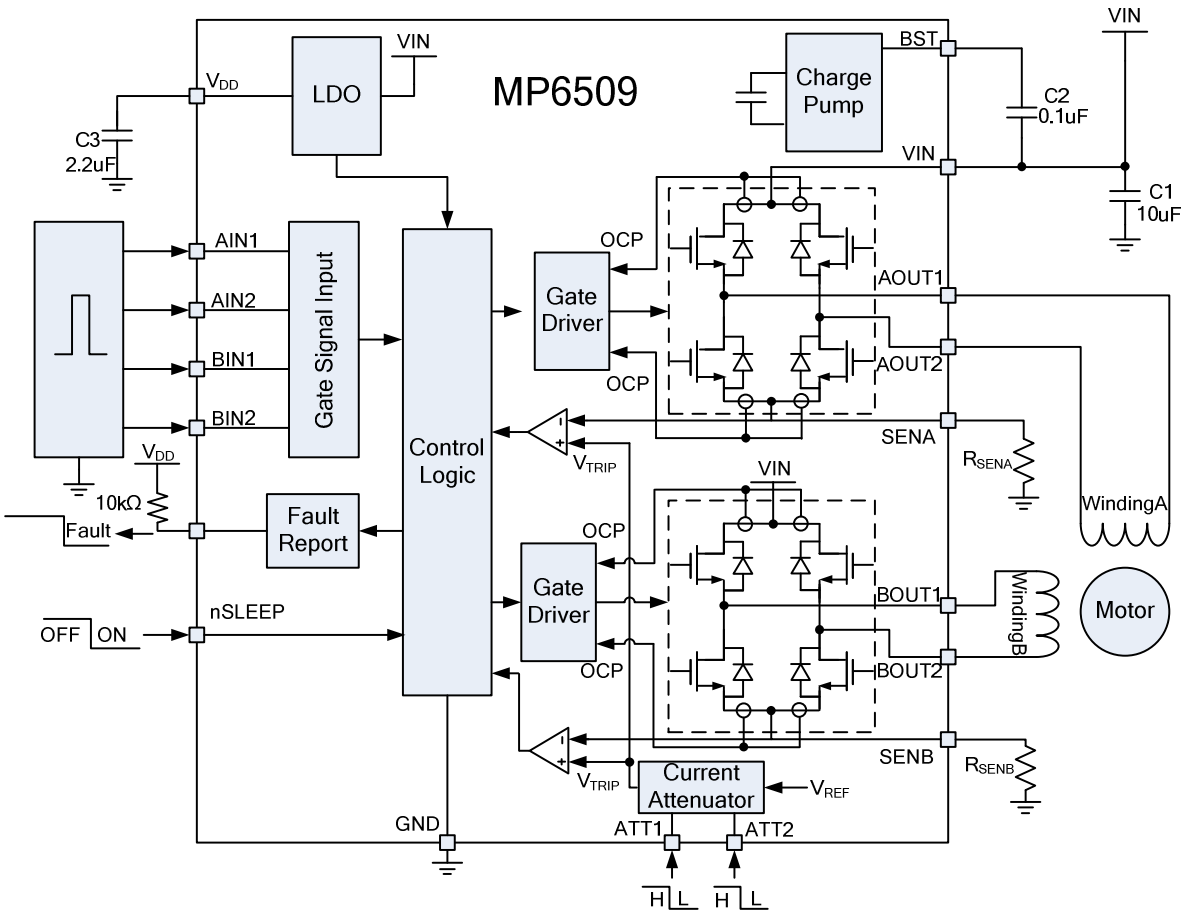

Figure 1: Function Block Diagram

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OPERATION

The MP6509 is a motor driver that integrates 8 N-channel power MOSFETs for dual, internal full-bridges with 1.2A output current capability over an input voltage range of 2.7V to 18V. It can drive a stepper motor or two DC motors.

The motor output current can be either controlled by an external pulse width modulator (PWM) or internal PWM current controller.

The MP6509 includes the following fault protections: over-current protection(OCP), under-voltage lockout(UVLO) and over-temperature protection(OTP).

It also provides a low-power sleep mode.

External PWM Current Control

The motor current can be regulated by applying external PWM signals on the input pins AIN1, AIN2, BIN1 and BIN2. For phase A, the AIN1 and AIN2 input pins control the state of the AOUT1 and AOUT2; similarly for phase B, the BIN1 and BIN2 input pins control the state of the BOUT1 and BOUT2.

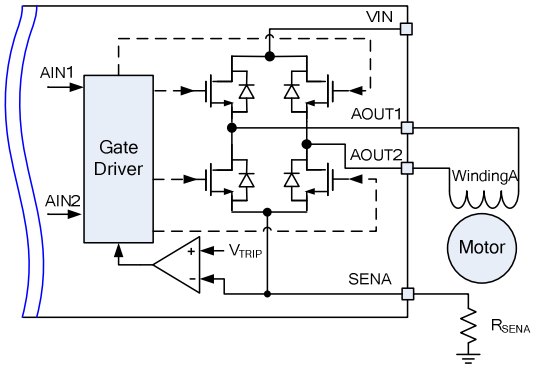

Figure 2: Full-Bridge Control Circuit

Table 1 shows the input signal logic and bridge output state.

Table 1: Full-Bridge Gate Logic

A/BIN1	A/BIN2	A/BOUT1	A/BOUT2
L	L	High Impedance	High Impedance
L	H	GND	VIN
H	L	VIN	GND
H	H	GND	GND

In external PWM control mode, the winding's inductive current ramps up when the high-side MOSFET is on and freewheels during the high-side MOSFET's off time to cause the recirculation current.

There are two modes for this recirculation current: slow decay and fast decay, both of which are shown in Figure 3 for forward operation and Figure 4 for reverse operation.

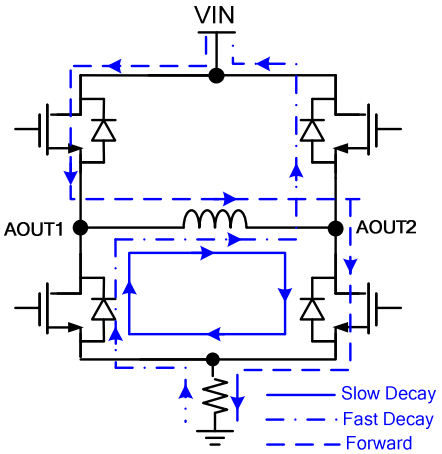

Figure 3: Forward Operation

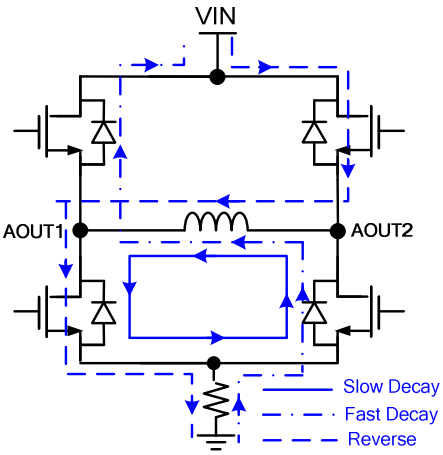

Figure 4: Reverse Operation

For slow decay mode, the current circulates through the two low-side MOSFETs. For fast decay mode, the current flows through the body diodes of the other diagonal two MOSFETS.

To configure the MP6509 for fast decay mode, apply the PWM signal to one input pin and keep

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the other input pin low; for slow decay mode, apply the PWM signal to one input pin and keep the other input pin high. See Table 2 for more configuration details and Figure 5 for detailed waveforms.

Table 2: PWM Control

A/BIN1	A/BIN2	Mode
H (PWM)	L	Forward
L (PWM)	L	Fast Decay
L	H (PWM)	Reverse
L	L (PWM)	Fast Decay
H	L (PWM)	Forward
H	H (PWM)	Slow Decay
L (PWM)	H	Reverse
H (PWM)	H	Slow Decay

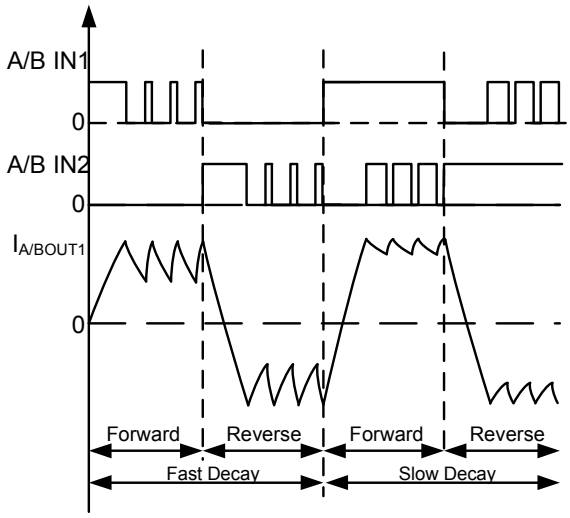

Figure 5: External PWM Current Control Waveform

Internal PWM Current Control

For this control method, the motor current is regulated by an internal constant off-time PWM current control circuit as the following:

- Initially, a diagonal pair of MOSFETs turns on so current can flow through the motor winding.
- The current increases in the motor winding, which is sensed by an external sense resistor (R_{SENSE}). During the initial blanking time T_{BLANK} (3us), the high-side MOSFET always turns on in spite of current limit detection.
- When the voltage across R_{SENSE} reaches the internal reference voltage threshold V_{TRIP}, the internal current comparator shuts off the high-side MOSFET.
- The stepper motor's inductance causes the current to freewheel through the two low-side MOSFETs (slow decay).
- During this freewheeling time, the current decreases until the internal clock reaches its' constant off time (typically 30μs). After that, the high-side MOSFET is enabled to increase the winding current again.
- The cycle then repeats.

Calculate the current limit as:

$$I_{LIMIT} = \frac{V_{REF}}{R_{SENSE}} \quad (1)$$

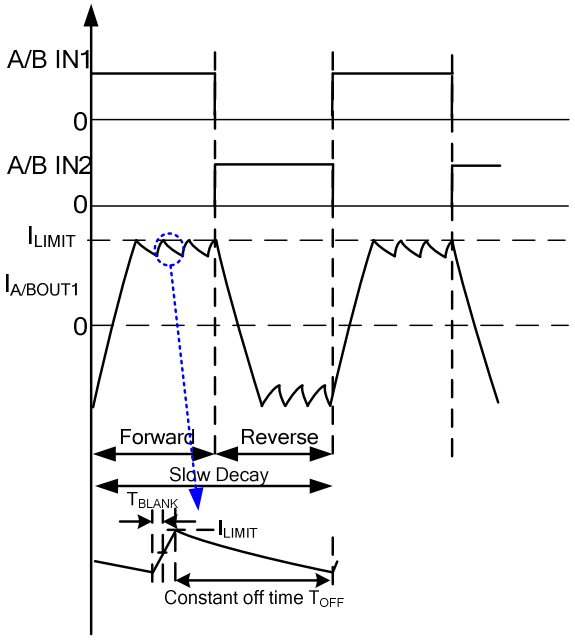

Figure 6: Internal PWM Current Control Waveform

The value of V_{REF} can be switched to four-step settings depending on the status of the two inputs ATT1 and ATT2. This is helpful to reduce the power dissipation when motor holding current is supplied. See Table 3 for more configuration details.

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Table 3: Attenuation Function for V_{REF} Value

ATT1	ATT2	Attenuation Ratio
L	L	100%
H	L	80%
L	H	50%
H	H	20%

The formula used to calculate the output current limit when using the function for attenuating the V_{REF} value is given below:

$$I_{LIMIT} = \frac{V_{REF}}{R_{SENSE}} \times \text{Attenuation Ratio} \quad (2)$$

Sleep Mode

The MP6509 provides low-power standby sleep mode.

Connect the nSLEEP pin to logic low to enable a low-power sleep state. In this state, the two full bridges are disabled and the internal circuits such as the gate drive, internal regulator, and charge pump all shut down. Connect the nSLEEP pin to logic high to wake up the MP6509 from sleep mode, though there is a delay time of ~1ms until the internal circuitry stabilizes.

Blanking Time

There is usually a current spike during the switching transition due to the body diode's reverse-recovery current or the distributed inductance or capacitance. This current spike requires filtering to prevent it from erroneously shutting down the high-side MOSFET. An internal blanking time T_{BLANK} blanks the output of the current sense comparator when the outputs are switched, which is also the minimum on time for high-side MOSFET.

Enable

If all the inputs (AIN1, AIN2, BIN1 and BIN2) are logic low, the MP6509's outputs are disabled while the charger pump and internal regulator remain active.

Synchronous Rectifier

The MP6509 enters a synchronous rectifier (SR) mode during the constant off-time period when the current limit threshold is exceeded, and the load current freewheels in slow decay SR mode. In slow decay mode, the current freewheels through one low-side MOSFET and the body diode of the other low-side MOSFET to short the winding. The SR mode enables both two low-side MOSFETs, which feature a lower voltage drop and lower power dissipation during decay operation.

Over-Current Protection

The over-current protection circuit limits the current through the FET by disable the gate driver. If the over-current limit threshold is reached and lasts for longer than the over-current deglitch time, all MOSFETs in the H-bridge will be disabled and the nFAULT pin will be driven low. The driver will remain disabled and is reset to enable state after 2ms(typ). Please note that only the H-bridge in which the OCP is detected will be disabled while the other bridge will operate normally.

Over-current conditions on both high and low side devices; i.e., a short to ground, supply, or across the motor winding will all result in an over-current shutdown. Note that over-current protection does not use the current sense circuitry used for PWM current control, and is independent of the sense resistor value or VREF voltage.

Thermal Shutdown

The junction temperature of the IC is internally monitored. If the junction temperature exceeds the threshold value (typically 165ºC), the converter is shut down (the fault pin goes low) and recoveries once the junction temperature drops to about 150ºC (15ºC hysteresis).

UVLO protection

The MP6509 has UVLO protection. When the VIN exceeds the UVLO rising threshold, the MP6509 powers up. It shuts off when VIN drops below the UVLO falling threshold.

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APPLICATION INFORMATION

Driver Mode:

The MP6509 could be configured for both full-step and half-step modes by sequentially energizing the two windings.

Full-step drive energizes two winding phases at any given time. The stator windings are energized as per the sequence shown in Table 4. There are a total of four steps for one cycle in the sequence [5]: AB→$\overline{A}$B→$\overline{A}\,\overline{B}$→A$\overline{B}$.

Half-step energizes the stator windings as per the sequence shown in

Table 5. There are a total of eight steps for one cycle: AB→B→$\overline{A}$B→$\overline{A}$→$\overline{A}\,\overline{B}$→$\overline{B}$→A$\overline{B}$→A.

Figure 7 shows the operating waveforms for both full and half step drives.

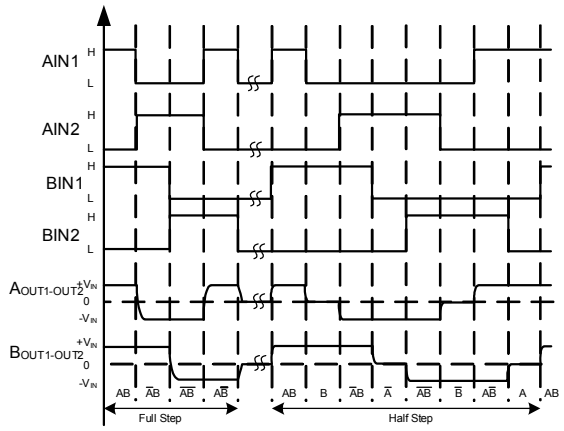

Figure 7: Signal Logic Sequences for Full-Step and Half-Step

Table 4 [6]: Full-Step Drive Sequence

Sequence (Full Step)	1	2	3	4
A	+			+
B	+	+		
$\overline{A}$		+	+	
$\overline{B}$			+	+

Table 5 [6]: Half-Step Drive Sequence

Sequence (Half Step)	1	2	3	4	5	6	7	8
A	+						+	+
B	+	+	+					
$\overline{A}$			+	+	+			
$\overline{B}$					+	+	+	

Note:

5) A means +VIN between AOUT1 and AOUT2 for winding A, while $\overline{A}$ means -VIN between AOUT1 and AOUT2. The same applies to winding B.
6) "+" item is the selected winding voltage.

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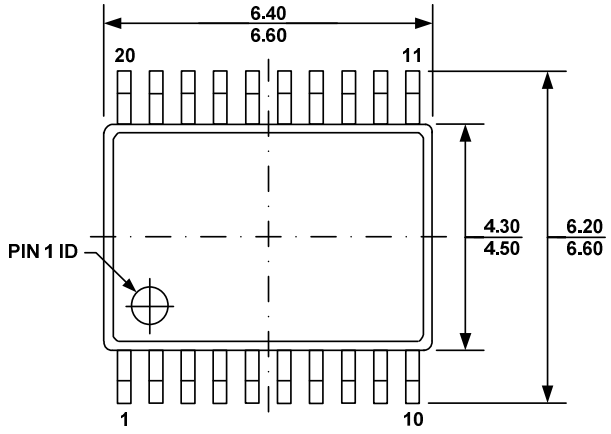
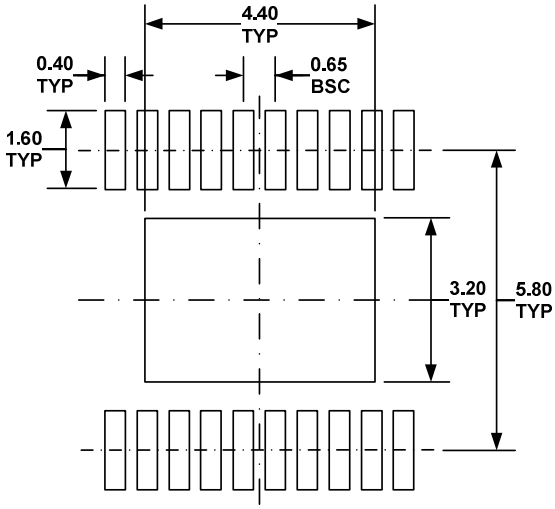
PACKAGE INFORMATION

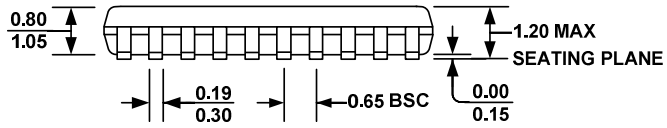
TSSOP-20



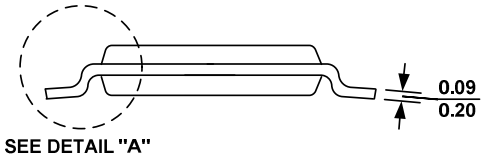
TOP VIEW



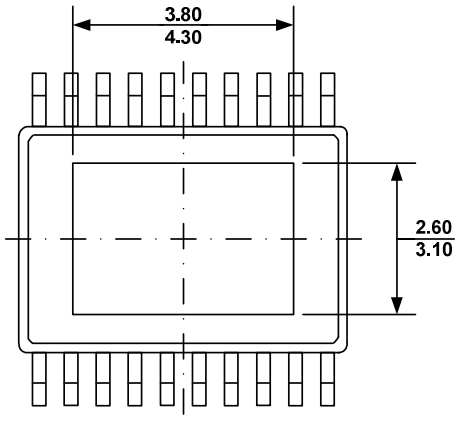
RECOMMENDED LAND PATTERN



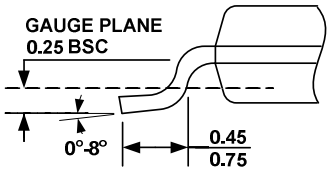
FRONT VIEW



SIDE VIEW



BOTTOM VIEW



DETAIL "A"

EP

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION ACT.
6) DRAWING IS NOT TO SCALE.

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