MP62180/MP62181

3.3V/5V, Single-Channel 2A Current-Limited Power Distribution Switch

The Future of Analog IC Technology

DESCRIPTION

The MP62180/MP62181 Power Distribution Switch features internal current limiting to prevent damage to host devices due to faulty load conditions. The MP62180/MP62181 operates from a 3.3V or 5V nominal input voltage and includes an 85mΩ Power MOSFET to handle up to 2A continuous load with a 2.8A typical current limit. The MP62180/MP62181 has built-in protection for both over current and increased thermal stress. For over-current protection (OCP), the device will limit the current by going into a constant current mode.

When continuous output overload condition exceeds power dissipation of the package, the thermal protection will shut the part off. The device will recover once the device temperature reduces to approx 120°C.

The MP62180/MP62181 is available in QFN8E, MSOP8E and SOIC8 packages.

FEATURES

- 2A Continuous Current
- 2.8A accurate Current Limit
- 2.7V to 5.5V Supply Range
- 90uA Quiescent Current
- 75mΩ MOSFET
- Thermal-Shutdown Protection
- Under-Voltage Lockout
- 8ms FLAG Deglitch Time
- No FLAG Glitch During Power Up
- Reverse Current Blocking
- Active High & Active Low Options

APPLICATIONS

- Smartphone and PDA
- Portable GPS Device
- Notebook PC
- Set-top-box
- Telecom and Network Systems
- PC Card Hot Swap
- USB Power Distribution

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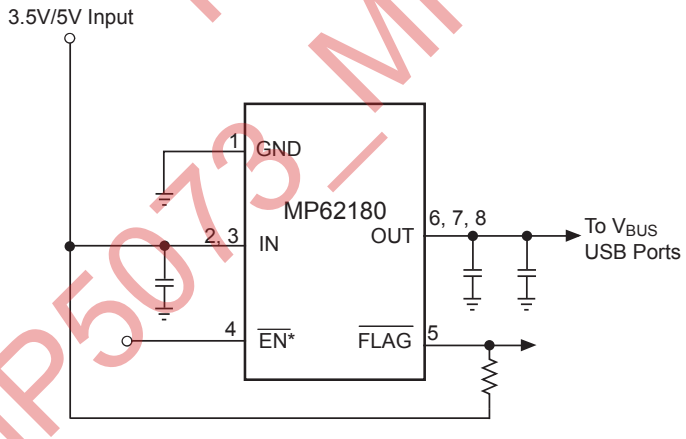
TYPICAL APPLICATION



SINGLE-CHANNEL
* EN is active high for MP62181

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ORDERING INFORMATION

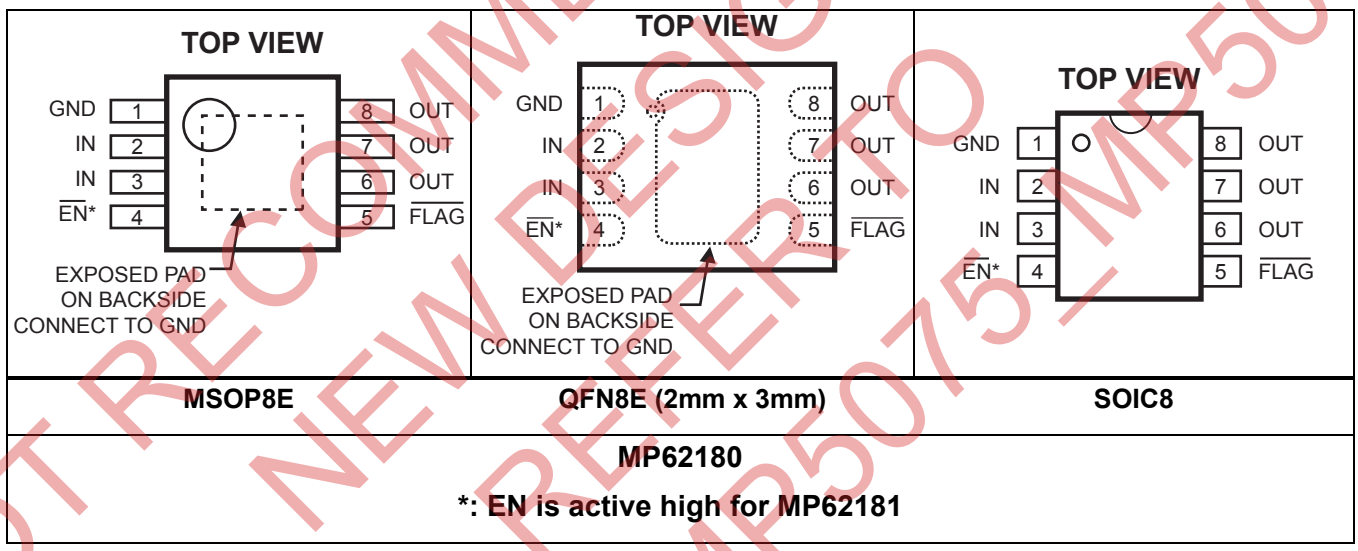
Part Number	Enable	Switch	Maximum Continuous Load Current	Typical Short-Circuit Current @ T_A=25C	Package	Top Marking	Free Air Temperature (T_A)
MP62180DS	Active Low	Single	2A	2.8A	SOIC8	62180DS	–40°C to +85°C
MP62180DD					QFN8E (2mm x 3mm)	62180DD	
MP62180DH					MSOP8E	62180DH	
MP62181DH	Active High				MSOP8E	62181DH	

Notes: NRFND for MP62180

* For Tape & Reel, add suffix –Z (e.g. MP62181DH–Z).

For RoHS Compliant Packaging, add suffix –LF (e.g. MP62181DH–LF–L)

PACKAGE REFERENCE



MSOP8E | **QFN8E (2mm x 3mm)** | **SOIC8**

MP62180

***: EN is active high for MP62181**

ABSOLUTE MAXIMUM RATINGS (1)

IN .....-0.3V to +6.0V
EN, FLAG, OUT to GND .....-0.3V to +6.0V
Continuous Power Dissipation (T_A = +25°C) (2)
MSOP8E 2.3W
QFN8E (2mm x 3mm) 2.3W
SOIC8 ..... 1.4W
Junction Temperature .....150°C
Lead Temperature .....260°C
Storage Temperature.....–65°C to +150°C
Operating Temperature.....–40°C to +85°C

Thermal Resistance (3) θ_{JA} θ_{JC}

MSOP8E..... 55 ..... 12... °C/W
QFN8E (2mm x 3mm) ..... 55 ..... 12... °C/W
SOIC8..... 90 ..... 42... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS (4)

V_{IN}=5V, T_A=+25°C, unless otherwise noted.

Parameter	Condition		Min	Typ	Max	Units
IN Voltage Range			2.7		5.5	V
Supply Current	Device Active, I_{OUT}=0			90	120	μA
Shutdown Current	Device Disable, V_{OUT}=float, V_{IN}=5.5V			1		μA
Off Switch Leakage	Device Disable, V_{IN}=5.5V			1		μA
Current Limit			2.1	2.8	3.5	A
Trip Current	Current Ramp (slew rate≤100A/s) on Output			3.1	4	A
Under-voltage Lockout	Rising Edge		1.95		2.65	V
Under-voltage Hysteresis				250		mV
FET On Resistance	I_{OUT}=100mA (-40°C≤ T_A ≤85°C)	MSOP8E		75	120	mΩ
		QFN8E (2mm x 3mm)		75	120	mΩ
		SOIC8		85	130	mΩ
EN Input Logic High Voltage			2			V
EN Input Logic Low Voltage					0.8	V
FLAG Output Logic Low Voltage	I_{SINK}=5mA				0.4	V
FLAG Output High Leakage Current	V_{IN}=V_{FLAG}=5.5V				1	μA
Thermal Shutdown				140		°C
Thermal Shutdown Hysteresis				20		°C
V_{OUT} Rising Time, Tr (5)	V_{IN}=5.5V, C_L=1uF, R_L=5Ω			0.9		ms
	V_{IN}=2.7V, C_L=1uF, R_L=5Ω			1.7		ms
V_{OUT} Falling Time, Tf (6)	V_{IN}=5.5V, C_L=1uF, R_L=5Ω				0.5	ms
	V_{IN}=2.7V, C_L=1uF, R_L=5Ω				0.5	ms
Turn On Time, Ton (7)	C_L=100μF, R_L=5Ω				3	ms
Turn Off Time, Toff (8)	C_L=100μF, R_L=5Ω				10	ms
FLAG Deglitch Time			4	8	15	ms
EN Input Leakage			-1			μA
Reverse Leakage Current	OUT=5.5V, IN=GND			0.2		μA

NOTE:

4) Production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.
5) Measured from 10% to 90%.
6) Measured from 90% to 10%.
7) Measured from (50%) EN signal to (90%) output signal.
8) Measured from (50%) EN signal to (10%) output signal.

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PIN FUNCTIONS

Pin # SOIC8	Pin # MSOP8E	Pin # QFN8E	Name	Description
1	1	1	GND	Ground.
2, 3	2, 3	2, 3	IN	Input Voltage. Accepts 2.7V to 5.5V input.
4	4	4	$\overline{EN}$	Active Low: (MP62180), Active High: (MP62181)
5	5	5	$\overline{FLAG}$	IN-to-OUT Over-current, active-low output flag. Open-Drain.
6, 7, 8	6, 7, 8	6, 7, 8	OUT	IN-to-OUT Power-Distribution Output (for all 3 output pins)

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25ºC, unless otherwise noted.

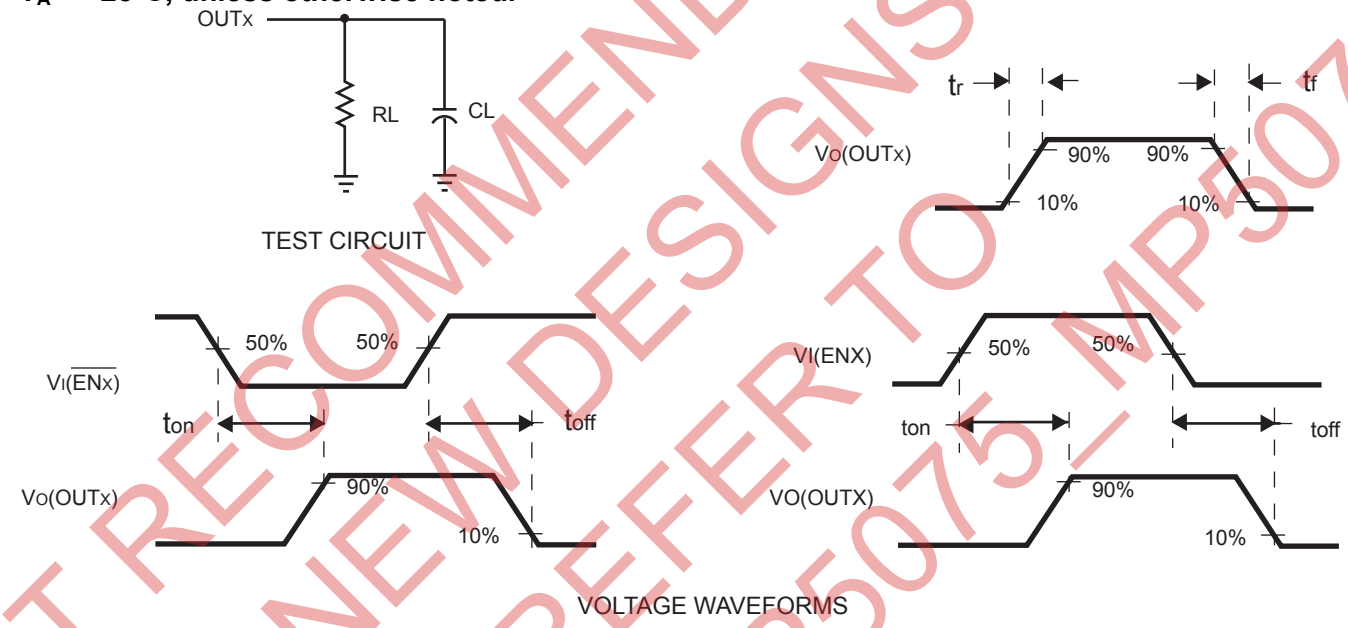

Figure 1—Test Circuit and Voltage Waveforms

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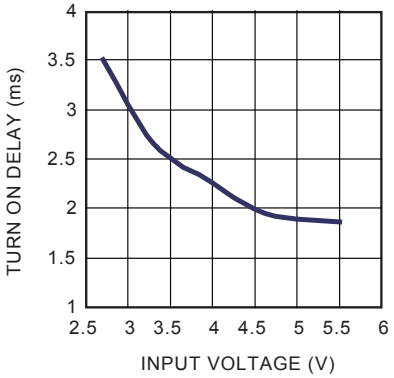
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} =5V, V_{EN}=0V for MP62180 or 5V for MP62181, C_L=2.2µF, T_A = +25ºC, unless otherwise noted.

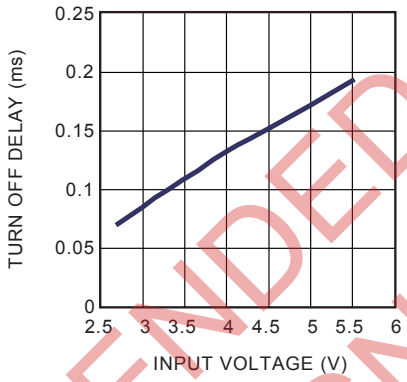
Turn on Delay vs. Input Votage

R_L=2.5Ω

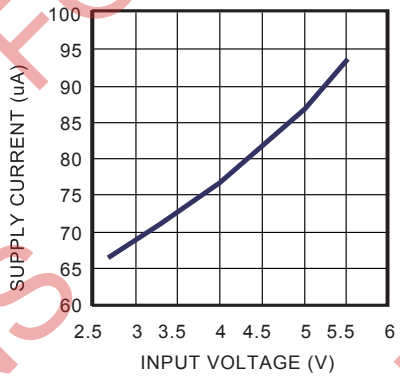


Turn off Delay vs. Input Votage

R_L=2.5Ω

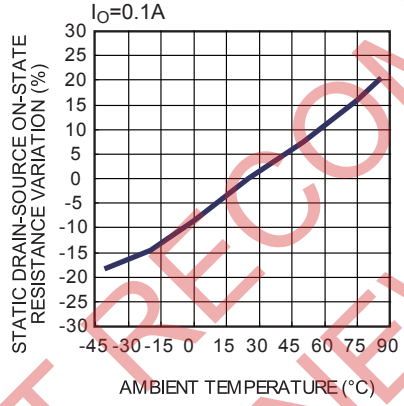


Supply Current, Output Enabled vs. Input Voltage



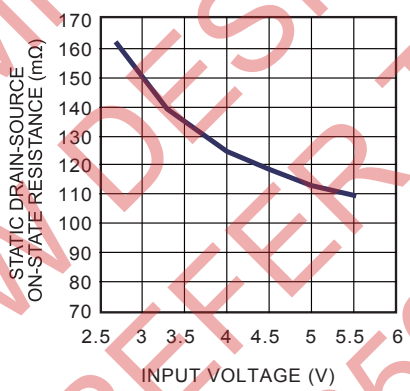
Static Drain-Source On-State Resistance Variation vs. Ambient Temperature

I_O=0.1A

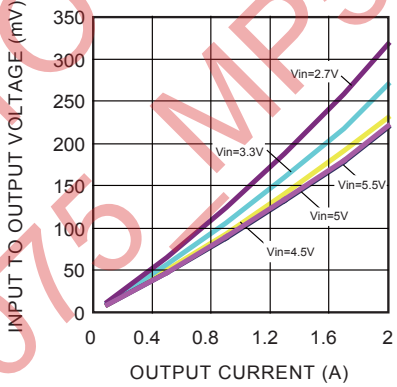


Static Drain-Source On-State Resistance vs. Input Voltage

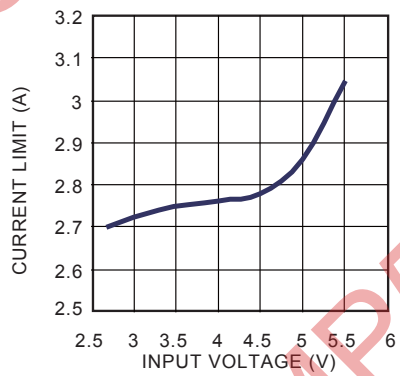
I_O=2A



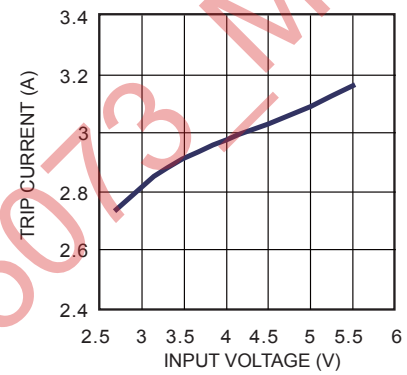
Input to Output Voltage vs. Load Current



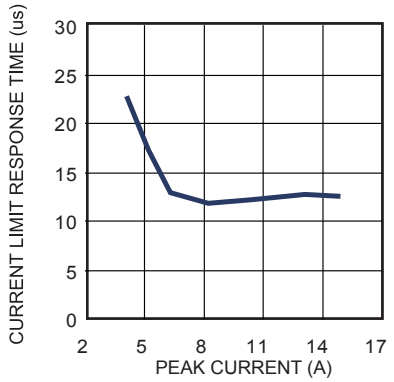
Current Limit vs. Input Voltage



Threshold Trip Current vs. Input Voltage



Current Limit Response Time vs. Peak Current



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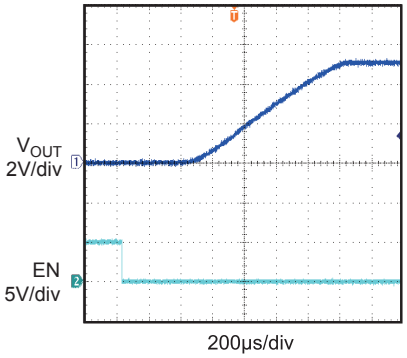
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} =5V, V_{EN}=0V for MP62180 or 5V for MP62181, C_L=2.2μF, T_A = +25°C, unless otherwise noted.

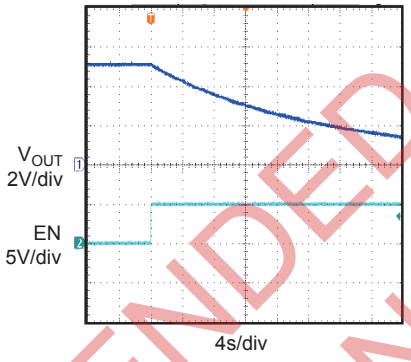
Turn On Delay and Rise Time with 0.22uF Load

C_L=0.22μF



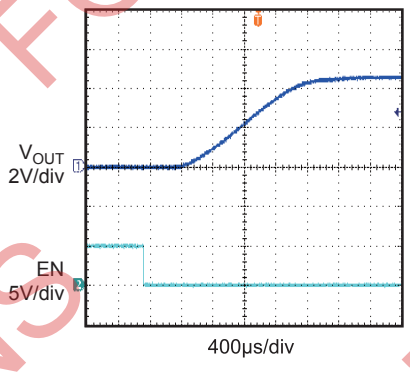
Turn Off Delay and Fall Time with 0.22uF Load

C_L=0.22μF



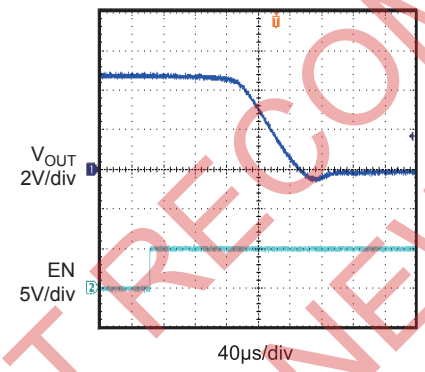
Turn On Delay and Rise Time with 2.2uF Load

R_L=2.5Ω

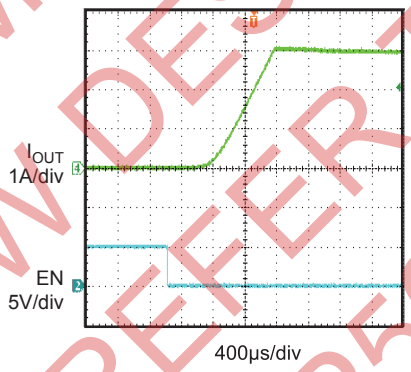


Turn Off Delay and Fall Time with 2.2uF Load

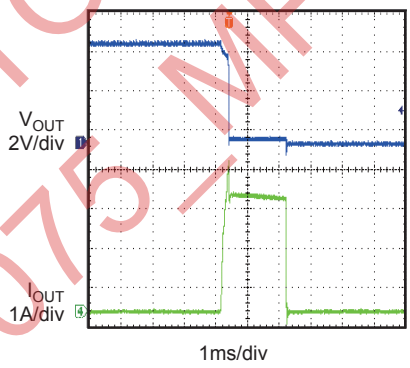
R_L=2.5Ω



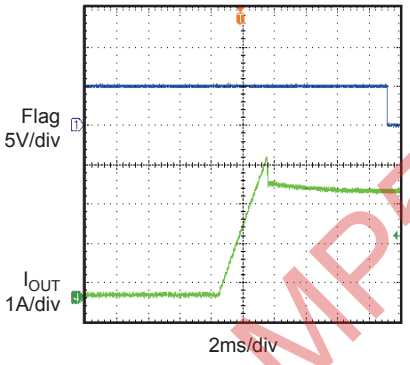
Short Circuit Current, Device Enabled into Short



Threshold Trip Current with Ramped Load on Enabled Device

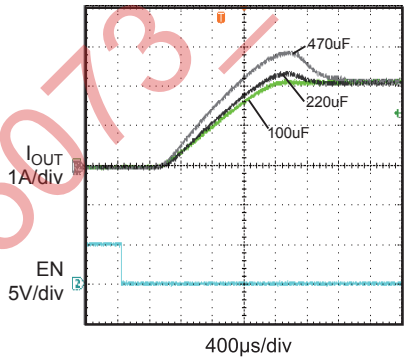


Ramped Load on Enabled Device

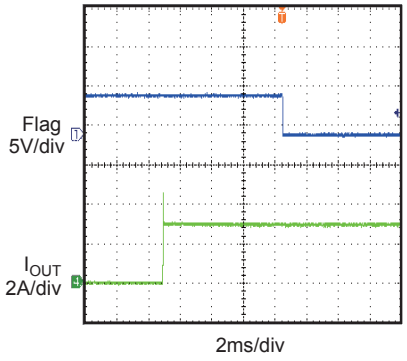


Inrush Current with Different Load Capacitance

R_L=2.5Ω



1Ω Load Connected to Enabled Device



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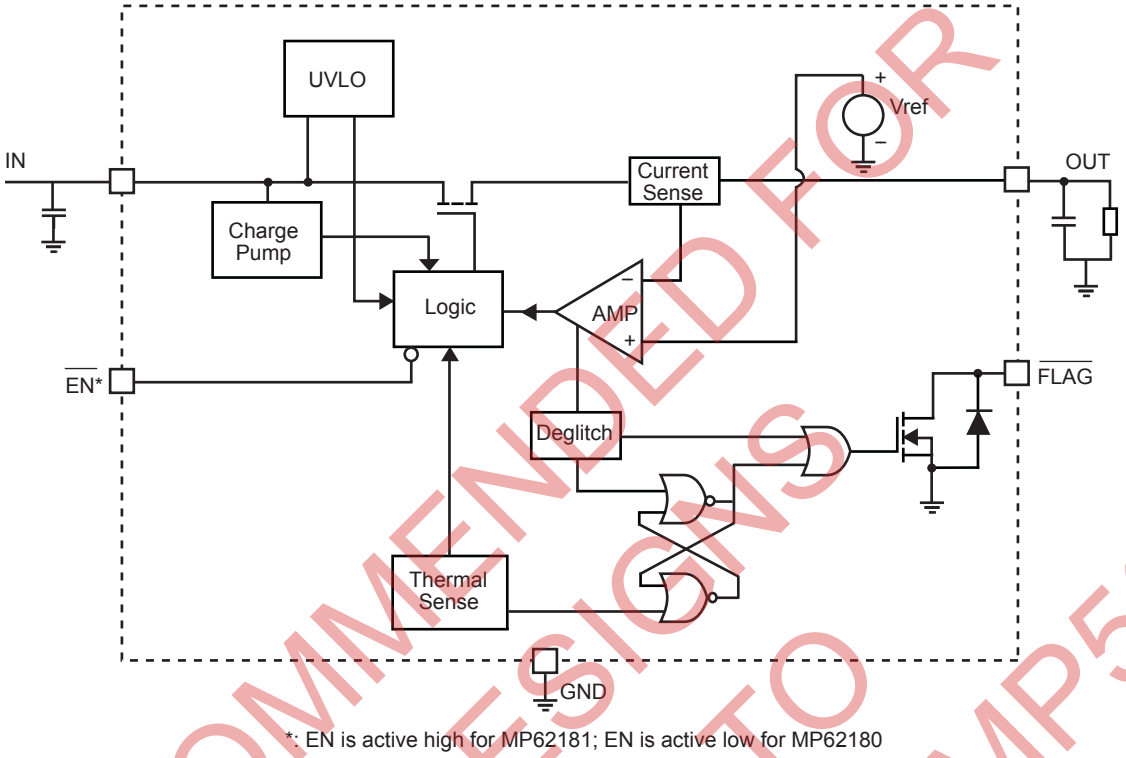
FUNCTION BLOCK DIAGRAM



*: EN is active high for MP62181; EN is active low for MP62180

Figure2—Function Block Diagram

DETAILED DESCRIPTION

Over Current

When the load exceeds trip current (minimum threshold current triggering constant-current mode) or a short is present, MP62180/MP62181 switches into to a constant-current mode (current limit value). MP62180/MP62181 will be shutdown only if the overcurrent condition stays long enough to trigger thermal protection.

Trigger overcurrent protection for different overload conditions occurring in applications:

1) The output has been shorted or overloaded before the device is enabled or input applied. MP62180/MP62181 detects the short or overload and immediately switches into a constant-current mode.
2) A short or an overload occurs after the device is enabled. After the current-limit circuit has been tripped (reached the trip current threshold), the device switches into constant-current mode. However, high current may flow for a short period of time before the current-limit circuit can react.
3) Output current has been gradually increased beyond the recommended operating current. The load current rises until the trip current threshold is reached or until the thermal limit of the device is exceeded. The MP62180/MP62181 is capable of delivering current up to the trip current threshold without damaging the device. Once the trip threshold has been reached, the device switches into its constant-current mode.

Flag Response

The FLAG pin is an open drain configuration. This FAULT will report a fail mode after an 8ms deglitch timeout. This is used to ensure that no false fault signals are reported. This internal deglitch circuit eliminates the need for extend components. The FLAG pin is not deglitched during an over temp. or a voltage lockout.

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Thermal Protection

The purpose of thermal protection is to prevent damage in the IC by allowing exceptive current to flow and heating the junction. The die temperature is internally monitored until the thermal limit is reached. Once this temperature is reached, the switch will turn off and allow the chip to cool. The switch has a built-in hysteresis.

Under-voltage Lockout (UVLO)

This circuit is used to monitor the input voltage to ensure that the MP62180/MP62181 is operating correctly.

This UVLO circuit also ensures that is no operation until the input voltage reaches the minimum spec.

Enable

The logic pin disables the switch to reduce overall supply current .Once the EN pin reaches logic enable threshold, the MP62180/MP62181 is enabled.

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APPLICATION INFORMATION

Power-Supply Considerations

Over 10μF capacitor between IN and GND is recommended. This precaution reduces power-supply transients that may cause ringing on the input and improves the immunity of the device to short-circuit transients.

In order to achieve smaller output load transient ripple, placing a high-value electrolytic capacitor on the output pin(s) is recommended when the load is heavy.

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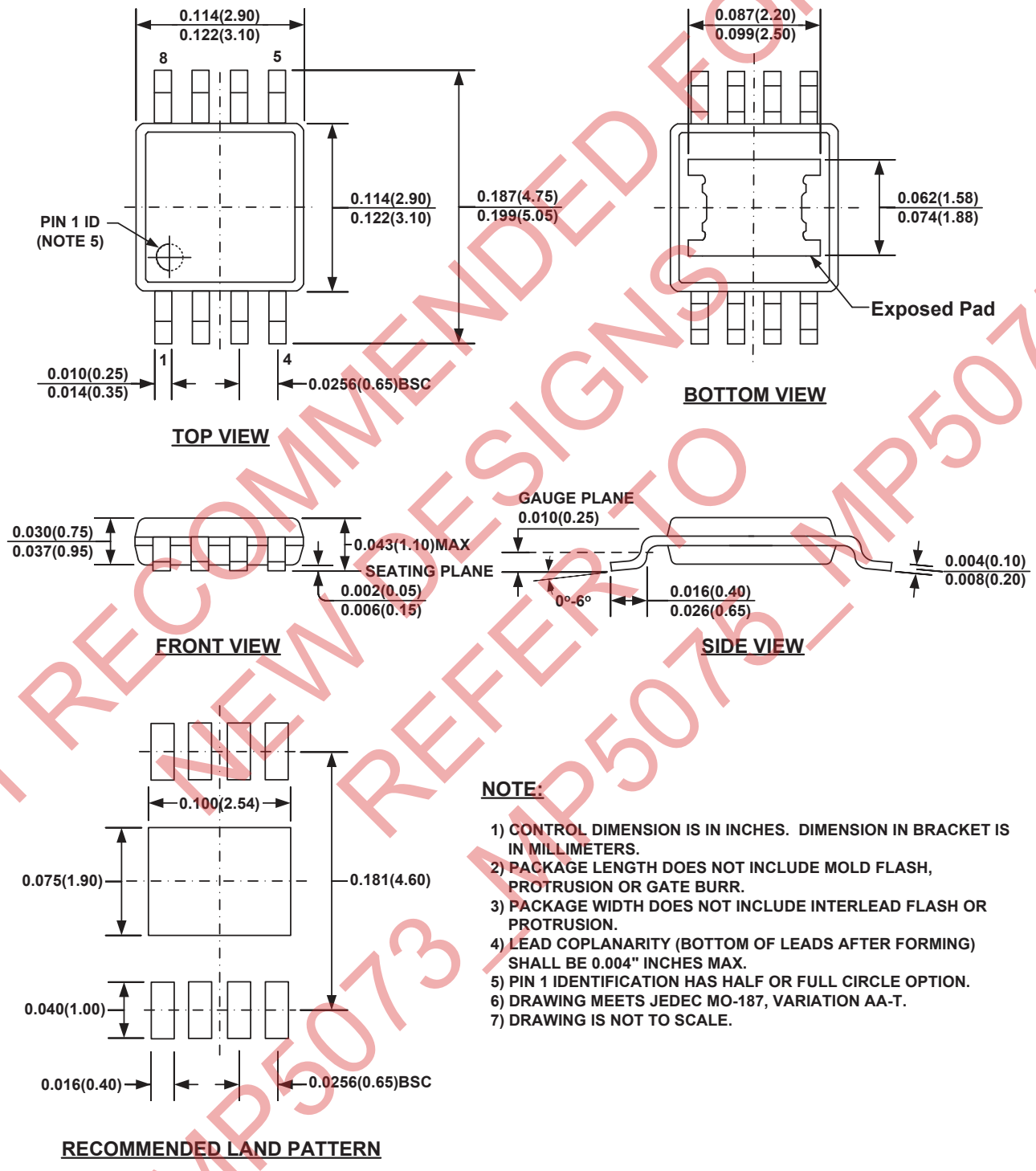
PACKAGE INFORMATION

MSOP8E (EXPOSED PAD)



NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) PIN 1 IDENTIFICATION HAS HALF OR FULL CIRCLE OPTION.
6) DRAWING MEETS JEDEC MO-187, VARIATION AA-T.
7) DRAWING IS NOT TO SCALE.

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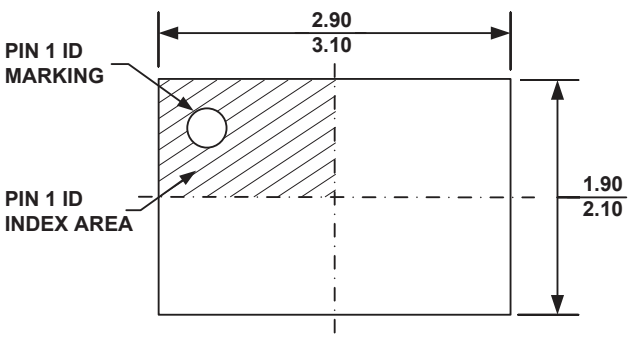
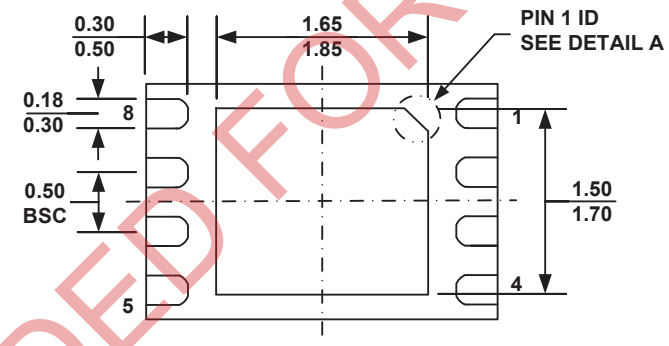
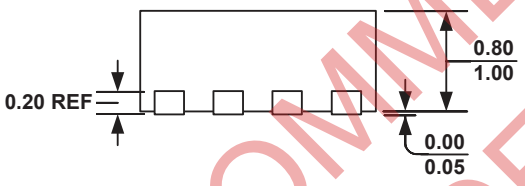
QFN8E (2mm x 3mm)



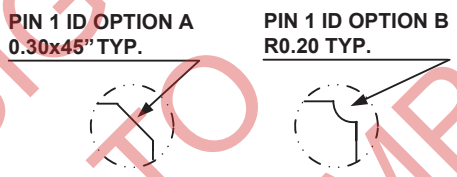
TOP VIEW



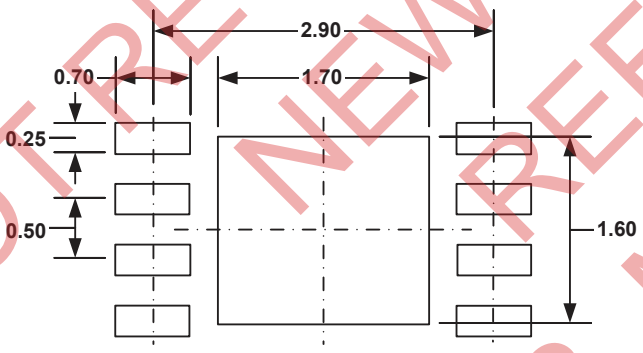
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VCED-2.
5) DRAWING IS NOT TO SCALE.

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP5073_MP5075 _MP5075L

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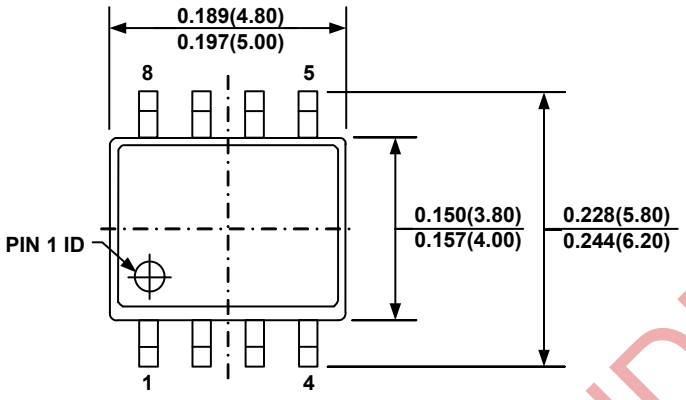
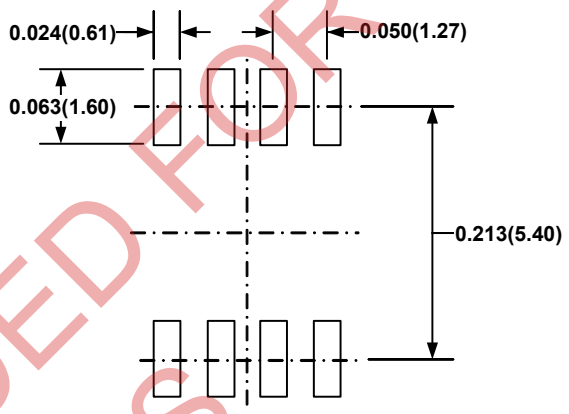
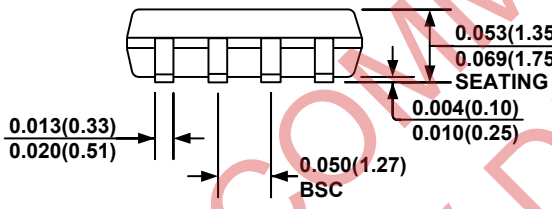
SOIC8



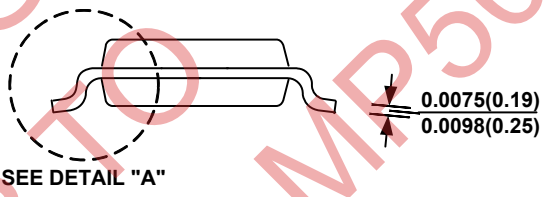
TOP VIEW



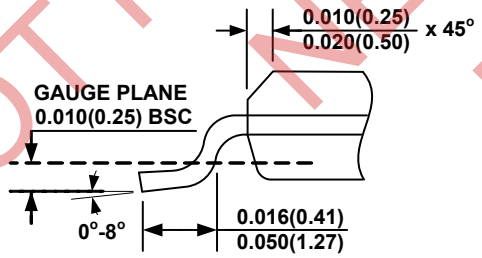
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP5073_MP5075L

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