MP5611

2.9V to 5.2V Input, Triple-Output, AMOLED Display Power Supply

DESCRIPTION

The MP5611 is a triple-output converter across a 2.9 to 5.2V input voltage (V_{IN}) range designed for small-size AMOLED (active matrix organic light-emitting diode) display power supplies.

The MP5611 integrates a boost converter for ELVDD, an inverting buck-boost (IBB) converter for ELVSS, and another boost converter for AVDD. The one wire digital control pin (CTRL) can program the ELVSS, ELVDD, and AVDD voltages following digital protocol.

The MP5611 supports an independent start-up sequence for AVDD and ELVDD via the separated enable pins (EN_AVDD and CTRL). It also integrates an optional fast discharge function after the IC has been disabled.

The device features rich protections, including V_{IN} under-voltage lockout (UVLO), cycle-by-cycle current limit protection, thermal shutdown protection, short output protection, and over-current protection (OCP) for AVDD and ELVDD.

The fully integrated synchronous rectification solution with low on resistance improves total system efficiency, minimizes external components, and reduces PCB layout size.

The MP5611 is available in a TQFN-16 (3mmx3mm) package.

FEATURES

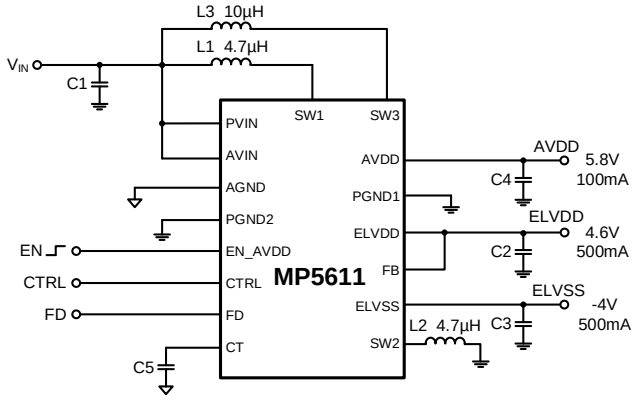
- 2.9 to 5.2V Input Voltage (V_{IN}) Range
- Triple Output AVDD, ELVDD, ELVSS
- High Accuracy for Output Voltage (V_{OUT})
- Good Line and Load Regulation
- Configurable V_{ELVDD} = 4.6V to 5.2V, Default 4.6V
- Configurable V_{ELVSS} = -1.4V to -6.4V, Default -4V
- 500mA Output Current (I_{OUT}) for ELVDD and ELVSS
- Configurable V_{AVDD} = 5V to 7.7V, Default 5.8V
- 100mA I_{OUT} for AVDD
- Respective Enable for AVDD and ELVDD
- Soft Start (SS)
- Active Fast Discharge Function
- Cycle-by-Cycle Current Limit Protection
- AVDD Output Over-Current Protection (OCP) 90mA to 270mA
- ELVDD Output OCP 80mA to 650mA
- Output Short-to-GND Protection
- Over-Temperature Protection (OTP)
- Available in a TQFN-16 (3mmx3mm) Package

APPLICATIONS

- AMOLED Smartphones
- AMOLED Displays

All MPS parts are lead-free, halogen free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. “MPS,” the MPS logo, and “Simple, Easy Solutions” are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

TYPICAL APPLICATION



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP5611GQT	TQFN-16 (3mmx3mm)	*See Below*	1

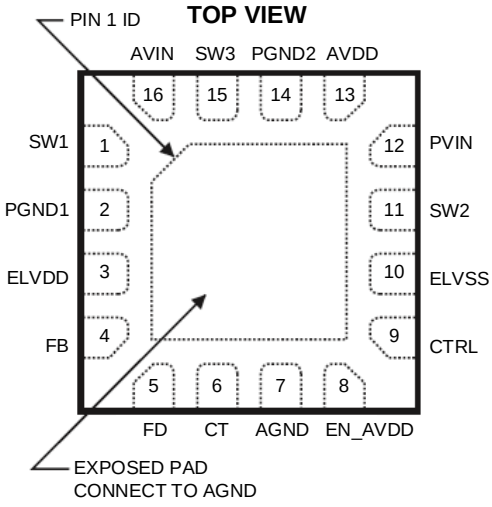
* For Tape & Reel, add suffix -Z (e.g. MP5611GQT-Z).

TOP MARKING

BKHY
LLL

BKH: Product code
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



TQFN-16 (3mmx3mm)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Description
1	SW1	**Switching node of the ELVDD boost converter.**
2	PGND1	**Power ground of the ELVDD boost converter.**
3	ELVDD	**Output of the ELVDD boost converter.**
4	FB	**Feedback.** ELVDD output voltage (V_{OUT}) sense pin.
5	FD	**Fast discharge enable and disable during shutdown.** Pull this pin high to enable fast discharge.
6	CT	**ELVSS transition time configured pin.**
7	AGND	**Analog ground.**
8	EN_AVDD	**AVDD boost converter enable pin.** Pull this pin high to enable the AVDD converter.
9	CTRL	**Digital control.** This pin also enables the ELVDD and ELVSS converter.
10	ELVSS	**Output of the ELVSS inverting buck-boost (IBB) converter.**
11	SW2	**Switching node of the ELVSS IBB converter.**
12	PVIN	**Power supply of the ELVSS IBB converter.**
13	AVDD	**Output of the AVDD boost converter.**
14	PGND2	**Power ground of the AVDD boost converter.**
15	SW3	**Switching node of the AVDD boost converter.**
16	AVIN	**Power supply for internal circuit.**
Exposed pad		**Exposed pad.** Connect this pin to AGND.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN}, SW1 ..... -0.3V to +5.3V
SW3, AVDD ..... -0.3V to +10V
ELVSS ..... -7.5V to +0.3V
SW2 ..... -7.5V to +5.3V
All other pins ..... -0.3V to +5.3V
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C
Continuous power dissipation (T_A = 25°C) (2)
TQFN-16 (3mmx3mm) 2.1W

ESD Ratings

Human body model (HBM) ..... ±1.5kV
Charged device model (CDM) ..... ±2kV

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 2.9V to 5.2V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TQFN-16 (3mmx3mm)……..…60……12...°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) – T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can generate an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.7V, $V_{ELVDD/ELVSS/AVDD}$ = default, T_A = -40°C to +85°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
General						
Operating input voltage	V_{IN}		2.9		5.2	V
Shutdown current	I_{SD}	EN_AVDD = CTRL = 0V		0.1		μA
Quiescent supply current	I_Q	V_{IN} = 3.7V, ELVDD switching		1.6	3	mA
Input under-voltage lockout (UVLO) threshold	V_{IN_UVLO}	Rising edge			2.65	V
Input UVLO hysteresis				300		mV
EN_AVDD/FD high voltage	V_{EN_HIGH}	Rising V_{EN}	1.35			V
EN_AVDD/FD low voltage	V_{EN_LOW}	Falling V_{EN}			0.4	V
EN_AVDD pull-down resister	R_{DOWN}			500		kΩ
Over-temperature protection (OTP) threshold (5)	T_{SD}			150		°C
Thermal protection hysteresis (5)				25		°C
Boost Converter ELVDD						
ELVDD voltage	V_{ELVDD}			4.6		V
ELVDD voltage variation		T_A = 25°C, no load	-0.5		+0.5	%
		-40°C to +85°C, no load	-0.8		+0.8	%
Low-side MOSFET (LS-FET) on resistance	$R_{ON_LS_ELVDD}$	I_{SW1} = 200mA		160		mΩ
High-side MOSFET (HS-FET) on resistance	$R_{ON_HS_ELVDD}$	I_{SW1} = 200mA		320		mΩ
Switching frequency	f_{SW1}			1.35		MHz
Current limit	I_{LIMIT1}			1.5		A
Output over-current protection (OCP) threshold	I_{OCP_ELVDD}	I_{OCP_ELVDD} = 650mA		650		mA
Short protection threshold		During operation		80		%
Short protection detection time		During operation		1		ms
ELVDD sense threshold	V_{TELVDD}	Increasing ELVDD-FB		350		mV
Feedback (FB) sense threshold	V_{TFB}	Decreasing ELVDD-FB		250		mV
ELVDD/FB leakage current	$I_{LEAKAGE}$	CTRL = FD = 0V			5	μA
FB pull-down resister	R_{DOWN_FB}			4		MΩ
Active discharge resistance	R_{DS_ELVDD}	CTRL = 0V, I_{ELVDD} = 1mA		75		Ω
Load regulation (5)		1mA < I_{ELVDD} < 300mA		0.2		%/A
Line regulation (5)		2.9V < V_{IN} < 4.3V, I_{ELVDD} = 200mA		0.015		%/V
		2.9V < V_{IN} < 5.2V, I_{ELVDD} = 200mA		1.5 (6)		

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.7V, $V_{ELVDD/ELVSS/AVDD}$ = default, T_A = -40°C to +85°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Buck-Boost Converter ELVSS						
ELVSS default output voltage (V_{OUT})	V_{ELVSS}			-4		V
ELVSS V_{OUT} range			-6.4		-1.4	V
ELVSS regulation		T_A = 25°C, no load	-30		+30	mV
		-40°C to +85°C, no load	-50		+50	mV
LS-FET on resistance	$R_{ON_LS_ELVSS}$	I_{SW2} = 200mA		200		mΩ
HS-FET on resistance	$R_{ON_HS_ELVSS}$	I_{SW2} = 200mA		350		mΩ
Switching frequency	f_{SW2}			1.7		MHz
Current limit	I_{LIMIT2}		2	3		A
Short protection threshold at start-up	V_{ELVSS_SCP}	At start-up		250		mV
Short protection threshold during operation		Voltage drop from normal ELVSS		600		mV
Short protection detection time	t_{SCP2}	At start-up		12.5		ms
		During operation		1		ms
ELVSS leakage current	$I_{LEAKAGE}$	CTRL = FD = 0V		0.01	5	μA
ELVSS discharge resistance	R_{DC_ELVSS}	CTRL = 0V, I_{ELVSS} = 1mA		150		Ω
CT output impedance	R_{CT}		130	300	490	kΩ
CT comparator				50		mV
Load regulation (5)		1mA < I_{ELVSS} < 300mA		1.5		%/A
Line regulation (5)		2.9V < V_{IN} < 5.2V, I_{ELVSS} = 200mA		0.45		%/V
		2.9V < V_{IN} < 5.2V, I_{ELVSS} = 200mA with an external rectifier diode		0.08 (7)		
Boost Converter AVDD						
AVDD default voltage	V_{AVDD}			5.8		V
AVDD voltage range			5		7.7	V
AVDD regulation		-40°C to +85°C, no load	-1		+1	%
LS-FET on resistance	$R_{ON_LS_AVDD}$	I_{SW3} = 200mA		500		mΩ
HS-FET on resistance	$R_{ON_HS_AVDD}$	I_{SW3} = 200mA		1400		mΩ
Switching frequency	f_{SW3}			1.35		MHz
Current limit	I_{LIMIT3}			0.5		A
Output OCP threshold	I_{OCP_AVDD}	I_{OCP_AVDD} = 210mA		210		mA
Short protection threshold		During operation		90		%
Short protection detection time		During operation		1		ms
AVDD leakage current	$I_{LEAKAGE}$	CTRL = FD = 0V		2.8	5.6	μA
Active discharge resistance	R_{DS_AVDD}	CTRL = 0V, I_{AVDD} = 1mA		30		Ω
Load regulation (5)		1mA < I_{AVDD} < 100mA		0.08		%/A
Line regulation (5)		2.9V < V_{IN} < 5.2V, I_{AVDD} = 50mA		0.015		%/V

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.7V, $V_{ELVDD/ELVSS/AVDD}$ = default, T_A = -40°C to +85°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
CTRL Interface						
Logic high voltage	V_H		1.35			V
Logic low voltage	V_L				0.4	V
Pull-down resistor	R			500		kΩ
Initialization time	t_{INIT}			340	470	µs
Shutdown period (5)	t_{OFF}		30		80	µs
Pulse high-level period (5)	t_{HIGH}		2	10	25	µs
Pulse low-level period (5)	t_{LOW}		2	10	25	µs
Data storage and acceptance period (5)	t_{STORE}		30		80	µs

Notes:

5) Guaranteed by characterization. Not tested in production.
6) When V_{IN} is between 4.3V and 4.5V, ELVDD line regulation increases since V_{IN} is close to ELVDD's V_{OUT}.
7) To improve ELVSS line regulation in heavy load when V_{IN} < 3.5V, use an external Schottky diode as a rectifier between ELVSS and SW2.

TIMING DIAGRAM

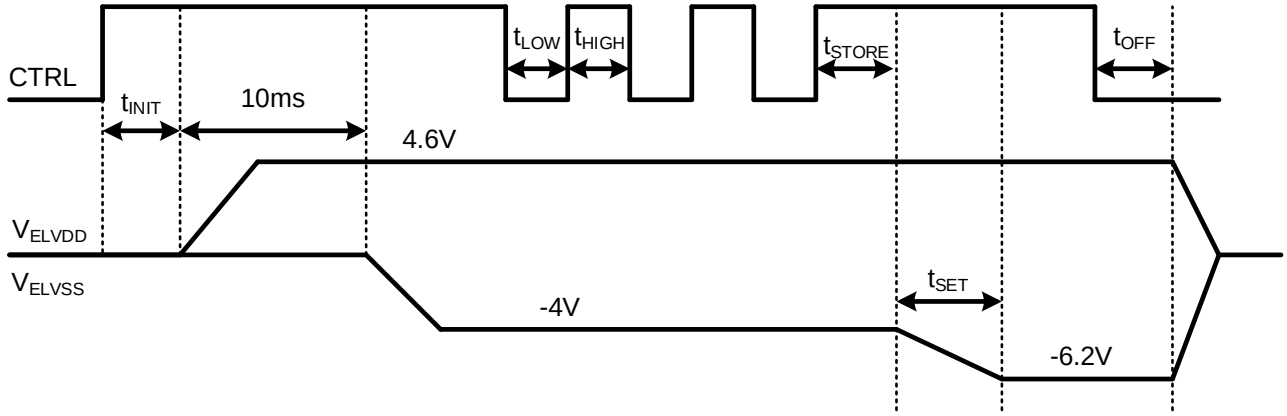


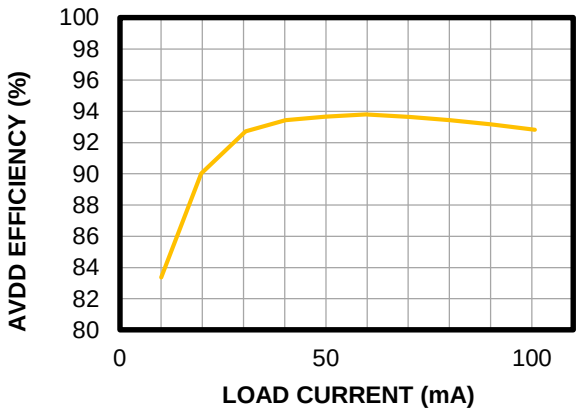
Figure 1: Digital Interface (CTRL) Timing Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

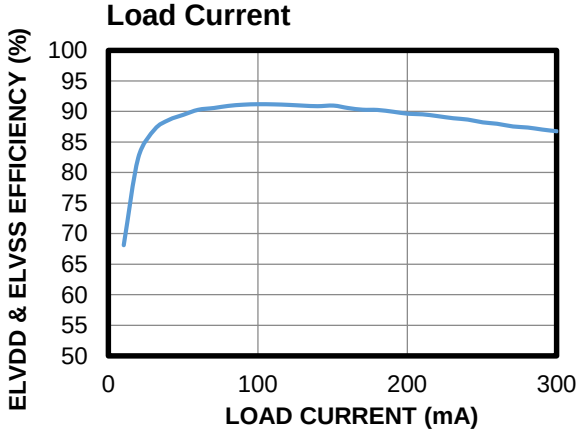
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.7V, $V_{ELVDD/ELVSS/AVDD}$ = default, L1 = L2 = 4.7µH, L3 = 10µH, T_A = 25°C, unless otherwise noted.

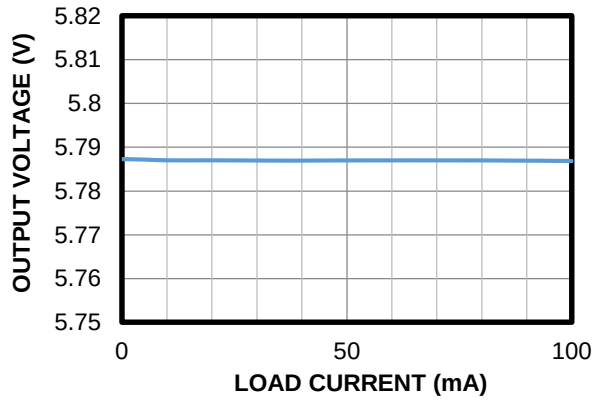
AVDD Efficiency vs. Load Current



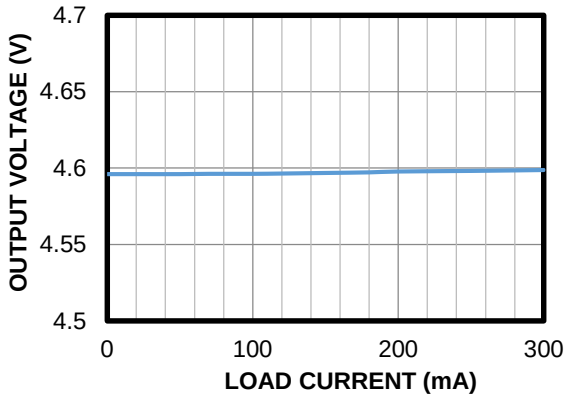
ELVDD & ELVSS Efficiency vs. Load Current



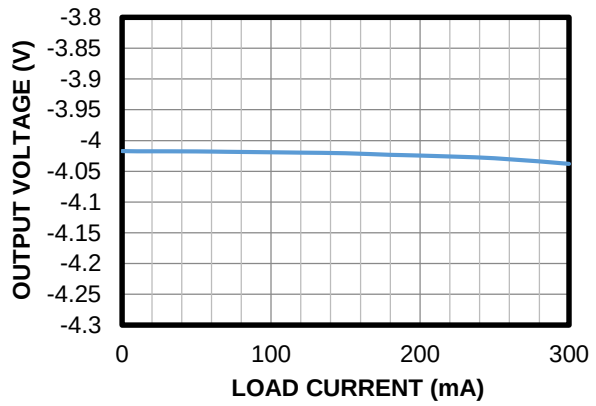
AVDD Load Regulation



ELVDD Load Regulation

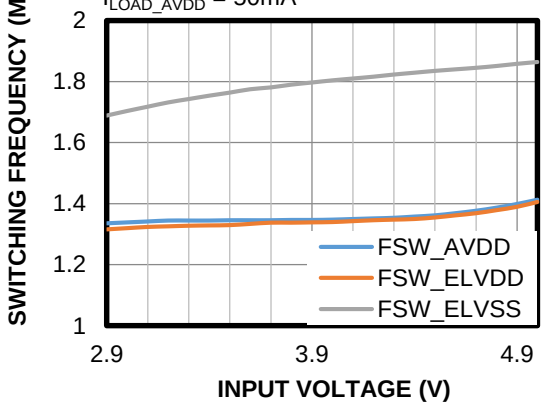


ELVSS Load Regulation



Switching Frequency vs. V_{IN}

I_{LOAD_ELVDD} = 100mA,
I_{LOAD_ELVSS} = 100mA,
I_{LOAD_AVDD} = 50mA



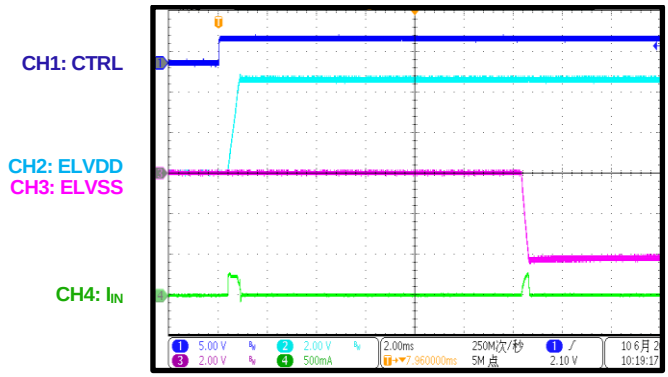
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.7V, $V_{ELVDD/ELVSS/AVDD}$ = default, L1 = L2 = 4.7µH, L3 = 10µH, T_A = 25°C, unless otherwise noted.

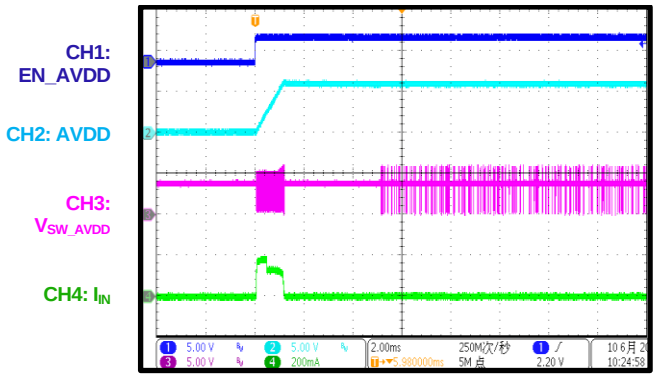
EVLDD and ELVSS Start-Up

I_{LOAD} = 0mA



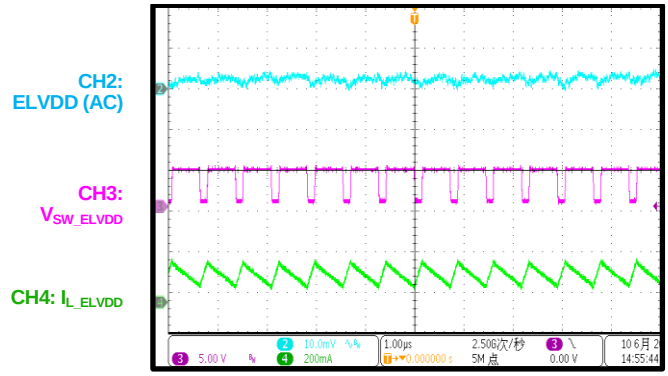
AVDD Start-Up

I_{LOAD} = 0mA



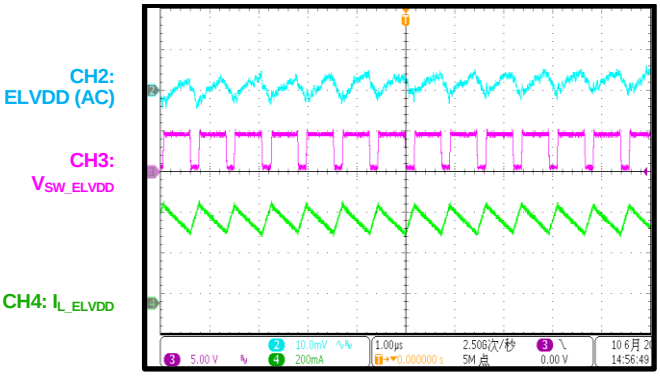
ELVDD Steady State

I_{LOAD} = 100mA



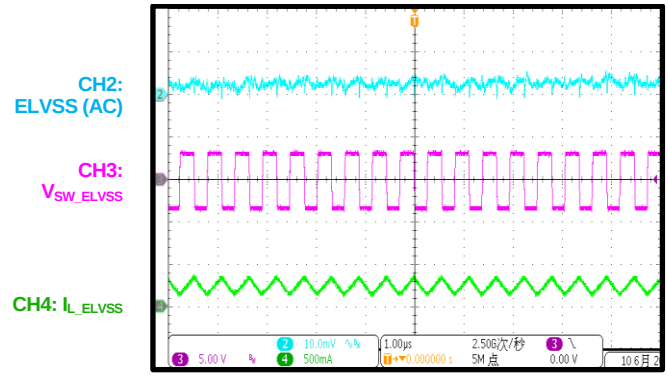
ELVDD Steady State

I_{LOAD} = 300mA



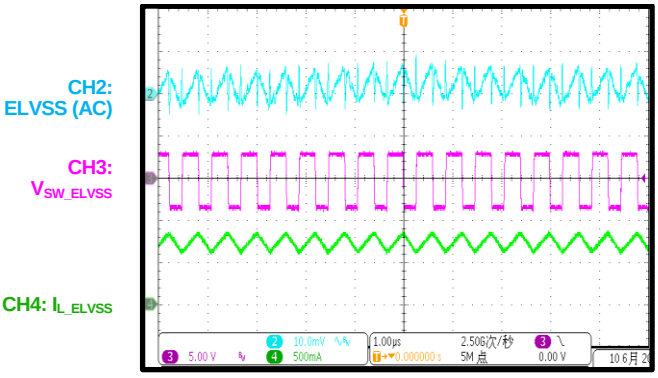
ELVSS Steady State

I_{LOAD} = 100mA



ELVSS Steady State

I_{LOAD} = 300mA



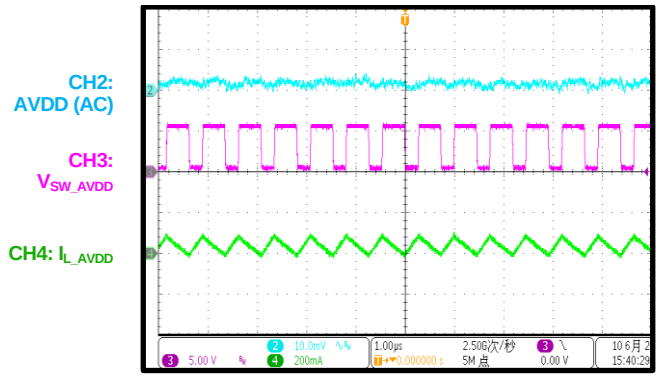
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.7V, $V_{ELVDD/ELVSS/AVDD}$ = default, L1 = L2 = 4.7µH, L3 = 10µH, T_A = 25°C, unless otherwise noted.

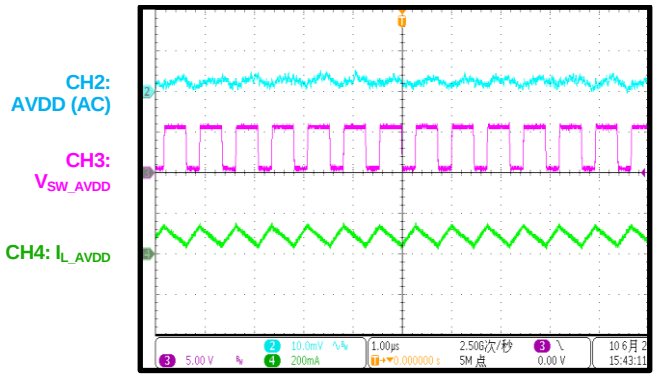
AVDD Steady State

I_{LOAD} = 20mA



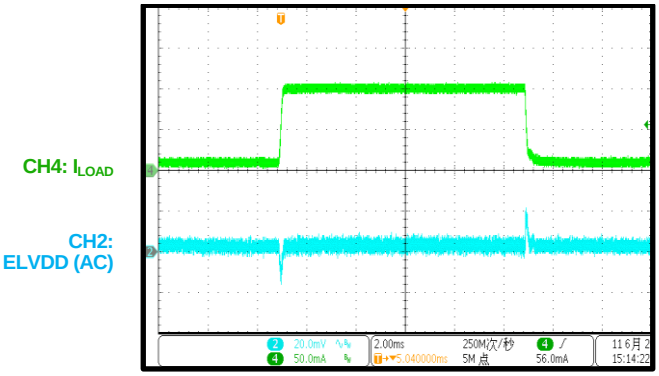
AVDD Steady State

I_{LOAD} = 50mA



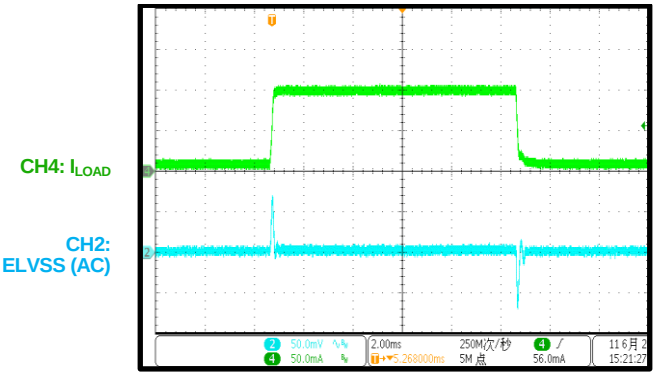
ELVDD Load Transient Response

I_{LOAD} = 10mA to 100mA in 180µs



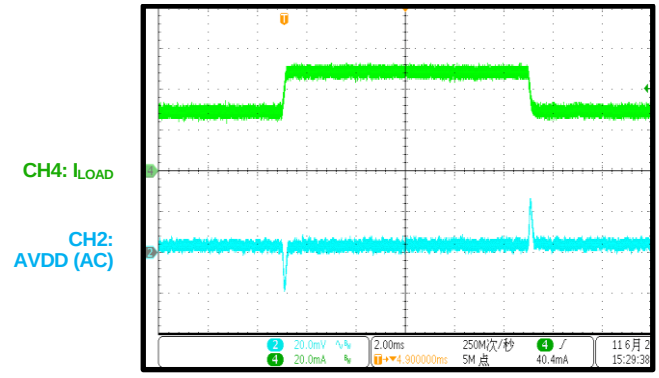
ELVSS Load Transient Response

I_{LOAD} = 10mA to 100mA in 180µs

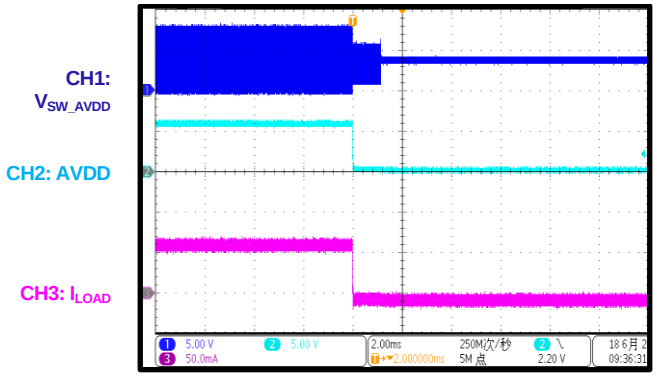


AVDD Load Transient Response

I_{LOAD} = 30mA to 50mA in 180µs



AVDD Short to GND Protection during Normal Operation

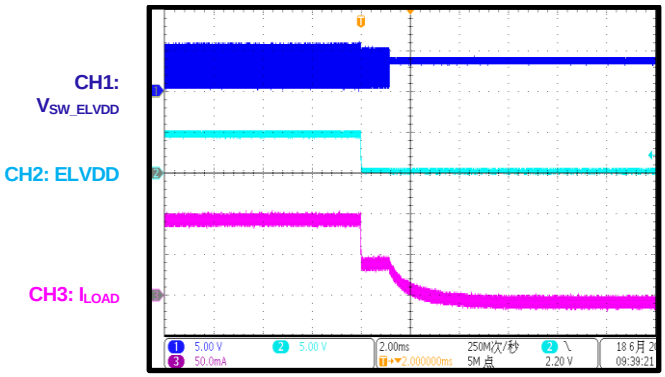


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

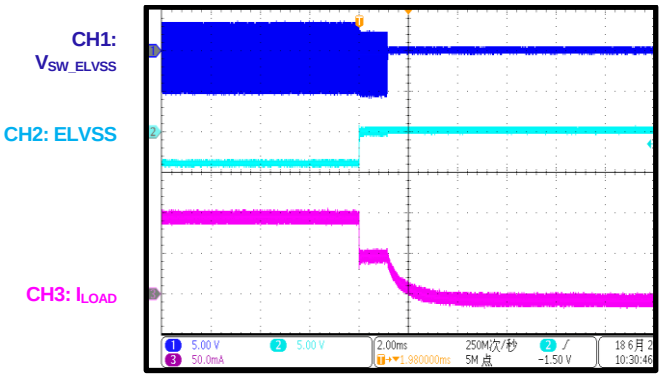
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.7V, $V_{ELVDD/ELVSS/AVDD}$ = default, L1 = L2 = 4.7µH, L3 = 10µH, T_A = 25°C, unless otherwise noted.

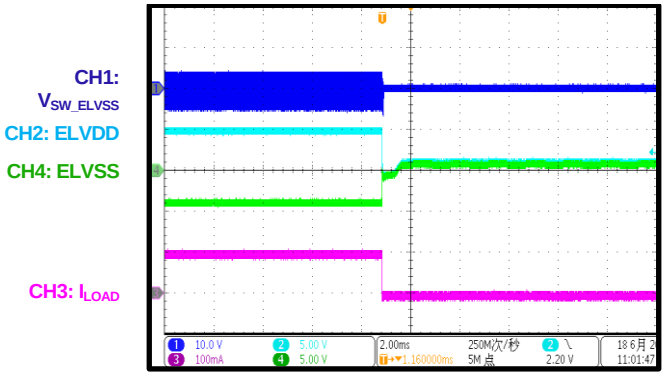
ELVDD Short to GND Protection during Normal Operation



ELVSS Short to GND Protection during Normal Operation



ELVDD Short to ELVSS Protection during Normal Operation



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

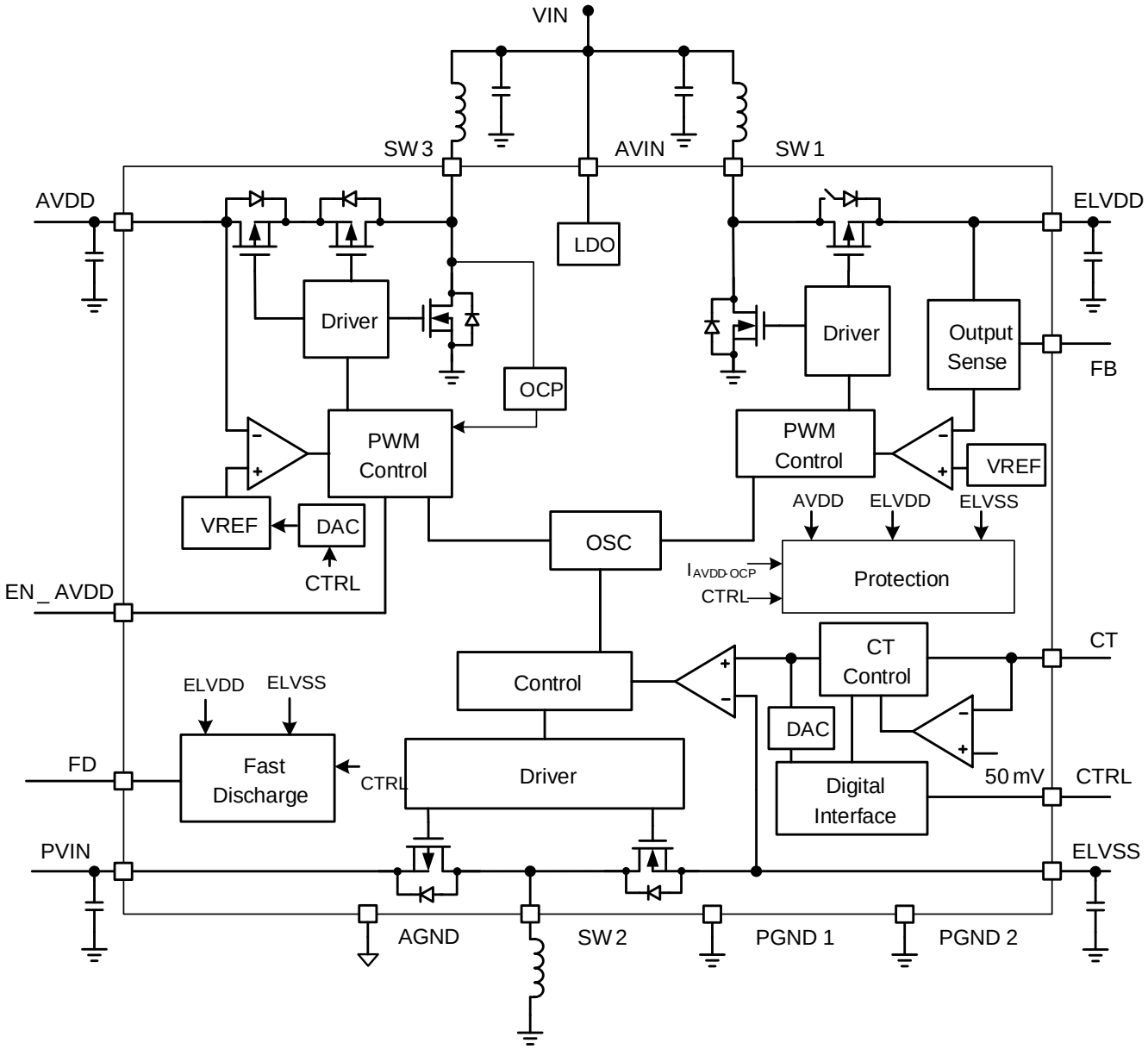


Figure 2: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

OPERATION

The MP5611 is a triple-output converter designed for small-size AMOLED (active matrix organic light-emitting diode) display power supplies. It integrates a boost converter for ELVDD, an inverting buck-boost (IBB) converter for ELVSS, and another boost converter for AVDD. The one wire digital control pin (CTRL) can program the ELVSS, ELVDD, and AVDD voltages following digital protocol.

Feedback (FB) Connection for ELVDD

If the FB pin is floating or tied to GND, or (V_{ELVDD} - V_{FB}) > 350mV, then the ELVDD boost converter's output voltage (V_{OUT}) is sensed via the ELVDD pin directly. To improve the ELVDD V_{OUT} sense performance, externally connect FB to the main ELVDD output capacitor's positive terminal. In this case, when (V_{ELVDD} - V_{FB}) < 250mV, V_{OUT} is sensed via FB pin with better sense accuracy.

Fast Discharge Function

Pull the FD pin high to enable the active fast discharge function when the MP5611 shuts down. By connecting FD to GND, all outputs are high-impedance when the IC shuts down. When FD is pulled high, the fast discharge function can also be disabled by applying 81 pulses to the CTRL pin.

Figure 3 shows the start-up/shutdown sequence, where the solid line is with active discharge enabled and the dotted line is without active discharge enabled.

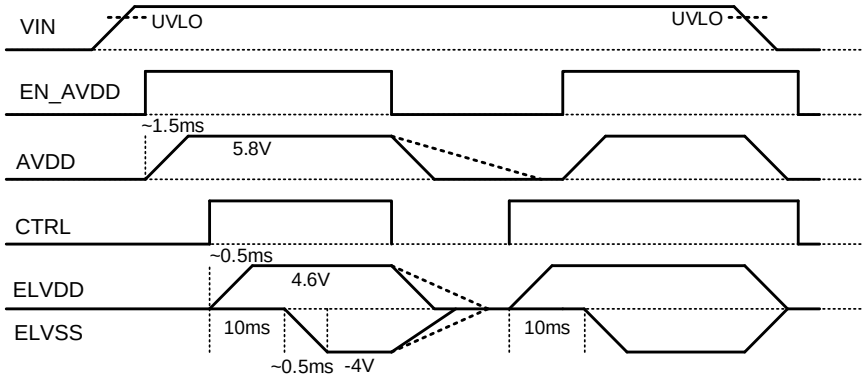


Figure 3: Start-Up/Shutdown Sequence with and without Active Discharge Enable

Configuring the ELVSS Transition Time

When ELVSS is controlled by the CTRL pulse, the voltage transition time can be configured by the capacitor on the CT pin ($C_{EXTERNAL}$), which can be estimated using Equation (1):

$$t\ (\mu s) = 3 \times R_{INTERNAL}\ (k\Omega) \times C_{EXTERNAL}\ (nF) \quad (1)$$

Where $R_{INTERNAL}$ = 300kΩ. $C_{EXTERNAL}$ e.g. 100nF is about 90ms of the transition time.

Digital Interface (CTRL)

The CTRL pin has two functions:

1. CTRL is the digital interface that configures the output of ELVSS, ELVDD, and AVDD, as well as the output over-current (OC) limit. The number of pulse signal's rising edges applied on the CTRL pin is counted for configuring the corresponding item to a certain value (see Table 1 on page 13).
2. CTRL is also ELVDD and ELVSS's enable signal. Once CTRL pulls high, ELVDD starts up to the default value. After 10ms, ELVSS establishes to its default value (see the Timing Diagram section on page 6).

The reset information for ELVSS, ELVDD, and AVDD follows:

- A power cycle resets all settings to default.
- CTRL is low, and lasts for a set time to reset ELVDD and ELVSS to the default value.
- EN_AVDD can enable/disable AVDD.
- EN_AVDD and CTRL are both pulled low to reset AVDD and all registers to the default value.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

Table 1: CTRL Configuration Table

Pulse #	ELVSS
1	-6.4V
2	-6.3V
3	-6.2V
4	-6.1V
5	-6V
6	-5.9V
7	-5.8V
8	-5.7V
9	-5.6V
10	-5.5V
11	-5.4V
12	-5.3V
13	-5.2V
14	-5.1V
15	-5V
16	-4.9V
17	-4.8V
18	-4.7V
19	-4.6V
20	-4.5V
21	-4.4V
22	-4.3V
23	-4.2V
24	-4.1V
25	-4V
26	-3.9V
27	-3.8V
28	-3.7V
29	-3.6V
30	-3.5V
31	-3.4V
32	-3.3V
33	-3.2V
34	-3.1V
35	-3V
36	-2.9V
37	-2.8V
38	-2.7V
39	-2.6V
40	-2.5V
41	-2.4V
42	-2.3V
43	-2.2V
44	-2.1V
45	-2V
46	-1.9V
47	-1.8V
48	-1.7V
49	-1.6V
50	-1.5V
51	-1.4V

Pulse #	AVDD
52	+5V
53	+5.1V
54	+5.2V
55	+5.3V
56	+5.4V
57	+5.5V
58	+5.6V
59	+5.7V
60	+5.8V
61	+5.9V
62	+6V
63	+6.1V
64	+6.2V
65	+6.3V
66	+6.4V
67	+6.5V
68	+6.6V
69	+6.7V
70	+6.8V
71	+6.9V
72	+7V
73	+7.1V
74	+7.2V
75	+7.3V
76	+7.4V
77	+7.5V
78	+7.6V
79	+7.7V
Pulse #	**V_{OUT} Fast Discharge**
0	Controlled by FD
80	On
81	Off
Pulse #	**250mV Detection**
0	Off
82	On
83	Off
Pulse #	**ELVDD**
0	4.6V
84	4.6V
85	4.7V
86	4.8V
87	4.9V
88	5V
89	5.1V
90	5.2V
Pulse #	**OCP (ELVDD)**
0	650mA
91	80mA
92	175mA
93	270mA
94	365mA

Pulse #	OCP (ELVDD)
95	460mA
96	555mA
97	650mA
Pulse #	**OCP (AVDD)**
0	210mA
98	90mA
99	120mA
100	150mA
101	180mA
102	210mA
103	240mA
104	270mA

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

Diode Mode when V_{IN} ≈ ELVDD

When the input voltage (V_{IN}) is close to ELVDD, the MP5611 operates in diode mode. In this mode, the ELVDD boost converter's high-side MOSFET (HS-FET) is disabled, and its body diode operates as a rectifier to regulate V_{OUT}. Note that the converter must work in continuous conduction mode (CCM) to achieve proper output regulation in diode mode.

ELVDD Over-Current Protection (OCP)

The MP5611 supports ELVDD over-current protection (OCP). If EVDD's output current (I_{OUT}) exceeds 650mA (default) or the threshold configured via the CTRL signal, and lasts for 1ms, then OCP is triggered and the IC shuts down until CTRL or the power resets.

AVDD OCP

The MP5611 supports AVDD OCP. When AVDD's I_{OUT} exceeds 210mA (default) or the threshold configured via the CTRL signal, and lasts for 1ms, then OCP is triggered and the IC shuts down until EN_AVDD or the power resets.

Short Output Voltage (V_{OUT}) Protection

The MP5611 features complete short protection functions, including AVDD, ELVDD, ELVSS short to GND protection, as well as ELVDD short to LEVSS protection.

The conditions required for the short protection functions follow:

1. If ELVDD does not reach its regulated voltage within 10ms after ELVDD is enabled (CTRL = high), all output voltages shut down (for ELVDD short to GND protection at start-up).
2. If ELVSS does not reach its regulated voltage within 12.5ms after ELVSS is enabled (22.5ms after CTRL = high), all output voltages shut down (for ELVSS short to GND protection at start-up).
3. If ELVSS > 250mV when ELVSS is enabled (10ms after CTRL = high), ELVDD and ELVSS shut down, and AVDD operates normally (for ELVDD short to ELVSS protection).
4. If AVDD decreases to 90% of its configured voltage for 1ms, all output voltages shut down (for AVDD short to GND protection during operation).
5. If ELVDD decreases to 80% of its configured voltage for 1ms, all output voltages shut down (for ELVDD short to GND protection during operation).
6. If ELVSS increases to >600mV for 1ms, all output voltages shut down (for ELVSS short to GND protection during operation).

Thermal Shutdown

To prevent the IC from operating at exceedingly high temperatures, thermal shutdown is implemented by monitoring the silicon die temperature. When the die temperature exceeds the upper threshold (T_{ST}), the IC shuts down. Once the die temperature drops below the lower threshold, the IC restarts and resumes normal operation. The hysteresis is 25°C.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

APPLICATION INFORMATION

Selecting the Inductor

It is recommended to use the ELVDD and ELVSS converters with 4.7µH inductors, and the AVDD boost converter with a 10µH inductor (see Table 2).

For a given inductance, the inductor DC current rating should be at least 40% greater than the maximum input peak inductor current for most applications. The inductor's DC resistance should be as small as possible for higher efficiency.

Selecting the Capacitor

Table 2 shows the recommended capacitors. Lower capacitance may lead to increased voltage ripple. Generally, the lower I_{OUT}, the lower the required capacitance. It is recommended to use ceramic capacitors with X5R or X7R dielectrics for their low ESR and small temperature coefficients.

Optional ELVSS External Rectifier Diode

Using an external Schottky diode as a rectifier for ELVSS can be beneficial for improving ELVSS line regulation in heavy load when V_{IN} < 3.5V. If necessary, a B0530WS Schottky diode in an SOD-323 package is sufficient. Connect this diode between ELVSS and SW2 (see the dotted box in Figure 4 on page 16).

Table 2: Recommended Inductors and Capacitors

Ref	Value	Manufacturer	Manufacturer PN
L_{SW1}, L_{SW2}	4.7µH	Coilcraft	XFL4020-4R7ML
L_{SW3}	10µH	Coilmaster	MMPP252012-100N
C_{IN}	3 x 10µF	Murata	GRM21BR71A106KE51
C_{O_AVDD}, C_{O_ELVDD}	10µF	Murata	GRM21BR71A106KE51
C_{O_ELVSS}	2 x 10µF	Murata	GRM21BR71A106KE51
C_{CT}	100nF	Murata	GRM155B11A104KA01

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

PCB Layout Guidelines

Efficient PCB layout and placement of the high-frequency switching path are critical to prevent noise and electromagnetic interference (EMI). For the best results, refer to Figure 4 and follow the guidelines below:

1. Place the input capacitors on PVIN and AVIN as close as possible to the device.
2. Place the output capacitors on AVDD, ELVDD, and ELVSS as close as possible to the device.
3. Use short and wide traces to connect the input capacitors on PVIN and AVIN.
4. Use short and wide traces to connect the output capacitors on AVDD, ELVDD, and ELVSS.
5. Connect the CT capacitor's negative terminal directly to the AGND pin.
6. Keep the loop between SW2, L2, the PVIN input capacitor, the ELVSS output capacitor, and GND as short as possible due to the high-frequency pulse current.
7. Connect the IC's exposed thermal pad to AGND, PGND1, and PGND2.

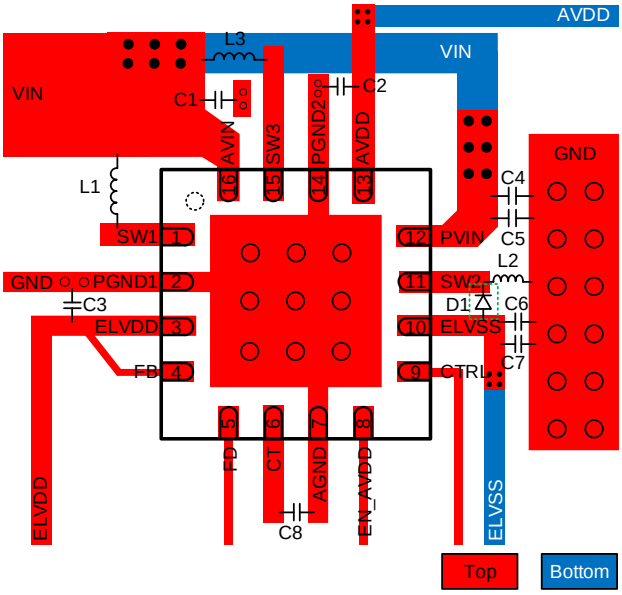


Figure 4: Recommended PCB Layout

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUIT

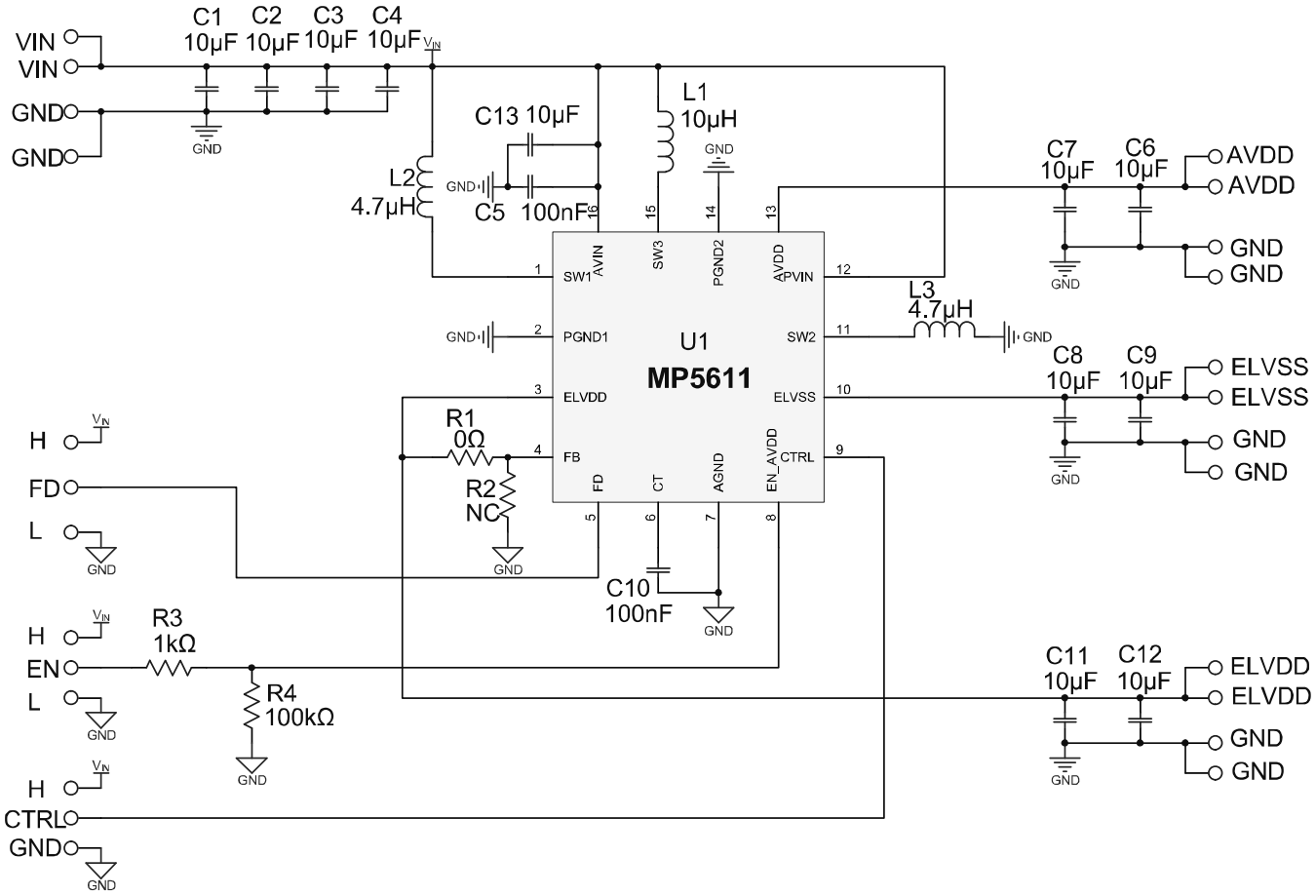
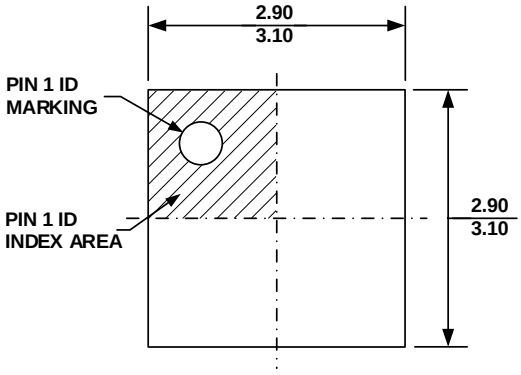


Figure 5: Typical Application Circuit

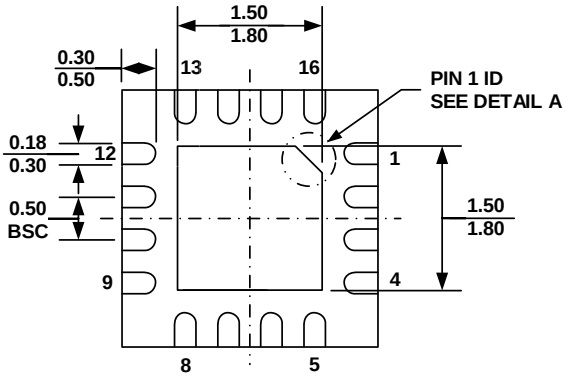
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

PACKAGE INFORMATION

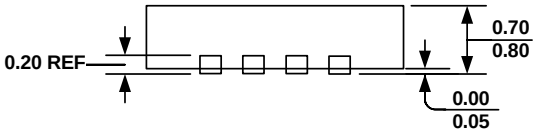
TQFN-16 (3mmx3mm)



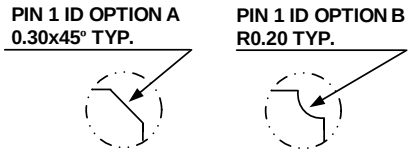
TOP VIEW



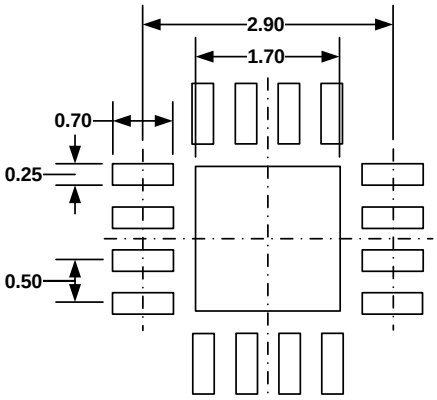
BOTTOM VIEW



SIDE VIEW



DETAIL A



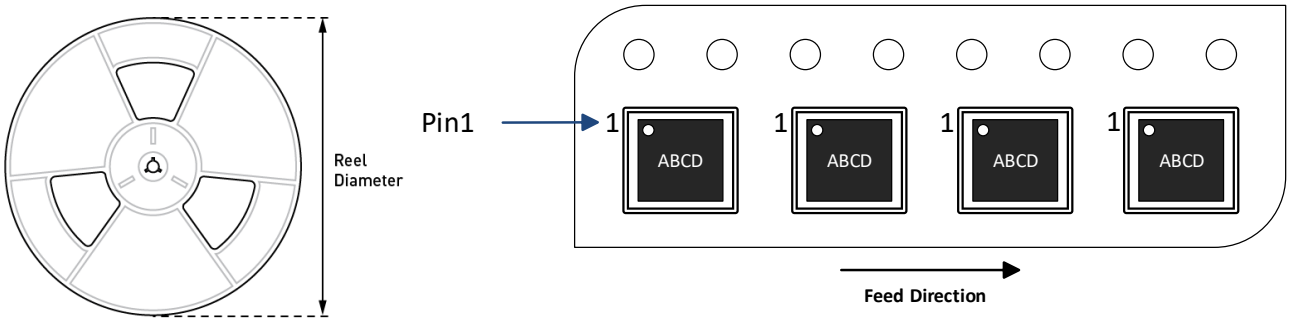
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-220, VARIATION WEED-4.
5) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP5611GQT-Z	TQFN-16 (3mmx3mm)	5000	N/A	N/A	13in	12mm	8mm

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/16/2021	Initial Release	-

Notice: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.