MP5410

Low Start-up Voltage Boost Converter with Four SPDT Switches

The Future of Analog IC Technology

DESCRIPTION

The MP5410 is a high efficiency, current mode step-up converter with four single-pole/double-throw (SPDT) switches designed for low-power bias supply application. The device can boost dual-cell NiCd/NiMH or single-cell Li+ battery to 10V output voltage.

The MP5410 can start up from an input voltage as low as 1.8V. It uses a current limited variable frequency control algorithm to optimize efficiency and minimize external component size and cost. The internal low resistance N-Channel MOSFET switch can withstand up to 10V allowing the MP5410 to produce high output voltage with high efficiency.

In addition, the MP5410 can disconnect all loads from input DC power supply. The integrated schottky diode reduces external parts to save critical board space.

The MP5410 features low shutdown current allowing the part to draw less than 1μA off current in shutdown mode. And it includes input under voltage and over temperature protection.

The MP5410 is available in a small 16-pin QFN 3x3mm package.

FEATURES

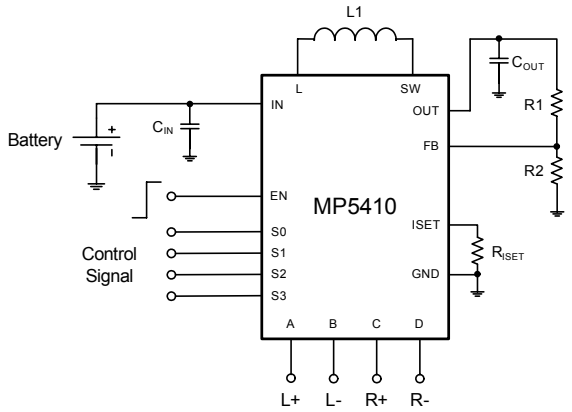
- 1.8V Low Voltage Start-Up
- 1.8V to 5.5V Input Range
- Output Disconnection
- Integrated Power MOS & Schottky Diode
- Variable Frequency Control
- <1μA Shutdown Current
- Current Mode Control with Internal Compensation
- More than 80% Efficiency at Light Load Conditions
- Tiny External Components
- Inrush Current Limiting and Internal Soft-Start
- Input UVLO
- Over Temperature Protection
- 3x3mm QFN16 Package

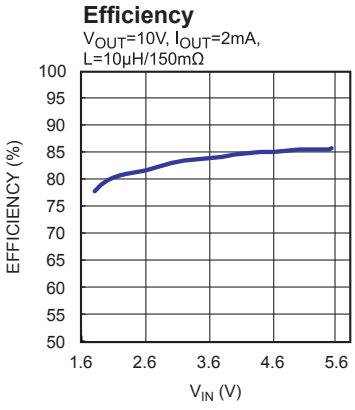
APPLICATIONS

- Dual-cell and Three-cell NiCd/NiMH or Single-cell Li Battery Consumer Products
- 3D Glass Driver
- Small LCD Displays Bias Supply
- Digital Still and Video Cameras
- Handheld Computers and PDAs
- Cell Phones

For MPS green status, please visit MPS website under Quality Assurance. "MPS" and "The Future of Analog IC Technology" are Registered Trademarks of Monolithic Power Systems, Inc.

TYPICAL APPLICATION





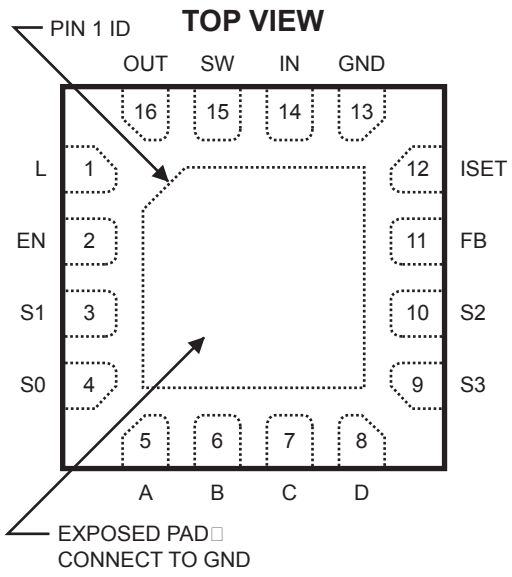
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2011 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
MP5410EQ	QFN16 (3x3mm)	ABAY	-20°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP5410EQ–Z);
For RoHS Compliant Packaging, add suffix –LF (e.g. MP5410EQ–LF–Z)

PACKAGE REFERENCE



QFN16 (3x3mm)

ABSOLUTE MAXIMUM RATINGS (1)

SW, OUT, A, B, C, D.....-0.5V to +12V
All other Pins.....-0.5V to +6.5V
Continuous Power Dissipation (T_A = +25°C) (2) 2.08W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 1.8V to 5.5V
Boost Converter Output Voltage.....V_{IN} to 10V
Maximum Junction Temp. (T_J)..... +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN16 (3x3mm) .....60 ..... 12 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operation conditions.
4) Measured on JESD51-7, 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2011 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 2.4V, V_{OUT} = 10V, I_{OUT} = 2mA, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Operating Input Voltage	V_{IN}		1.8		5.5	V
Minimum Startup Voltage	V_{ST}	V_{OUT}=0V			1.8	V
Quiescent Current	I_{Q_NS}	I_{OUT}=0, V_{FB}=1.3V, No switching		28	50	μA
Shutdown Current	I_{SD}	V_{EN}=0V		0.1	1	μA
IN Under Voltage Lockout	V_{UVLO}	V_{IN} Rising		1.58	1.7	V
Under Voltage Lockout Hysteresis				100		mV
Step-up Converter						
Maximum On Time	T_{ON}		4	6	7.5	μs
Minimum Off Time	T_{OFF}		400	550	700	ns
SW On-Resistance	R_{DS_ON}	I_{SW} = 200mA		0.65	0.8	Ω
SW Leakage Current	I_{SW_LKG}	V_{SW}=12V			2	μA
SW Current Limit	I_{SW_LIMIT}	R_{ISET}=300kΩ		180		mA
Schottky Diode Forward Voltage	V_{FW}	I_{FW}=100mA	0.4	0.5	0.6	V
Fixed OUT Supply Voltage	V_{OUT_FIXED}	Let FB pin floating, 1.8V<V_{IN}<5.5V	9.7	10	10.3	V
FB Voltage (Regulation Mode)	V_{FB}	Connect R-divider to FB, 1.8V<V_{IN}<5.5V	1.20	1.23	1.26	V
FB Input Bias Current	I_{FB}	V_{FB} = 1.23V			1	μA
Control Interface						
EN/SX Input High Voltage	V_{EN_H}		1.4			V
EN/SX Input Low Voltage	V_{EN_L}				0.4	V
EN/SX Input Bias Current	I_{EN}				1	μA
SPDT Switch						
Switch On-Resistance	R_{SPDT_ON}	V_{OUT}=10V, I_A, I_B, I_C, I_D=2mA		25	50	Ω
Switch On-Resistance Match Between Channels	ΔR_{SPDT_ON}	V_{OUT}=10V, I_A, I_B, I_C, I_D=2mA			10	Ω
Turn-on Time	T_{ON}	R_L= 300Ω, C_L= 35pF		80		ns
Turn-off Time	T_{OFF}	R_L= 300Ω, C_L= 35pF		170		ns
Protection						
Output Disconnect Switch On-Resistance	R_{DISC_ON}	V_{OUT}=10V		0.7	0.8	Ω
Thermal Shutdown				150		°C

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2011 MPS. All Rights Reserved.

PIN FUNCTIONS

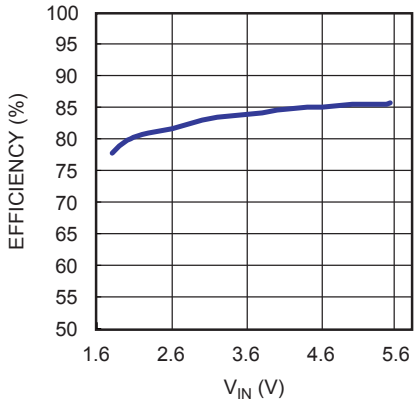
Pin #	Name	Pin Function
1	L	Inductor Output Pin. L is the output node of the internal disconnecting switch. Connect the inductor to this pin.
2	EN	On/Off control input. A logic high input turns on the chip. A logic low input turns off the chip. This pin should not be left floating.
3	S1	Channel B SPDT Switch Control Input. If the chip is enabled, a logic low input switches B to GND and a logic high input switches B to OUT. This pin should not be left floating.
4	S0	Channel A SPDT Switch Control Input. If the chip is enabled, a logic low input switches A to GND and a logic high input switches A to OUT. This pin should not be left floating.
5	A	Channel A SPDT Switch Output.
6	B	Channel B SPDT Switch Output.
7	C	Channel C SPDT Switch Output.
8	D	Channel D SPDT Switch Output.
9	S3	Channel D SPDT Switch Control Input. If the chip is enabled, a logic low input switches D to GND and a logic high input switches D to OUT. This pin should not be left floating.
10	S2	Channel C SPDT Switch Control Input. If the chip is enabled, a logic low input switches C to GND and a logic high input switches C to OUT. This pin should not be left floating.
11	FB	Regulation Feedback Input. Connect to an external resistive voltage divider from the output to FB to set the boost converter output voltage. Floating this pin to achieve fixed 10V output.
12	ISET	Constant Peak Current Set. Connect to an external resistor to GND to set the boost converter peak current.
13	GND	Ground.
14	IN	Input Supply Pin. IN pin powers the internal circuitry and is the input node of the internal disconnecting switch. Must be locally bypassed.
15	SW	Output Switch Node. SW is the drain node of the internal low-side N-Channel MOSFET. Connect the inductor to SW to complete the step-up converter.
16	OUT	Step-up Converter Output.
	Exposed Pad	Connect exposed pad to GND plane in PCB for proper thermal performance.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2011 MPS. All Rights Reserved.

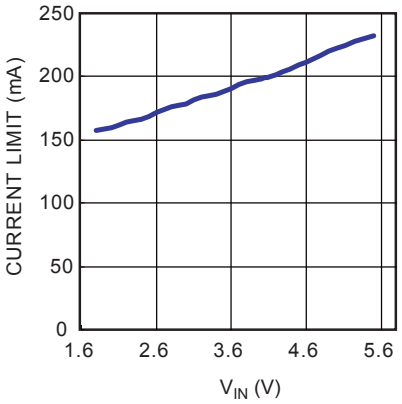
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = V_{EN} = 2.4V, V_{OUT} = 10V, I_{OUT} = 2mA, L = 10µH/150mΩ, unless otherwise noted.

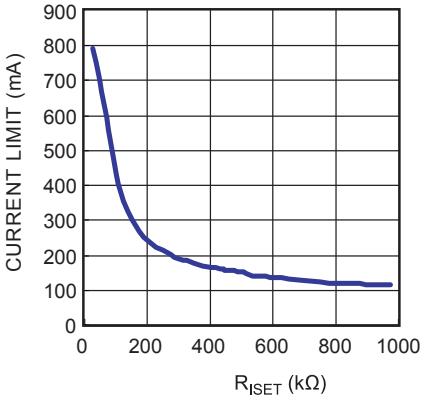
Efficiency



V_{IN} vs. Current Limit



R_{ISET} vs. Current Limit

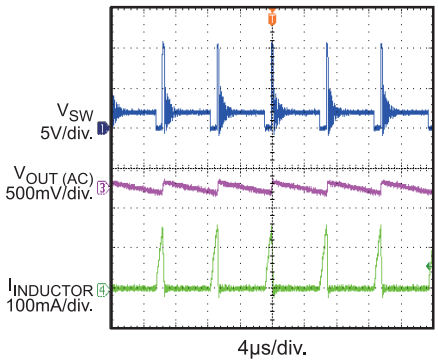


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2011 MPS. All Rights Reserved.

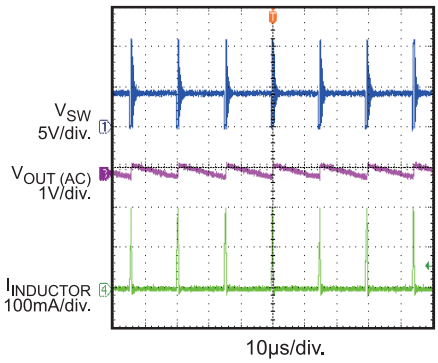
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = V_{EN} = 2.4V, V_{OUT} = 10V, I_{OUT} = 2mA, L = 10µH/150mΩ, unless otherwise noted.

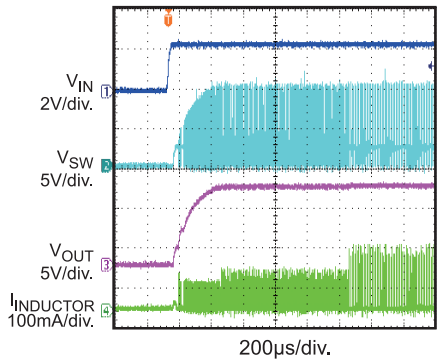
Steady State Waveforms
V_{IN}=2V



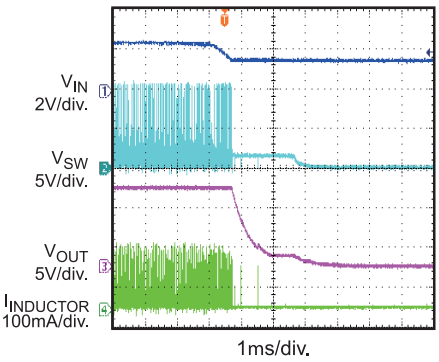
Steady State Waveforms
V_{IN}=4.2V



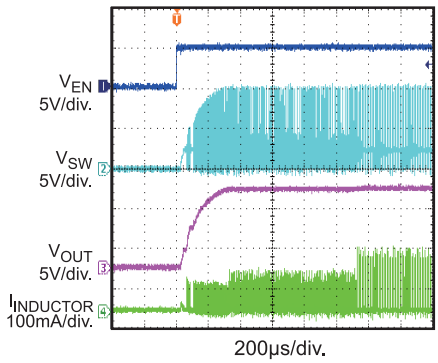
V_{IN} Power On



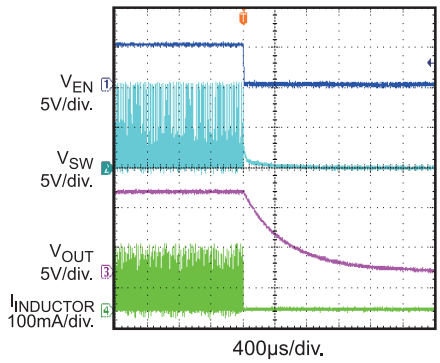
V_{IN} Power Off



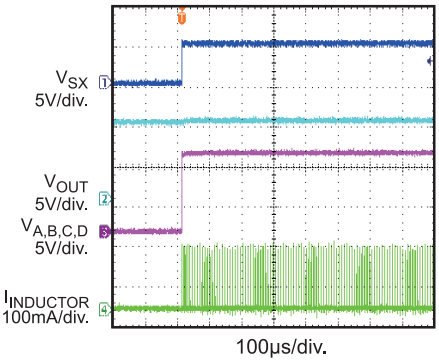
V_{EN} Power On



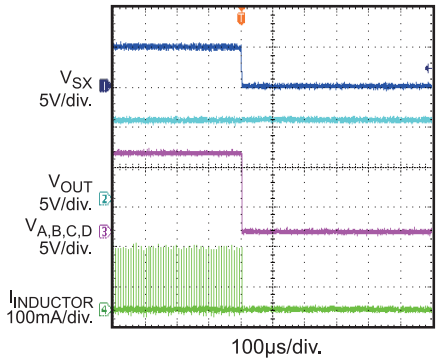
V_{EN} Power Off



Control Signal Turn On Channel A, B, C, D



Control Signal Turn Off Channel A, B, C, D



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2011 MPS. All Rights Reserved.

FUNCTION BLOCK DIAGRAM

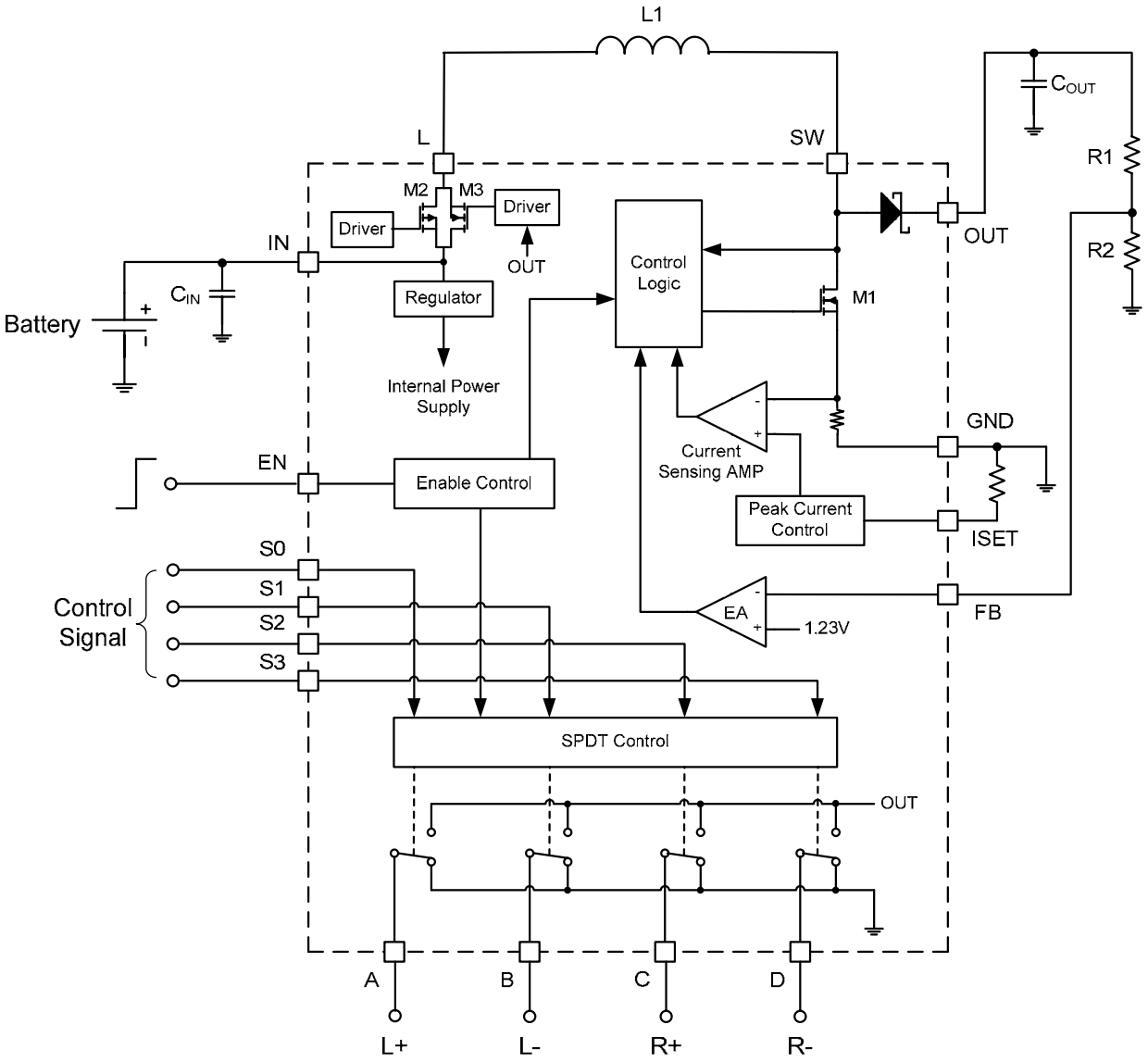


Figure 1—MP5410 Function Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2011 MPS. All Rights Reserved.

OPERATION

The MP5410 is a step-up converter with four single-pole/double-throw (SPDT) switches designed for low-power bias supply application. It operates from an input voltage as low as 1.8V. The 0.65Ω internal N-Channel MOSFET power switch and low dropout voltage schottky diode are driven with a variable frequency, constant peak-current architecture for improved regulation and low operating current. Operation can be best understood by referring to the Block Diagram.

Output Disconnection

The MP5410 integrates disconnect switch between IN pin & L pin. The disconnect switch is composed of a NMOS and a PMOS in parallel. The MP5410 can disconnect all loads from input DC power supply when EN pin is connected to ground.

Under Voltage Lockout

An under voltage lockout function prevents device startup if the supply voltage on VBat is lower than approximately 1.5V. When in operation and the battery is being discharged, the device automatically enters the shutdown mode if the voltage on V_{IN} drops below 1.5V.

System Start-Up

When the MP5410 is enabled, the PMOS of disconnect switch is turned on first, and then the system starts boosting the step-up converter with an internal soft-start and the output voltage rises up. The NMOS of disconnect switch is driven by Vout. It will be turned on once the output voltage reaches the threshold level. The on-resistance of NMOS is smaller than that of PMOS, so the PMOS is shorted by NOMS at normal operation to reduce the conduction loss.

It is recommended on the start up sequence that the enable signal comes after input voltage established.

Soft-start and inrush current limiting are provided during start-up as well as normal mode operation.

Soft-Start

The MP5410 provides soft-start by charging an internal capacitor with a very weak current source. The voltage on this capacitor, in turn, slowly ramps the peak inductor current limit from zero to the setting value. The MP5410 limits this inrush current by increasing the current limit in two steps, starting from $I_{LIM}/4$ for 256 switching cycles to $I_{LIM}/2$ for the next 256 cycles, and then full current limit. The soft-start time varies greatly with load current; output voltage and input voltage.

Variable Frequency Constant-Peak-Current Operation

When the power MOSFET is turned on the inductor current increases until the current limit is reached. The Power MOSFET is then turned off for a setting minimum off time. At the end of this minimum of time transition if the feedback pin is still lower than the 1.23V internal reference the power MOSFET will again be turned on, otherwise the MP5410 waits until the voltage drops below the threshold before turning on the MOSFET again. This process allows for optimal use of the inductor, while minimizing the output ripple and size of the output capacitor and maintaining low operating current.

Integrated Schottky Diode

The high switching frequency demands a high-speed rectification for optimum efficiency The MP5410 integrates a low voltage-drop schottky diode to reduce external parts to save critical board space.

Four SPDT Switches

The MP5410 includes four SPDT analog switches. S0~S1 control the switches respectively. If the chip is enabled, a logic low input switches the relative channel output to GND and a logic high input switches it to OUT.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2011 MPS. All Rights Reserved.

Table 1—Switching Selection Control Logic

EN	Control Input				Switch Output			
	S0	S1	S2	S3	A	B	C	D
L	X	X	X	X	Open	Open	Open	Open
H	L	L	L	L	GND	GND	GND	GND
H	H	L	L	L	OUT	GND	GND	GND
H	L	H	L	L	GND	OUT	GND	GND
H	H	H	L	L	OUT	OUT	GND	GND
H	L	L	H	L	GND	GND	OUT	GND
H	H	L	H	L	OUT	GND	OUT	GND
H	L	H	H	L	GND	OUT	OUT	GND
H	H	H	H	L	OUT	OUT	OUT	GND
H	L	L	L	H	GND	GND	GND	OUT
H	H	L	L	H	OUT	GND	GND	OUT
H	L	H	L	H	GND	OUT	GND	OUT
H	H	H	L	H	OUT	OUT	GND	OUT
H	L	L	H	H	GND	GND	OUT	OUT
H	H	L	H	H	OUT	GND	OUT	OUT
H	L	H	H	H	GND	OUT	OUT	OUT
H	H	H	H	H	OUT	OUT	OUT	OUT
H: High Level L: Low Level X: Don't Care								

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2011 MPS. All Rights Reserved.

APPLICATION INFORMATION

Components referenced below apply to Typical Application Circuit on page 11.

Setting the SW Current Limit

The resistor on ISET pin is used to set the SW current limit. The relationship of the SW current limit vs. the ISET resistor is showed as the curve in page 5. For Constant-Peak-Current Operation, when the power MOSFET is turned on the inductor current increases until the current limit is reached. Since the response delay, the actual SW peak current value exceeds the setting current limit a little. Under the higher input voltage and with the lower inductor, the actual SW peak current is higher due to the faster SW current di/dt. Under same condition, a lower current limit allows lower SW current and higher switching frequency, while a higher current limit allows higher SW current and lower switching frequency.

Setting the Output Voltage

MP5410 features internal resistive voltage divider, so floating the FB pin to achieve fixed about 10V output. Connect to an external resistive voltage divider from the output to FB to set the boost converter output voltage. Set the output voltage by selecting the resistive voltage divider ratio by the equation:

$$V_{OUT} = V_{FB} \times \frac{R1+R2}{R2}$$

Where, V_{OUT} is the output voltage, V_{FB} = 1.23V.

For R1=178kΩ and R2 = 24.9kΩ, then V_{OUT} = 10V.

Selecting the Inductor

A inductor with a DC current rating of at least 40% higher than the maximum input current is recommended for most applications at wide input range. For highest efficiency, the inductor's DC resistance should be as small as possible.

Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input supply and the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent high frequency switching current from passing through the input. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 4.7μF or 10μF capacitor is sufficient.

Selecting the Output Capacitor

The output capacitor keeps the output voltage ripple small and ensures feedback loop stability. The output capacitor impedance should be low at the switching frequency. Ceramic capacitors with X7R dielectrics are recommended for their low ESR characteristics. For most applications, a less than 10μF ceramic capacitor is sufficient.

Layout Considerations

Careful attention must be paid to the PCB board layout and components placement. Proper layout of the high frequency switching path is critical to prevent noise and electromagnetic interference problems. The loop of MP5410 SW to GND pin, SW to OUT pin, and output capacitor is flowing with high frequency pulse current. It must be as short as possible. The IN pin is the power supply input for the internal MOSFET switch gate driver and the internal control circuitry. It must be locally bypassed. See the MP5410 demo board layout for reference.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2011 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUIT

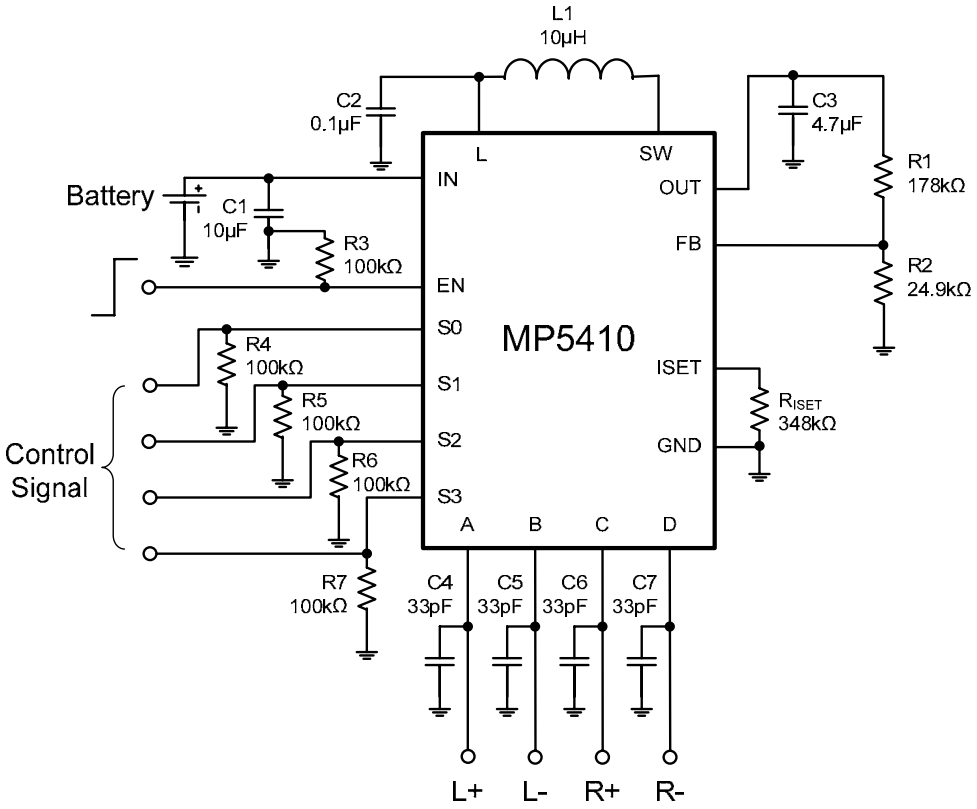
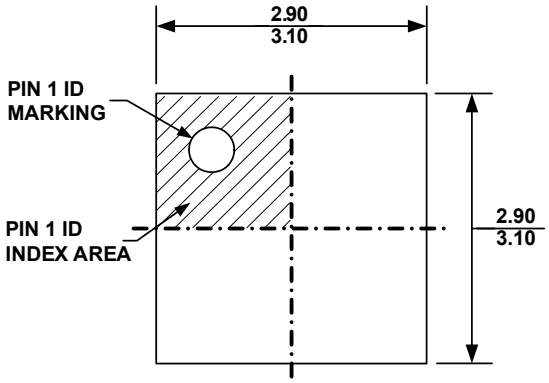


Figure 2—Battery Powered, V_{OUT}=10V, 3D Glass Driver

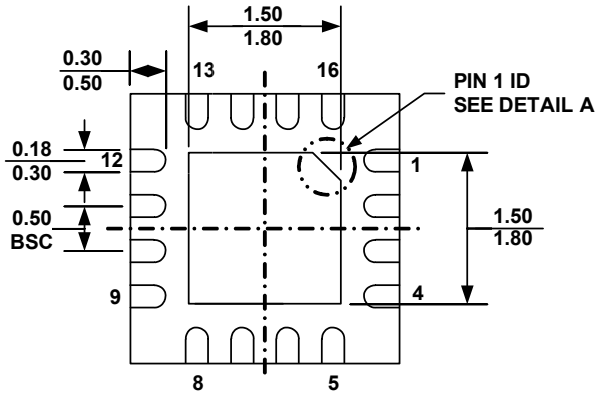
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2011 MPS. All Rights Reserved.

PACKAGE INFORMATION

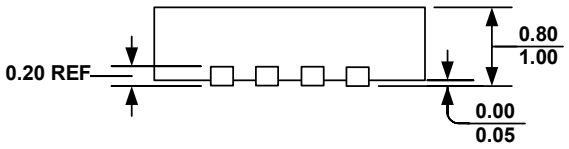
QFN16 (3x3mm)



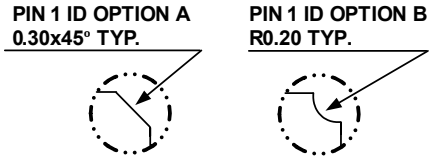
TOP VIEW



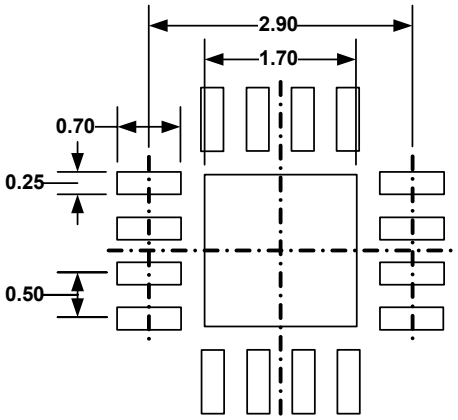
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH
3) LEAD COPLANARITY SHALL BE0.10 MILLIMETER MAX
4) DRAWING CONFORMS TO JEDEC MO-220, VARIATION VEED-4.
5) DRAWING IS NOT TO SCALE

NOTICE: The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2011 MPS. All Rights Reserved.